IMPLEMENTATION OF A VLC HDTV DISTRIBUTION SYSTEM FOR CONSUMER PREMISES

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Publications

This work has produced two publications; these are listed in chronological order below:

i. Distribution of SDTV and HDTV Using VLC Techniques for Domestic Applications, T. J. Amsdon, M. J. N. Sibley, P. J. Mather, Wireless Satellite Systems, 8th International Conference, WiSATS 2016 Cardiff, UK, September 19–20, 2016 Proceedings, ISBN 978-3-319-53849-5.

ii. Theoretical Concepts and MATLAB Modelling of VLC Based MIMO Systems, T. J. Amsdon, M. J. N. Sibley, CERC, University of Huddersfield, December 2013, ISBN 978-1-86218-121-2.

Abstract

A unidirectional, visible light communication (VLC) system intended for the distribution of Digital Video Broadcasting (DVB), high-definition television (HDTV) content to DVB compatible TVs within consumer premises is presented.

The system receives off-air HDTV content through a consumer grade DVB-T/T2 terrestrial set-top-box (STB) and re-encodes its Moving Picture Experts Group (MPEG) transport stream (TS) using a pulse position modulation (PPM) scheme called inversion offset PPM (IOPPM). The re-encoded TS is used to intensity modulate (IM) a blue light-emitting diode (LED) operating at a wavelength of 470 nm. Directed line-of-sight (DLOS) transmission is used over a free-space optical (FSO) channel exhibiting a Gaussian impulse response. A direct-detection (DD) receiver is used to detect the transmitted IOPPM stream, which is then decoded to recover the original MPEG TS. A STB supporting a high-definition multimedia interface (HDMI) is used to decode the MPEG TS and enable connectivity to an HD monitor.

The system is presented as a complementary or an alternative distribution system to existing Wi-Fi and power-line technologies. VLC connectivity is promoted as a safer, securer, unlicensed and unregulated approach. The system is intended to enable TV manufacturers to reduce costs by, firstly, relocating the TV's region specific radio frequency (RF) tuner and demodulator blocks to an external STB capable of supporting DVB reception standards, and, secondly, by eliminating all input and output connectors interfaces from the TV. Given the current trend for consumers to wall-mount TVs, the elimination of all connector interfaces, except the power cable, makes mounting simpler and easier.

The operation of the final system was verified using real-world, off-air broadcast DVB-T/T2 channels supporting HDTV content. A serial optical transmission at a frequency of 66 MHz was achieved. The system also achieved 60 Mbit/s, error free transmission over a distance of 1.2 m without using error correction techniques.

The methodology used to realise the system was a top-down, modular approach. Results were obtained from electrical modelling, simulation and experimental techniques, and using time-domain and FFT based measurements and analysis. The modular approach was adopted to enable design, development and testing of the subsystems independently of the overall system.

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The beginning of my life-long passion for all things electrical and electronic began the day my father, Ronald William Amsdon, removed the rear panel of a Philips G11 Colour TV to adjust its convergence circuits. As a curious nine year old, I peered inside the open TV and to my astonishment, discovered a fascinating new world. My father must have seen my eyes widen, because he enthusiastically explained what each circuit of the TV did in order to bring pictures and sound into our living room. I was captivated, and knew I wanted to know more about this intriguing new world.

In later years, as an experienced engineer, I have recalled my father's summary of the G11 chassis, and marvelled at how much he knew. My father was not trained as an engineer, but as a salesman, he was more accustomed to selling TV's than repairing them, but he had the mind and spirit of an engineer. He learnt from service technicians at the now long since defunct British Relay, and read service manuals to further his knowledge and understanding. From this rudimentary education, he was able to read and understand circuit schematics and layouts, as well as fault-find and fix to component level. Through practice, he also developed excellent soldering skills. I am eternally grateful to him for introducing me to electronics.

An immeasurable amount of thanks also goes to my mother, Jean Amsdon, for purchasing my first computer, a ZX Spectrum 48K, back in the Christmas of 1984. At first she was sceptical about my interest in this emerging technology, but she quickly realised I had a passion and aptitude for computing and programming, and encouraged my fascination by purchasing books and magazines on these subjects. My 48K was my pride and joy, providing me with a gateway into digital electronics and programming.

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I dedicate this thesis to my father, Ronald William Amsdon (1925–1999). I only wish he had lived to see all the things that I have achieved, all because I saw the inside of a Philips G11 Colour TV when I was nine years' old.

Contents

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Glossary

Acronyms

AC	alternating current
ADC	analogue-to-digital converter/conversion
AGC	automatic gain control
AlGaAs	aluminium gallium arsenide
AlGaInP	aluminium gallium indium phosphide
AM	amplitude modulation
ANSI	American National Standards Institute
APD	avalanche photodiode
ATSC	Advanced Television Systems Committee
AVC	Advanced Video Coding
BCH	Bose-Chaudhuri-Hocquenghem
BER	bit-error rate

BOM	bill-of-materials
BPF	band-pass filter
CAS	conditional access
CATV	community access television or community antenna television
CC	convolutional coding
Ce	cerium
CENELEC	European Committee for Electrotechnical Standardization
CFL	compact fluorescent lighting
CFR	Code of Federal Regulations
CMOS	complementary metal-oxide semiconductor
CNR	carrier-to-noise ratio
Codec	compression/decompression
COFDM	coded orthogonal frequency division multiplexing
CPE	consumer premises equipment
CRT	cathode-ray tube
CVBS	composite video, blanking and synchronisation or composite video baseband signal
CW	continuous wave
DC	direct current
DCO-OFDM	direct-current-biased optical orthogonal frequency division multiplexing
DD	direct-detection
DLIF	digital low intermediate frequency
DLOS	directed line-of-sight
DMT	discrete multi-tones
DSP	digital signal processing
DSSS	direct-sequence spread spectrum

DTH	direct-to-home satellite
DTMB	Digital Terrestrial Multimedia Broadcast
DVB	Digital Video Broadcasting
DVD	digital versatile/video disc
DVR	digital video recorder
EIRP	equivalent isotropically radiated power
EPG	electronic programme guide
ES	elementary stream
ETSI	European Telecommunications Standards Institute
EVB	evaluation board
FCC	Federal Communications Commission
FEC	forward-error correction
FER	frame-error rate
FET	field-effect transistor
FOV	field of view
FPGA	field-programmable gate array
FSO	free-space optical
FFT	fast Fourier transform
GaAs	gallium arsenide
GaAsP	gallium arsenide phosphide
GaN	gallium nitride
GBP	gain bandwidth product
GUI	graphical user interface
HD	high-definition
HDMI	high-definition multimedia interface
HDTV	high-definition television

HEVC	high efficiency video coding
I^2C	inter-integrated circuit
IC	integrated circuit
IEC	International Electrotechnical Commission
IF	intermediate frequency
IM	intensity modulation
InGaN	indium gallium nitride
IOPPM	inversion offset pulse position modulation
IP	internet protocol
IPTV	internet protocol television
IR	infrared
IRC	infrared communications
ISDB	Integrated Services Digital Broadcasting
ISI	inter-symbol interference
ITU	International Telecommunications Union
LASER/laser	light amplification by stimulated emission of radiation
LCD	liquid crystal display
LDPC	low-density parity-check
LED	light-emitting diode
LFL	linear fluorescent lighting
LNA	low-noise amplifier
LO	local oscillator
LOS	line-of-sight
LPF	low-pass filter
LSB	least significant bit
LTI	linear time-invariant

LVCMOS	low-voltage CMOS
MIMO	multiple-in-multiple-out
MIS	metal-insulator-semiconductor
MPEG	Moving Picture Experts Group
MSB	most signification bit
NDA	non-disclosure agreement
NLOS	nondirected line-of-sight
NRZ	non-return-to-zero
NTSC	National Television System Committee
OEM	original equipment manufacturer
OFDM	orthogonal frequency division multiplexing
OLED	organic light-emitting diode
OOK	on-off keying
Op-amp	operational amplifier
OPPM	offset pulse position modulation
OWC	optical wireless communications
PAL	phase alternate line
PECL	positive emitter-coupled logic
PMT	programme map table
PbS	lead sulphide
PCB	printed circuit board
PCM	pulse code modulation
PD	photodiode/photodetector (interchangeable)
PES	packetized elementary stream
PGA	programmable gain amplifier
PID	packet identifier

PIM	pulse interval modulation
PIN	positive-intrinsic-negative (as in PIN diode)
PISO	parallel-in-serial-out
PLL	phase-locked loop
PMT	programme map table
PPM	pulse position modulation
QAM	quadrature amplitude modulation
QPSK	quadrature phase-shift keying
RF	radio frequency
RGB	red, green and blue
RMS	root mean square
RS	Reed-Solomon
Rx	receiver
SCART	Syndicat des Constructeurs d'Appareils Radiorécepteurs et Téléviseurs
SDTV	standard-definition television
SECAM	séquentiel couleur à mémoire
SiC	silicon carbide
SISO	serial-in-serial-out
SMD	surface-mount device
SMPS	switched-mode power supply
SNR	signal-to-noise ratio
SSL	solid-state lighting
STB	set-top-box
TCA	transconductance amplifier
TCP	transmission control protocol
TIA	transimpedance amplifier

TOP	take-over-point
TS	transport stream
TTL	transistor-transistor logic
TV	television
Tx	transmitter
UHDTV	ultra-high-definition television
USB	universal serial bus
VCR	video cassette recorder
VGA	video graphics array
VHDL	VHSIC hardware description language
VHS	video home system
VHSIC	very high speed integrated circuit
VLC	visible light communications
VLCC	Visible Light Communications Consortium
YAG	yttrium aluminium garnet (as in YAG phosphor)

Notation

$\otimes$	linear time-invariant convolution operator
A_{Rx}	PD active area
Av	voltage gain
C_{CM}	common-mode capacitance
C_D	diode capacitance
C_d	LED depletion capacitance
C_{DM}	differential-mode capacitance
C_f	feedback capacitance
C_s	LED charge diffusion and storage capacitance
d	distance between Tx and Rx
E	photon energy (emitted by an LED)
F_s	sampling frequency
f_c	centre frequency
$f_{MIN\ SER\ CLK}$	minimum serial PISO clock frequency
f_{TS_CLK}	frequency of the MPEG TS clock (at receiver demodulator)
f'_{TS_CLK}	frequency primed is the actual MPEG TS clock (at transmission)
$g(\psi)$	concentrator optical gain (as a function of incident angle)

g_m	transconductance
$h_{LOS}(t)$	optical channel impulse response
$h_p(t)$	Gaussian pulse response
$H_{LOS}(0)$	DC gain for DLOS transmission
$H_p(\omega)$	modulating pulse frequency response
I	in-phase component
I_D	diode current
I_{DS}	FET drain-source current
I_F	LED forward current
I_p	PD photocurrent
I_S	diode reverse saturation current
j	imaginary number $j = \sqrt{-1}$
k	number of nk encoder input bits
m	order of the Lambertian emission
M	number of coder input bits/modulation order
n	number of nk encoder output bits or ideality factor for diodes
N	number of bits
$n(t)$	additive noise

P_{er}	probability of erasure error
P_f	probability of false alarm error
P_{Rx}	optical power received at PD
P_s	probability of wrong slot error
P_{Tx}	optical power transmitted by LED
Q	quadrature component
$\|r\|$	magnitude
R	PD responsivity
$R_{DS\,ON}$	FET drain-source resistance in the on state
R_f	feedback resistor
R_0	Lambertian radiant intensity
S_i	time domain symbol (QPSK)
t	time variable
t_d	decision time
T	period (representing one cycle) or temperature
$T(\varphi)$	optical band-pass filter attenuation (as a function of incident angle)
T_{offset}	time offset due to additional clock MPEG TS clock cycles

T_S	bit period or slot-time
$T_{TS\_DATA[n]}$	period of the MPEG TS data bit, bit number denoted by n
T_{TS_SYNC}	period of the MPEG TS synchronisation pulse
T_{TS_VALID}	period of the MPEG TS valid signal
v_{ISI}	any signal voltage present in a particular time slot
v_{pk}	peak signal voltage within the slot-time
$V_{A\ IOPPM+}$	composite positive IOPPM analogue pulse
$V_{A\ IOPPM-}$	composite negative IOPPM analogue pulse
V_D	diode voltage
$V_{D\ IOPPM+}$	window comparator positive IOPPM digital pulse output
$V_{D\ IOPPM-}$	window comparator negative IOPPM digital pulse output
V_{DS}	FET drain-source voltage
V_F	diode forward voltage
V_{GS}	FET gate-source voltage
V_{in}	input voltage
V_{output}	output voltage
V_R	diode reverse voltage
V_{REF}	comparator reference voltage

V_{REF+}	IOPPM positive threshold voltage
V_{REF-}	IOPPM negative threshold voltage
$m(t)$	modulating signal (data-carrying signal)
n_o	noise
$x(t)$	optical intensity modulating signal
$y(t)$	receiver photocurrent signal (including additive noise)
Z_T	transimpedance
α	Gaussian pulse peak height
η_{qe}	quantum efficiency
θ	angle in radians
λ	wavelength
τ	pulse period
τ_R	time (autocorrelation)
$\emptyset$	irradiance angle
$\emptyset_{1/2}$	emission semi-angle/half-power/3 dB point
ψ	incident angle (angle between Tx and Rx)
ψ_c	FOV angle

Constants

c	speed of light (approximately $299792458\ m\ s^{-1}$)
h	Planck's constant (exactly $6.62607015 \times 10^{-34}\ J\ s$)
k	Boltzmann's constant (approximately $1.38064852\ \times 10^{23}\ m^2\ kg\ s^{-2}\ K^{-1}$)
q	charge of an electron (approximately $1.60217662\ \times 10^{-19}\ C$)

1 Introduction

1.1 Background

A proof-of-concept, unidirectional free-space visible light communication (VLC) system for distributing high-definition television (HDTV) content to wall-mounted TVs is presented. Specifically, the system is intended to distribute content received by Digital Video Broadcast (DVB) standard terrestrial set-top-box (STB) receivers.

VLC based transmission techniques are offered as an alternative or a complementary solution to current radio frequency (RF) and power-line technologies for content distribution. This approach is also presented as a way for TV manufacturers to eliminate the need for region specific RF tuner and demodulator functions within a TV, replacing them with a simpler baseband optical receiver which interfaces directly with the Moving Picture Experts Group (MPEG) decoder. Using this approach the tuner and demodulator functions are relocated to a low-cost STB, which provides an integrated RF to VLC system external to the TV. This VLC enabled STB essentially receives and demodulates DVB content, and re-encodes it using a coding scheme suitable for free-space optical (FSO) transmission, and transmits to the TV over an optical channel exhibiting an inverse square attenuation characteristic and Gaussian impulse response. Figure 1-1 shows the conceptual block diagram of the system, with the key VLC blocks highlighted in pink.

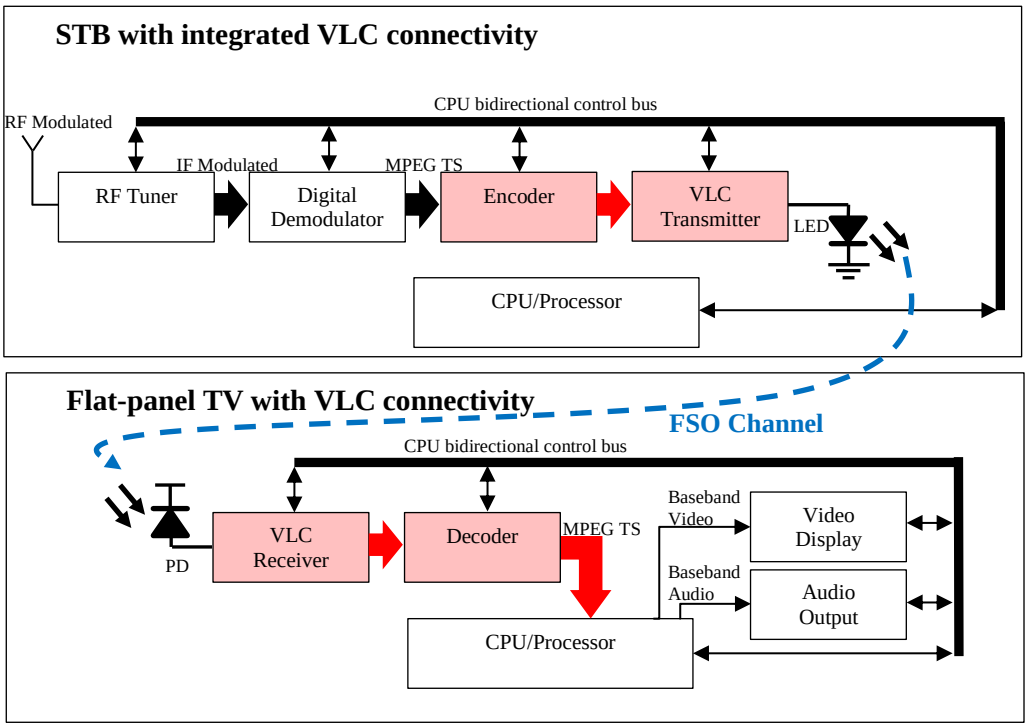


Figure 1-1 VLC broadcast (MPEG TS) distribution system (author generated image)

This work also proves that all connector interfaces, except the mains power cable, can be eliminated from a digital TV to further reduce costs and complexity. The elimination of the interfaces also has the added benefit of making it easier to wall-mount a TV.

In this chapter, the concept of a VLC enabled content distribution system is defined. The evolution of TV interconnects from analogue to digital interfaces is introduced, and an explanation as to why TVs fitted with multiple interconnects pose wall-mounting challenges is given. Current trends in digital broadcasting are also discussed, highlighting the worldwide migration to all-digital based broadcast systems, with particular emphasis placed on the DVB standard. The current DVB compatible STB and TV architectures are summarised, and a new conceptual content distribution architecture is introduced. Wi-Fi and power-line technologies and the associated disadvantages are also presented, followed by an introduction to VLC systems suitability for content

distribution. A physical realisation of the conceptual VLC based system is also given. The chapter closes with a summary of the key aims and objectives of this work, highlighting the areas of originality.

1.1.1 TV Interconnects

The earliest electronic TVs received analogue broadcast video and audio content directly through an RF connector which was connected to a 75 Ω un-balanced coaxial feeder cable. The opposite end of the feeder was connected to either a set-top loop or roof-top Yagi array antenna capable of receiving off-air broadcasts from a line-of-sight (LOS) RF transmitter. Received signals were presented to a tuner and demodulator which selected the desired channel content and converted it to the required baseband video and audio signals needed for the respective reproduction (Zarach & Morris, 1979). This fundamental TV system architecture has remained largely the same throughout the decades, although TVs in the developed world now use a digital architecture, and receive only digital broadcasts (ITU, 2013). Furthermore, modern TVs are no longer limited to terrestrial reception, but can also receive cable and satellite broadcasts (ITU, 2013). All of these digital broadcasts use RF based transmissions techniques and channel specific modulation schemes, with a common baseband digital transport stream (TS) layer at the transmitter and receiver.

Early TVs did not have any baseband connectivity, but since the mass deployment of Betamax and video home system (VHS) video cassette recorders (VCR) in the 1980s, TVs evolved to support, not only RF connectivity, but direct wireline connectivity of baseband signals. These interconnects were used to support VCRs, games consoles and home computers, as well as, starting in the 1990s, digital STBs and digital video recorders (DVR) (O'Driscoll, 2000). The first analogue baseband phono connectors

supported mono audio, and video in the form of the composite video, blanking and synchronisation (CVBS) signal used for phase alternate line (PAL) and SECAM (Séquentiel couleur avec mémoire) standards in Europe, and the NTSC (National Television System Committee) standard in North America (Jack, 2001). The analogue interconnects were expanded to included component video (P_R, P_B, Y), video graphics array (VGA), and S-video. In Europe the SCART (Syndicat des Constructeurs d'Appareils Radiorécepteurs et Téléviseurs) connector was developed to support analogue video, stereo audio and device-to-device signalling in a single interface. Stereo audio interfaces also evolved in the form phono and jack connectors. Digital interfaces appeared in the mid-1980s in the form of the audio optical fibre connector, and then in the 2000s, the high-definition multimedia interface (HDMI) connector appeared, capable of supporting digital video, audio and data (Whitaker, 1998). Ethernet interfaces have also been added to support internet connectivity, as well universal serial bus USB support for digital peripheral devices. Figure 1-2 and Figure 1-3 show the typical connectors found on the rear-panel of modern TVs in Europe and North America, respectively.

Figure 1-2 European: Samsung LE40A656 40” 1080p LCD HDTV

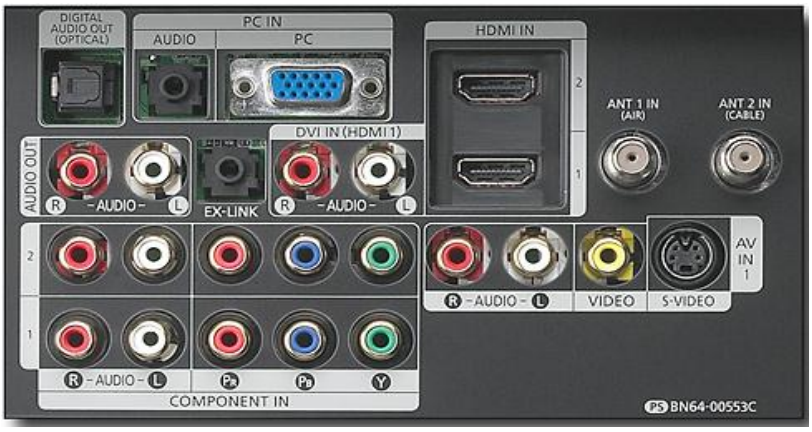


Figure 1-3 North America: Samsung LN-T5265F 52” 1080p LCD HDTV

1.1.2 Flat-panel TV Wall-mounting Challenges

Modern TVs use flat-panel screen technologies such as liquid-crystal display (LCD) and organic LED (OLED), which are lighter, less bulky, and have larger screen sizes than TVs built with cathode ray tubes (CRT). These advances have enabled consumers to wall-mount TVs, but challenges are introduced due to the TVs large number of connector interfaces. Firstly, a TV cannot operate without power, so a mains power cable input is essential and cannot be eliminated. Secondly, an RF input connector is required to enable the reception of terrestrial, cable and satellite broadcasts signals. Finally, a multitude of analogue and digital interconnects that have evolved since the 1980s are required to support connectivity to external peripheral devices. All these interfaces need cables that require channelling, either within the walls of the consumers premises i.e. chasing wall channels, or through the use of wall-mounted conduit; both of which are potentially expensive and inconvenient for the consumer. Furthermore, if the distance between the TV and the peripheral devices is a number of metres, the electrical performance of the baseband signals is degraded due to the long cable lengths. Specifically, increased cable length for baseband signals results in decreased signal-to-noise ratio (SNR) due to per unit length losses, and increased probability of ingress of

interference signals, both of which can lead to degraded picture quality. In the case of analogue baseband systems these effects lead to increased noise (reduced signal-to-noise ratio SNR) or beat-patterns (spurious ingress) in the reproduced picture. In digital baseband systems these effects can lead to errors, resulting in macro-blocking, and in severe cases, complete loss of picture.

1.1.3 Digital TV Trends

In 2013, the International Telecommunications Union (ITU), which is a respected institution that has been collecting data on TV trends since the 1960s, published a detailed report about global TV trends (ITU, 2013). The report highlighted that TV, unlike radio and fixed telephony, had not seen any decline in penetration, and that 79% of worldwide households had at least one TV. It also stated that most of developed world, US, Europe, Russia, and Arab States, has access to TV services through digital based technologies. The report stated that 55% of the total worldwide households with a TV are able to receive digital broadcasts, and it also stated that the most rapidly growing digital TV deployments are occurring in developing countries in Asia and Africa.

As TV is still an extremely important mass communication system, able to reach large audiences, broadcasts for terrestrial, cable TV (CATV), direct-to-home satellite (DTH) are rapidly moving towards an all-digital based transmission system. Additionally, internet protocol TV (IPTV) is another method of accessing broadcast content.

Broadcast TV is still extremely important for mass communication and deployments are increasing, specifically using digital technologies. As the adoption of digital TV progresses, support for legacy analogue baseband connector interfaces will continue to diminish (ITU, 2013). Legacy peripheral devices such as VCRs, which are no longer in

mass production (Overly, 2016), will ultimately be replaced by modern digital based technologies.

Even digital baseband connector interfaces, used to support physical media such as digital versatile discs (DVD) and Blu-ray, will be eliminated, replaced by growing cloud-based storage and subscription based online streaming services, such as Netflix, Hulu and YouTube. Similarly, games consoles such as PlayStation and Xbox could be replaced by subscription based online gaming services.

1.1.4 All-Digital TV and DVB MPEG TS

In the future, it is likely that almost all baseband connector interfaces will be eliminated from the TV. Given this scenario, it is possible to envision a connector-less TV having only a mains power cable and some form of generic transceiver to enable internet access and reception of traditional RF based terrestrial, cable, and satellite broadcasts. It is also possible to envision a TV that is able to operate in any region of the world regardless of the broadcast standards used in that specific region – in effect, a region-less TV.

In order to take this concept further, it is necessary to consider the standards for broadcast content. Firstly, it is important to mention that TCP/IP is a worldwide standard protocol for internet communications, so worldwide interoperability already exists for TCP/IP connected devices (Kurose, Ross, & Paul, 2013). However, there is no such worldwide standardisation or interoperability for digital TV broadcasts (Jack, 2001). The TV tuner and digital demodulator functions are region-specific (ATSC, 2010; DVB, 2015; Song et al., 2007), meaning that different modulation and channel coding schemes are used around the world for digital TV broadcasts. TV manufacturers currently need to fit specific tuner and demodulator types for the region of the world where the TV operates. This is a non-optimal solution, as manufacturers need to design

and support a number of TV platforms with different receiver requirements. Ideally, manufacturers might prefer to produce a generic, region-less TV platform to enable cost savings in the design, compliance testing and manufacturing processes, as well as simplify in-the-field support.

To achieve a region-less TV architecture, it is impossible to immediately standardise worldwide digital TV broadcasts, as this would require expensive upgrades to both broadcast transmitter stations and consumer premises equipment (CPE). A better strategy is to eliminate the tuner and demodulator from TVs, and externalise these functions in a low-cost STB which is able to receive and retransmit digital broadcast content to the TV using a standardised TS bus and wireless connection. Also, by externalising the region-specific elements of the TV, future upgrades to the broadcast system only require replacement of the low-cost STB and not the high-cost TV.

Most households in the developed world use some type of STB to access digital broadcast services, increasingly through STBs that provide internet protocol TV (IPTV), as well as terrestrial, cable or satellite access. STBs already provide a viable and cost-optimised method for receiving digital content, so this further strengthens the argument for externalising the tuner and demodulator functions of the TV to a STB. By relocating the tuner and demodulator functions to a STB, standardised connectivity between the STB and TV can be achieved by identifying a common digital interface used across all digital broadcast TV systems. This common interface can effectively unify all broadcast standards through a single interface which can then be re-encoded for wireless distribution of content from the STB to the TV. This interface can also be used to provide internet and IPTV connectivity through the TCP/IP protocol.

The unification process begins by examining existing digital broadcast systems to identify common digital interfaces that can be used for STB to TV connectivity. Although there are a number of digital TV broadcast standards used around the world, for the sake of clarity, only the most prevalent digital broadcast standard, DVB, is discussed here.

The DVB standard is subdivided by transmission type and provides for terrestrial broadcasts with DVB-T (SDTV) and DVB-T2 (HDTV), cable broadcasts with DVB-C (SDTV) and DVB-C2 (HDTV), and satellite broadcasts with DVB-S (SDTV) and DVB-S2 (HDTV). Most notably, the DVB-T standard is used extensively across Europe, Russia, Australasia, Africa, and certain parts of the Middle and Far-East. These standards specify all aspects of the broadcast system from transmission to reception, including source coding, channel coding and modulation schemes (NorDig, 2014).

Figure 1-4 shows a simplified block diagram of the DVB system architecture for DVB-T/T2, DVB-S/S2 and DVB-C/C2. As illustrated in the diagram, the transmission type determines the modulation scheme used; terrestrial DVB-T/T2 uses coded orthogonal frequency division multiplexing (COFDM) modulation because of a resistance to signal multipath interference; satellite DVB-S/S2 uses quadrature phase-shift keying (QPSK) because of a high immunity to noise; and cable DVB-C/C2 uses quadrature amplitude modulation (QAM) because it is able to accommodate a significant number of bits-per-symbol over well controlled, largely interference free, cable networks. Each modulation scheme uses a specific channel coding scheme, optimised for the channel type the broadcast content is transmitted over. The source coding, however, is common across all DVB standards (Bing, 2015). Currently MPEG-2 (H.262) is used for SDTV broadcasts and H.264, also referred to as MPEG-4 Part 10, Advanced Video Coding (MPEG-4

AVC), is used for HDTV broadcasts, and in future, ultra-HDTV (UHDTV) broadcasts will be made possible using H.265, also known as high efficiency video coding (HEVC) (Bing, 2015). These video codecs, in conjunction with multiplexing techniques, enable the transmission of multiple, highly compressed video and audio streams over band-limited RF channels. Multiplexing, is effectively a way of interleaving independent compressed video streams into a single serial TS which is channel coded. Each symbol of the channel coded data is then mapped to the respective modulation scheme for transmission over the broadcast channel. The multiplexer generates the TS, also known as the MPEG TS, by interleaving the compressed video and audio streams with data, and in cases where the content must be secured, it is scrambled. The MPEG TS is a packetized stream with a fixed packet size consisting of 1504 bits (188 bytes) per packet, and is a format consistent across all broadcast standards (Whitaker, 1998).

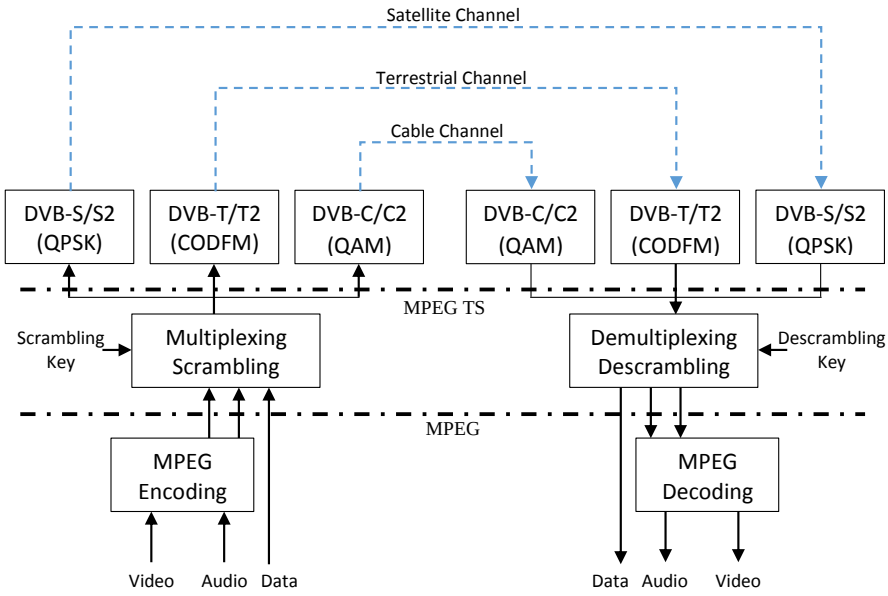


Figure 1-4 Simplified DVB system architecture (author generated image)

Given that the MPEG TS is the common digital interface across all DVB broadcast systems, the logical approach is to use this interface as the data source for a wireless

connectivity system, enabling the distribution of digital content to region-less TVs. The MPEG TS is also highly compressed with bit rates well defined by the applicable DVB standards.

Shown in Table 1-1 are the maximum bit rates for each DVB standard; currently, DVB-C2 has the highest bit rate at 83.1 Mbit/s (Živić, 2016).

Broadcast Type	Standard	TS Bit rate (Mbit/s)	Conditions
Cable	DVB-C2	83.1	QAM (QAM-4096), RF channel bandwidth 8MHz
	DVB-C	51.3	QAM (QAM-256), RF channel bandwidth 8MHz
Satellite	DVB-S2	64.5	8PSK, RF channel bandwidth 36MHz
	DVB-S	42.9	QPSK, RF channel bandwidth 36MHz
Terrestrial	DVB-T2	50.324	COFDM (256-QAM), code rate 5/6, guard interval 1/128, 32K FFT, RF channel bandwidth 8MHz
	DVB-T	31.668	COFDM (64-QAM), code rate 7/8, guard interval 1/32, 8K FFT, RF channel bandwidth 8MHz

Taken from: DVB-C: (ETSI, 1998); DVB-C2: (ETSI, 2010); DVB-S: (ETSI, 2006); DBV-S2: (ETSI, 2009b); DVB-T: (ETSI, 2009a); DVB-T2: (EBU, 2014).

Table 1-1 DVB standards (taken from DVB terrestrial, cable and satellite broadcast standards) (author generated table)

Before moving to the next section, it is worthwhile explaining the simplified operation of the DVB system using an example based on a DVB-T2 transmission. If four uncompressed HD video and audio streams, along with data relating to electronic programme guide (EPG) information are transmitted using the system shown in Figure 1-4, the transmit and receive process will be as follows. At the transmitter, the video and audio streams are compressed in the MPEG encoder using the appropriate H.624 codec to generate four independent packetized MPEG streams. These packets are then presented to the multiplexer which interleaves the streams with the EPG data to create the MPEG TS. The packets of the independent streams are assigned identifiers, known as packet identifiers (PID), which enables the correct reconstruction of the independent

streams in the receiver demultiplexer. The MPEG TS is then channel coded and transmitted sequentially over the terrestrial channel.

At the receiver, the transmitter processes are reversed; the stream is channel decoded, and following suitable error detection and correction, the MPEG TS is recovered. The MPEG TS is then passed to the demultiplexer where the PIDs are used to reconstruct the four independent HD MPEG streams, one of which will be selected by the consumer for MPEG decoding. The MPEG decoder then outputs uncompressed baseband video, audio and data which is presented to the TV for reproduction and ultimately viewed by consumer.

1.1.5 New All-Digital Architecture

Using the MPEG TS as the standard interface for digital content distribution, it is possible to conceptualise a connector-less and region-less TV architecture, but before doing this, it is necessary to introduce the current architectures for DVB based TV and STB platforms. Figure 1-5 shows the current DVB architectures used for DVB TV and STB platforms. In the current DVB STB architecture, broadcast services are received through an RF tuner which selects the desired broadcast channel, and a digital demodulator which recovers the MPEG TS. The recovered MPEG TS is then passed to a central processing unit (CPU), often simply referred to as the '*processor*', which performs error detection and correction on the MPEG TS, demultiplexes the individual video, audio and data streams, descrambles the streams if necessary, and then finally performs MPEG decoding in order to generate the baseband video and audio signals needed for reproduction in the TV. Baseband video and audio outputs, generally available in digital or analogue formats, are provided for direct feed into the baseband inputs of the TV. Internet access is provided through network connectivity to an internet

service provider (ISP). The processor is capable of transmitting and receiving TCP/IP packets, thus enabling web-page browsing and video streaming.

Modern TV architectures are very similar to the STB, except that the TV also needs processor functionality to control baseband video display and audio reproduction subsystems. In addition, the processor needs to be capable of processing numerous baseband inputs for video and audio signals in analogue and digital formats. It is noteworthy that the STB RF tuner, demodulator and internet functions are duplicated in the TV, which is unnecessary if the consumer is using a STB for primary reception of broadcast and internet based content.

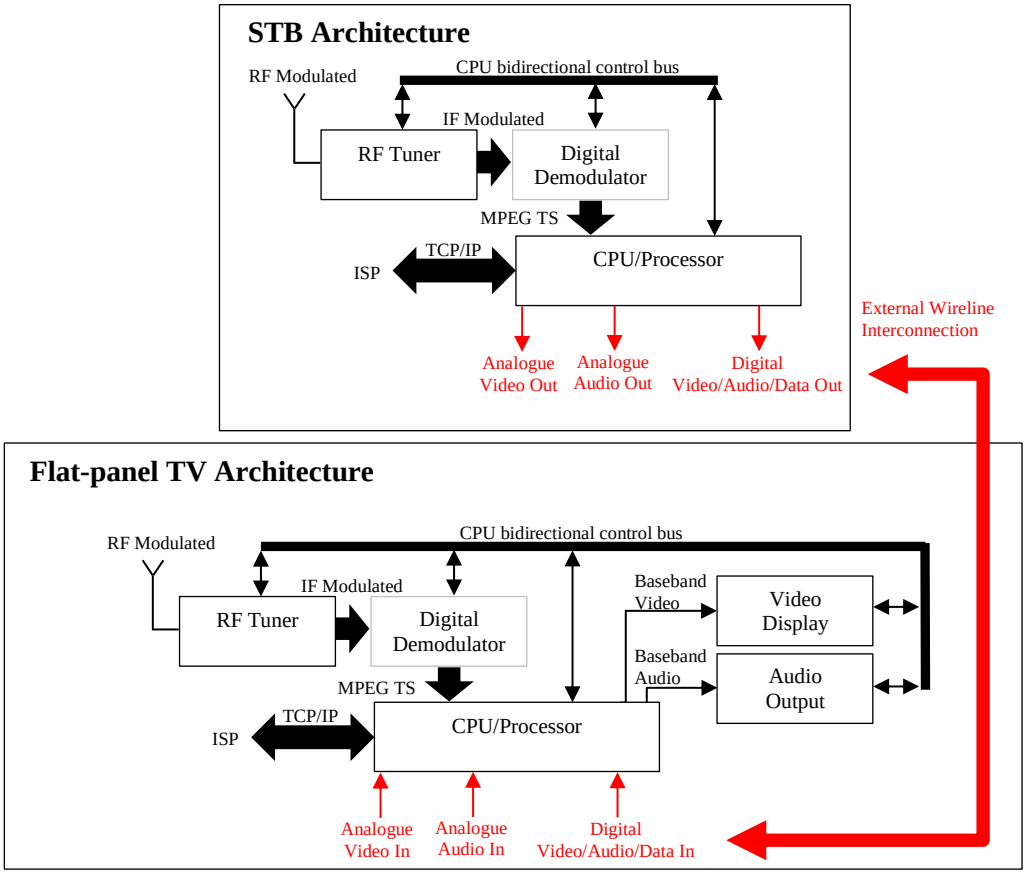


Figure 1-5 Simplified block diagram of current DVB STB and TV architectures

In both the STB and TV architectures, the processor lies at the core of the system, providing the necessary processing of internet and broadcast services. It also controls subsystems within the STBs via a bidirectional control bus, which uses the inter-integrated circuit (I^2C) protocol, developed by NXP Semiconductors (formerly known as Philips Semiconductors).

Provided with the evidence that analogue peripherals will most likely be eliminated in the future, and that physical media such as DVD and Blu-ray are replaced by online streaming services, cost savings and design simplification opportunities are achievable by using a connector-less and region-less TV architecture. The bill-of-materials (BOM) of the TV can be reduced by relocating the RF tuner and demodulator functions to the external STB; this also eliminates duplication of these blocks in the TV. Further cost reduction and simplification of the TV is achieved through elimination of all baseband connectors, and associated support circuitry, PCB area, and software overhead. Also, region specific compliance testing of the tuner and demodulator and connector interfaces would only be necessary for the STB.

Another potential cost saving arising from the elimination of the tuner and demodulator from the TV, is that some countries levy an importation tariff on TVs fitted with RF tuners (HMRC, 2019). These tariffs might be circumvented, or at least reduced, if the TV is reclassified as a monitor. This of course is more of a legal challenge than a technical one, but it may be of significance to TV manufacturers attempting to reduce cost per unit produced. Of course, the STB will still incur the tariff, but if the tariff is imposed as a percentage of the total cost of the product, the STB will incur a lower tariff than a high cost TV.

Using the TCP/IP and MPEG TS as the common baseband interfaces for the wireless link between the STB and TV, a new conceptual architecture is envisioned as shown in the functional block diagram of Figure 1-6.

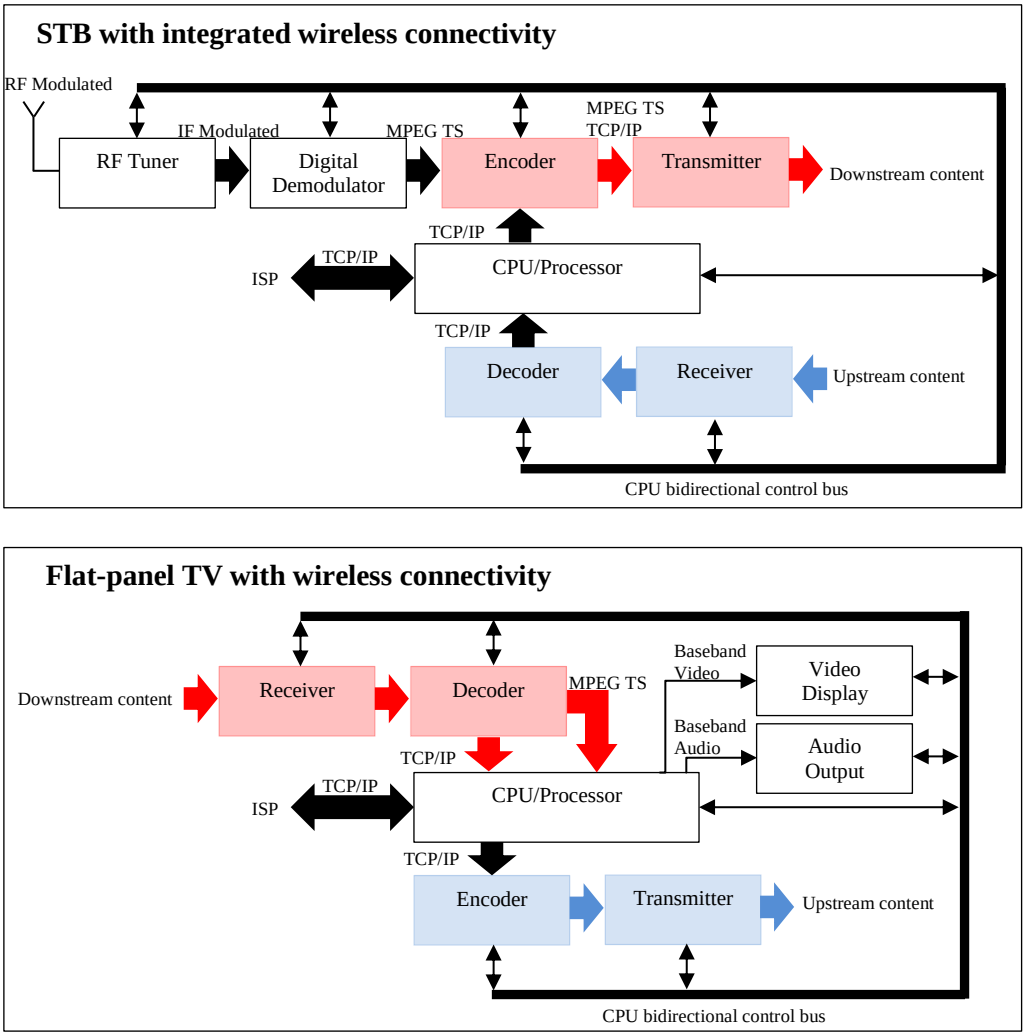


Figure 1-6 Conceptual block diagram of a broadcast (MPEG TS) and internet (TCP/IP) wireless distribution system (author generated image)

In this bidirectional architecture, the STB blocks remain largely the same, except that all interfaces, excluding TCP/IP and broadcast RF tuner connectivity, are eliminated, and replaced with encoder and transmitter blocks (highlighted in pink) which provide downstream connectivity to the TV. These blocks interface directly with the MPEG TS

and TCP/IP streams and suitably re-encode them to enable transmission over a wireless channel. Upstream connectivity from TV to STB is provided by receiver and decoder blocks (highlighted in blue) which enable upstream TCP/IP traffic, such as web-page requests. It is also worth noting at this point that interleaving of downstream TCP/IP and MPEG TS packets is not possible in this architecture, as is the case with modern smart TVs which do not permit simultaneous web-browsing and viewing of broadcast TV.

In the TV, all RF and baseband interfaces, as well as the tuner and demodulator blocks are eliminated. Receiver and decoder blocks (highlighted in pink) enable downstream connectivity from the STB. Upstream connectivity to the STB is enabled by encoder and transmitter blocks (highlighted in blue).

Communication between the STB and TV processors to enable channel scanning, channel selection and other system control commands is managed using existing IR remote control commands; note that the blocks for this part of the system are not shown for clarity.

Ideally, all new blocks introduced into the STB and TV architectures could be integrated into the processor and interfaced directly with the MPEG TS and TCP/IP buses, but again for clarity, they are shown as external blocks.

Note: Bluetooth connectivity could be included in the architecture to allow consumers to connect digital audio output to external Bluetooth enabled audio amplifier or speaker systems.

The following sections present the current connectivity technologies, such as Wi-Fi and power-line, that could be used for distributing broadcast content within the new architecture; the disadvantages of these technologies is discussed. VLC as an alternative

or complement to these technologies is introduced, along with compelling reasons why VLC is the preferred connectivity technology for this new TV architecture.

1.1.6 Wi-Fi

One technology that can be used for content distribution is Wi-Fi. Many of the TVs available on the market today are capable of receiving content through Wi-Fi, which uses bidirectional packet based transmission. In this system the content is encoded using TCP/IP, and then the packets are transmitted using direct-sequence spread spectrum (DSSS). Wi-Fi standard 802.11b uses DSSS, while 802.11a (5 GHz), 802.11g (2.4 GHz), 802.11n (2.4 or 5 GHz) and 802.11ac (2.4 or 5 GHz) use orthogonal frequency-division multiplexing (OFDM) (Gast, 2005). However, using Wi-Fi based schemes for streaming content can be demanding on the RF bandwidth of such systems, leading to capacity issues, especially in densely populated areas where there are many Wi-Fi transmissions taking place. Even if bit rates were reduced in order to limit bandwidth, TVs might need to increase memory storage capability to support buffering, which ultimately leads to an increase in the cost of the TVs. Buffering, via memory storage, also increases the delay between the selection of the desired content and it being displayed on the TV, which ultimately degrades the consumer experience. Furthermore, Wi-Fi systems are susceptible to electrical interference, and if interference levels are high enough, it can lead to signal dropout.

Wi-Fi transmissions also suffer from an inherent security weaknesses caused by the fact that RF signals can penetrate the walls of buildings and therefore can be broadcast beyond the consumer premises. This means that the transmission can be intercepted and the content accessed by potential eavesdroppers. This is of particularly concern when the content has been purchased by the consumer, as is the case with scrambled content

streamed from a pay-per-view channel requiring subscription and/or a conditional access (CAS) card. In such cases the eavesdropper can directly intercept the streamed content, and with appropriate de-encryption keys, access it.

In terms of the coverage ranges of the most commonly used Wi-Fi standards, such as 802.11b, 802.11g and 802.11n, the first two standards have typical indoor coverage ranges of around 50 metres, and the later around 100 metres (Gast, 2005). These ranges are optimistic and can be significantly reduced by obstructions in the consumer premises, such as brick or concrete walls and metal frameworks.

1.1.7 Power-Line

Although not a wireless based technology, an alternative to Wi-Fi is power-line networking. Using this method, all interconnects to the TV are eliminated with the exception of the power cable. In this case the cable has a dual purpose, where not only is it used to provide power to the TV, it is also used as a transmission line to transmit content. An OFDM signal, modulated with TCP/IP packets, is combined with the mains supply voltage to enable delivery of data to the TV (Ferreira, 2010). Initially, this type of system seems an excellent method to minimise the number of interfaces, however, there are issues associated with this approach. Firstly, the mains power network in consumer premises was designed to carry a 50 Hz (UK and Europe) or 60 Hz (North America) sine wave, and the transmission of video, audio and data content requires much higher frequencies to be supported. Higher frequencies in the power network are highly attenuated as a function of per unit length of the cable, resulting in the reduced transmissions range. Also, power networks in consumer premises are completely unshielded and susceptible to ingress from radiating electromagnetic fields, such as switching transients from lightning, and appliances with motors such as washing

machines, refrigerators and vacuum cleaners. Also, conducted noise and interferers from other devices such as switched-mode power supplies (SMPS), fluorescent lights and any other unfiltered appliances can disrupt OFDM transmissions resulting in signal dropout. This lack of shielding also means that eavesdropping is possible, but to a lesser extent, since the radiated fields from such systems do not have the same range as Wi-Fi based systems.

In addition, power-line systems, because they interface with the mains power system, must comply with stringent safety standards (Innocenzo, Bucci, Fiorucci, & Ciancetta, 2017).

In order to maximise data throughput and alleviate capacity issues with Wi-Fi, systems have been developed that utilise both Wi-Fi and power-line transmission technologies in parallel (Ali, Liu, Pefkianakis, & Kim, 2018). This has been undertaken to enable continuous data throughput in the event of either Wi-Fi or power-line suffering from interference events or capacity issues within the respective channels. This approach does reduce the probability of dropout, but it greatly increases the cost and complexity of the system. One particular problem is that determining the handover from one transmission system to the other without causing dropout.

1.2 VLC

1.2.1 System Architecture

The issues related to Wi-Fi and power-line transmission technologies, give rise to opportunities for VLC technologies, which are largely free of such issues and constraints. In this section, the main blocks and operation of a VLC system are

presented, along with the key advantages of VLC over Wi-Fi and power-line technologies.

VLC systems are a subset of optical wireless communication (OWC) systems, which is defined as any form of telecommunications that uses light as the transmission medium (Dimitrov, 2015). Infrared communication (IRC) systems use wavelengths in the electromagnetic spectrum region from 780 nm to 950 nm, and VLC systems use visible light wavelengths from 375 nm to 780 nm (Lee, 2011).

OWC systems can use either visible or IR wavelengths to transmit information. Figure 1-7 shows the block diagram of a free-space OWC system capable of transmitting and receiving digital data (Minh et al., 2009).

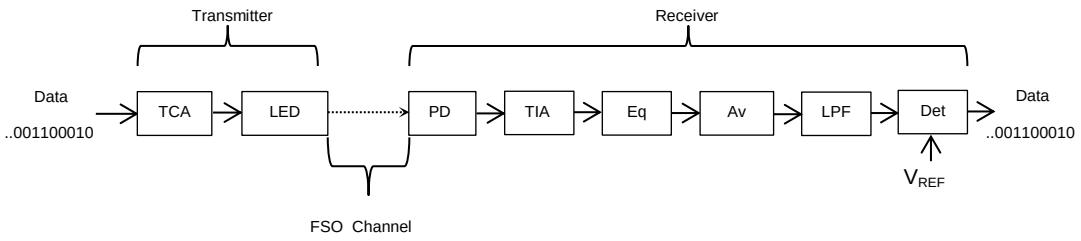


Figure 1-7 Block diagram of a OWC system (author generated image)

The simplest form of transmitter uses intensity modulation (IM), whereby the intensity of the light emitted by the source, in this case an LED, is directly proportional to the voltage of the modulating signal. This type of modulation is achieved using a transconductance amplifier (TCA) to convert the alternating electrical voltage of the modulating signal into drive current for the LED. The modulated light emission is then transmitted over a FSO channel, which exhibits an inverse square attenuation relationship between transmitter and receiver, and a Gaussian impulse response.

At the receiver, direct-detection (DD) is used to detect the changes in the intensity of the received light. A photodetector (PD) is used to convert the received modulated light into a photocurrent which is proportional to the received light intensity. A transimpedance amplifier (TIA) then converts the current back into a voltage. An equalisation stage (Eq) compensates for the non-flat frequency response of the LED and optical channel. Following equalisation, a voltage gain stage (Av) is used to increase the received signal level and a low-pass pre-detection filtering (LPF) is then applied prior to threshold detection (Det) of the signal. Note that suitable encoding and decoding of the data is necessary at the transmitter and receiver, respectively to enable transmission over the FSO channel.

1.2.2 Advantages of VLC Systems

A controversial and often debated topic in the scientific community is whether human exposure to RF and microwave frequencies is safe. No such controversy exists about the safety of visible light, as humans have been exposed to visible light wavelengths for millennia with no documented adverse effects (Dimitrov, 2015). Also, the human eye has evolved a natural reflex response to intense visible light, whereby the eyelid closes, or blinks, to protect the retina from damage. IRC systems, however, use wavelengths invisible to human eye, and therefore can potentially damage the retina, since the blink response is defeated.

In terms of regulatory compliance, RF and microwave emission limits are strictly enforced by Federal Communications Commission (FCC) regulations in the United States (US) and by European Directives in the European Union (EU). The European Telecommunications Standards Institute (ETSI) and the European Committee for Electrotechnical Standardization (CENELEC) specify these limits, such as spectral

profile limits, maximum spurious emissions and maximum radiated power. For example, the ETSI equivalent isotropically radiated power (EIRP) of a 2.4 GHz Wi-Fi transmission using DSSS modulation is +18 dBm (63 mW), and that of an OFDM transmission is +20 dBm (100 mW) (ETSI, 2014a). 5 GHz transmissions have a maximum EIRP of +30 dBm (1000 mW) (ETSI, 2014b). Wi-Fi equipment manufacturers must comply with these strict specifications or risk prosecution.

In contrast to RF and microwave, VLC systems use an unlicensed and unregulated region of the electromagnetic spectrum, enabling such systems to be produced without regulatory compliance testing or spectrum licensing. However, the optical power output of the light emitting devices used in these systems is regulated. In particular, lasers are strictly regulated due to low-divergence angle and coherent monochromatic emissions; coherent meaning that wavelength of the emissions are in phase in space and time, and monochromatic meaning that the emitted light is concentrated at a single wavelength. The combination of these properties results in lasers being able to concentrate large amounts of energy into a very small area, making them an eye safety hazard. Safety standards exist, such as the International Electrotechnical Commission (IEC) 60825-1:2014 (IEC, 2014) and US 21 Code of Federal Regulations (CFR) Part 1040 (FDA, 2018), which state the safety requirements by categorising lasers into '*classes*', which are defined by the lasers power and wavelength.

Solid-state lighting (SSL), which uses white LED technology, emerged in 1996 (Schubert, 2006) and is continuing to rapidly replace lower efficiency incandescent, fluorescent and halogen technologies. SSL, due to the fact semiconductor devices permit high frequency switching, is also enabling the coexistence of VLC systems within the lighting infrastructure. These systems are also subject to optical power output

restriction, however, white LED emissions differ compared to those of lasers. White LEDs have high-divergence angle, non-coherent polychromatic emissions; non-coherent meaning that wavelength of the emissions are out of phase in space and time, and polychromatic meaning that the emitted light is distributed over multiple wavelengths of the spectrum. The combination of these properties means that the energy emitted by LEDs is distributed both spatially and spectrally, and is therefore significantly less of an eye safety hazard than lasers. Similar to lasers, safety standards exist for LEDs, such as the IEC 62471 '*Photobiological safety of lamps and lamp systems*' (IEC, 2008), and the American National Standards Institute (ANSI) RP-27 (ANSI/IESNA, 2013). The IEC 62471 standard provides guidance for evaluating the photobiological safety of LEDs and specifies the exposure limits using '*risk group*' categories.

Even though, the light source used in VLC systems is controlled, this is only for high-power LEDs and lasers, and generally there is no other regulatory requirements imposed on VLC systems.

Another advantage of VLC is that visible light transmissions are immune to electrical interference, and therefore the modulated light signals are not impaired by electrical noise or spurious signals, which it has been shown is not the case with Wi-Fi and power-line systems.

Visible light also addresses the problem of security; as the opportunity for eavesdropping is extremely limited, since visible light is highly directive and cannot penetrate walls. The coverage range of VLC systems can therefore very easily be restricted within the consumer premises.

1.2.3 Physical Arrangement

The simplest form of VLC system uses directed line-of-sight (DLOS) transmission, where the light emitting source has a direct and unimpeded transmission path to the PD. Figure 1-8 shows the author's interpretation of a gimbaled LED mounted to the ceiling of a room. The light emission from the LED has a DLOS transmission path to the PD fitted to the front panel of the wall-mounted TV. In this physical arrangement, the LED can be rotated through 360° in the horizontal plane and tilted up to 90° in the vertical plane, enabling the LEDs light emission to be optimally positioned for DLOS transmission to the PD. Alignment and focussing of the transmission onto the PD is simple, due to the fact that the LED emission is visible. This simple alignment and focussing is not possible if an IR based LED is used. Note that cowlings, containing concentrators (lenses) for collimation, can be used over the LED and PD to assist with directivity of the emission.

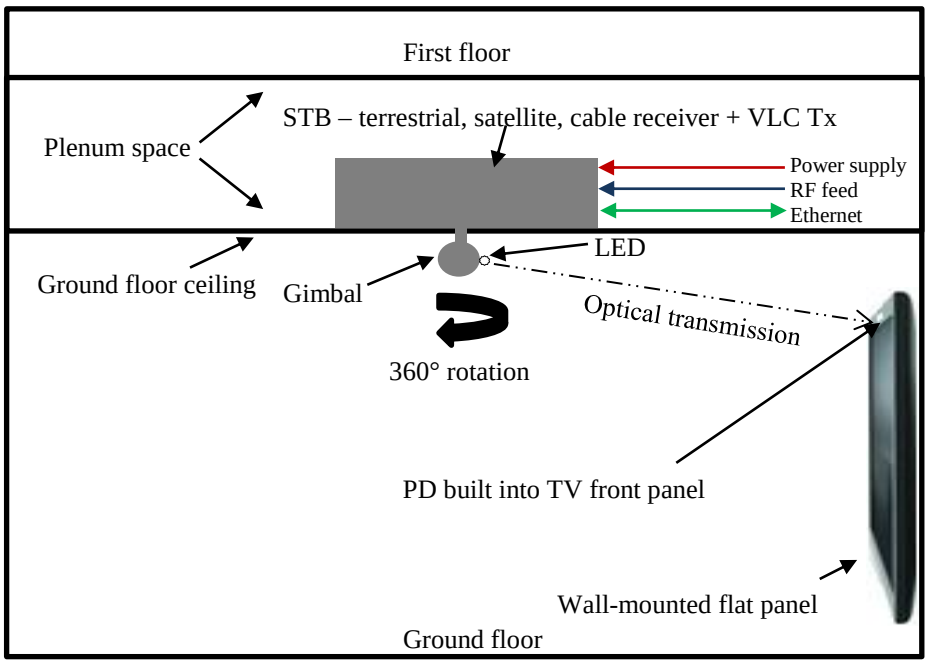


Figure 1-8 Gimbaled LED transmitter and target TV fitted with a PD (room side view) (author generated image)

The required power supply and modulating signal for the LED is provided by a STB with integrated VLC system, located in the plenum space, directly above the gimbaled LED. The key advantage of using the plenum space is that it can be used without chasing or fitting conduit to the walls of the room. The mains power for the STB can be taken from a lighting circuit in the plenum space; STB power consumption is, typically, under 10 W. Furthermore, accessing cabling from antennas, satellite dishes, and cable networks for broadcast and internet connectivity is more convenient for an installer, and less disruptive to the consumer premises. Also, locating the STB in the plenum space effectively releases floor space in the room, and means that the receiver technology is now invisible to the consumer.

Figure 1-9 shows a plan view of the room, and indicates how the 360° horizontal rotation of the gimbal enables the TV to be positioned on any wall within the room. The only consideration needed is the power cable for the TV.

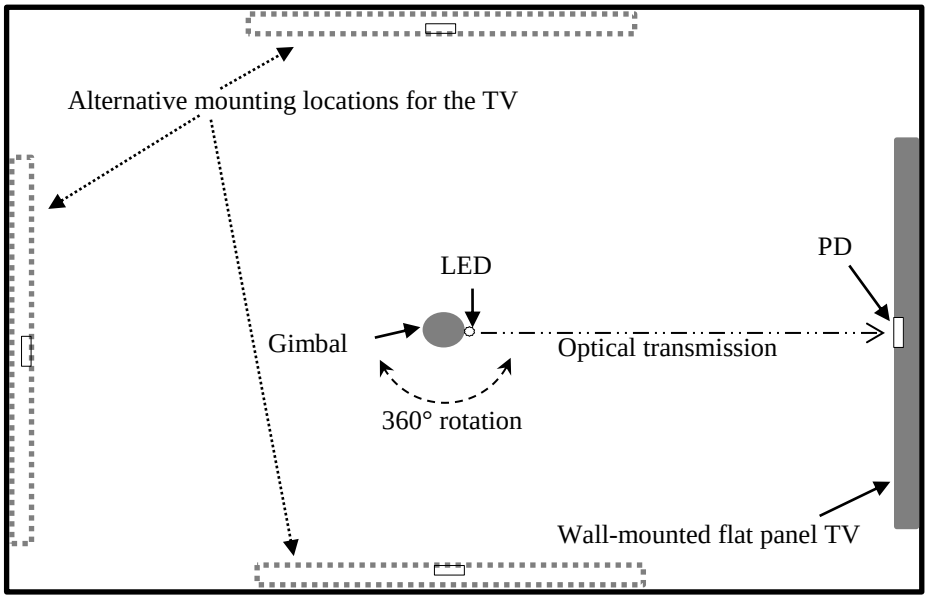


Figure 1-9 Gimbaled LED transmitter and target TV fitted with a PD (room plan view) (author generated image)

1.2.4 Proof-of-Concept System

The primary focus of this work is to produce a proof-of-concept, LED based FSO VLC system to distribute DVB HDTV content to wall-mounted TVs. An LED based transmitter was chosen due to its lower cost and less stringent eye safety requirements than that of a laser.

The scope of the architecture investigated in this work is a subset of the bidirectional architecture presented in Section 1.1.5, and is shown in Figure 1-10. This subset differs from that presented in Section 1.1.5, in that it does not support TCP/IP connectivity and upstream communication, and instead enables only the unidirectional, downstream broadcast MPEG TS connectivity. This was done to reduce the complexity of the system, and make the realisation of the system achievable within the timeframe of the research work.

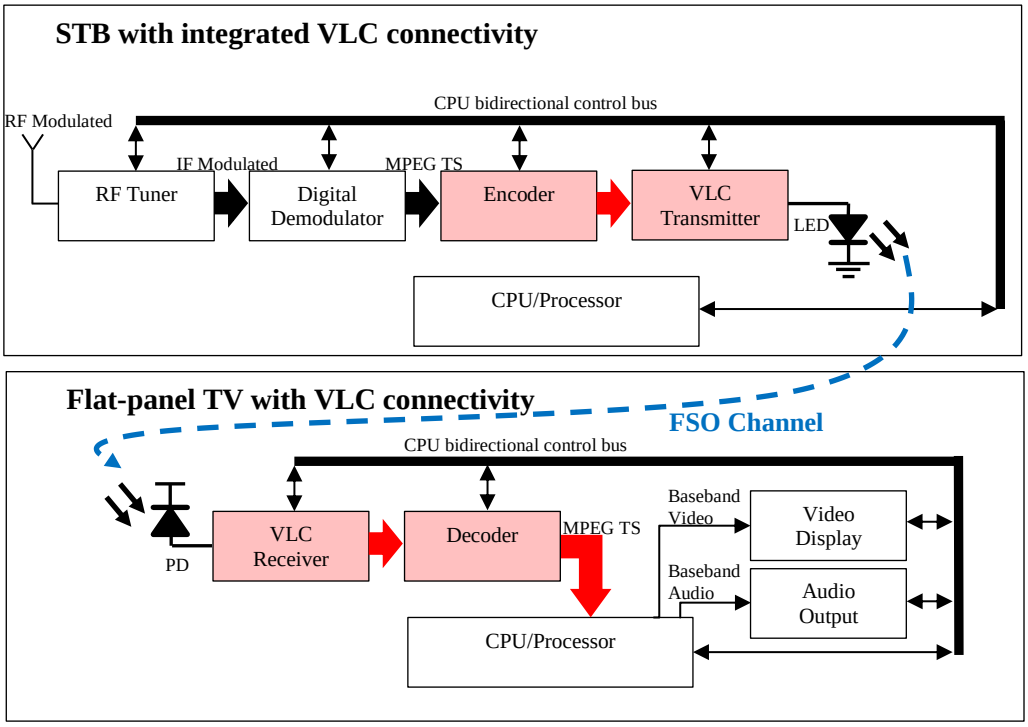


Figure 1-10 Proof-of-concept block diagram of a VLC broadcast (MPEG TS) distribution system (author generated image)

The DVB-T/T2 broadcast standard is used because DVB-T/T2 STBs are widely available, low-cost, and unlike DVB-S/S2 and DVB-C/C2 STBs, do not require specialist installation or subscriptions to enable network connectivity. Furthermore, DVB-T/T2 STBs also have the lowest output bit rate of 50 Mbit/s which is considered achievable for this system.

1.3 Aims and Objectives

The main aims of this work were to analyse, design, implement and evaluate a unidirectional, LED based, FSO VLC HDTV video distribution system using consumer grade STB receiver technology.

1.3.1 Aims

The primary aims of the work were to:

1) Produce an LED based, FSO VLC unidirectional HDTV distribution system.
2) Produce a FSO VLC transmitter and receiver system that interfaces directly with existing DVB MPEG TS buses used in consumer grade STBs.
3) Produce a link bit rate of at least 50 Mbit/s to support DVB-T2 broadcasts.
4) Demonstrate end-to-end transmission of MPEG TS content, and successfully display recovered content on an HD monitor.

1.3.2 Objectives

The specific objectives of the work were to:

1) Implement the system using low-cost terrestrial STBs
    a. Source STB for receiving off-air DVB-T/T2 content. Providing RF to MPEG TS.

b. Sink STB capable of decoding MPEG TS and supporting HDMI baseband output, enabling display on an HD monitor.

2) Fully analyse MPEG TS and design a modulation scheme capable of re-encoding the MPEG TS for transmission over a visible light FSO channel.
3) Select an appropriate LED type for the system based on optimal characteristics.
4) Select an appropriate type of receiving PD for the system based on optimal characteristics.
5) Design and develop circuitry to modulate the transmitting LED based on the modulation scheme.
6) Design and develop appropriate pre and post-gain stages and filtering for the receiver.
7) Design and develop passive equalisation circuitry in the receiver to overcome bandwidth limitations of the LED.
8) Implement MPEG TS encoding and decoding using a field programmable gate array (FPGA) platform.
9) Design and develop appropriate comparator circuitry to detect the received re-encoded MPEG TS.

1.4 Original Work

The system presented is currently the only published VLC system that interfaces directly with MPEG TS of consumer grade STB to form an end-to-end VLC distribution system. The main areas of original contribution are:

1) The system and subsystem level design and implementation of a new end-to-end VLC video distribution system that interfaces directly with the MPEG TS of consumer grade DVB-T/T2 STB technology, directly re-encoding the TS for

transmission over a FSO channel, without modifying the software or hardware of the STB.

2) The design and implementation of a new modulation scheme permitting transmission of DVB-T/T2 broadcast HDTV content over a FSO channel without the use of error correcting codes.
3) The design and implementation of a switching circuit, working in conjunction with the new modulation scheme, to enable intensity modulation of an LED to achieve transmission of content over a FSO channel.

1.5 Thesis Structure

This thesis is structured in the following manner:

Chapter 2

Presents a literature review of the DVB transmitter and receiver system, with particular emphasis on the DVB-T and DVB-T2 standards. The MPEG TS bus is analysed at the physical layer, in order to determine the requirements for serial transmission over the FSO by the VLC system.

A review of modern FSO VLC systems based on non-coherent LED light sources is also presented. An overview of the emergence of VLC is given, followed by a brief history of the evolution of LEDs which then leads into the development of VLC systems. Theoretical information relating to channel models, modulation schemes, and LEDs and PDs and their supporting circuitry is given.

Chapter 3

The proposed coding scheme for the VLC system is presented.

Chapter 4

Presents the characterisation measurements and analyses of the MPEG TS source and sink devices, and the LED required for the hardware implementation of the VLC system.

The findings of this chapter were key to determining the bandwidth requirements of the entire system, and the type and amount of bandwidth compensation applied to the LED. The findings were used in the modelling of the system in Chapter 5.

Chapter 5

Presents the definition, design and simulation of the VLC system.

Chapter 6

Presents the hardware implementation of the VLC system.

Chapter 7

The comparison between measured and simulated results of the system is presented.

Chapter 8

Provides discussion of the on the final VLC system.

Chapter 9

Conclusions regarding the overall achievements are provided, along with suggestions for further work.

2 Literature Review and Theory

This chapter presents a theoretical review of the DVB transmit and receive path used, respectively, to encode and decode broadcast video, audio and data content. A detailed system overview of the DVB transmitter and receiver is provided, with particular emphasis on the DVB-T and DVB-T2 standards. The encoding and multiplexing of the MPEG TS in the transmitter, and demultiplexing and decoding in the receiver is presented, along with a detailed analysis of the physical layer of the MPEG TS bus at the DVB receiver.

A review of modern FSO VLC systems based on non-coherent LED light sources is also presented. An overview of the emergence of VLC is given, followed by a brief history of the evolution of LEDs which leads into the development of VLC systems. The theory of channel models, modulation schemes, and LEDs and PDs and supporting circuitry is also given.

The Chapter concludes with a proposed candidate for the modulation scheme of the VLC system, which enables the re-encoding the MPEG TS bus, suitable for FSO transmission.

2.1 DVB MPEG TS Bus

It was identified in section 1.1.4, that DVB terrestrial, cable and satellite standards all use different channel coding and modulation schemes. However, it was also identified that all three standards use a common baseband, highly compressed, serial data bus called the MPEG TS in both the transmitting and receiving systems. Furthermore, it was identified that this MPEG TS could be suitably re-encoded, enabling it to be transmitted over a FSO channel. Before VLC systems and FSO modulation schemes are introduced;

it is necessary to understand how the MPEG TS is generated at the broadcast transmitter, and how it is processed at the consumer receiver.

2.1.1 DVB Transmit Path

The key blocks in a DVB transmitter are shown in Figure 2-1.

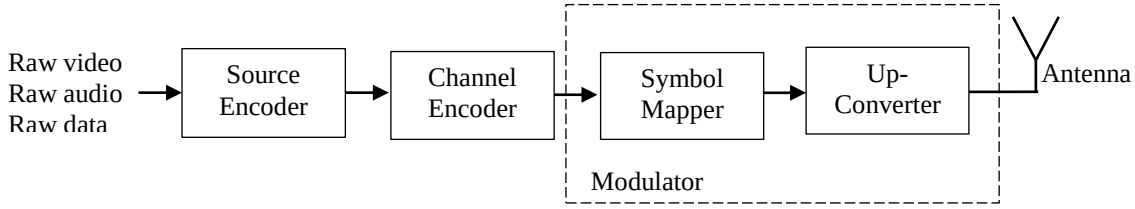


Figure 2-1 DVB transmitter (author generated image)

The first block in the transmitter is the source encoder, which compresses the video, audio and data streams of the broadcast. The primary function of the encoder is to reduce the bit rate of all three data streams by removing redundancies from the picture, audio and data content. The resulting reduced bit rate stream improves the spectral efficiency of the transmission and also enables the transmission of multiple video, audio and data streams over the same bandlimited RF channel; 8 MHz maximum channel bandwidth for DVB-T/T2 transmissions. Video encoding is applied as per the required picture definition: SD, HD or UHD. Table 2-1 shows the relative bit rates for pre- and post-video compression.

Standard	**Video Codec**	**Picture Resolution**	**Pre-compression bit rate (Mbit/s)**	**Post-compression bit rate (Mbit/s)**	**Bit rate reduction (%)**
SD (8-bit)	MPEG-2 H.262	720 pixels 576 line Interlaced/progressive	165	3.5	97.88
HD 1080i (8-bit)	MPEG-4 AVC H.264	1440 pixels × 1080 lines	622	9.6	98.46
HD 720p (8-bit)		1280 pixels × 720 lines	737	10	98.64
UHD (10-bit)	HEVC H.265	3840 pixels × 2160 lines progressive	8300	40	99.52

i = interlaced scanning and p = progressive scanning

Table 2-1 Relative video bit rates (Bing, 2015)

The audio signal is also encoded, typically using MPEG 2 audio layer I and II codec. Following compression, the source encoder multiplexes, or interleaves, multiple compressed video, audio and data streams into a single stream referred to as the transport stream (TS) or MPEG TS; note that headers and additional information are added to the MPEG TS to enable correct decoding at the receiver. The MPEG TS is then passed to the channel encoder, which is optimised for the broadcast channel type used, and adds bits to the TS to enable error detection and correction at the receiver; this is referred to as forward-error correction (FEC). The bandwidth of the TS is increased slightly due to the addition of these redundant bits, but the benefit of error detection and correction makes the transmission more robust to noise and other channel impairments, and outweighs the slight bandwidth increase. Two layers of channel coding are used for DVB-T and DVB-T 2 transmissions. DVB-T uses inner convolutional coding (CC) and outer Reed-Solomon (RS) coding. DVB-T2 uses inner LDPC (Low Density Parity Check) coding and outer Bose-Chaudhuri-Hocquenghem (BCH) coding (NorDig, 2014); RS, LPDC and BCH are block codes. The channel encoder is an $n-k$ encoder, which means for every k number of bits input to the encoder, additional $(n-k)$ bits are added to enable error detection and correction at the receiver. The code rate of the encoder is defined by Equation 2-1.

$$Code\ rate = \frac{k}{n} \qquad \text{Equation 2-1}$$

Where k is the number of bits at the input of the encoder, and n is the number of bits at the output. The code rate is stated as a fraction, and the larger the fraction, the higher the coding rate; the more bits that are added to for error correction, the more robust the

transmission. Conversely, the smaller the fraction, the lower the coding rate and hence the less bits are added for error correction, resulting in a less robust transmission.

After channel encoding, the bit stream is then passed to the first block of the modulator, which is the symbol mapper. In this block, the bits in the bit stream are mapped to symbols using an in-phase (I) and quadrature (Q) constellation; this is fundamentally an Argand diagram with real and imaginary axis. For clarity, the simplest DVB modulation scheme, QPSK, is used to illustrate the modulation process. Figure 2-2 shows the constellation for QPSK modulation.

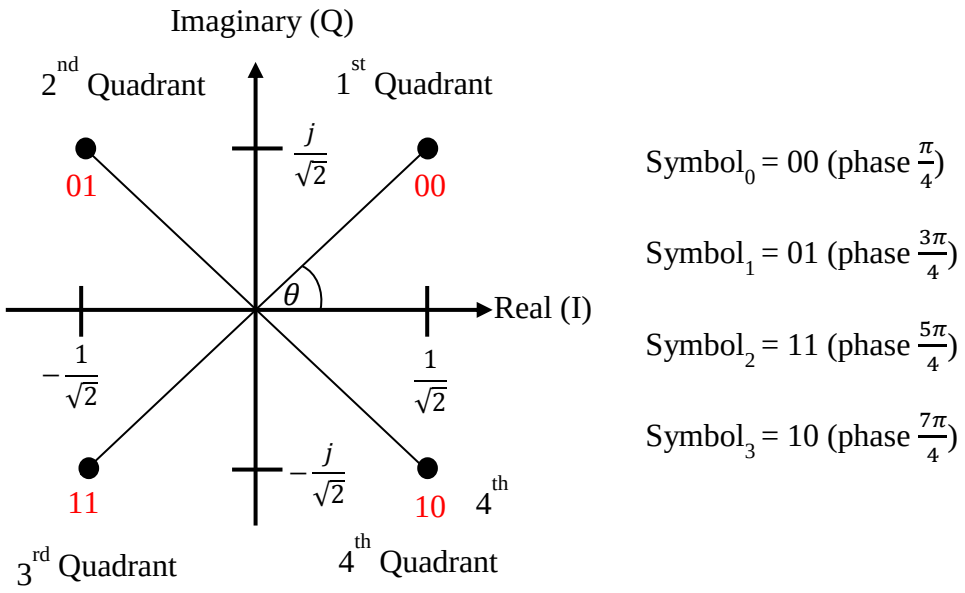


Figure 2-2 QPSK constellation (author generated image)

In this scheme, two bits of the bit stream are mapped to one of four symbols, where the number of symbols (M) in the constellation is determined by the number of bits (N) representing each symbol, as defined by Equation 2-2.

$$M = 2^N \qquad \text{Equation 2-2}$$

If the number of symbols is known, it is also possible to determine the number of bits per symbol using Equation 2-3.

$$N = log_2(M) \qquad \text{Equation 2-3}$$

The magnitude, or modulus, of the four symbols in the constellation is determined using the real (in-phase) and imaginary (quadrature) coordinates for each symbol position in the constellation, and the Pythagorean Theorem defined by Equation 2-4.

$$|r| = \sqrt{I^2 + Q^2} \qquad \text{Equation 2-4}$$

In QPSK, the magnitude of all four constellation points is unity.

The angle, or argument, for each constellation point, as shown in Figure 2-2 , is determined using Equation 2-5.

$$\theta = tan^{-1}\left(\frac{Q}{I}\right)\ (rad) \qquad \text{Equation 2-5}$$

The resultant angle of the constellation point in the first quadrant is $\frac{\pi}{4}$ radians, the second is $\frac{3\pi}{4}$ radians, the third is $\frac{5\pi}{4}$ radians, and finally, the fourth is $\frac{7\pi}{4}$ radians.

The angle of the symbol is then mapped to the phase angle of a cosine with a frequency of f_c and amplitude of unity, as defined by Equation 2-6.

$$S_i = cos\left[2\pi f_m t + (2i+1)\frac{\pi}{4}\right], \qquad -\frac{T}{2} \le t \le \frac{T}{2}, (for\ i = 0,1,2,3) \qquad \text{Equation 2-6}$$

Figure 2-3 shows the mapping of the constellation point angle to that of the cosine phase angle. The phase modulated cosine appears at the output of the symbol mapping block and is then passed to the up-converter block, which translates f_c to a high frequency carrier to enable transmission over its respective channel.

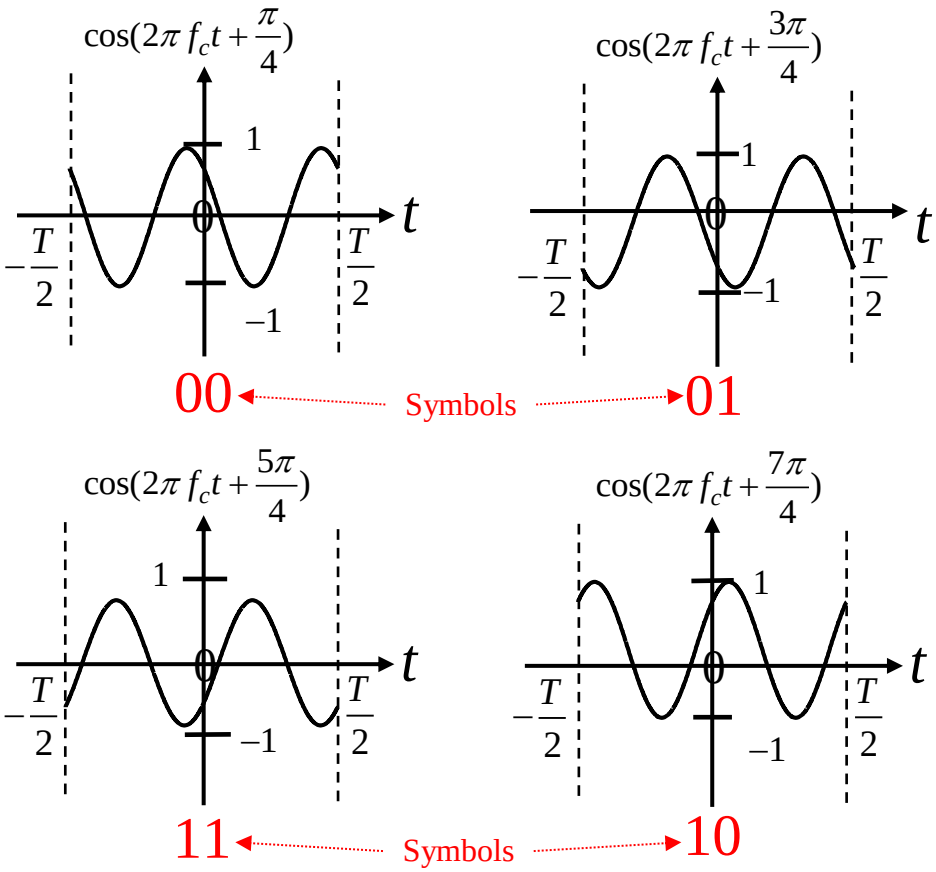


Figure 2-3 Constellation points mapped to cosine (author generated image)

All DVB modulation schemes are M-ary based, and generally use higher order constellations, where symbols are mapped to both amplitude and phase components of a carrier wave. Higher order constellations enable more bits per symbol to be transmitted over the channel, but at the cost of increased susceptibly to error from noise and other channel impairments. In conditions where the channel is highly impaired, the code rate of the transmission is increased to make the transmission more robust, and therefore increase the ability of the receiver to detect and correct errors. Furthermore, higher order constellations require higher performance receivers with low noise and clock jitter to enable successful de-mapping of symbols at the receiver (Bissell & Chapman, 1992).

The COFDM modulation scheme is used predominantly for DVB-T and DVB-T2 transmissions, since it has greater robustness against multipath interference, which is inherent in terrestrial transmissions. Multipath interference occurs when the direct transmission path, and an indirect transmission path caused by reflections from buildings and other objects, are received simultaneously. The indirect path, which is also referred to as an echo, is simply the direct path delayed in time. The direct and indirect paths can either constructively or destructively sum at the receiver. When constructive addition occurs, the receiver is able to detect bits without errors, but when destructive addition occurs, bits may be detected with errors.

COFDM reduces the effect of multipath by using discrete Fourier transform (DFT) techniques, which spreads the high bit rate, generated by digital TV broadcasts, over multiple, orthogonal, low bit rate sub-carriers within the broadcast channel (8 MHz maximum); note, increasing the number of sub-carriers, reduces the bit rate per sub-carrier. The term orthogonal means that the sub-carriers do not interfere with each other, since at the peak frequency of any one sub-carrier, the interaction of all the adjacent sub-carriers below the peak frequencies are at a null. Figure 2-4 illustrates the principle using five sub-carriers. Note that the number of sub-carriers used in real terrestrial broadcasts are described by the FFT mode. In the case of DVB-T, two FFT modes exist, one consisting of 2 k sub-carriers and one of 8 k sub-carriers (ETSI, 2009a). DVB-T2 has six FFT modes:- 1 k, 2 k, 4 k, 8 k, 16 k, and 32 k (NorDig, 2014).

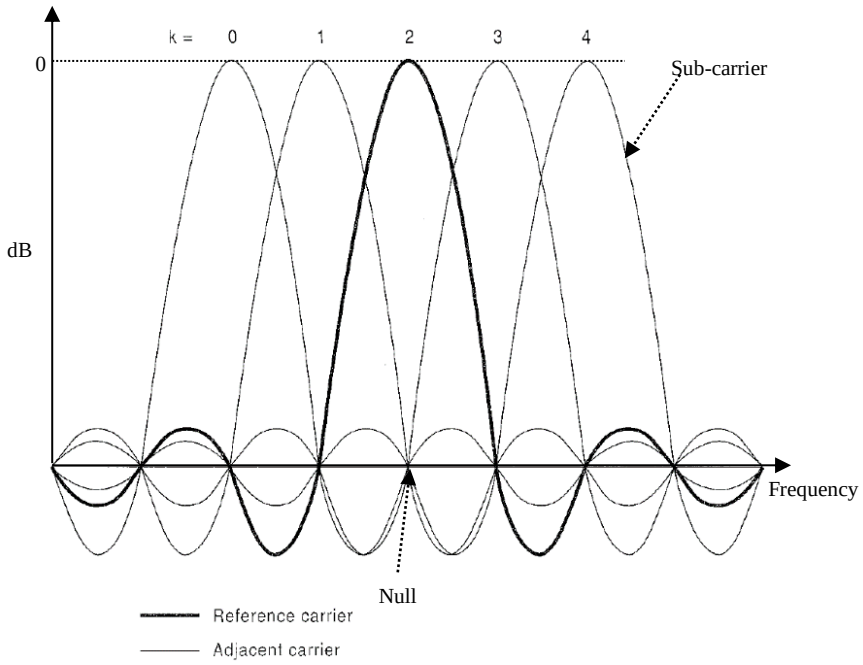


Figure 2-4 COFDM sub-carriers (Benoit, 1997)

In the event of destructive multipath interference, the orthogonality between sub-carriers is reduced, causing inter-symbol interference (ISI) and increased bit errors in the receiver. However, orthogonality is restored through the addition of a guard interval, or time delay, inserted at the beginning of each transmitted symbol. The guard interval is adjusted until multipath echoes occur only during guard interval and can be ignored by the receiver.

The spectrum of a DVB-T transmission, centred at DC (zero Hertz), and with an 8 MHz bandwidth, 2 k FFT mode and guard interval of $\frac{1}{4}$ is shown in Figure 2-5.

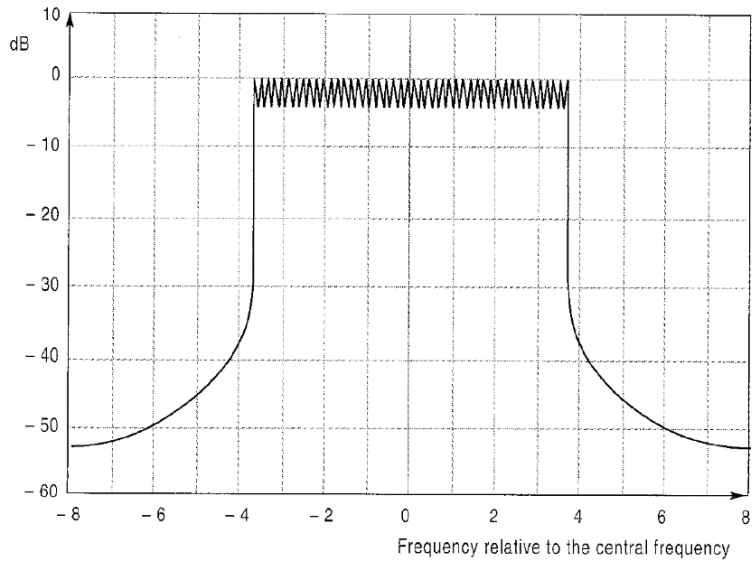


Figure 2-5 DVB-T transmission spectrum (Benoit, 1997)

The key parameters used for DVB-T and DVB-T2 transmission are summarised in Table 2-2. This is useful for understanding the MPEG TS characterisation presented in Chapter 4.

Parameter	DVB-T	DVB-T2
FEC type and Code Rates	CC and RS $\frac{1}{2}, \frac{2}{3}, \frac{3}{4}, \frac{5}{6}, \frac{7}{8}$	LDPC and BCH $\frac{1}{2}, \frac{3}{5}, \frac{2}{3}, \frac{3}{4}, \frac{4}{5}, \frac{5}{6}, \frac{6}{8}, \frac{8}{9}$
Modulation	COFDM	
Constellation	QPSK, 16 QAM, 64 QAM	QPSK, 16 QAM, 64 QAM, 256 QAM
Guard Interval	$\frac{1}{4}, \frac{1}{8}, \frac{1}{16}, \frac{1}{32}$	$\frac{1}{4}, \frac{19}{128}, \frac{1}{8}, \frac{19}{256}, \frac{1}{16}, \frac{1}{32}, \frac{1}{128}$
FFT modes	2 k, 8 k	1 k, 2 k, 4 k, 8 k, 16 k, 32 k

Table 2-2 DVB-T versus DVB-T2 (NorDig, 2014)

2.1.2 Source Encoding and Multiplexing: MPEG TS

The function of the source coder and generation of the MPEG-2 TS in the transmitter is now explained in greater detail. The expanded diagram of DVB source encoder block is shown in Figure 2-6, and consists of three encoder blocks, three packetizer blocks, a programme multiplexer and a transport multiplexer. Note that multiple packetizer and

programme stream multiplexer blocks exist in real systems, but only one of these blocks is shown here for clarity.

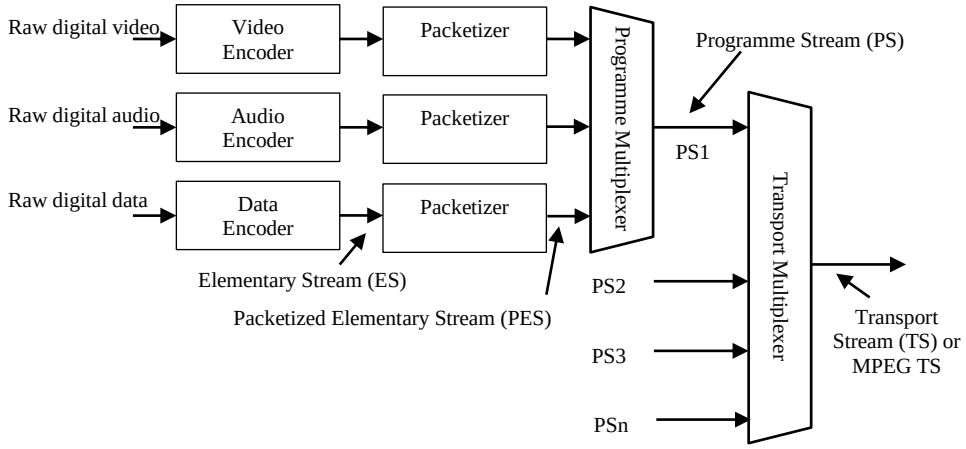


Figure 2-6 DVB MPEG encoding path (ISO, 2010)

The following operational description of MPEG TS encoding and multiplexing process is based on the ISO/IEC 13818-1 Information technology – Generic coding of moving pictures and associated audio information systems standard (2nd edition 01/12/2000) (ISO, 2010).

The first step in the generation of the MPEG TS, is to acquire the raw, uncompressed digital video, audio and data content. In the case of a live broadcast, independent digitised feeds are sourced from a TV camera and a microphone. The feeds are then compressed by the encoder blocks, using the applicable video and audio compression codecs e.g. MPEG-4 AVC/H2.64 for HD video and MPEG-2 for audio. The data stream is also compressed using a suitable data compression codec. The output signal of the encoder blocks is called the elementary stream (ES) and is a continuous, near-real time signal. The second step is to take the independent video, audio and data ESs and packetize them into variable sized data blocks. The output signal of the packetizer is referred to as packetized elementary stream (PES) and contains the PES packet, also

referred to as the PES payload, and an inserted header (PES header). The PES header indicates the start of the packet, and time stamping information to enable synchronisation of the video with the audio at the receiver. The third step is to multiplex the PESs for the video, audio and data into a continuous, variable length programme stream (PS). The final step is to take multiple PSs, represented by PS2, PS3 and Pn in Figure 2-6, and multiplex them into the MPEG TS. During the multiplexing process, additional metadata is also added to the stream, along with a header (TS header). The metadata consists of a programme association table (PAT), which registers all the PSs in the TS. Each item in the PAT points to a programme map table (PMT) which lists all the individual ESs contained in the PSs. Also, information about scrambled PESs is also carried in the metadata, and is necessary for pay-per-view channels requiring subscription and/or a conditional access. The MPEG TS consists of fixed-sized data packets (MPEG packets), each containing 188 bytes (1504 bits) (Tektronix, 2013). The TS header of each packet carries a PID. Packets in the same ES all have the same PID, so that the decoder in the receiver can select the correct ESs and reconstruct the video, audio and data streams prior to MPEG decoding. Figure 2-7 illustrates the packetization, multiplexing and addition of headers to the ES and PES. For clarity, only the packetization of a single ES and PES is shown, in reality the diagram contains multiple PSs. The fixed-sized TS packets consisting of 188 bytes (1504 bits) per packet including the TS header and payload data as shown. The packet size is consistent across all DVB standards (Benoit, 1997).

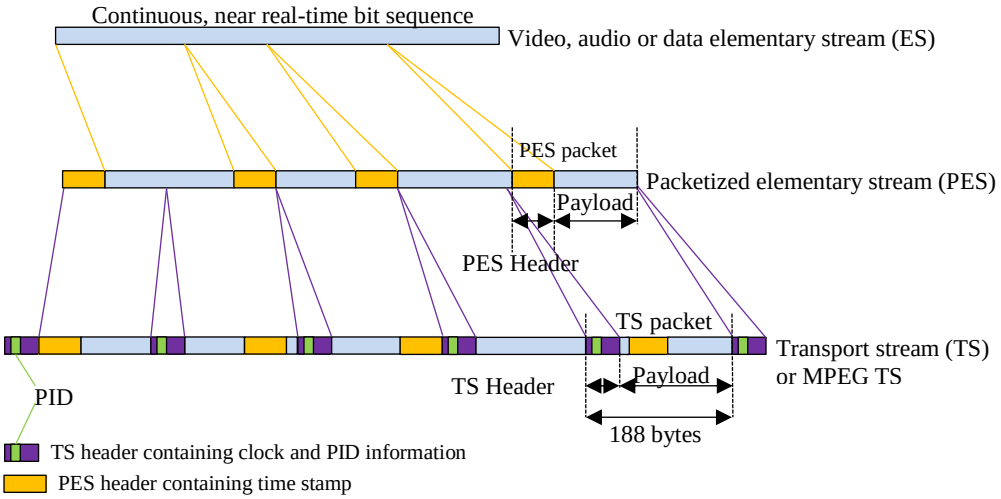


Figure 2-7 DVB multiplexing and headers (author generated image)

The formatting of the 188 bytes of MPEG TS packet is shown in Figure 2-8, with the key bytes highlighted. The TS header consists of 4-bytes of data; the sync byte, which occurs every 188 bytes and is represented by a constant value of 47_{hex}, and is used to synchronize the packet to the transport stream; a 1-bit transport error indicator, which at transmission is set to zero, can be set to one by the receiver demodulator if channel decoding fails to correct errors within the packet; and finally, a 13-bit PID which is used to identify the contents of the payload, and specifically identify the programme stream ESs contained in the packet. The remaining 184 bytes of the MPEG TS packet represent the programme stream data (Fischer, 2010).

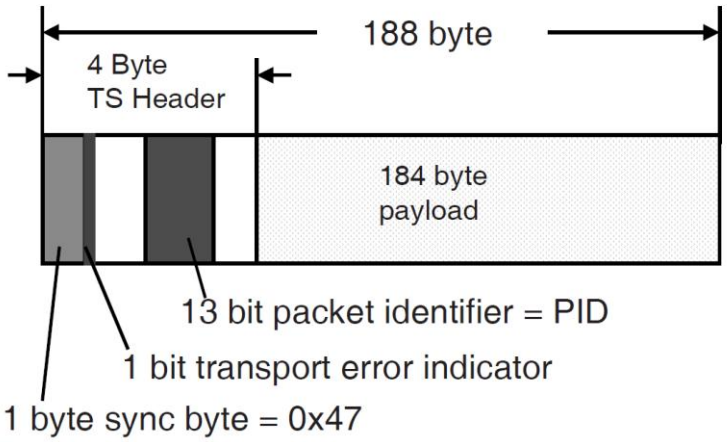


Figure 2-8 MPEG TS Packet (Fischer, 2010)

2.1.3 DVB Receive Path

The key blocks in a DVB receiver are shown in Figure 2-9.

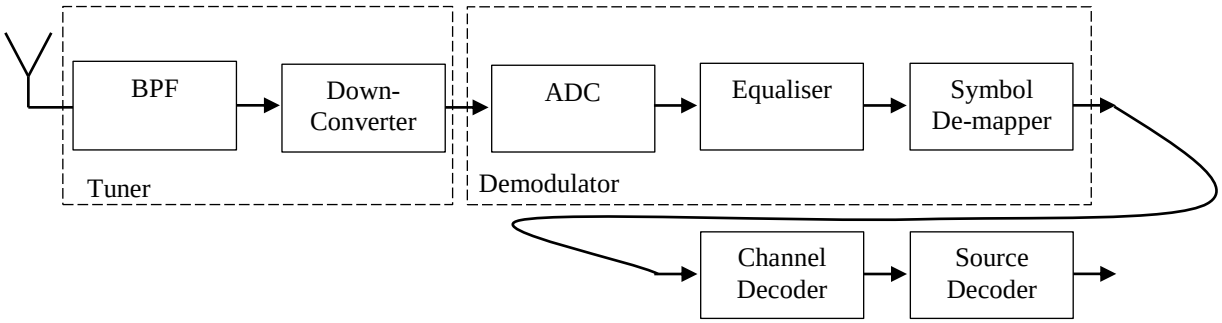


Figure 2-9 DVB receiver (author generated image)

The first block in the receiver is the tuner, which is required by each DVB broadcast standard (terrestrial, cable, satellite) to enable reception of content. The tuner is necessary to isolate and select the desired channel from a multitude of other channels in the RF spectrum, and then translate the channel to a lower frequency to enable further processing by the demodulator. The tuner isolates the desired channel using a band-pass filter (BPF) which reduces the band of received frequencies. Selection of the desired channel is then achieved using the down-converter, which tunes to the desired channels

RF centre frequency, and using frequency mixing, translates it to a lower common intermediate frequency (IF). Terrestrial and cable tuners generally use heterodyne mixing to achieve translation, where the desired channel RF centre frequency (RF_C) is combined in a mixer with a local oscillator frequency (LO) set to $RF_C + IF$ (high-sided LO). The mixer produces sum and difference frequencies at the output, and in the case of high-side LO, the difference signal is used as the IF. The IF is defined by Equation 2-7.

$$IF = RF_C \pm LO\ (Hz) \qquad \text{Equation 2-7}$$

Note that the IF refers to the centre frequency of the down-converted RF centre frequency (RF_C) of the desired channel.

It is also noteworthy, that satellite, and even some terrestrial tuners, use homodyne mixing, where the tuners LO is set to exactly the same frequency as the RF_C. In this case, the RF_C is down-converted to an IF_C centred at DC (zero Hz); this is also referred to as zero-IF.

Following down-conversion, the IF is presented to the demodulator, the first stage of which is the ADC, which digitises the IF so that it can be processed using DSP techniques. After digitisation, the digital signal is passed to the equaliser which performs channel estimation, and provides compensation for channel impairments. The signal is then fed to the symbol de-mapper which reverses the process of the symbol mapper in the transmitter by translating the amplitude and phase of the I and Q signals to a respective constellation point (decision point/boundary) and binary representation. Following de-mapping, forward-error correction is performed on the bit stream by the channel decoder, which checks for errors and, where possible, performs correction. In

the case of DVB-T content, convolutional (inner) decoding is performed by a Viterbi decoder, followed by RS (outer) decoding. In the case of DVB-T2, LDPC (inner) decoding is performed first, followed by BCH (outer) decoding. The channel decoder also calculates the bit-error rate (BER) of the bit stream from the ratio of the number or bits received in error, to the total number of bits received, as defined by Equation 2-8. The BER is based on the bit stream before the RS decoder in DVB-T and before the BCH decoder in DVB-T2.

$$BER = \frac{No.\,bits\ received\ in\ error}{Total\ no.\ \ bits\ received} \qquad \text{Equation 2-8}$$

Ideally, the BER should be zero following inner decoding, however, BER at or below the quasi-error free (QEF) limit of 2×10^{-4}, which is defined by the occurrence of a single error event every 30 minutes, is considered acceptable; note that a BER of 2×10^{-4} is a single bit in error, for every 5 k bits received without error (Benoit, 1997). The channel decoder also calculates the frame-error rate (FER), and tracks the number of uncorrectable MPEG TS packets; note the 1-bit transport error indicator in the TS header is modified when uncorrectable packets occur. In good reception conditions these parameters are at zero.

2.1.4 MPEG TS Demultiplexing and Decoding

The MPEG TS emerges from the channel decoder and is then fed to the source decoder which reverses the multiplexing and encoding performed by the source encoder at the transmitter.

The expanded diagram of DVB source decoder block is shown in Figure 2-10, and consists of a transport demultiplexer, a programme demultiplexer, three depacketizer blocks, and three decoder blocks.

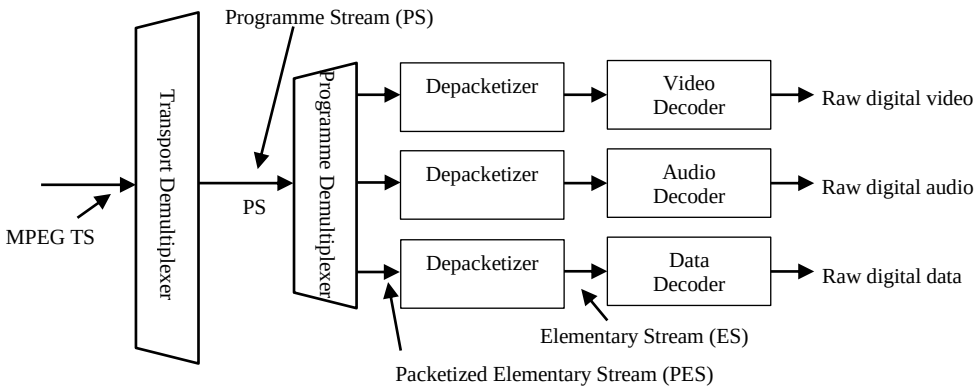


Figure 2-10 DVB MPEG decoding path (author generated image)

The following operational description of MPEG-2 TS demultiplexing and decoding process is based on the ISO/IEC 13818-1 Information technology – Generic coding of moving pictures and associated audio information systems standard (2nd edition 01/12/2000) (ISO, 2010).

Comparing the encoding of Figure 2-6 with the decoding of Figure 2-10, it is clear that the MPEG TS decoding is a mirror image of the MPEG TS encoding process. The purpose of demultiplexing and decoding of the MPEG TS is to recover the ESs from a programme stream selected by the consumer at the DVB receiver. In order to achieve this, the first task the transport demultiplexer performs, is to determine the start of a TS packet using the sync byte in the TS header. The sync byte always has a value of 47_{hex}, and occurs at intervals of 188 bytes. However, 47_{hex} can also occur within the payload data, so the receiver has to be able to differentiate between sync bytes and payload data bytes. Confirmation of valid sync byte is determined after five consecutive 47_{hex} bytes are detected (Fischer, 2010). Following the detection of the fifth sync byte the receiver is considered to be locked to the MPEG TS. Following synchronisation of the MPEG TS, the second task is to extract the PAT from the MPEG TS. The PAT is repeated precisely every 0.5 seconds in the TS and has a PID of 0×000, so it is easily identified

(Fischer, 2010). Once extracted, the PAT is read to determine the number of PSs contained in the transmission, and is also used to identify the packets in the TS containing the PMT information. Following the identification of the PMT packets, the third task is to extract the PMT from the TS and determine PIDs for each of the ESs contained in the TS. At this stage the consumer is required to select the required ESs using the PIDs, which is done when consumer selects a programme using the receivers programme guide menus or the remote control channel change controls. Once selected, the PIDs are used to identify the PES packets containing the required ESs. The fourth step is to then demultiplex the required PS and extract the appropriate PESs. The fifth step is to then depacketize the PESs. It must be noted that system memory is needed to buffer the PES streams as these are spread over the entire MPEG TS, so it takes time to receive all the necessary packets. Following depacketisation, the final step is to pass the ESs to source decoders, where the applicable decompression codecs are applied in order to recovery the original uncompressed video, audio and data streams. The raw signals can then be used to drive the respective video display and audio reproduction devices.

2.1.5 Real-world DVB-T/T2 Receiver Architecture

A real-world consumer DVB-T/T2 TV and STB receiver architecture is represented by the block diagram shown in Figure 2-11.

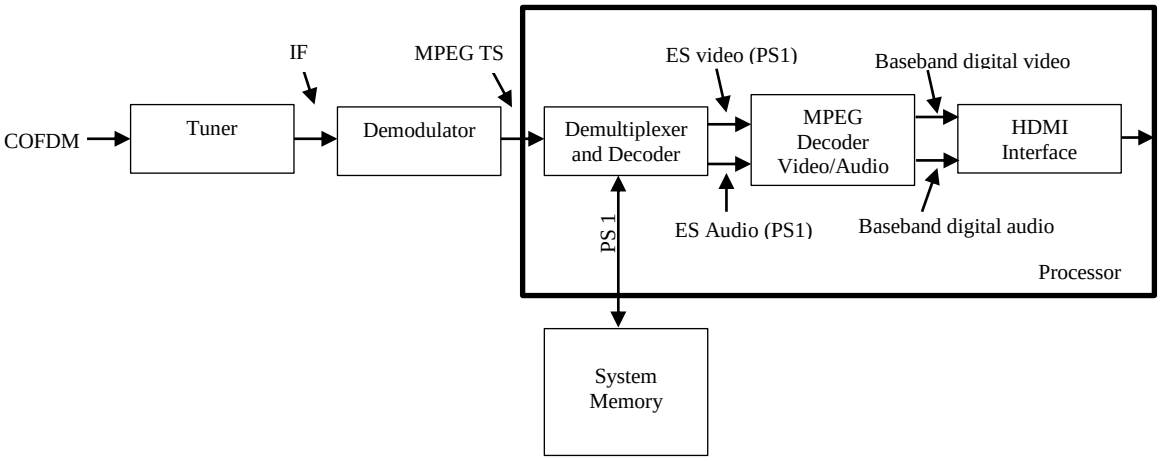


Figure 2-11 DVB-T/T2 receiver MPEG TS (author generated image)

In this architecture, the tuning function is performed by a tuner integrated circuit (IC), represented by a single block, which accepts an RF COFDM channel, down-converts it to the IF and then presents the signal to the demodulator block. The demodulator function is also performed by a single IC, which accepts the IF and digitises it using an ADC and then performs all the other demodulator functions using DSP, up to and including the channel decoding block. The demodulator outputs MPEG TS in either parallel mode or serial mode and feeds it the input of a processor IC which performs the demultiplexing and decoding of the MPEG TS. Memory storage is used in the receiver to enable correct reconstruction and sequencing of the chosen programme stream. Following the demultiplexing and depacketization of the program stream, the remaining compressed video and audio ESs are passed to the MPEG decoder, where the video and audio streams are the decompressed using the appropriate codecs. The MPEG decoder then outputs the raw video and audio streams, which are then formatted for output on the

receivers HDMI interface. The main point of interest in the architecture is that the MPEG TS is accessible at the output of the demodulator IC in two formats: parallel mode and serial mode. Knowledge of which devices in the STB where MPEG TS is sourced and sinked is necessary when considering the interfacing of the VLC systems encoder and decoder.

2.1.6 MPEG TS Physical Layer

Parallel TS Mode

At the physical layer, the MPEG TS parallel output of a demodulator IC has eight data lines (D7 to D0), one TS_VALID line, one TS_SYNC line, and one TS_ERR line. These lines are all clocked out of the demodulator IC simultaneously using the TS_CLK signal. The clock is effectively a byte clock, since 8-bits are output for every cycle of the clock. The clock has a 50% duty cycle, and data clocking occurs, selectively, on the either the rising or falling-edge of the clock signal. If clocking occurs on the rising-edge of the clock, this is referred to as non-inverted clocking, and if it occurs on the falling-edge, it is referred to as inverted clocking. The eight data lines act as the data bus for the MPEG TS, where D7 is the most significant bit (MSB) and D0 is the least significant bit (LSB).

The function of the TS_VALID line is to indicate when a valid TS packet is available on the data bus. The line is active high from the beginning of byte 0, to the end byte of byte 187 for the entire 188 byte TS packet, when valid data is available. The line is active low when no valid data is present. It is important to note that there are clock periods during which TS_VALID will signal that no valid data is present, which is due to the TS_CLK frequency is being higher than the TS byte (parallel mode) or bit (serial mode)

clock; in affect, the MPEG TS clock at the transmitter is lower in frequency than the STB receiver clock. TS_VALID is active low when there is no TS synchronisation.

The function of the TS_SYNC line is to indicate the start of a TS packet, and is active high for the duration of a sync byte and when TS synchronization exists.

The function of the TS_ERR line is to indicate when an uncorrectable error has been detected in the outer decoding – channel decoding has failed to correct errors in the TS packet. The TS_ERR line is active high during the entire duration of the TS packet containing errors. The TS_ERR line is generally redundant, because the 1-bit transport error indicator in the TS header is set to one when errors are uncorrectable, and notifies the demultiplexer and decoding block in the processor of the TS packet error.

Figure 2-12 shows the timing diagram when non-inverted clocking is used.

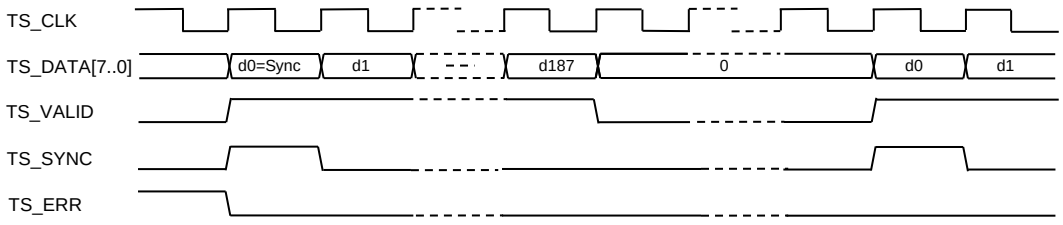


Figure 2-12 MPEG TS parallel mode (CLK non-inverted)

The following equations express the timing of the MPEG TS as a function of the TS_CLK (f_{TS_CLK}).

The period of a single data bit [D7...0] is given by Equation 2-9.

$$T_{TS\_DATA[7...0]} = \frac{1}{f_{TS\_CLK}} \ (s)$$

Equation 2-9

The period of the TS_VALID signal when the data is valid is given by Equation 2-10.

$$T_{TS\_VALID} = 188\frac{1}{f_{TS\_CLK}}\ (s)$$ Equation 2-10

The period of the TS_SYNC pulse is given by Equation 2-11.

$$T_{TS\_SYNC} = \left(188\frac{1}{f_{TS_{CLK}}}\right) + T_{offset}\ (s)$$ Equation 2-11

Where the constant 188 is the number of bytes in each MPEG TS packet, and the T_{offset} is the timing offset caused when the TS_CLK frequency is higher than the transmitter MPEG TS clock frequency.

In cases where the TS_CLK is at the same frequency as the transmitter MPEG TS clock, the difference between the T_{TS_SYNC} and T_{TS_VALID} periods is zero, and so too is T_{offset}, as defined by Equation 2-12.

$$T_{offset} = T_{TS\_SYNC} - T_{TS_{VALID}}\ (s)$$ Equation 2-12

For instances where T_{TS_SYNC} is greater than T_{TS_VALID}, T_{offset} is greater than zero. In these instances, the transmitter MPEG TS clock frequency can be calculated using Equation 2-13.

$$f'_{TS\_CLK} = 188\frac{1}{T_{TS\_SYNC}}\ (Hz)$$ Equation 2-13

Serial TS Mode

The MPEG TS serial output of a demodulator IC provides only one data line, from which all data 8-bits emerge, LSB first; note LSB or MSB first is programmable on some devices. Separate outputs for the TS_VALID, TS_SYNC and TS_ERR lines are still provided. The TS_CLK, still has a 50% duty cycle, but since the TS now has a

single line out, the clock acts as a bit clock, clocking the data out at eight times the frequency of the byte clock used in parallel mode. The serial clock also still has non-inverting and inverting modes which behave the same as in the parallel mode.

The waveforms for serial mode, using non-inverted clocking, are shown in Figure 2-13.

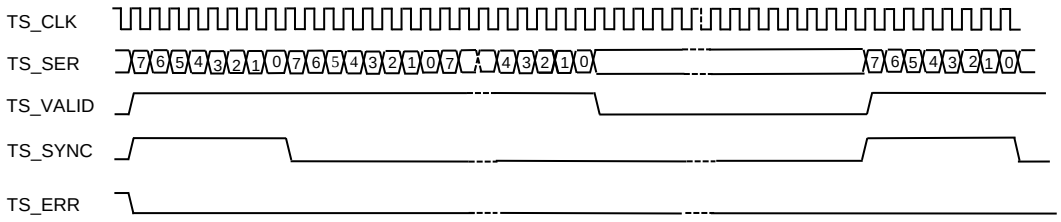


Figure 2-13 MPEG TS serial mode (CLK non-inverted)

Based on the authors industrial experience, the parallel mode is most commonly used mode due to its lower clock transients, which generates less spurious inside STB platforms – effectively this reduces unwanted interference inside the STB. The lower clock frequency and parallel data bus also makes processing of the TS easier, since combinational logic circuits can be designed to encode and decode the bits in a parallel. Effectively, a parallel data bus consisiting of ten signal lines that can be used as the data input and output of the VLC video distribution system, where eight lines are used for the data signals (D7 to D0), one for the TS_VALID signal, and one for the TS_SYNC signal. As mentioned previously, the TS_ERR signal is redundant. All ten signal lines will be clocked simultaneously using the rising or falling edge of the parallel TS_CLK signal. The minimum serial clock frequency, and bandwidth, of the VLC system is calculated using Equation 2-14.

$$f_{MIN\ SER\ CLK} = N\ f_{TS\_CLK}\ (Hz) \qquad \text{Equation 2-14}$$

Where N is the number of parallel lines (bits) in the MPEG TS bus.

It is the intention of this research to use the parallel bus for the VLC. The MPEG TS is a continuous stream, and therefore ideally, real-time coding of the stream is desirable in the hardware implementation of the VLC video distribution system, since no memory buffering is required, and therefore system cost and complexity is reduced.

Characterisation and analyses of STB platforms is necessary in order to determine the logic levels used for the MPEG TS and also to determine the parallel clock frequency used, which ultimately determines the minimum serial clock and bandwidth of the VLC system. The minimum bit rate generated by the STB for a real off-air broadcast can also be determined; 50.3 Mbit/s is the maximum expected for DVB-T2 broadcasts.

2.2 VLC Overview

Modern LED based VLC research and development began in Japan in 2003 at Keio University's Nakagawa Laboratory (Tanaka, 2003). The research was motivated by the emergence of high-powered white LED technology and the application in SSL replacement lighting. Researchers at the Nakagawa identified an opportunity to combine the light emitting properties of LEDs with the high-frequency switching properties of the semiconductors (Tanaka, 2003). This integrated lighting and communication system was intend to alleviate channel spectrum capacity issues emerging from the ever increasing demand for RF and microwave bandwidth for internet services.

A VLC consortium (VLCC) was also formed in 2003 (Nakagawa, 2007), of which a number of large multi-national companies are members: Casio, Nakagawa Laboratories, NEC, NTT Docomo, Samsung Electronics, Sharp, Sony, and Toshiba. The intension of the consortium is to support research and development, and also coordinate planning and standardization of VLC systems (Haruyama, 2008). This has resulted in the development of the JEITA CP-1221 VLC system standard. VLC system standards have

also been developed in Europe and North America; in 2008, the Framework programme 7 OMEGA project (hOME Gigabit Access), funded by the European Commission, was established to develop global standards for home networking that uses IR and VLC technologies (Bouchet et al., 2010). In North America the IEEE 802.15.7 VLC Task Group is developing media access control (MAC) and physical (PHY) layer standards (Roberts, Rajagopal, & Lim, 2011). There are also a number of UK universities engaged in VLC research, such as Oxford, Glasgow, Northumbria and Strathclyde. Notably, the University of Edinburgh's Institute for Digital Communications established the D-Light project in 2010, which resulted in the founding of PureLiFi Ltd, which produces VLC based communications products (PureLiFi, 2019). In the USA, Boston University, Rensselaer Polytechnic Institute, the University of New Mexico, and UC Davies's, centre for Ubiquitous Communication by Light (UC-Light) (UCLight, 2019) are running VLC research activities. Given that VLC research was initially motivated by the invention of the high intensity white LEDs, it is appropriate to start with a brief overview of the evolution of LEDs, before introducing VLC systems.

2.2.1 Semiconductor LEDs

The invention of the p-n junction LED is credited to Oleg V. Lossev, when in 1927, he wrote a paper on electroluminescence (Lossev, 1928). The paper was based on his observation of light emission from a silicon carbide (SiC) point-contact junction. Lossev also, correctly, connected electroluminescence with the photoelectric effect described in Einstein's 1905 paper (Einstein, 1905). Although Lossev takes credit for the invention, it is noteworthy that H. J. Round in 1908, whilst at Marconi Labs, observed the same phenomenon using a SiC crystal and a cat's-whisker detector (Sze, 1991).

LEDs are semiconductor devices that emit light at specific wavelengths, or colours, of the electromagnetic spectrum. The emission wavelength is predominantly determined by the materials and processes used to fabricate the devices. The evolution of LED began with the development of IR LEDs in the 1950s, and then progressed to visible devices. The first visible red LED was developed in 1962 by Nick Holonyak, Jr., whilst at General Electric (GE), using a gallium arsenide phosphide (GaAsP) p-n junction (Holonyak & Bevacqua, 1962). The first yellow LED was developed in 1972 by M. George Craford, whilst at Monsanto, using a nitrogen-doped (N-doped) GaAsP device grown on a GaAs substrate. Craford was also a member of a team at Monsanto that used N-doped GaAsP devices to produce visible red, orange and green emissions (Groves, Herzog, & Craford, 1971). In 1969, Craford, whilst at Hewlett Packard (HP), increased the intensity of LEDs using aluminium gallium arsenide (AlGaAs) for red LEDs, and aluminium gallium indium phosphide (AlGaInP) for orange and green LEDs (Rostky, 1997).

2.2.2 Blue LEDs

The first blue LED was demonstrated by Jacques Pankove in 1972, whilst at RCA, using a zinc-doped (Zn-doped) GaN device which produced an emission at a wavelength of 470 nm. A year later, Pankove developed the first current-injected LED using Zn-doped GaN and an indium surface contact (Pankove, Miller, & Berkeyheiser, 1971, 1972). This device emitted a green and blue light, and was referred to as a metal-insulator-semiconductor (MIS) diode. RCA also experimented with magnesium-doped (Mg-doped) GaN, as magnesium was considered a better dopant than zinc. In 1972, Maruska demonstrated an Mg-doped GaN device that produced a blue and violet emission, centred at a wavelength of 430 nm (Maruska, Rhines, & Stevenson, 1972). However, the

device suffered from high electrical-to-optical power inefficiency, and based on this, RCA ceased further development. Consequently, blue LED research only resumed in the 1980s and SiC based materials, first investigated by Lossev and Round, were revisited, but were also found to be highly inefficient (Potter, Blank, & Addamiano, 1969). SiC devices from the late 1980s, capable of emissions at 470 nm, were only 0.03% efficient (Edmond, Kong, & Carter, 1993). However, low-emission, SiC blue LEDs were produced for a short while by Cree, Sanyo and Siemens up until the 1990s. Significantly, the key breakthrough in blue LED technology came in 1993, when Shuji Nakamura of Nichia Corporation produced the first high-power , high-efficiency indium gallium nitride (InGaN) based blue and green LEDs (Nakamura, Senoh, & Mukai, 1993a, 1993b) (Nakamura, Mukai, & Senoh, 1994).Table 2-3 summarises the LED colours, emission wavelengths, frequencies, and specific semiconductor materials. The relationship between emission wavelength and frequency is defined by Equation 2-15.

$$\lambda = \frac{c}{f}\ (m) \qquad \text{Equation 2-15}$$

Where c is the speed of light (ms^{-1}), and λ (m) is the wavelength of the emission.

As well as the wavelength of the LEDs emission, there is also the photon energy of the emission, which is defined by the Planck–Einstein relation shown Equation 2-16.

$$E = \frac{hc}{\lambda}\ (J) \qquad \text{Equation 2-16}$$

Where E is the photon energy in (J) h is Planck's constant (Js), c is the speed of light (ms^{-1}), and λ (m) is the wavelength of the emission.

The LED wavelength determines the photon energy of the emission, which effects the sensitivity of the receiver in VLC systems, as is discussed in a later section.

Colour	Wavelength λ (nm)	Frequency f (THz)	Semiconductor Materials
Red	~ 610 to 760	~ 394 to 491	AlGaAs, GaAsP, AlGaInP
Orange	~ 590 to 610	~ 491 to 508	GaAsP, AlGaInP
Yellow	~ 570 to 590	~ 508 to 526	GaAsP, AlGaInP
Green	~ 500 to 570	~ 526 to 600	InGaN, AlGaInP
Blue	~ 450 to 500	~ 600 to 666	InGaN
Violet	~ 400 to 450	~ 666 to 750	InGaN

Table 2-3 Visible LED semiconductor materials (author generated table)

2.2.3 White-Light LED and Solid-State Lighting

The invention of InGaN blue LEDs resulted in the development of white LEDs, and ultimately SSL systems. However, blue LEDs are unable to independently produce white light, since an almost monochromatic, or narrow range of wavelengths, is centred on a peak blue emission. Conversely, white light is polychromatic, meaning that it consists of a wide range of wavelengths, hence SSL manufacturers therefore use two key methods to produce white light emissions. The first, uses a multi-LED device consisting of red, green and blue (RGB) LEDs, and the colour mixing process (Newton, 1718), which combines the emissions of all three LEDs at the appropriate intensities to produce an overall white light emission (Schubert, 2006). The second, simpler and lower cost method, uses a device composed of a blue LED and a cerium-doped yttrium aluminium garnet phosphor (YAG:Ce phosphor). White light emission is generated through the '*partial conversion*' effect, whereby a fraction of the blue LEDs emission (electroluminescence) is absorbed by the phosphor, causing it to fluoresce at longer wavelengths, and thus generate a yellow emission (Schubert, 2006). The components of the electroluminescent and fluorescent emissions are then combined, again through colour mixing, to produce overall white emission. Figure 2-14 shows a plot of the emission spectrum of the first InGaN and YAG: Ce phosphor LED. The electroluminescent components of the blue InGaN LED are shown centred at 460 nm,

and the fluorescent components of the phosphor are shown centred at 560 nm. It is important to note that the fluorescent components cover a wider range of the spectrum and have lower frequencies than the electroluminescent components. It will be demonstrated in section 2.3 that these lower frequency yellow components reduce the bandwidth of VLC systems.

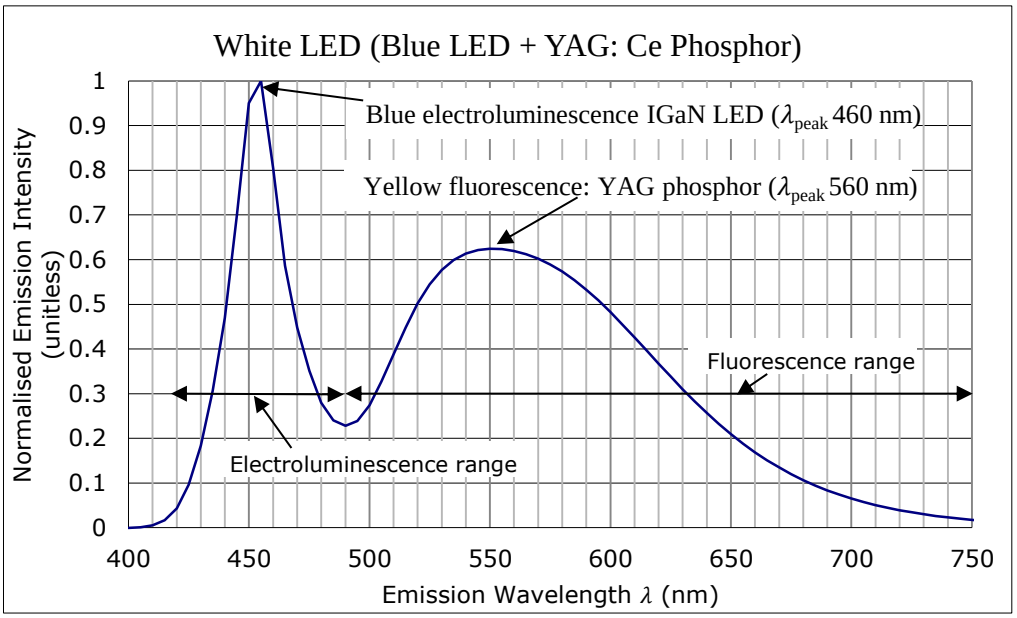


Figure 2-14 Emission spectrum of an InGaN blue LED and YAG:Ce phosphor (Schubert, 2006)

InGaN and YAG: Ce phosphor LEDs were first demonstrated by Yoshinori Shimizu of Nichia Corporation in 1996. In the same year, Nichia Corporation began mass-production of the device for SSL applications. Also, in 1996, Osram filed a patent for a similar partial conversion device (Schubert, 2006). SSL was rapidly adopted as replacement lighting for traditional incandescent, fluorescent and halogen technologies, due to higher efficiency, longer lifespan and lower overall cost (Schubert, 2006). Table 2-4 shows the performance and cost differences between SSL and traditional lighting technologies.

Type	Efficacy (lmW^{-1})	Lifespan (hours)	Cost (60W bulb equivalent comparison) (US Dollars)
Incandescent (tungsten filament)	10 ~18	~1000	~$1.00
Halogen (tungsten filament)	16 ~ 24	~2,000	~$2.00
LFL	65 ~ 95	~15,000	~$2.00
CFL	50 ~ 70	~15,000	~$5.00
SSL	150 ~ 250	~50,000	~$8.00

LFL = linear fluorescent light, CFL = compact fluorescent light

Table 2-4 Lighting comparison (Schubert, 2006)

Note: efficacy is defined in units of lumens per Watt (lmW^{-1}) and is a measure of the devices ability to convert electrical power to illumination. Specifically, the lumen defines total quantity of visible light emitted by a source per unit of time.

IRC Systems

2.2.4 Line-of-sight and Diffuse Transmission

As mentioned in the previous section, IR LEDs were developed in the 1950s, and a number of important IRC systems were developed based on these devices. Before discussing VLC systems, it is worth mentioning two notable optical links that evolved using IR LEDs, and from which, important conclusions were drawn. The first link is an analogue FSO IR link, demonstrated by Rubin Braunstein in 1957, whilst he was working at RCA (Kroemer, 2013). Using the output of a record player to modulate the forward bias current of an IR gallium arsenide (GaAs) diode, Braunstein was able to transmit, using directed LOS (DLOS), the modulated light emission over a short distance. The receiver was constructed using a lead sulfide (PbS) diode, which was used to detect the transmission, and an audio amplifier and loudspeaker to respectively amplify and reproduce the audio signal. The link was an early example of an analogue intensity modulation and direct-detection (IM/DD), where the LEDs emitted light intensity is proportional to the amplitude of the modulating signal, and the receivers PD

output photocurrent is proportional to the integral of the incident optical power over the area of the PD (Z. e. Ghassemlooy, Alves, Zvanovec, & Khalighi, 2013).

Braunstein's system used DLOS transmission, which is the simplest form of transmission, and relies on a direct path from the transmitting LED to the receiving PD (Kahn & Barry, 1997). In DLOS systems, the divergence, or irradiance angle, of the LED and field-of-view (FOV) of the PD is narrow, in order to ensure that most of the optical power emitted by the LED is received at the receiver, and that multipath interference is minimised, where multipath is caused by reflections from objects that can add constructively and destructively at the receiver, causing interference similar to that described for RF systems in section 2.1.1. In addition to using low irradiance and FOV angles to increase optical power at the receiver, the light emission of the LED can be collimated and focussed using concentrators (lenses), both at the transmitter and receiver, to further increase the received power. DLOS based systems, however, require accurate alignment, and are subject to blocking by people or objects that interrupt the LOS path. Figure 2-15 illustrates the physical arrangement of a DLOS system; concentrators are omitted for clarity.

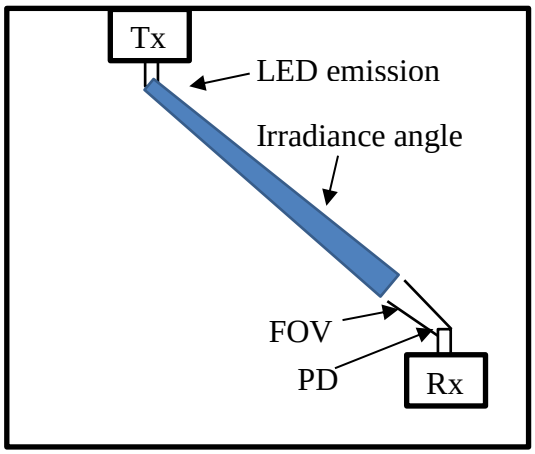


Figure 2-15 Directed LOS transmission

In contrast to DLOS transmission, nondirected LOS (NLOS) transmission uses a wider irradiance angle for the LED and field-of-view (FOV) for the PD in order to increase coverage area (Z. e. Ghassemlooy, Alves, Zvanovec, & Khalighi, 2013). Figure 2-16 illustrates the NLOS transmission, where the receiver can be positioned anywhere under the LED, and is not necessarily at the peak power output of the LED, as is the case in DLOS transmission. NLOS therefore achieves wider coverage areas at the expense of lower received power, due increased path loss, and increased multipath caused by reflections which leads to increase ISI.

Essentially NLOS is used for point-to-multipoint applications, whereas DLOS is used for fixed point-to-point applications. DLOS is therefore better suited to the video distribution system since it achieves higher received power and the multipath effects are negligible.

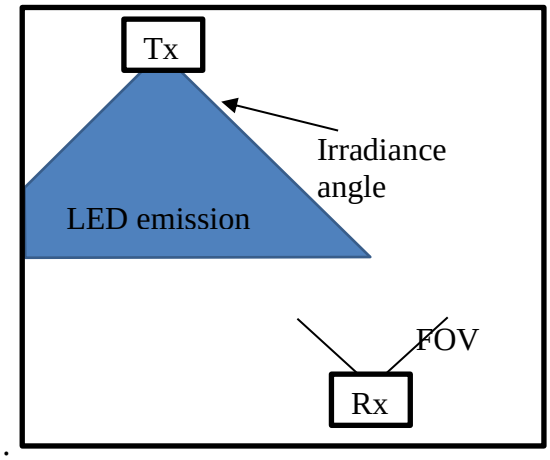


Figure 2-16 Nondirected LOS transmission

The second link was the first demonstration of a digital IRC system, and was made in 1979, by the often cited Gfeller and Bapst (Gfeller, 1979). In this case, diffuse transmission was used, where a wide irradiance angle LED was pointed up towards the ceiling of a room, and the light reflected from the ceiling, walls, floor and other objects

in the room was collected by a receiver with a wide FOV (Kahn & Barry, 1997). Figure 2-17 illustrates the physical arrangement of a diffuse system. The system significantly increased the coverage area, and using a near-IR LED centred at a wavelength of 950 nm, enabled the transmission of data to a cluster of fixed position computer terminals in a room. The system was capable of supporting bit rates of up to 1 Mbit/s, using on-off keying (OOK) modulation. Gfeller and Bapst reported that the bit rate in diffuse systems is limited by the LEDs power output and bandwidth, and that such systems inherently suffer from multipath interference, which is a consequence of using reflections to increase coverage area.

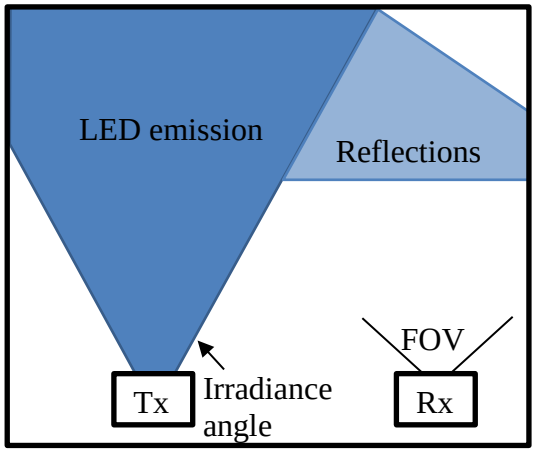


Figure 2-17 Diffuse transmission

The key conclusions from these early inventions were that DLOS transmission is the simplest to implement and achieves the highest optical power at the receiver. DLOS transmission is ideal for the VLC video distribution system of this research, since the LED on the ceiling gimbal and the wall-mounted TV are in fixed LOS positions. This means that precise alignment of the transmitting LED relative to the receiving PD is possible using a low divergence angle LED and a low FOV PD, enabling minimisation of multipath interference; effectively the optical transmission is optimally controlled and

received power at the receiver is maximised. In contrast, the NLOS and diffuse transmissions are intended for applications where wide coverage area is desirable, but is subject to lower received power and increased multipath. Another important conclusion from these early systems was that bit rates in digital links are limited by the LEDs output power and bandwidth.

2.3 VLC Systems

2.3.1 Intensity Modulation and Direct-Detection

The first digital VLC system using white light LEDs appeared in 2003, when Tanaka et al. demonstrated a dual purpose indoor room illumination and integrated FSO communication system. The system used OOK modulation in an IM/DD system that achieved a bit rate of 400 Mbit/s(Tanaka, 2003).

In 2006, Afgani et al. stated that OFDM could be used to enhance the performance of IM/DD VLC systems which used phase, frequency, polarization, or intensity (Afgani, 2006). It was also reiterated that IM/DD has the advantage of being particularly easy to implement, as the optical output power of the emitting LED is simply varied according to the modulating signal. The resultant optical output signal is then directly detected by a PD at the receiver. However, it was also stated that the penalty for the simplicity of such an IM/DD system is reduced sensitivity and a vulnerability to noise. In order to mitigate these effects, a modulation scheme known as direct-current-biased optical OFDM (DCO-OFDM) was proposed. The modulation scheme required complex digital signal processing (DSP) at both the transmitter and receiver, compared to the IM/DD OOK 400 Mbit/s system proposed by Tanaka et al.

DCO-OFDM was improved upon, when in 2010, Vucic et al., demonstrated a 500 Mbit/s discrete multitones (DMT) based system (Vucic, 2010). Again, the system was complex in order achieve the higher bit rate. The advantage of using the OFDM based modulation scheme is that it is able to handle multipath created by the reflections from the ceiling, walls, floor and other surfaces in diffuse systems. The scheme is ideal for systems where maximum coverage is required in a room, and where the receiving device is mobile.

It is tempting, at first, to adopt either DCO-OFDM or DMT based modulation schemes in order to achieve the highest possible bit rates. However, the DVB systems considered for the VLC video distribution system are band-limited by the RF channel bandwidth of the transmission, and therefore so too are DVB bit rates. Given that the highest bit rate for DVB systems is currently only 83.1 Mbit/s, the use of DCO-OFDM or DMT modulation, results in an over engineered system that would be complex, expensive, and given the bit rate limitation set by the broadcast system, underutilised. The rationale for not pursuing these modulation schemes is further supported by the fact that the research is focussed on the distribution of digital terrestrial broadcasts where the upper bit rates are even lower, with DVB-T set at 31.7 Mbit/s and DVB-T2 at 50.3 Mbit/s. The argument against pursuing DCO-OFDM or DMT is further supported by the fact that these modulation schemes are used primarily in diffuse transmission systems where the maximisation of coverage area is required and the light emitting source acts as both an illuminator and as a multi-user data transmitter for mobile devices. The diffuse transmission inherently suffers from multipath issues, which OFDM is able to mitigate. The target receiving devices for such high data rate systems are mobile, broadband internet (TCP/IP) receiving devices such as smart phones, tablets and laptops, as

described by Khalid et al (Cossu, 2012). Given these facts, a solution with lower cost and complexity can be considered using IM/DD and a simpler modulation scheme, even though Afgani et al. expressed concerns about sensitivity and a vulnerability to noise in such systems. This is further supported by Tanaka et al. who were able to demonstrate bit rates of 400 Mbit/s using IM/DD and OOK modulation with a phosphor-coated LED. Therefore, based on the bit rates defined by DVB, it is viable to design the VLC system using IM/DD techniques to achieve a simpler, less expensive and more optimised solution, appropriate to the DVB-T and DVB-T2 target bit rates. Furthermore, the adoption of the IM/DD approach also means that simpler modulation schemes such as OOK and pulse-position modulation (PPM) can be considered, as will be discussed later in this chapter.

2.3.2 White LED Bandwidth and Blue Optical Filtering

As mentioned in section 2.2.4, the bandwidth of the LED is one of the key limiting factors in an IRC and VLC based system. In 2012, Khalid et al. presented a DMT system capable of 1 Gbit/s using a single phosphor-coated white LED and optical blue filtering at the receiver, prior to detection by the photodiode (Khalid, 2012). The filtering attenuated the fluorescence components generated by the phosphor through partial-conversion, and hence increased the bandwidth of the received emission. Figure 2-18, shows the emission intensity of a single phosphor-coated white LED versus wavelength measured at the receiver PD, with and without blue filtering; note that idealised filtering is shown in the plot. The solid blue trace shows the unfiltered response of the LED, with the blue LED electroluminescence emission shown centred at 460 nm, and the yellow fluorescence centred at 560 nm. The blue dotted trace shows the idealised filtered response of blue LEDs emission, with fluorescence components

completely eliminated. In reality, the blue optical filter is not able to completely remove the fluorescence components, but even non-idealised filtering results in almost an order of magnitude increase in the bandwidth of the received emission (Z. e. Ghassemlooy et al., 2013).

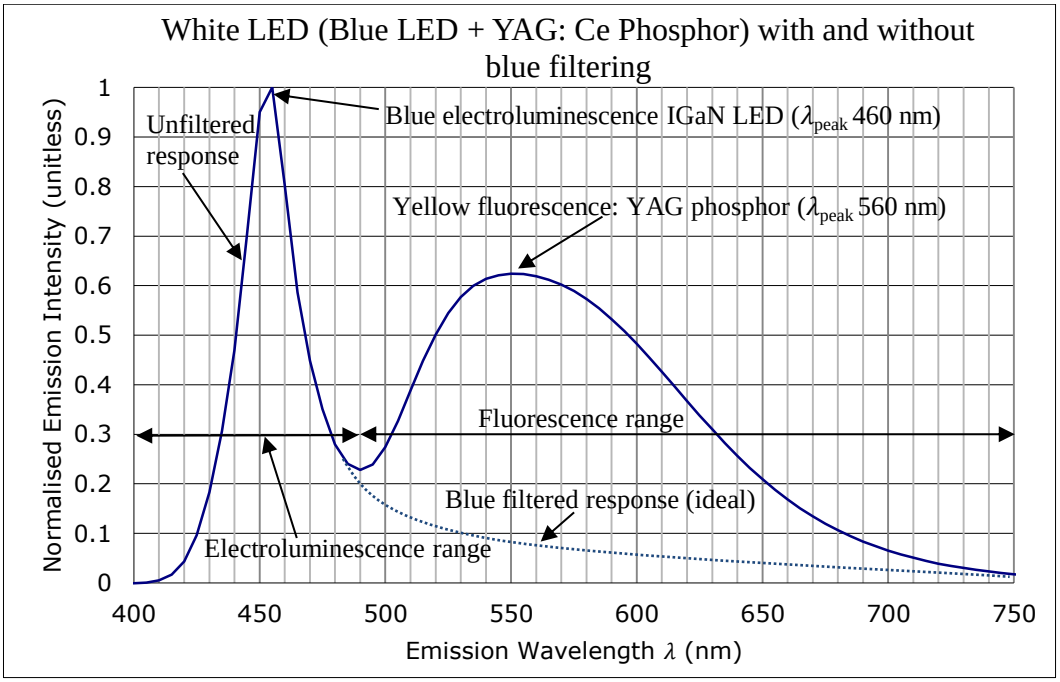


Figure 2-18 Emission spectrum of an InGaN blue LED and YAG:Ce phosphor with and without blue filtering (Schubert, 2006)

Figure 2-19, shows the frequency response of an Osram Ostar white LED, with and without filtering at the receiver; in this case non-ideal filtering is applied. Without filtering, the 3 dB cut-off of the response occurs at approximately 2.5 MHz, and with filtering, it occurs at 20 MHz (Z. e. Ghassemlooy et al., 2013). However, the increase in bandwidth is traded-off against the optical power loss incurred by the filter, which results in reduced sensitivity at the receiver.

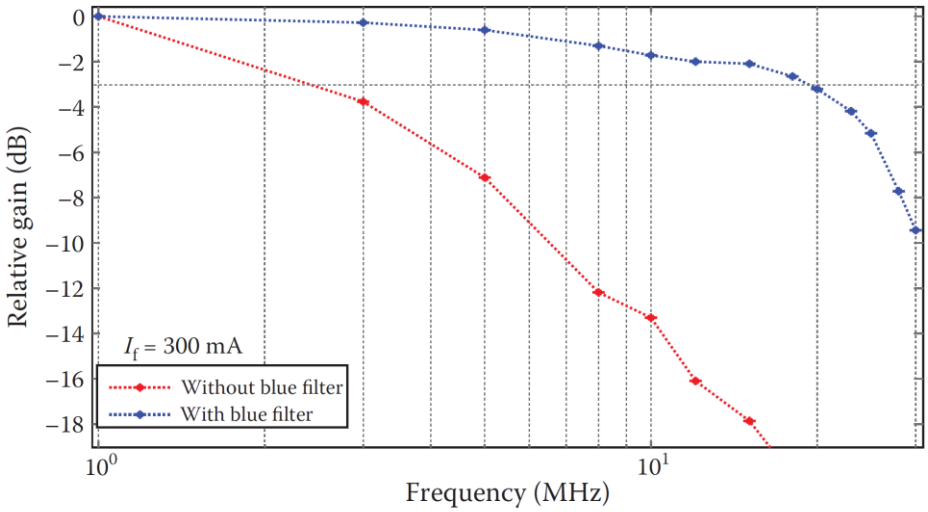


Figure 2-19 White LEDs normalised frequency response with and without blue filtering (Z. e. Ghassemlooy et al., 2013)

2.3.3 RGB and Single Colour LED Bandwidth

In 2012, Khalid et al. reported a 3.4 Gbit/s system using an RGB LED (Cossu, 2012). It was also reported that such high data rate FSO systems were achievable in dual purpose applications, where the primary purpose was illumination and the secondary was for supporting Gbit/s broadband internet applications. Bandwidth limitations of the LED were stated, with bandwidths of 10 MHz demonstrated for off-the-shelf LEDs, where no optical filtering or electrical equalisation at the receiver was used to provide bandwidth compensation.

In 2013, Azhar et al. demonstrated a Gbit/s bit rate using a 4x4 MIMO-OFDM based system (Azhar, 2013), and also, Tsonev et al. reported a bit rate of 3.5 Gbit/s from a serial-in-serial-out (SISO) based system using a single-colour LED (Tsonev, 2014).

In addition to the use of optical filtering and non-phosphor based LED, bandwidth extension is also possible at the receiver, using electrical equalisation techniques as reported by Li et al., in a paper which described the use of both passive and active equalisation (post-equalisation) to increase the bandwidth of a white LED up to 151

MHz (Li, 2014). In this case a white LED and blue optical filtering was employed, in conjunction with the post-equalisation, to achieve bit rates of 340 Mbit/s using an OOK modulated signal. Furthermore, concentrators were used to increase the optical power at the receiver, specifically biconvex collimating concentrators at the transmitter and receiver to focus the LED emission onto the receiver PD. The transmitter and receiver in the experiments were separated by 0.5 m in a DLOS arrangement.

In conclusion, LEDs that generate white light using a blue LED and phosphor, require blue filtering at the receiver to extend the bandwidth from 2.5 MHz to 20 MHz. However, receiver sensitivity is reduced by the attenuation introduced by the optical filter. The use of RGB or single colour LEDs has greater benefits, since these devices have wider bandwidths, of the order of 10 MHz, without optical filtering, and therefore enable higher sensitivity at the receiver. The use of a single colour, blue LED for example, provides a wider bandwidth, and theoretically a higher sensitivity at the receiver due to the higher photon energy stated by the Planck–Einstein relation (Equation 2-16). The use of a single colour LED in the VLC video distribution system is acceptable given that the system is not intended for dual illumination purposes, as is the case with most VLC systems.

Additionally, bandwidth extension is possible using post-equalisation at the receiver, using passive and/or active equalisation techniques, with bandwidth extensions reported up to 151 MHz, where OOK modulation and IM/DD was used to achieve bit rates of 340 Mbit/s, and which far exceeds the 31.7 Mbit/s (DVB-T) and 50.3 Mbit/s (DVB-T2) required for the VLC video distribution system.

It is the intention of this research to characterise and analyse both white and blue LEDs as potential candidates for the transmitting source of the VLC system, and apply further

bandwidth extension using post-equalisation at the receiver. Furthermore, collimating concentrators and DLOS transmission will be used to maximise received power.

2.4 Transmission Model

2.4.1 Lambertian Emission

LEDs produce a Lambertian emission (Haigh, 2011) as defined by Equation 2-17.

$$R_0(\emptyset) = \left[\frac{m+1}{2\pi}\right] cos^m(\emptyset) \qquad \text{Equation 2-17}$$

Where m is the order of the Lambertian emission, and is related to the semi-angle $\emptyset_{1/2}$ of the LED emission. The semi-angle is defined as the point where the optical power of the emission falls to 3 dB. The equation for m is defined by Equation 2-18.

$$m = \frac{-ln\,2}{ln\ (cos(\emptyset_{1/2}))} \qquad \text{Equation 2-18}$$

Based on Equation 2-17 and Equation 2-18, a MATLAB simulation (refer to Appendix A.1 for code listing) was generated by the author in order to analyse the radiant intensity of a single LED. Figure 2-20 shows the simulated radiant intensity of a single LED located in a 3D space with dimensions 8 × 8 × 2 m. The LED is located at the centre of the space, and at the maximum height of 2 m. The semi-angle in this case is arbitrarily set at 60°.

The simulation demonstrates that the highest radiant intensity of the emission occurs directly beneath the LED, and confirms that DLOS transmission achieves maximum optical power at the PD, if the PD is positioned directly beneath the LED. This confirms that if the gimbal mounted LED, described in the physical arrangement of the VLC video distribution system in section 1.2.3, is pointed directly at the PD located on the

front-panel of a TV, maximum signal power is achieved at the receiver. It can also be shown from the simulation that minimising the semi-angle increases the received power, and therefore SNR, at a PD positioned directly beneath the LED. It can also be deduced that if the emission is only directed at the PD, reflections will be minimised, and therefore so too will multipath interference at the receiver.

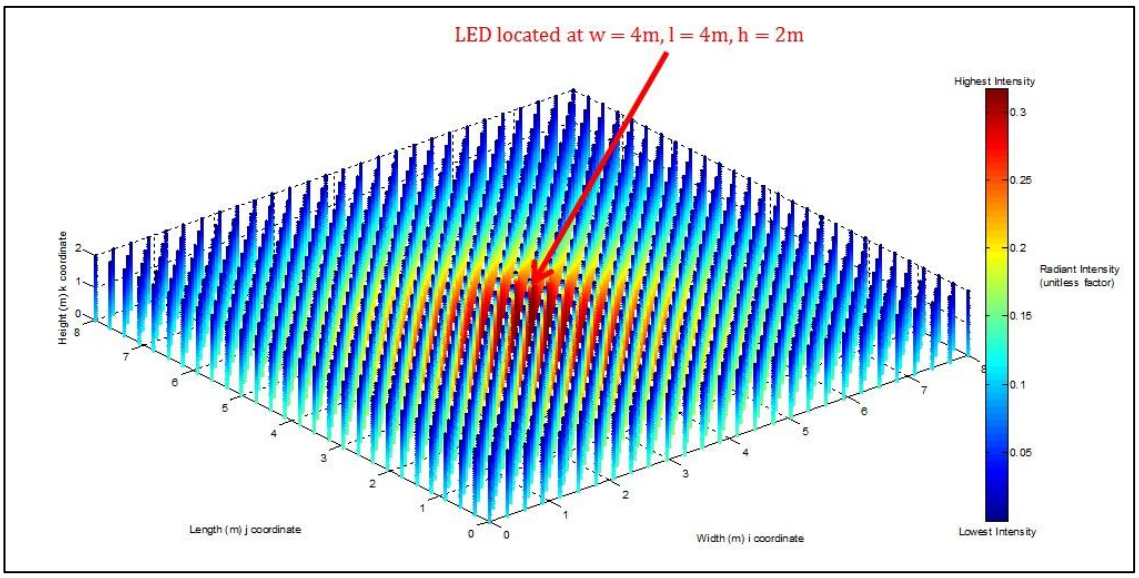


Figure 2-20 Single LEDs Lambertian radiant intensity

2.4.2 DLOS Transmission Model

The DLOS transmission model assumes that multipath reflections from the ceiling, walls, floor and other surfaces are not presented at the receivers PD (Z. e. Ghassemlooy et al., 2013). Under this condition, the DC gain of a receiver located at a distance of d and angle of $\emptyset$ is approximated by Equation 2-19.

$$H_{LOS}(0) = \begin{cases} \frac{A_{Rx}}{d^2} R_0(\emptyset)\cos(\psi) & 0 \leq \psi \leq \psi_c \\ 0 & elsewhere \end{cases} \quad \text{Equation 2-19}$$

Where A_{Rx} is defined as the PD area, d is the distance between the LED transmitter and the PD receiver, ψ is the angle of incidence, and ψ_c is the field of view FOV of the PD, and $R_0(\emptyset)$ is the LEDs radiant intensity, where $\emptyset$ is the irradiance angle of the emission. It should be noted that the inverse-square term $\frac{1}{d^2}$, represents the path loss between the LED transmitter and the PD at the receiver (Ryer, 1998). Figure 2-21 shows the diagrammatical representation of the spatial components of Equation 2-19. In this diagram, the incident angle ψ is zero, since the LED and PD are in perfect direct alignment. This means that maximum optical power is received at the PD, where the received power reduces with the inverse-square of the distance; effectively, the shorter the distance between transmitter and receiver, the higher the received power. Optical power at the receiver is also increased by reducing the irradiance angle of the LED, and by a larger surface area PD. However, increasing the surface area of the PD reduces the bandwidth of the system due the increased junction capacitance of the PD. Furthermore, the larger the surface area of PD the greater the noise introduced into the system.

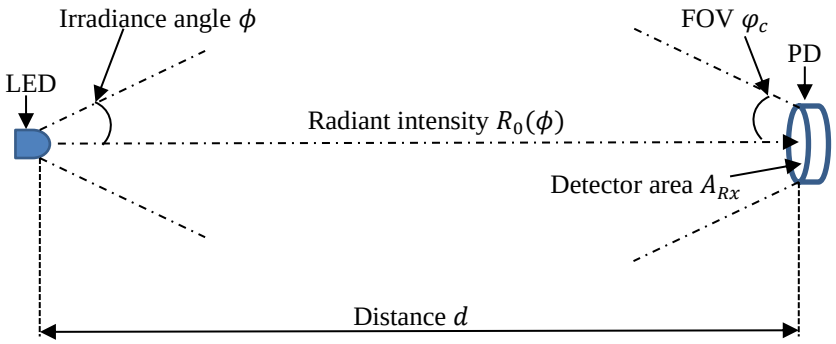


Figure 2-21 Spatial components of directed LOS transmission

Figure 2-21 is referred to as a non-imaging system, since the PD simply collects all photons incident on its active region. Concentrators are added to the arrangement to further increase optical power incident at the PD, as shown in Figure 2-22. This figure

also includes an optical filter which is used to increase the bandwidth of phosphor based white LEDs. The concentrators increase received optical power, whilst the filter causes attenuation. The gain of the concentrators is denoted by $g(\varphi)$ and the loss of the filter (band-pass) is denoted by $T(\varphi)$.

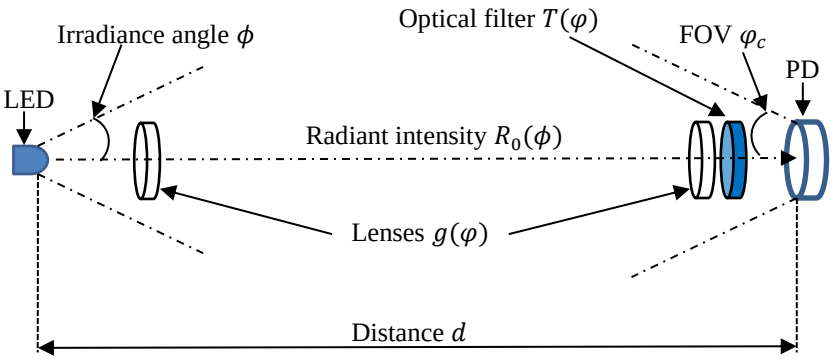


Figure 2-22 Directed LOS transmission with concentrators and optical filter

The gain of the idealised, non-imaging concentrator is defined by Equation 2-20 (Z. e. Ghassemlooy et al., 2013).

$$g(\psi) = \begin{cases} \dfrac{n^2}{\sin^2 \psi_c} & 0 \leq \psi \leq \psi_c \\ 0 & \psi > \psi_c \end{cases} \qquad \text{Equation 2-20}$$

Where n is the internal refractive index, and $\psi_c \leq \frac{2}{\pi}$.

The DC gain of Equation 2-19 is thus modified to include the gain of the concentrators and the loss of the bandpass optical filter, as defined by Equation 2-21.

$$H_{LOS}(0) = \begin{cases} \dfrac{A_{Rx}}{d^2} R_0(\emptyset) \cos(\psi)\, g(\varphi)\, T(\varphi) & 0 \leq \psi \leq \psi_c \\ 0 & \text{elsewhere} \end{cases} \qquad \text{Equation 2-21}$$

The received power is therefore defined by Equation 2-22.

$$P_{Rx} = H_{LOS}(0)P_{Tx}$$

Equation 2-22

Where P_{Rx} is the received optical power at the PD and P_{Tx} is the optical output power of the LED.

The channel can therefore be modelled as a linear attenuation and delay (Z. e. Ghassemlooy et al., 2013). The impulse response is expressed as shown in Equation 2-23.

$$h_{LOS}(t) = \frac{A_{Rx}}{d^2} R_0(\emptyset) \cos(\psi)\, g(\varphi)\, T(\varphi) \delta\left(t - \frac{d}{c}\right)$$

Equation 2-23

Where c is the speed of light in free-space, $\delta(.)$ is the Dirac function and $\delta(t - \frac{d}{c})$ is the signal propagation delay.

In conclusion, the DLOS transmission model, including the use of concentrators to increase the received power at the receiver, is suitable for the VLC system. At the receiver, reflections are not considered and therefore do not cause performance degrading issues such as ISI, as long as the LED and PD are positioned horizontally in the same plane, as shown in Figure 2-22, and carefully aligned to achieve optimal received power. The DLOS physical arrangement will be used for the hardware implementation of the system.

2.5 Intensity Modulation and Direct Detection Architecture

The simplest VLC architecture uses IM to transmit a serialised data stream to a DD receiver. This type of serial transmission system is referred to as a SISO system. The basic analogue signal processing blocks of a digital IM/DD SISO system are shown in

Figure 2-23 (Minh et al., 2009). At the input of the system, the digital logic voltage levels of the serial data stream are presented to the transconductance amplifier (TCA) which converts the voltage to current. The current is used to intensity modulate the light emission of the LED. The resultant light emission is transmitted through the free-space channel, and is received by the receivers PD, located some distance away. The PD converts the received photons into a photocurrent which is proportional to the integrated optical power incident on the PDs active region. The photocurrent is then presented to the transimpedance amplifier (TIA), also known as the pre-amplifier, which amplifies the photocurrent and converts it to a voltage signal. Post-equalisation (Eq) is then performed on the voltage signal to compensate for the roll-off of the LED and optical channel. The equalised signal is then amplified in the voltage amplifier (Av), which is also referred to as the post-amplifier, prior to low-pass (LPF) filtering. The LPF, which is more generally referred to as the pre-detection filter, provides signal conditioning in the form of pulse shaping, that increases the probability of correctly detecting the received data stream. Finally, the conditioned signal is then passed to a detector, formed from a voltage comparator, which compares the input signal voltage with a reference threshold voltage (V_{REF}). If the input voltage is above the threshold voltage, the comparator outputs a voltage level representing logic one, and conversely, if the input voltage is below the threshold voltage, a voltage level representing logic zero is output. The comparator output is also sampled at the serial data streams clock frequency (F_s), so that the comparators decision is selected at a certain instant in time, usually at the centre of the detected logic pulse; this is referred to as central decision detection.

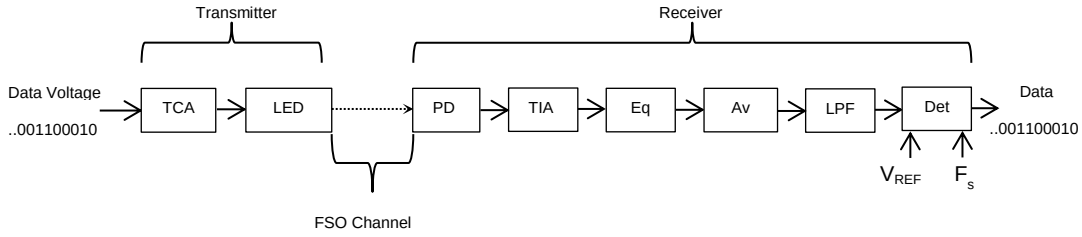


Figure 2-23 Block diagram of a digital OWC system (author generated image)

2.5.1 Channel Model

In the single channel OWC system model, the received PD photocurrent, $y\,(t)$, is a function of the LEDs optical intensity modulating signal, $x(t)$, which is generated by the digital modulating signal $m(t)$. Figure 2-24, shows $x(t)$ output at the LED, and $y(t)$ output at PD. Noise is also added to the photocurrent, where the primary noise sources are white Gaussian noise (AWGN), shot noise introduced by ambient light sources, and RMS noise current, $\sqrt{\overline{i^2}}$, introduced by the receiver. In reality, noise in the system is distributed, but for convenience, it is summed at the output of the PD. The transfer function of this system is given by Equation 2-24 (Z. Ghassemlooy, 2003).

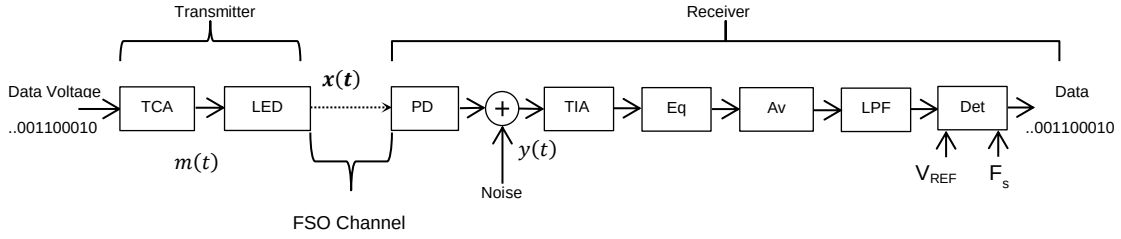


Figure 2-24 Analogue signal processing blocks of a SISO OWC system (including noise source) (author generated image)

$$y\,(t) = x(t) \otimes Rh_{LOS}(t) + n(t) \qquad \text{Equation 2-24}$$

Where $h_{LOS}(t)$ is the optical impulse response of the channel, and $n(t)$ is the additive noise introduced to the system. The symbol $\otimes$ denotes convolution, where $x(t)$ is

convolved with $Rh_{LOS}(t)$. The term R is responsivity, and is determined by the ratio between the PDs electrical photocurrent output and the received optical power (P_{Rx}), and has the units Amperes per Watt (AW^{-1}), as shown in Equation 2-25.

$$R = \frac{I_p}{P_{Rx}} \quad (A/W) \qquad \text{Equation 2-25}$$

Note that $y(t)$ is equal to the linear time-invariant (LTI) convolution formula shown in Equation 2-26.

$$y(t) = \left(\int_{-\infty}^{\infty} Rx(\tau)\, h_{LOS}(t-\tau)\; d\tau \right) + n(t) \qquad \text{Equation 2-26}$$

The equation for $y(t)$ yields the photocurrent of a single PD receiver, which is stimulated by a single LED transmitter, as defined in Equation 2-27.

$$y\,(t) = R\, \cdot P_{Tx}\, [x(t) \otimes h_{LOS}\,(t)] + n(t) \qquad \text{Equation 2-27}$$

2.5.2 Optical Channel Impulse Response

Assuming the digital modulating signal $m(t)$ is based on rectangular pulses, as is the case with OOK and PPM, then the logic levels of the pulses are used to represent logic one and zero. The LED is driven using these pulses, either to fully on to represent a logic one (maximum radiant intensity), or fully off to represent a logic zero (minimum radiant intensity). The optical intensity modulating signal, $x(t)$, generated by the pulses, propagates over the optical channel, and at the receiver, the received pulses are assumed to have a Gaussian pulse shape, as defined by Equation 2-28 (Cryan, Unwin, Garrett, Sibley, & Calvert, 1990).

$$h_p(t) = \frac{1}{\alpha\sqrt{(2\pi)}} \exp\left(-\frac{1}{2}\frac{t^2}{\alpha}\right)$$ Equation 2-28

Where α determines the peak amplitude of the pulse and t is time. The response of Equation 2-28, with α set to 0.4, is shown in Figure 2-25. The amplitude is shown in volts, as would be the case at the output of the pre-amplifier of the OWC system.

At the receiver, the Gaussian impulse response also exhibits ringing, due to the finite bandwidth of the channel. Effectively, the channel introduces a low-pass filter characteristic which causes the energy in the pulses to be dispersed over time, and results in ISI, where the ringing interferes with adjacent transmitted pulses, resulting in increased BER at the receiver.

A technique for generating electrical pulses, approximated to the Gaussian shape, will be demonstrated in Chapter 5, and will enable the OWC receiver to be completely modelled using an electrical circuit simulator, thereby greatly simplifying the design and analysis of the system.

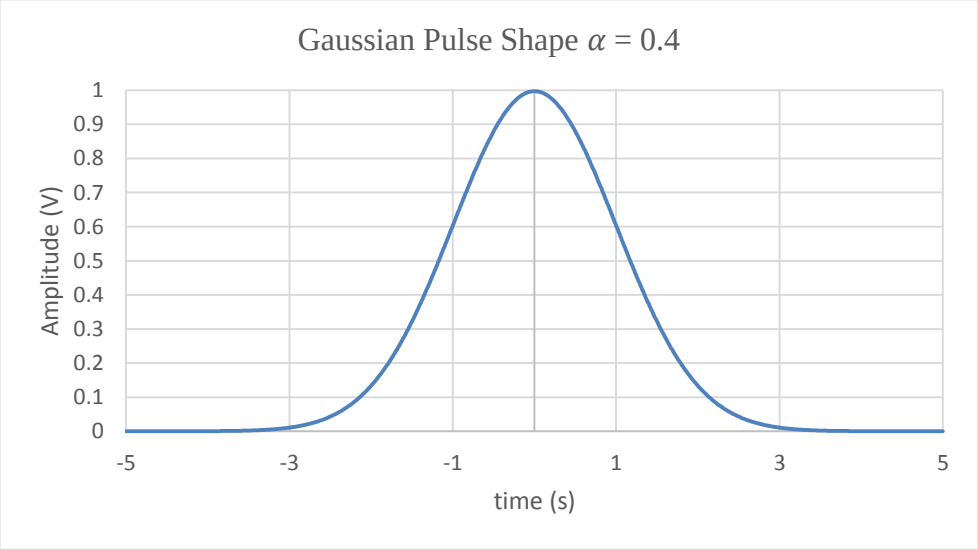


Figure 2-25 Gaussian impulse response (author generated image)

2.5.3 ISI and Pulse Shaping

The effect of ISI is demonstrated using rectangular pulses, defined by the sinc function of Equation 2-29 (Bateman, 1998).

$$sinc = \frac{sin(x)}{x} \quad (V) \qquad \text{Equation 2-29}$$

Where, x, is defined as πt, and which generates a pulse with a period of one second. Figure 2-26 shows the response of a sinc pulse (N), with identical adjacent pulses (N+1 and N-1). The ringing components are shown with zero crossings nulls at time zero, plus one and minus one, and indicate that no ISI occurs at the peaks of the pulses. This means the optimal sampling instances following the comparator, must occur at the peaks of the pulses to eliminate ISI. When sampling at the centre of the received pulse is used, this is referred to as central decision detection (M. J. N. Sibley, 1995).

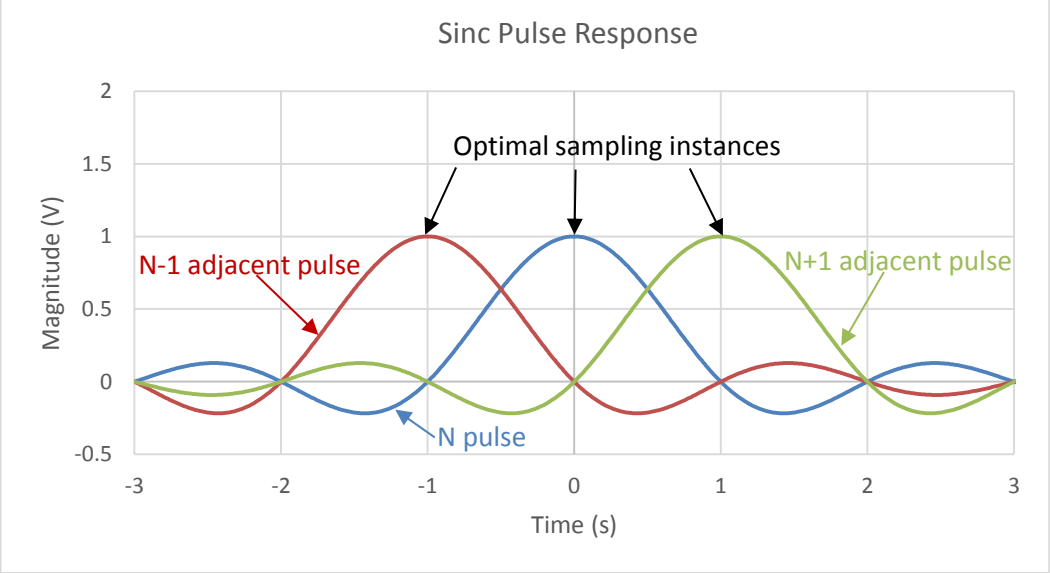


Figure 2-26 Sinc pulse response (author generated image)

In order to limit the effects of ISI, pulse shaping of the received pulses is necessary in the pre-amplifier and in the pre-detection filter. The bandwidth of the OWC systems

pre-amplifier is limited to 50% pulse bandwidth, and the pre-detection filter is limited to 70% of the pulse bandwidth, where the pre-detection filter is realised using a 3rd order Butterworth low-pass filter (M. J. N. Sibley, 1995).

2.5.4 Pulse Bandwidth

The spectrum of rectangular pulse based modulation scheme, such as OOK or PPM, is defined by the sinc function shown in Equation 2-30 (Bateman, 1998).

$$\left|H_p(\omega)\right| = \left|V\tau\ sinc\left(\frac{\omega\tau}{2}\right)\right| \quad (V) \qquad \text{Equation 2-30}$$

Where V is the maximum amplitude of the spectrum in volts, and τ is the period of the pulse in seconds. The spectrum of Equation 2-30, where the amplitude and pulse period are at unity, is shown in Figure 2-27.

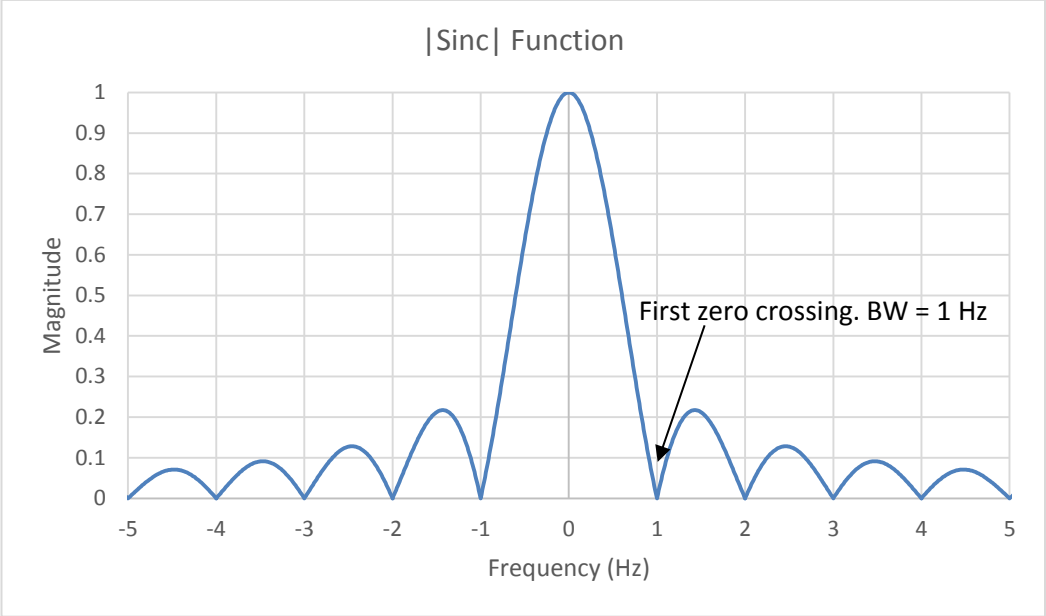


Figure 2-27 Rectangular pulse spectrum (author generated image)

Although, the spectrum extends to infinity, the bandwidth of the pulse is generally defined at the first zero crossing, which in this case is shown at 1 Hz, and is given by Equation 2-31 (Bateman, 1998).

$$BW = \frac{1}{\tau}\ (Hz) \qquad \text{Equation 2-31}$$

The bandwidth of a pulse based modulation scheme, is defined by the inverse of the pulse period, which is equal to the serial clock frequency of the system used to transmit the pulse. In the case of the VLC system, the minimum serial clock is defined by Equation 2-14 as described in section 2.1.6.

$$f_{MIN\ SER\ CLK} = N\ f_{TS\_CLK}\ (Hz) \qquad \text{Equation 2-14}$$

In conclusion, the system model for the IM/DD architecture consists of simple analogue processing blocks that are easy to implement. Using this architecture, it is possible to encode the parallel MPEG TS output of a STB, using a suitable digital modulation scheme, serialise the resultant encoded stream, and use it to intensity modulate the LEDs light emission and transmit it over the optical channel. At the receiver, the optical intensity of the light, which is directly proportional to the encoded MPEG TS, is detected by the PD and converted to a photocurrent. The pulses emerging from the PD, are assumed to exhibit a Gaussian shape with ringing, where the ringing causes an effect called ISI which increases the BER of the system, therefore, the receiver is required to process the pulses in such a way as to minimise ISI. It was indicated that a pre-amplifier bandwidth should be limited to 50% of the pulse bandwidth and pre-detection filter limited to 70% of the pulse bandwidth in order to reduce ISI. The received pulses, following conditioning, are optimally sampled at the centre of the pulses using central decision detection. The bandwidth of the OWC system is defined by the first zero

crossing of the pulse spectrum, which is ultimately determined by the inverse of the pulse period, and therefore the serial clock frequency of the system.

2.6 OWC System Electrical Modelling

This section provides details about the theory and modelling of the analogue devices and subsystems required by the VLC system.

2.6.1 TCA

The purpose of the TCA is to translate the fixed voltage levels representing ones and zeroes in a digital stream, into equivalent current levels which are directly proportional to the voltage levels, and that act as the drive current for the LED. Field-effect transistors (FET), configured to operate as switches, can be arranged into a number of circuit topologies that enable on/off modulation of the LED (Z. e. Ghassemlooy et al., 2013). Figure 2-28 shows three LED current driver topologies that use a digital input voltage as a signal source. The key reason for using the FET device, is its low conduction resistance, which enables the device to carry high drain-source current (I_{DS}) with low-power dissipation.

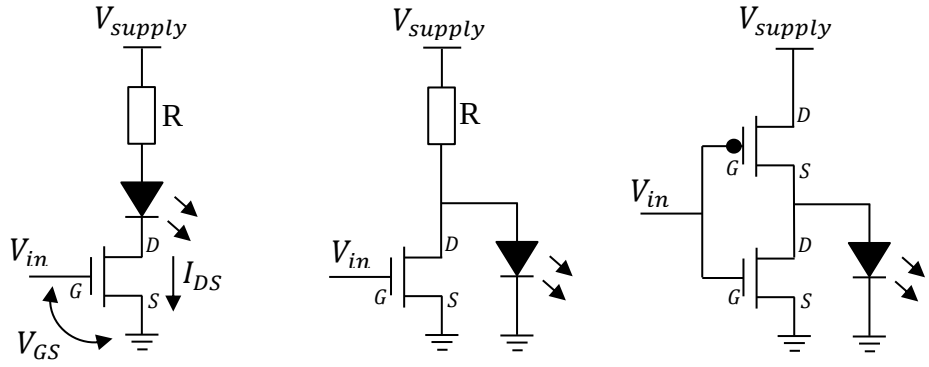


Figure 2-28 On/off FET switch topologies (Z. e. Ghassemlooy et al., 2013)

The circuit in Figure 2-28a uses a FET connected in series with a resistor and an LED. A digital voltage stream, V_{in}, is applied across the gate and source (V_{GS}) of the FET, and as V_{in} increases, the I_{DS} current flowing through the FET also increases, resulting in current flowing through the LED. In this condition, the FET is switched on and a voltage develops across the drain-source junction (V_{DS}) which is smaller than the forward bias voltage of the LED (V_F), therefore a series resistor, R, is required to limit forward bias current (I_F) flowing through the LED. I_F is calculated using Ohm's law, as defined by Equation 2-32.

$$I_F = \frac{V_{supply} - V_F}{R} \quad (A) \qquad \text{Equation 2-32}$$

The transconductance (g_m) of the FET is defined by Equation 2-33, and has the unit Siemens (S).

$$g_m = \frac{I_{DS}}{V_{GS}} \quad (S) \qquad \text{Equation 2-33}$$

The LED in this circuit is switched on when a positive voltage (logic one) is applied to the gate of the FET (Halbritter, Jäger, Weber, Schwind, & Möllmer, 2014). The switching speed of the circuit is limited by the internal capacitance of the LED and the series resistor, which form an RC circuit. It is therefore important that the capacitance and resistance in the circuit are as small as possible to achieve high-speed switching. An alternative circuit is shown in Figure 2-28b, where the LED is constantly forward biased by the limiting resistor, and the LED is switched off when a positive voltage (logic one) is applied at the gate of the FET. In this instance, when the FET is switched on, the LED current is bypassed via the drain-source junction of the FET, enabling fast discharge of the LED through the low resistance of the drain-source junction ($R_{DS\,ON}$). This circuit,

however, produces asymmetrical rise and fall-times, which is caused by difference in the values of the series resistor and drain-source junction resistance. Issues introduced by this asymmetry are overcome by using the CMOS inverter circuit shown in Figure 2-28c. In this configuration, when the input voltage is at zero (logic zero), the lower FET is switched off, and the upper FET is switched on, enabling forward bias current to flow through the LED. When a positive voltage (logic one) is applied to the input of the circuit, the upper FET is switched-off, and the lower FET is switched on, enabling fast discharge of the LEDs internal capacitance. The parameters of the upper and lower FETs can be optimised to achieve symmetrical rise and fall-times.

The FET circuits are modelled using standard SPICE models for FET devices, which are provided by semiconductor vendors.

2.6.2 LED

The LED is modelled with a series resistor (R_S) and inductor (L) circuit, connected to parallel capacitor (C_D) and diode (D) circuit, as shown in Figure 2-29 (O'Brien, Zeng, Minh, & Faulkner, 2008). Behaviourally, the LED operation is similar to a P-N junction diode, where the ideal current–voltage characteristic of the device is defined by Equation 2-34.

$$I_D = I_S\, e^{\frac{qV_D}{nkT}} - 1 \qquad (A)$$ Equation 2-34

Where I_D and V_D are the diode current and voltage, respectively, I_S is the reverse saturation current, q is the charge on an electron, k is Boltzmann's constant, T is temperature in degrees Kelvin, and n is the ideality factor: n=1 for indirect semiconductors such as Si or Ge, and n=2 for direct semiconductors such as GaAs and InP.

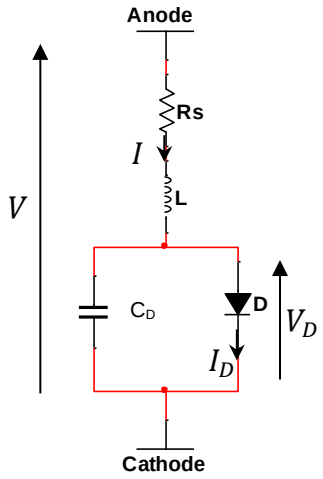


Figure 2-29 LED electrical model (O'Brien et al., 2008)

The capacitor, C_D, in the circuit, represents the internal intrinsic capacitance of the diode (this is the internal capacitance mentioned in the TCA section), and is comprised of two parallel capacitances; the depletion capacitance C_d , which is due to the P-N junction depletion region and is dominant under reverse bias conditions, and the charge diffusion and storage capacitance, C_s, which is dominant under forward bias conditions. The total capacitance is expressed by Equation 2-35.

$$C_D = C_d + C_s \qquad (F) \qquad \text{Equation 2-35}$$

Using the LED electrical model as the load for the TCA circuit, enables the switching speed of the transmitted to be simulated. Model parameters for an Osram Luxeon, phosphor based LED were reported by O'Brien et al.: $R_S = 0.9727\ \Omega$, $L = 33.342\ nH$, $C_d = 2.567\ nF$ and $C_s = 2.8\ nF$ $(C = 5.367\ nF)$ (O'Brien et al., 2008). These data represent the range of the parameters expected for an LED. Characterisation of a white and blue LED will be presented in Chapter 5.

2.6.3 PD

Photodetectors are square-law devices which generate a photocurrent that is proportional to square of the optical field incident on the active detection surface of the PD. There are two key types of PDs available: the first is the positive-intrinsic-negative (PIN) PD and the second is the avalanche PD (APD) (Z. e. Ghassemlooy et al., 2013). Silicon based PD devices have the highest sensitivity over visible wavelengths of the electromagnetic spectrum (375–780 nm). Silicon APD devices are used in high-speed applications due to their fast rise time. The devices also provide amplification of the photocurrent. However, APDs suffer from higher noise levels and require high bias voltages, typically of the order of 200 V, when compared to PIN based devices. In particular, the APDs bias voltage is impractical for STBs, since such high voltage rails are not support. Silicon PIN PDs are more practical in STB applications, since their bias voltages are lower, of the order of tens of volts. Table 2-5 shows the comparison between PIN and APD silicon PD.

Parameter	**PIN**	**APD**
Wavelength range (nm)	400-1100	
Peak (nm)	900	830
Responsivity R (A/W)	0.6	77-130
Quantum efficiency (%)	65-90	77
Gain	1	150-250
Bias voltage (-V)	45-100	220
Dark current (nA)	1-10	0.1-1.0
Capacitance (pF)	1.2-3	1.3-2
Rise time (ns)	0.5-1	0.1-2

Table 2-5 PIN and APD silicon PD comparison (Z. e. Ghassemlooy et al., 2013)

The PDs ability to convert photons in to electrons is referred to as the quantum efficiency, η, and is given by Equation 2-36 (Z. e. Ghassemlooy et al., 2013).

$$\eta_{qe} = \frac{Output\ electrons}{input\ photons}$$ Equation 2-36

Quantum efficiency is also related to the responsivity of the PD, and is given by Equation 2-37.

$$R = \frac{\lambda q \eta_{qe}}{hc} = \frac{\lambda}{1.24}\eta_{qe} \qquad (A/W)$$ Equation 2-37

Where λ is the operating wavelength of the PD in μm, q is the charge of an electron, h is Planck's constant and c is the speed of light. High responsivity is desirable as the PD exhibits higher sensitivity i.e. lower optical power is required to generate photocurrent.

Dark current is the current that flows in the PD in the absence of incident light on the PD, and effectively sets the noise floor of the device in a VLC system, since the minimum detectable optical signal must generate a photocurrent which exceeds the dark current. The dark current is caused by background radiation and the saturation current of the semiconductor junction.

Low capacitance is also desirable in the PD, as this parameter limits the bandwidth and response time of the device. The larger the surface area of the PD, the larger the capacitance of the PD, and hence the lower the bandwidth (Z. e. Ghassemlooy et al., 2013).

The practical choice for the PD of the VLC system is the PIN based device, since it has the lowest bias voltage, which can be accommodated by the STB platform. The PD is easily modelled as a current source in parallel with a capacitor, however, since the device has both an optical and electrical interface, it is more appropriate to characterise the device using empirical measurements.

2.6.4 Pre-amplifier

The pre-amplifier in the VLC system translates the photocurrent of the PD into a voltage, and also provides signal gain. The transimpedance of the pre-amplifier is defined by Equation 2-38.

$$Z_T = \frac{V_{out}}{I_p} \quad (\Omega) \qquad \text{Equation 2-38}$$

Where I_p is the photocurrent generated by the PD, and is applied to the input of the pre-amplifier, and V_{out} is the output voltage of the pre-amplifier.

The pre-amplifier can be modelled for rectangular input pulses using an operational-amplifier (op-amp) with a transfer function approximated by a single-pole frequency response (M. J. N. Sibley, 1995). The transimpedance amplifier circuit shown in Figure 2-30 produces a maximally flat 2nd order Butterworth response (Horowitz, 2015). The PD is connected to the inverting input of the op-amp, and is modelled as a current source (photocurrent) connected in parallel with a capacitor (C_D). Feedback is provided by R_f and C_f. The non-inverting input is connected to ground via a resistor (R_1) and appropriate decoupling capacitance.

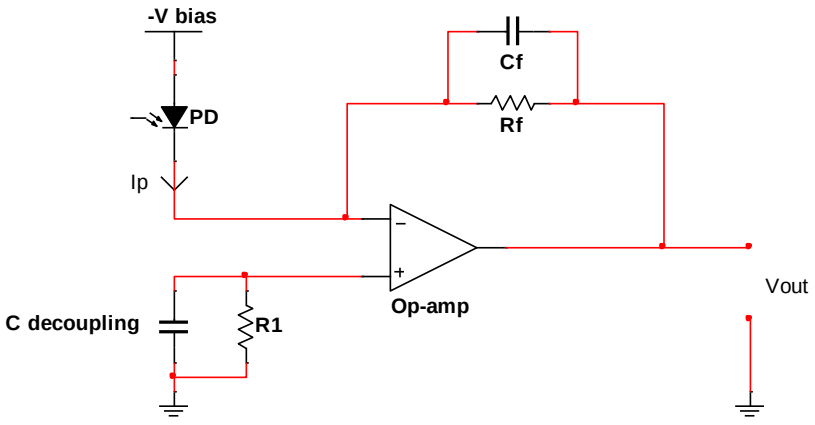


Figure 2-30 Transimpedance amplifier circuit (Horowitz, 2015)

The transimpedance of the circuit is defined by Equation 2-39 (Horowitz, 2015).

$$-R_f = \frac{V_{out}}{I_p} \qquad (\Omega)$$ Equation 2-39

Where the negative sign indicates 180° phase inversion, introduced by the inverting input of the op-amp.

The feedback pole of the circuit is determined by Equation 2-40.

$$\frac{1}{2\pi R_f C_f} = \sqrt{\frac{GBP}{4\pi R_f C_D}} \qquad (Hz)$$ Equation 2-40

Where GBP is the gain-bandwidth product of the op-amp. Note that the value of R_1 is equal to R_f.

The 3dB bandwidth of the circuit is approximated by Equation 2-41.

$$BW_{3dB} = \sqrt{\frac{GBP}{2\pi R_f C_D}} \qquad (Hz)$$ Equation 2-41

Noting that Sibley stated that the 3dB cut-off of the pre-amplifier should be limited to 50% of the transmitter pulse bandwidth (M. J. N. Sibley, 1995).

The pre-amplifier circuit can be modelled using standard SPICE models for op-amp devices, which are provided by semiconductor vendors.

2.6.5 Equalisation

Although Li et al. demonstrated a bandwidth extension of 151 MHz for white LEDs using a combination of passive and active equalisation (Li, 2014), Minh et al. demonstrated a 50 MHz extension using a simple, low-cost, passive 2nd order equaliser

circuit, consisting of resistor and capacitor connected in parallel, as shown in Figure 2-31 (Minh et al., 2009).

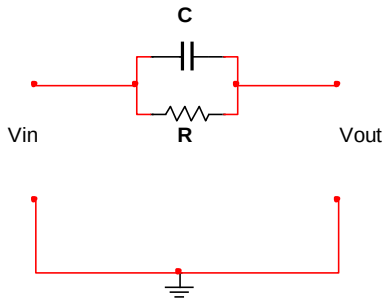


Figure 2-31 Passive equaliser (Minh et al., 2009)

The transfer function of the circuit is defined by Equation 2-42.

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{k} \quad \frac{1 + sT}{1 + s\frac{T}{k}} \qquad \text{Equation 2-42}$$

Where $s = \sigma + j\omega$ is the complex frequency, $\frac{1}{k} = \frac{Z_L}{R+Z_L}$ and $T = RC$. Z_L is the load impedance. The magnitude of the equaliser response is given by Equation 2-43.

$$|H(j\omega)| = \frac{1}{k}\sqrt{\frac{1 + \omega^2 T^2}{1 + \omega^2\left(\frac{T}{k}\right)^2}} \qquad \text{Equation 2-43}$$

This circuit will be used for the initial modelling of the VLC system, and if further bandwidth extension is necessary, active filtering using op-amps will be explored.

2.6.6 Post-amplifier

The post-amplifier is a voltage amplifier which increases the level of the equalised signal prior to detection. The amplifier can be modelled using an inverting op-amp, with feedback, as shown in Figure 2-32.

The voltage gain of the circuit is defined by Equation 2-44 (Horowitz, 2015).

$$Av = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_1} \qquad \text{Equation 2-44}$$

The input impedance of the circuit is determined by the input resistor, R_1, is defined by Equation 2-45

$$Z_{in} = R_1 \qquad \text{Equation 2-45}$$

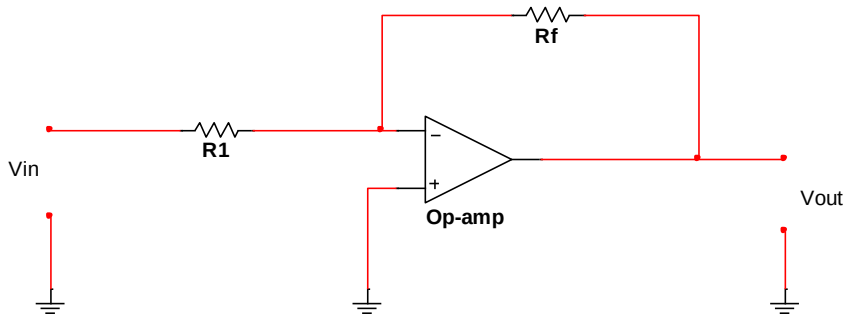


Figure 2-32 Voltage amplifier circuit (Horowitz, 2015)

The post-amplifier circuit can be modelled using standard SPICE models for op-amp devices, which are provided by semiconductor vendors.

2.6.7 Pre-detection Filter

The pre-detection filter is modelled using a 3rd order Butterworth low-pass filter (LPF) and has a 3dB cut-off at 70% of the transmitted pulse bandwidth, as stated by Sibley (M. J. N. Sibley, 1995). A shunt-first Butterworth prototype is shown in Figure 2-33 (Fink & Christiansen, 1989).

The transfer function of the Butterworth prototype is defined by Equation 2-46.

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1 + 2s + 2s^2 + s^3}$$ Equation 2-46

Where $s = \sigma + j\omega$ is the complex frequency.

The magnitude of the LPF is given by Equation 2-47.

$$|H(j\omega)| = \sqrt{\frac{1}{1 + \omega^6}}$$ Equation 2-47

And the phase angle of the LPF is given by Equation 2-48.

$$\theta(\omega) = \arg\big(H(j\omega)\big)$$ Equation 2-48

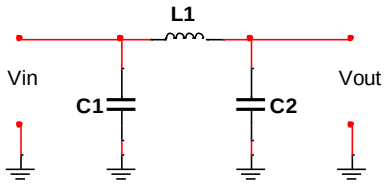


Figure 2-33 3rd order Butterworth LPF

2.6.8 Comparator

Following the pre-detection filter, the comparator is used to detect when the received signal exceeds a predetermined threshold reference voltage. Ideally, when detecting digital pulses, which have only two possible voltage levels, the threshold voltage is set to 50% of the input voltage range. For example, if the input voltage range is 0 to 1 V, and the threshold reference is 0.5 V, a logic one is output by the comparator when the input is greater than or equal to 0.5 V, and the logic zero when the input is less than 0.5 V. Figure 2-34 illustrates the input-output transfer characteristic of an ideal comparator, where the input signal is a 1V Gaussian pulse (blue trace) and is compared to a reference voltage of 0.5 V (green trace), resulting in a digital comparator output (red trace).

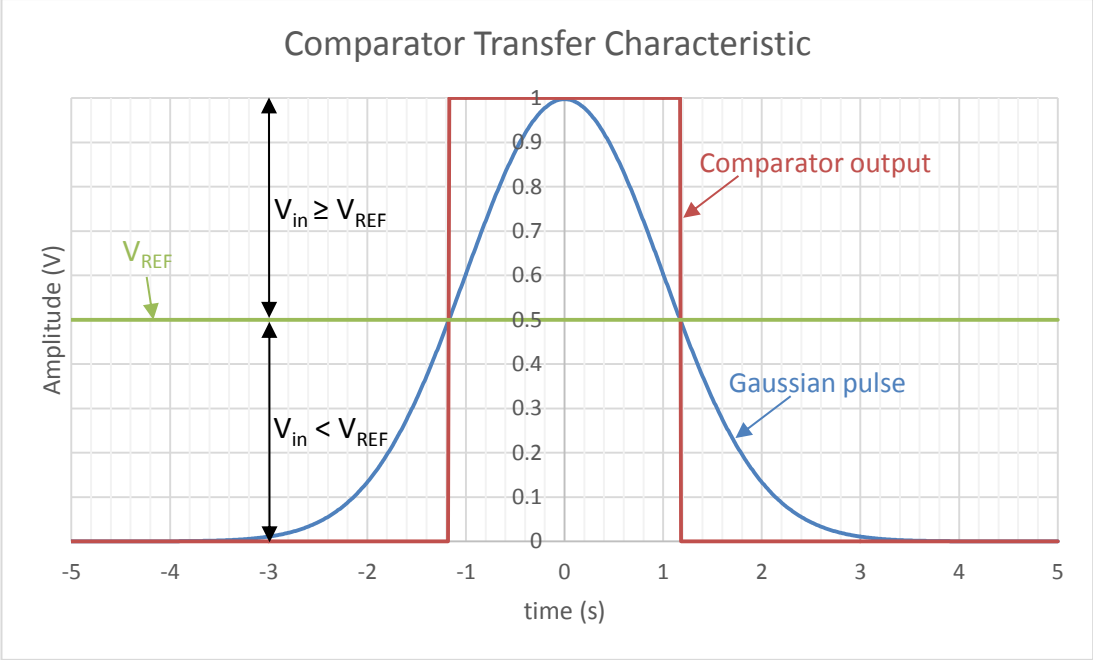


Figure 2-34 Comparator transfer characteristic

The non-inverting voltage comparator circuit is shown Figure 2-35, where the reference voltage, V_{REF}, is set by the potential divider formed by R_1 and R_2 and the supply rail. The input signal is applied to the positive input of the comparator, and the reference voltage is applied to the negative input.

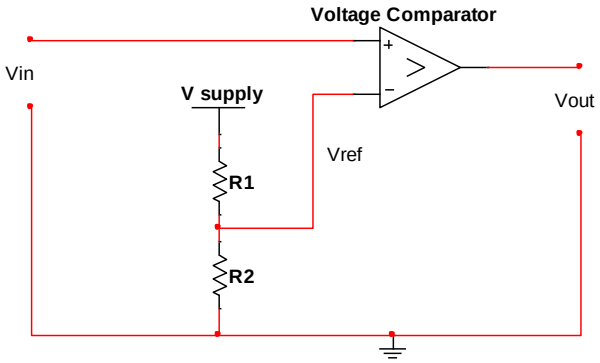


Figure 2-35 Non-inverting voltage comparator circuit (Horowitz, 2015)

The comparator is generally defined by Equation 2-49.

$$V_{out} = \begin{cases} 1, & if\ V_{in} \geq V_{REF} \\ 0, & if\ V_{in} < V_{REF} \end{cases}$$ Equation 2-49

A key parameter of the comparator is that it must be able to switch at a speed which tracks the voltage changes of the applied input signal.

The comparator circuit can be modelled using standard SPICE models for voltage comparator devices, which are provided by semiconductor vendors.

With the analogue processing subsystems defined for digital pulses, it is possible to specify the digital modulation scheme for the VLC system.

2.7 Digital Modulation Scheme

The most commonly used modulation scheme for DLOS based OWC systems is OOK, mainly because of its simplicity and ease of implementation. The scheme was proven by Tanaka et al. in an IM/DD system that achieved a bit rate of 400 Mbit/s (Tanaka, 2003). The scheme is more than capable of supporting the DVB bit rates required by the video distribution system, however, the author decided to pursue a PPM based scheme, because opportunities to reduce the bandwidth of the coding scheme were identified.

2.7.1 Offset PPM

Offset PPM (OPPM), first proposed by Sibley in 2010 (M.J.N. Sibley, 2010), was selected by the author for investigation. OPPM is a variation on digital PPM, and achieves comparable performance, but at half the line rate. The main reasons for choosing to investigate OPPM, were firstly, that the scheme allows continuous coding of the input data stream, which enables the MPEG TS to be coded without the need for costly memory buffering. The second reason is that the scheme is simple to implement using an FPGA platform, since OPPM generates symbols using codewords that rely on

the position of a pulse within a frame, therefore the encoder and decoder subsystems only need to have accurate timing to ensure that the pulse is generated and detected at the correct instance in time; this is a function that is easy to achieve using an FPGA platform.

The comparison between digital PPM and OPPM codewords, based on the coding of 3-bit pulse code modulated (PCM) words, is shown in Table 2-6. In the case of digital PPM, the coding of a 3-bit PCM word, results in the generation of an 8-bit digital PPM codeword ($N_{output\ bits} = 2^{\mathrm{M_{input\ bits}}}$) or frame, which contains only a single pulse, the location of which shifts for each PCM word. Each bit represents a time period referred to as slot-time, and given that only one pulse occurs in each frame, results in a low mark-to-space ratio which improves sensitivity at the receiver (M.J.N. Sibley, 2010). The transmission of a single pulse in each frame also means that the 3rd order Butterworth pre-detection filter described in section 2.6.7 can be used, which further increases sensitivity (M.J.N. Sibley, 2010).

Original PCM word	**Digital PPM codeword**	**Offset PPM codeword**
000	0000 0001	***0*** 000
001	0000 0010	***0*** 001
010	0000 0100	***0*** 010
011	0000 1000	***0*** 100
100	0001 0000	***1*** 000
101	0010 0000	***1*** 001
110	0100 0000	***1*** 010
111	1000 0000	***1*** 100

Table 2-6 Coding table for OPPM and digital PPM (3-bit coding)

(M.J.N. Sibley, 2010)

In the case of OPPM, the scheme is able to operate at half the line rate of digital PPM, through the introduction of a sign bit (shown in bold italic), which enables the coding of a 3-bit PCM word, that results in the generation of a 4-bit OPPM codeword

($N_{output\ bits} = 2^{\mathrm{M_{input\ bits}}-1}$). It can be seen from Table 2-6, that for PCM words below 100_{PCM}, the resultant OPPM codewords are similar to digital PPM, in that only one pulse is transmitted in each frame, except for 000_{PCM} where no pulse at all is transmitted. However, when 100_{PCM} is reached, the sign bit, which is the most-significant-bit (MSB), indicates whether the offset is to be taken from 000_{PCM} or 100_{PCM}. Using this approach, the line rate of offset PPM is exactly half that digital PPM. However, it can be seen that half of the frames now contain two pulses, which Sibley stated would reduce sensitivity at the receiver.(M.J.N. Sibley, 2010). Sibley also reported that the effects of ISI dominate both OPPM and digital PPM schemes, and that in low bandwidth systems the threshold level must be set high enough to counter ISI-induced errors and resolve adjacent pulses.

Other PPM schemes were also investigated, such as differential PPM, digital PIM and DH-PIM, but these schemes require block coding of the data stream to enable the suppression of empty time slots following a pulse, which consequently reduces bandwidth (M.J.N. Sibley, 2010). However, these schemes generate variable length frames, which require complicated encoder and decoder implementations, including the need for memory buffering to avoid under- and over-runs. OPPM eliminates these issues, since the transmitter implementation only requires an M-bit shift register, down-counter, and a 2^{M-1} bit delay to generate the encoded stream. Also, the receiver only requires a simple combinational logic based decoder. Figure 2-36 shows an OPPM encoder/transmitter and receiver/decoder system. The transmitter (Figure 2-36a) works by removing the MSB from the incoming PCM word and delaying it by 2^{M-1} time slots, which generates the offset shown in Table 2-6. The remaining PCM bits are loaded into a down-counter that counts down to zero, and the carry pulse from the counter varies its

position in the frame according to the truncated PCM word. The resultant frame is used to provide current drive for the LED, enabling signal transmission over the FSO channel.

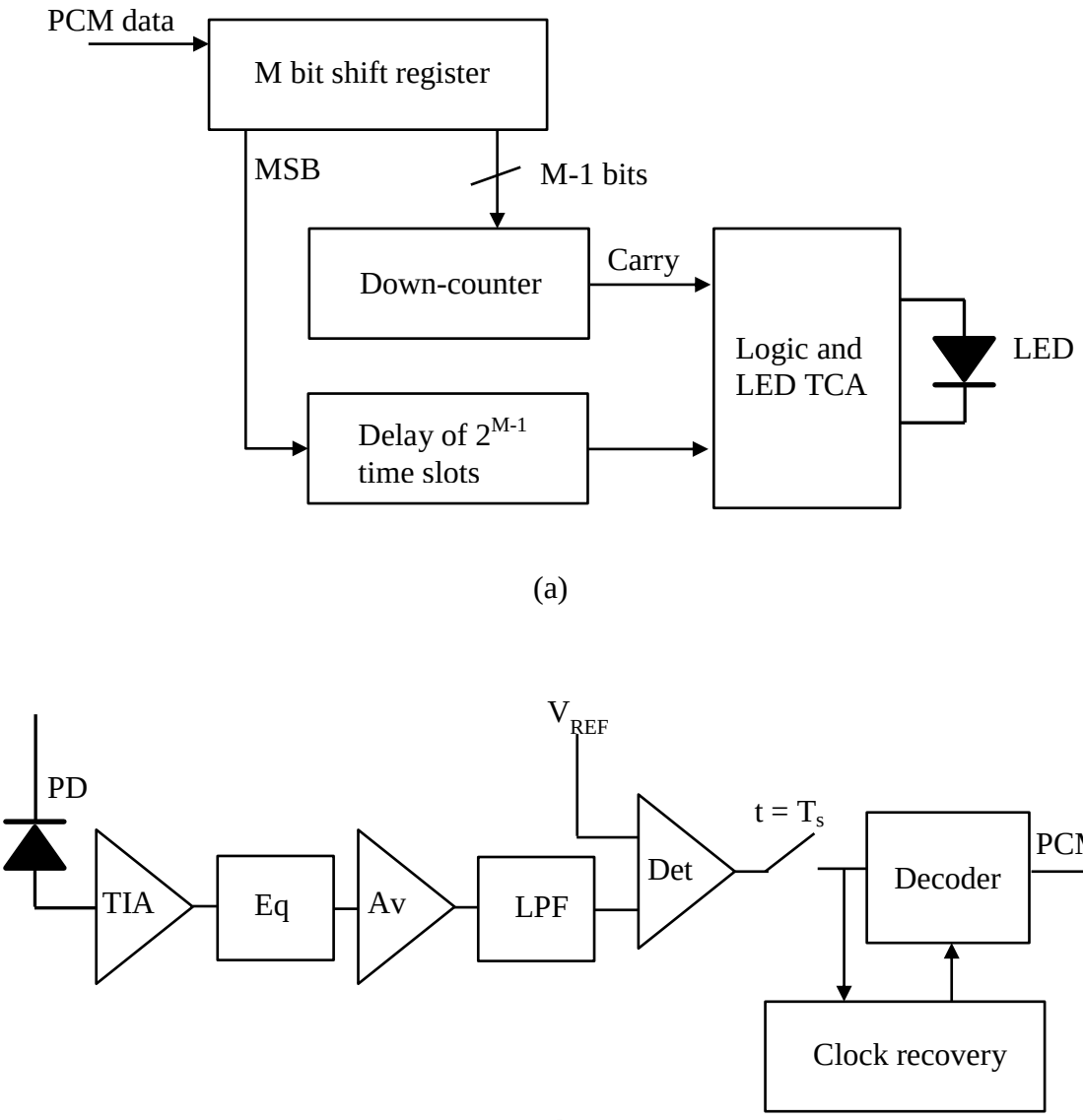


Figure 2-36 Block diagram of an OPPM transmitter and receiver (M.J.N. Sibley, 2010)

At the receiver (Figure 2-36b), the PD photocurrent is amplified and converted to a voltage by the pre-amplifier (TIA), the signal is equalised to compensate for channel and LED roll-off and then amplified by the post-amplifier (Av), pre-detection filtering (LPF)

is then applied. The output signal of the filter is then fed to a comparator (Det), whose threshold is set by V_{REF}. The output of the comparator is sampled at time periods T_s, which is equal to the slot-time of the OPPM encoded signal, but shifted so that the sample time coincides with the centre of the detected pulse (central decision detection). The sampled signals are then reconstructed into OPPM frames and decoded. Clock recovery circuitry is used to recreate the serial clock used to transmit the OPPM frames, and also enables synchronisation of the clocks in the transmitter and receiver.

2.7.2 OPPM Errors

Three error types of error are generated in OPPM systems: wrong slot, erasure and false-alarm errors. A wrong slot error occurs when noise on the leading edge of the pulse causes a threshold crossing in the time slot immediately before or immediately after the current slot. The probability of this error occurring is given by Equation 2-50.

$$P_s = \frac{1}{2}\, erfc\left(\frac{Q_s}{\sqrt{2}}\right) \qquad \text{Equation 2-50}$$

Where Q_s is defined by Equation 2-51.

$$Q_s = \frac{T_s}{2}\,\frac{slope(t_d)}{\sqrt{\langle n_o^2 \rangle}} \qquad \text{Equation 2-51}$$

The parameter T_s is the slot time, $slope(t_d)$ is the slope of the received pulse at the decision time t_d and $\langle n_o^2 \rangle$ is the mean squared noise presented to the threshold detector represented by the voltage comparator in Figure 2-36. The decision time is dependent on where V_{REF} is set for the received pulse. This form of error occurs when the bandwidth of the system is low, resulting in slow rise and fall time and pronounced slopes on the pulses.

An erasure error occurs when noise corrupts the pulse amplitude, such that the voltage level of the pulse drops below V_{REF}. The probability of this error occurring is given by Equation 2-52.

$$P_{er} = \frac{1}{2}\, erfc\left(\frac{Q_{er}}{\sqrt{2}}\right) \qquad \text{Equation 2-52}$$

Where Q_{er} is defined by Equation 2-53.

$$Q_{er} = \frac{v_{pk} - V_{REF}}{\sqrt{\langle n_o^2 \rangle}} \qquad \text{Equation 2-53}$$

The parameter v_{pk} is the peak signal voltage within the slot-time.

Finally, a false alarm error occurs when noise that occurs in an empty slot causing a threshold crossing, and therefore a false pulse. The probability of this occurring is given by Equation 2-54.

$$P_f = \frac{T_s}{\tau_R}\frac{1}{2}\, erfc\left(\frac{Q_t}{\sqrt{2}}\right) \qquad \text{Equation 2-54}$$

Where the term $\frac{T_s}{\tau_R}$ is the number of uncorrelated noise samples per time slot, and τ_R is the time at which the autocorrelation time has become small. Q_t is given by Equation 2-55.

$$Q_t = \frac{V_{REF} - v_{ISI}}{\sqrt{\langle n_o^2 \rangle}} \qquad \text{Equation 2-55}$$

Where v_{ISI} is any signal voltage that is present in a particular time slot.

Sibley concluded that OPPM achieved a bit rate, half that of digital PPM, and with a sensitivity improvement of 3.1 dB in low bandwidth systems. It was also concluded that the effects of inter-symbol interference dominate both OPPM and digital PPM schemes,

and that in low bandwidth systems the threshold level must be set high enough to counter ISI-induced errors and resolve adjacent pulses.

2.7.3 OPPM Encoder/Transmitter (MPEG TS)

It is possible to apply 3-bit OPPM coding to the 10-bit parallel MPEG TS output by a STB. OPPM generates N number of time slots based on M number of input bits to be coded, as described by Equation 2-56.

$$N = 2^{\mathrm{M}-1} \qquad \text{Equation 2-56}$$

The OPPM bandwidth is defined by Equation 2-57.

$$\mathrm{B} = \frac{N}{T} \qquad (Hz) \qquad \text{Equation 2-57}$$

Where T represents the total time required to transmit the OPPM frame. In order to reduce the bandwidth, either the total time required to transmit the OPPM frame must be increased or the number of slots per frame must be reduced. In the case of the parallel MPEG TS frames, T is fixed, and is defined by the inverse of the parallel MPEG clock frequency. Since the MPEG TS is continuous, one coded MPEG TS frame must be transmitted by the VLC system for every MPEG TS clock cycle.

The OPPM architecture proposed by Sibley, can be modified to enable 3-bit encoding of the 10-bit parallel MPEG TS, as shown in Figure 2-37. In this architecture, nine bits of the MPEG TS, namely the eight MPEG TS data bits and the synchronisation bit, are encoded using three, 3-bit OPPM encoders. The tenth bit, which is the MPEG TS valid bit, is left un-encoded since the bit changes state infrequently and therefore has a lower error probability than the other MPEG TS bits. The OPPM encoders, rather than using

the down-counter and delay blocks used by Sibley, can be implemented using simple combinational logic circuits.

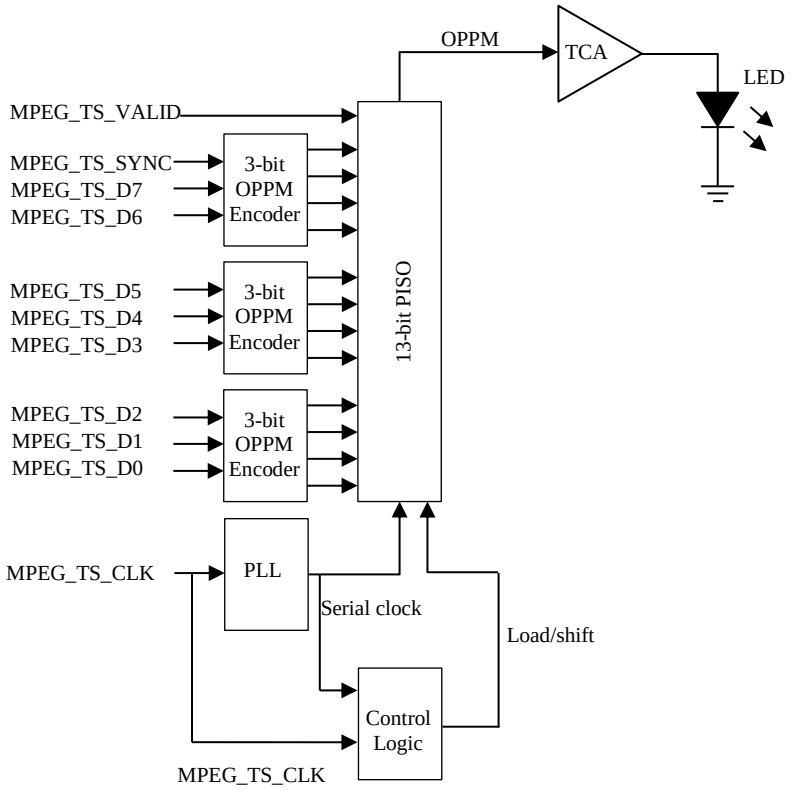


Figure 2-37 OPPM MPEG TS encoder and transmitter

The operation of the systems is thus: following the encoding of the MPEG TS, the 13-bit output is loaded into a parallel-in-serial-out (PISO) shift-register. The parallel loading and serial shifting of the PISO is performed by the control logic block, which produces the load and shift control signals based on the parallel MPEG TS and serial clocks. In order to load the PISO, the falling- or rising-edge of the parallel MPEG TS CLK must be detected. Assuming the parallel clock uses rising-edge clocking, the PISO is loaded on falling-edge of the clock, which is precisely half-way through a complete parallel clock cycle, meaning that the propagation delay of the OPPM combinational logic encoders must be less than the half the period of the parallel clock. The serial clock is

provided by a phase-lock loop (PLL) which is phase-locked to the parallel MPEG TS CLK, and since 13-bits must be clocked out of the PISO, the serial clock operates at fourteen times the MPEG TS clock frequency; one serial clock cycle is needed to load the PISO and thirteen clock cycles are needed to clock-out the 13-bits. During the load operation of the PISO, the falling-edge of the parallel clock is detected, and is used to trigger the load pulse for the PISO, the control logic block then counts one cycle of the serial clock and then sets the PISO into the shift mode. The serial clock, then clocks-out the 13-bits stored in the PISO, before the next rising-edge of the parallel MPEG TS clock occurs. The serialised bits are fed to the TCA which provides the drive current needed to intensity modulate LED.

The three independent, 3-bit OPPM encoders output three, 4-bit sub-frames, plus the un-encoded valid bit for every 10-bit MPEG TS frame. The bandwidth of the system is now expressed by Equation 2-58.

$$B = \frac{(\mathrm{PN}) + \mathrm{U} + 1}{\mathrm{T}} \qquad (Hz)$$ Equation 2-58

Where, P represents the number of OPPM sub-frames, U represents the number of un-coded bits added to the beginning or end of the cascaded frames. The plus one term indicates the additional clock cycle needed to load the PISO. Figure 2-38 illustrates the 10-bit MPEG TS frame and how it is mapped to a 13-bit sequence, following the 3-bit OPPM coding and the addition of the un-coded valid bit.

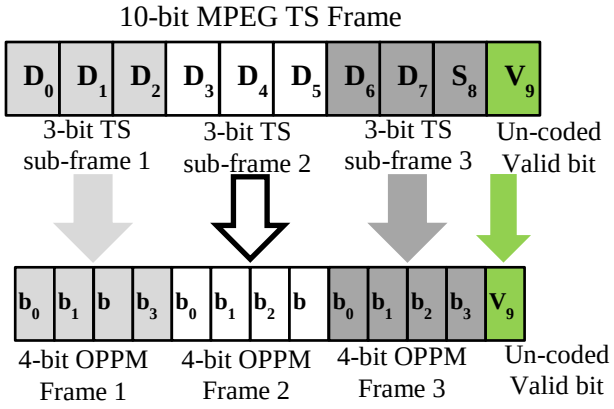


Figure 2-38 10-bit MPEG TS to 4-bit sub-frame OPPM

2.7.4 OPPM On/Off LED Driver

OPPM permits the use of a simple on/off LED driver circuit, such as one of the topologies described in section 2.6.1. Assuming the driver circuit of section 2.6.1, Figure 2-28a is used, the serialised OPPM signal can be applied directly to the gate of the driving FET. Figure 2-39 illustrates a 4-bit OPPM frame, 1001_{OPPM} (101_{PCM}), applied, MSB bit first, to the gate of a FET on/off LED driver. The OPPM frame time period (T) is comprised of equal bit periods (t_n), representing the slot-time. At t_1, a logic '1' is applied to the gate, which switches the FET on, allowing current to flow through the drain-source junction of the device and through the LED, resulting in light emission. The intensity of the LED emission is set by the limiting resistor, R. At t_2, a logic '0' is applied to gate and the FET is switched off, causing the flow of the drain-source and LED current and light emission to cease. This on/off modulation of the LED is repeated for t_3 through t_4. The presence or absence of the light emission is used to transmit the bits of OPPM frame over the FSO channel.

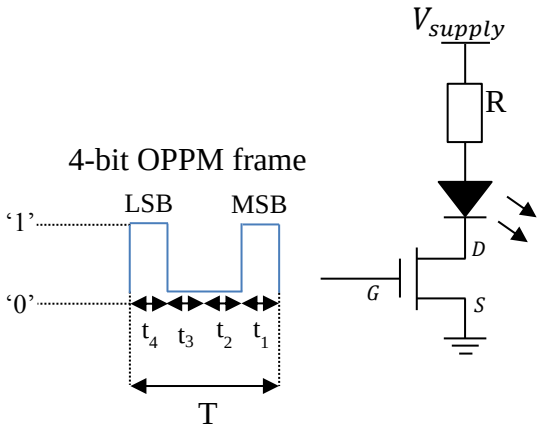


Figure 2-39 OPPM LED driver

2.7.5 OPPM Receiver/Decoder (MPEG TS)

The OPPM receiver architecture is shown in Figure 2-40. The transmitted light signal is received by the photodiode, and the signal is processed by the analogue sub-systems.

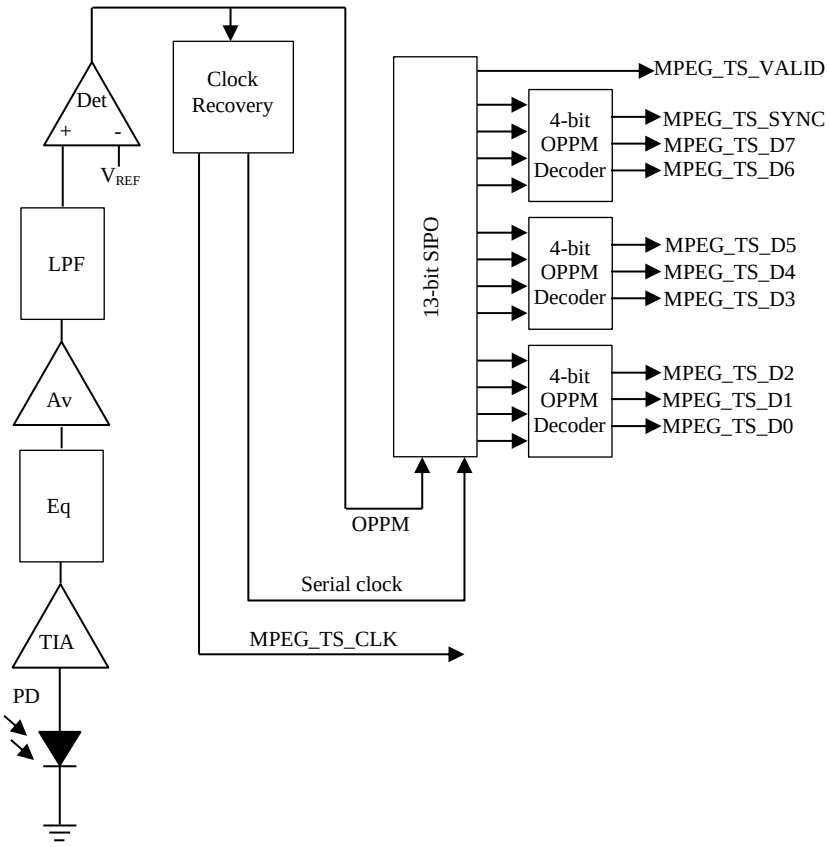


Figure 2-40 OPPM MPEG TS receiver and decoder

The comparator (Det) outputs a digital signal which is fed to a clock recovery block that phase-locks the serial and parallel clock frequencies. This block also provides synchronisation of the 13-bit OPPM frame with receiver, so serial shift and parallel load timing of the serial-in-parallel-out (SIPO) is performed correctly. Parallel OPPM decoding is performed by three, 4-bit OPPM decoders which are implemented using combination logic circuits. The output MPEG TS is then available to be clocked in parallel into the STBs processor for decoding.

The OPPM architecture described could be used for the VLC system, however, the author identified a modification to the OPPM scheme which enabled the number of bits from the encoders to be reduced from 12-bits to 9-bits, thereby reducing the bandwidth of the system. The modified scheme is presented in Chapter 3.

2.8 Conclusions

In the first section of this chapter, a theoretical review of the DVB transmit and receive path used, respectively, to encode and decode broadcast video, audio and data content was presented. A detailed system overview of the DVB transmitter and receiver, with particular emphasis on the DVB-T and DVB-T2 standards, was provided. The encoding and multiplexing of the MPEG TS in the transmitter, and demultiplexing and decoding in the receiver was presented, along with a detailed analysis of the physical layer of the MPEG TS bus at the DVB receiver.

It was concluded in this section of the chapter that:

- The MPEG TS is sourced at the output of a demodulator IC and sinked at the input of the processor IC, and that the VLC systems encoder and decoder can be connected at these interface points.

- The MPEG TS is output in either parallel or serial mode, and that parallel mode is the most commonly used mode in STB platforms. It was also stated that the parallel mode enables combinational logic circuits to be used to encode and decode the MPEG TS.
- The parallel MPEG TS uses a10-bit wide data bus, comprising eight data lines ($D7_{MSB}$ to $D0_{LSB}$), one TS_VALID line, one TS_SYNC line. All 10-bits are clocked in parallel and simultaneously using a clock referred to as the TS_CLK. The VLC system must re-encode bus using a suitable modulation scheme, and serialise the encoded stream to enable its transmission over the FSO channel.
- The MPEG TS has a TS_ERR line, but this bit is redundant and not required in the VLC system, since packet errors are reported by the 1-bit transport error indicator in the TS header. This eliminates the TS_ERR line from the transmitted bits, and therefore saves bandwidth.
- The minimum serial clock frequency of the VLC system is calculated using Equation 2-14, where the number of bits in the MPEG TS is multiplied by the frequency of the parallel MPEG TS clock. The minimum serial clock frequency also defines the minimum bandwidth of the VLC system.
- Real-time coding of the MPEG TS is desirable in the hardware implementation of the VLC video distribution system, since no memory buffering is needed, therefore system cost and complexity is reduced.
- Characterisation and analyses of STB platforms is necessary in order to determine the logic levels used for the MPEG TS and also to determine the parallel clock frequency used, which ultimately determines the minimum serial clock and bandwidth of the VLC system. This work is addressed in Chapter 4.

- The minimum bit rate of the VLC system was identified by the DVB-T2 maximum bit rate of 50.3 Mbit/s required to support HDTV multiplexes.

The second section of the chapter, provided a detailed review of modern FSO VLC systems based on non-coherent LED light sources. An overview of the emergence of VLC was given, followed by a brief history of the evolution of LEDs and their role in the development of VLC systems. The theory of channel models, modulation schemes, and LEDs and PDs and supporting circuitry was also given.

It was concluded in this section of the chapter that:

- Directed LOS (DLOS) transmission was appropriate for the VLC system, since it is the simplest to implement and achieves the highest optical power at the receivers PD. In addition to low irradiance angle at the LED and low FOV angle at the PD, it was also concluded that collimation and focussing of the transmitted light using of concentrators (lenses) at the transmitter and receiver could be used to increase power at the receiver. The use of DLOS also reduced multipath interference.
- An intensity modulated (IM) and direct detection architecture is the simplest to implement for the VLC system.
- A white, phosphor based LED is a potential optical source candidate for the VLC system. However, it was indicated that blue optical filtering was needed to increase the LEDs unfiltered bandwidth from 2.5 MHz to 20 MHz with filtering. Using this technique, sensitivity is reduced at receiver, due to the power loss incurred by the optical attenuation of the filter.
- A single colour blue wavelength LED, was also presented as an optical source candidate. Unfiltered bandwidths of 10 MHz were reported, with potential to

achieve higher sensitivity at the receiver, since blue wavelength LEDs generate higher photon energy as stated by the Planck–Einstein relation (Equation 2 16).

- Characterisation and analyses of white and blue LEDs is necessary to determine the device with the widest bandwidth and the amount of post-equalisation necessary in the receiver. This work is addressed in Chapter 4.
- Intensity modulation of the LED using on/off switching and FET based was suitable.
- Electrical bandwidth extension of the LED is possible using passive and/or active post-equalisation; where post-equalisation is performed in the receiver. Bandwidths of up to 151 MHz were stated, where a combination of passive and active electrical equalisation, and blue optical filtering was used. Passive equalisation using a 2^{nd} order RC circuit will be attempted first, followed by active equalisation if the passive approach is inadequate.
- A PIN PD was suitable for the VLC system, since it has the lowest bias voltage, which can be accommodated by the STB platform.
- The optical channel is expected to generate Gaussian shaped pulses at the receiver. A technique for electrical modelling of the Gaussian shape of the pulses will be introduced in Chapter 5. Modelling the optical channel using electrical techniques enables the entire VLC system to be modelled using an electrical circuit simulator.
- The bandwidth of the pulse was defined by the sinc function. The received pulses would incur ringing caused by the optical channel, resulting in ISI. The effects of ISI is limited by controlling bandwidth of the pre-amplifier and pre-detection filter in the receiver. The pre-amplifier requires a bandwidth of 50% the pulse bandwidth, where the pulse width is equal to the serial clock frequency

of the system, and the pre-detection filter is limited to 70% of the pulse bandwidth. The pre-detection filter is realised using a 3rd order Butterworth low-pass filter.

- Central decision detection is required to sample the detected pulse in order to limit the effects of ISI.
- The bandwidth of the VLC system is determined by the first zero crossing of the received pulse spectrum.
- The VLC system will be modelled using an electrical simulator, and SPICE models used for key semiconductor devices.
- Pre- and post-amplification is achievable using op-amp circuit topologies.
- Pulse detection is achievable using a voltage comparator.
- Offset PPM was identified as a potential candidate for re-encoding the MPEG TS, because of its simplicity and ease of implementation in an FPGA. OPPM also enables continuous coding of the MPEG TS, meaning that memory buffering is unnecessary; therefore the coding scheme is low-cost to implement.
- An OPPM encoder/transmitter and receiver/decoder architecture for the VLC system was presented. However, a modification to the OPPM scheme that can offer reduced bandwidth is proposed in Chapter 3.

With the theoretical aspects of the VLC system now defined, the first task is to establish the coding scheme used by the VLC system. The OPPM architecture presented in this Chapter, forms the basis of the proposed scheme which will be presented in Chapter 3. The second task is to characterise and analyse MPEG TS source and sink devices and LED devices, in order to determine the serial clock requirements and ultimately the bandwidth of the VLC system.

3 Proposed Coding Scheme

In this chapter, the modification to OPPM, and its application as the proposed coding scheme for the VLC system, is presented. The position of the coding scheme blocks (highlighted in pink) responsible for re-encoding and decoding the MPEG TS in the overall VLC system, is shown in Figure 3-1.

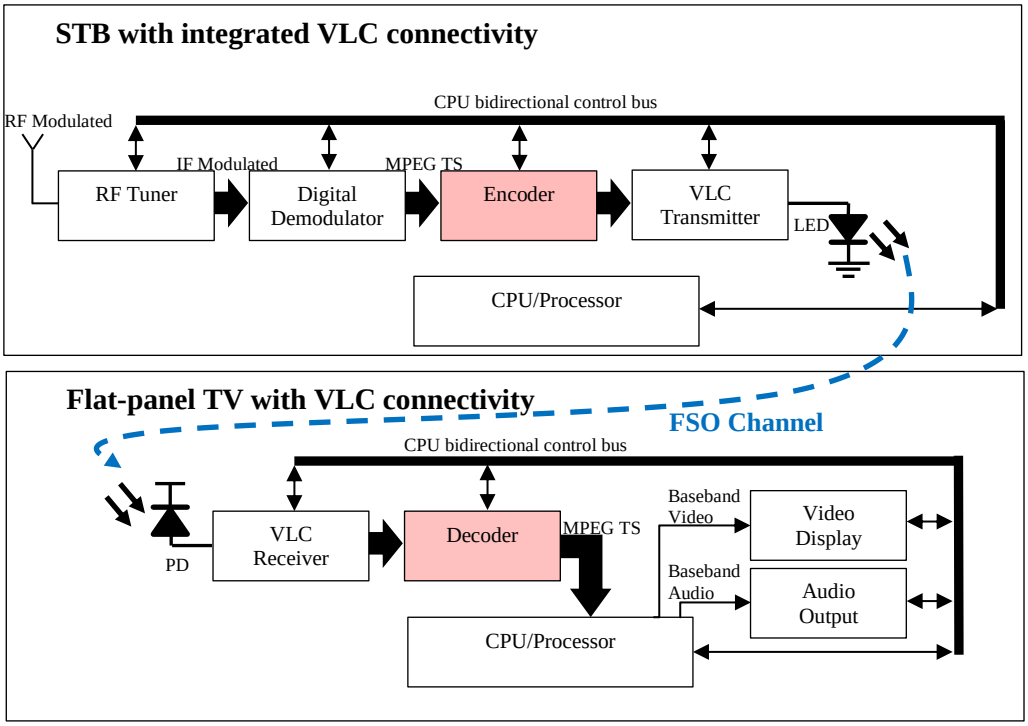


Figure 3-1 VLC MPEG TS encoder and decoder blocks (author generated image)

3.1 Inversion OPPM

3.1.1 IOPPM Encoding (MPEG TS)

It was demonstrated in Chapter 2, section 2.7, that OPPM could be used to encode the 10-bit parallel MPEG TS, resulting in a 13-bit serial stream that could be transmitted over the FSO channel. However, a reduction in the number of bits generated by the OPPM coding scheme is possible, but at the cost of reduced sensitivity at the receiver.

The bit reduction is possible by eliminating the sign bit, and thus its associated time slot, and instead representing it as bipolar voltage levels. This approach results in the generation of two signed codewords for every coded PCM word. Table 3-1 illustrates the comparison between the PCM word, which is subject to coding, and the resulting OPPM and IOPPM codewords. In the case of IOPPM, a positive (IOPPM+) and a negative (IOPPM-) codeword is produced at the output of the encoder; the positive codeword is highlighted in red and the negative in blue. Upon inspection of the IOPPM codewords, it can be seen that only a single pulse exists in each frame, with the exception of two cases, where a single pulse occurs in both the positive and negative codewords for OPPM unsigned (0000_{OPPM}) and signed (1000_{OPPM}) zeroes. The inclusion of two pulses is necessary to distinguish between these two codewords; note that these codewords are horizontal mirror images of each other to ensure uniqueness. The codewords are also constructed so that the positive and negative pulses can coexist in a single, composite binary level signal. This coexistence is illustrated in Figure 3-2, which shows the 3-bit IOPPM codewords for 0000_{OPPM} (000_{PCM}) represented by positive and negative voltage levels with respect to time. The positive pulse (shown in red) represents the logic one in the 100_{IOPPM+} codeword and the negative pulse (shown in blue) represents the logic one in the 001_{IOPPM-} codeword.

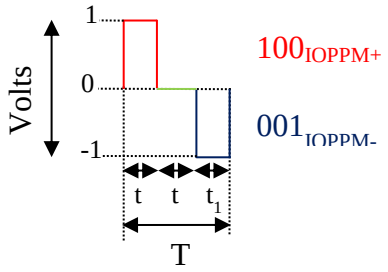


Figure 3-2 IOPPM composite signal (author generated image)

The signal is comprised of three time slots, and the signal swings about the zero volt line (shown in green); positively for IOPPM+ codewords, and negatively for IOPPM- codewords. Given that the MPEG TS is pseudorandom, the IOPPM composite signal has a zero mean voltage, which can be used to generate a DC term at the receiver, enabling the IOPPM+ and IOPPM- pulses to be distinguished from each another.

Further inspection of Table 3-1 shows that the IOPPM codewords for 0001_{OPPM} (001_{PCM}) through 0100_{OPPM} (011_{PCM}) generate an IOPPM signal containing a single positive pulse, which occurs in the same time slot as the 3-bit OPPM codeword. This pattern is repeated for the IOPPM codewords for 1001_{OPPM} (101_{PCM}) through 1100_{OPPM} (111_{PCM}), but with a single negative pulse in each IOPPM frame. This switching between positive and negative codewords enables the sign bit to be conveyed without an additional time-slot, and therefore reduces bandwidth, albeit at the cost of 3 dB in sensitivity at the receiver.

Original PCM word	**OPPM codeword**	**IOPPM codewords** $\frac{IOPPM^{+}}{IOPPM^{-}}$
000	***0***000	**100**
		001
001	***0***001	**001**
		000
010	***0***010	**010**
		000
011	***0***100	**100**
		000
100	***1***000	**001**
		100
101	***1***001	**000**
		001
110	***1***010	**000**
		010
111	***1***100	**000**
		100

Table 3-1 Coding table for OPPM versus IOPPM (3-bit coding)

As discussed in Chapter 2, section 2.7.1, since only one pulse occurs in each frame, a low mark-to-space ratio is achieved, which improves sensitivity at the receiver as stated by Sibley (M.J.N. Sibley, 2010). The transmission of a single pulse in each frame also means that the 3rd order Butterworth pre-detection filter described in section 2.6.7 can be used, which further increases sensitivity, again as stated by Sibley (M.J.N. Sibley, 2010).

The modified coding scheme has been named by the author as 'inversion OPPM' (IOPPM), since the sign bit is conveyed using binary signal polarity inversion. This approach is new and enables the IOPPM encoder to generate an equal number of output bits to input bits i.e. a 3-bit encoder generates 3-bits at the output, as defined by Equation 3-1.

$$N = 2^{M-1} - 1 \qquad \text{Equation 3-1}$$

The elimination of the sign bits from each encoder block, results in the number of bits in the encoded serial MPEG TS being reduced from 13-bits to 10-bits. This makes IOPPM desirable in the VLC system, due to its bandwidth reduction; note the bandwidth of IOPPM is still calculated using Equation 2-58, described in Chapter 2. The 3 dB reduction in sensitivity is considered acceptable for a short-range link, which only has a range in the order of a few metres, and only occurs when the composite signal approach is adopted. It is possible, however, to recover the 3 dB in sensitivity, if the two IOPPM streams are transmitted using separate LEDs. The disadvantage of this approach, however, is an increases system cost and complexity.

3.1.2 IOPPM Encoder and Decoder Logic

As with the OPPM encoder, the IOPPM encoder can also be implemented using combinational logic circuits. Table 3-2 shows the input and outputs for a 3-bit IOPPM encoder; IOPPM+ output terms are shown in red and IOPPM- output terms are shown in blue. Effectively, the 3-bit IOPPM encoder generates two 3-bit codewords, one for IOPPM+ and one for IOPPM-. This results in a total of 6-bits being generated at the output of the encoders, but since the two codewords coexist in the same timeframe, only 3-bits and hence three bit periods are used to represent both codewords, and the sign of the codewords is conveyed using positive polarity for IOPPM+ and negative polarity for IOPPM-. The derived Boolean expressions for each of the encoder outputs are presented in sum of products form, and are implementable using only AND, OR and NOT gates.

	Input Data			**Output IOPPM+**			**Output IOPPM-**		
Min Term	D_2	D_1	D_0	Y_2	Y_1	Y_0	Z_2	Z_1	Z_0
0	0	0	0	1	0	0	0	0	1
1	0	0	1	0	0	1	0	0	0
2	0	1	0	0	1	0	0	0	0
3	0	1	1	1	0	0	0	0	0
4	1	0	0	0	0	1	1	0	0
5	1	0	1	0	0	0	0	0	1
6	1	1	0	0	0	0	0	1	0
7	1	1	1	0	0	0	1	0	0

Table 3-2 IOPPM encoder (3-bit coding)

The IOPPM+ outputs are defined by Equation B.1-1, Equation B.1-2 and Equation B.1-3.

$$Y_0(D_2, D_1, D_0) = \sum (\overline{D_2}.\overline{D_1}.D_0 + D_2.\overline{D_1}.\overline{D_0}) \qquad \text{Equation B.1-1}$$

$$Y_1(D_2, D_1, D_0) = \sum (\overline{D_2}.D_1.\overline{D_0}) \qquad \text{Equation B.1-2}$$

$$Y_2(D_2, D_1, D_0) = \sum(\overline{D_2}.\overline{D_1}.\overline{D_0} + \overline{D_2}.D_1.D_0) \quad \text{Equation B.1-3}$$

The IOPPM- outputs are defined by Equation B.1-4, Equation B.1-5 and Equation B.1-6.

$$Z_0(D_2, D_1, D_0) = \sum(\overline{D_2}.\overline{D_1}.\overline{D_0} + D_2.\overline{D_1}.D_0) \quad \text{Equation B.1-4}$$

$$Z_1(D_2, D_1, D_0) = \sum(D_2.D_1.\overline{D_0}) \quad \text{Equation B.1-5}$$

$$Z_2(D_2, D_1, D_0) = \sum(D_2.\overline{D_1}.\overline{D_0} + D_2.D_1.D_0) \quad \text{Equation B.1-6}$$

The complete derivation and testing of the encoder expressions is presented in Appendix B.

The IOPPM decoder can also be implemented using combinational logic circuits. Table 3-3 shows the valid input codewords and outputs for a 6-bit IOPPM decoder. IOPPM+ input terms are shown in red and input IOPPM- terms are shown in blue. The derived Boolean expressions for each of the decoder outputs are presented in the sum of products form, and are implementable using only AND, OR and NOT gates. Note that the input of invalid codewords results in the decoder outputting all zeroes.

	Input IOPPM+			**Input IOPPM-**			**Output Data**		
Min Term	Y_2	Y_1	Y_0	Z_2	Z_1	Z_0	D_2	D_1	D_0
33	1	0	0	0	0	1	0	0	0
8	0	0	1	0	0	0	0	0	1
16	0	1	0	0	0	0	0	1	0
32	1	0	0	0	0	0	0	1	1
12	0	0	1	1	0	0	1	0	0
1	0	0	0	0	0	1	1	0	1
2	0	0	0	0	1	0	1	1	0
4	0	0	0	1	0	0	1	1	1

Table 3-3 IOPPM decoder valid codewords (6-bit decoding)

The IOPPM decoder outputs are defined by Equation B.5-7, Equation B.5-8 and Equation B.5-10.

$$D_0(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.Z_0 + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.Z_2.\overline{Z_1}.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.Y_0.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} + \\ Y_2.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} \end{pmatrix} \qquad \text{Equation B.5-7}$$

$$D_1(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.Z_1.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.Z_2.\overline{Z_1}.\overline{Z_0} + \\ \overline{Y_2}.Y_1.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} + \\ Y_2.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} \end{pmatrix} \qquad \text{Equation B.5-8}$$

$$D_2(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.Z_0 + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.Z_1.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.Z_2.\overline{Z_1}.\overline{Z_0} \end{pmatrix} \qquad \text{Equation B.5-10}$$

The complete derivation and testing of the decoder expressions is presented in Appendix B. Note that Equation B.5-10 is not incorrectly numbered in this section, but is incremented in the appendix due to a simplification to the originally derived Equation B.5-9.

3.1.3 IOPPM Encoder/Transmitter (Single LED)

As described by the Boolean expressions, the IOPPM encoder produces two output paths, IOPPM+ and IOPPM-, therefore modification to the OPPM encoder/transmitter, presented in Chapter 2, section 2.7.3, is necessary to accommodate both paths. Two architectural approaches can be used to accommodate the IOPPM paths. The first approach uses a single LED, and a TCA driver which is capable of converting the two IOPPM streams into the single composite signal that is used to intensity modulate the LED. Figure 3-3 illustrates the system architecture required to support this approach,

and consists of two MPEG TS encoder/PISO blocks; the IOPPM+ encoder/PISO block (highlight in pink) and the IOPPM- encoder/PISO blocks (highlighted in grey). The 3-bit IOPPM encoder blocks are implemented using combinational logic circuits based on the Boolean expression presented in section 3.1.2. The system operates by taking 10-bits of the parallel MPEG TS bus and presenting them to the IOPPM encoders, which occurs following a clock cycle of the parallel MPEG TS clock. 9-bits of the bus are encoded simultaneously by the IOPPM+ and IOPPM- encoders which produce a total of 18-bits at the output. However, the time slots for both the IOPPM+ and IOPPM- encoder outputs occupy the same time periods, therefore only nine time slots are actually used for transmission. The tenth bit of the system is the valid bit, which is again un-coded, and is presented only to the IOPPM+ PISO, whilst its equivalent IOPPM- time slot is set at a constant logic zero in order to keep the IOPPM+ and IOPPM- bits symmetrical. The loading and shifting of both PISOs occurs in unison and is handled using the same PLL and control logic blocks used in the OPPM architecture. Timing and synchronisation of both paths is critical to ensure that pulses in the positive and negative codewords do not interfere with adjacent time slots and corrupt the composite signal.

The IOPPM PLL differs from the OPPM PPL in that it generates a serial clock frequency which operates at eleven times the parallel MPEG TS clock frequency; one serial clock cycle is needed to load both PISOs and ten clock cycles are needed to clock-out the 10-bits from both PISO. The serialised IOPPM+ and IOPPM- bits generated by the PISOs are fed to the TCA, which provides the drive current needed to intensity modulate the LED. The IOPPM+ path is used to increase the radiant intensity of the LED, and the IOPPM- path is used to reduce the radiant intensity of the LED, thereby enabling the binary levels to be optically conveyed to the receiver. The pseudorandom

characteristic of the MPEG TS generates a zero mean for the composite IOPPM signal, therefore this creates a mean radiant intensity at the receiver, which results in a DC term that can be used to differentiate between the IOPPM+ and IOPPM- levels.

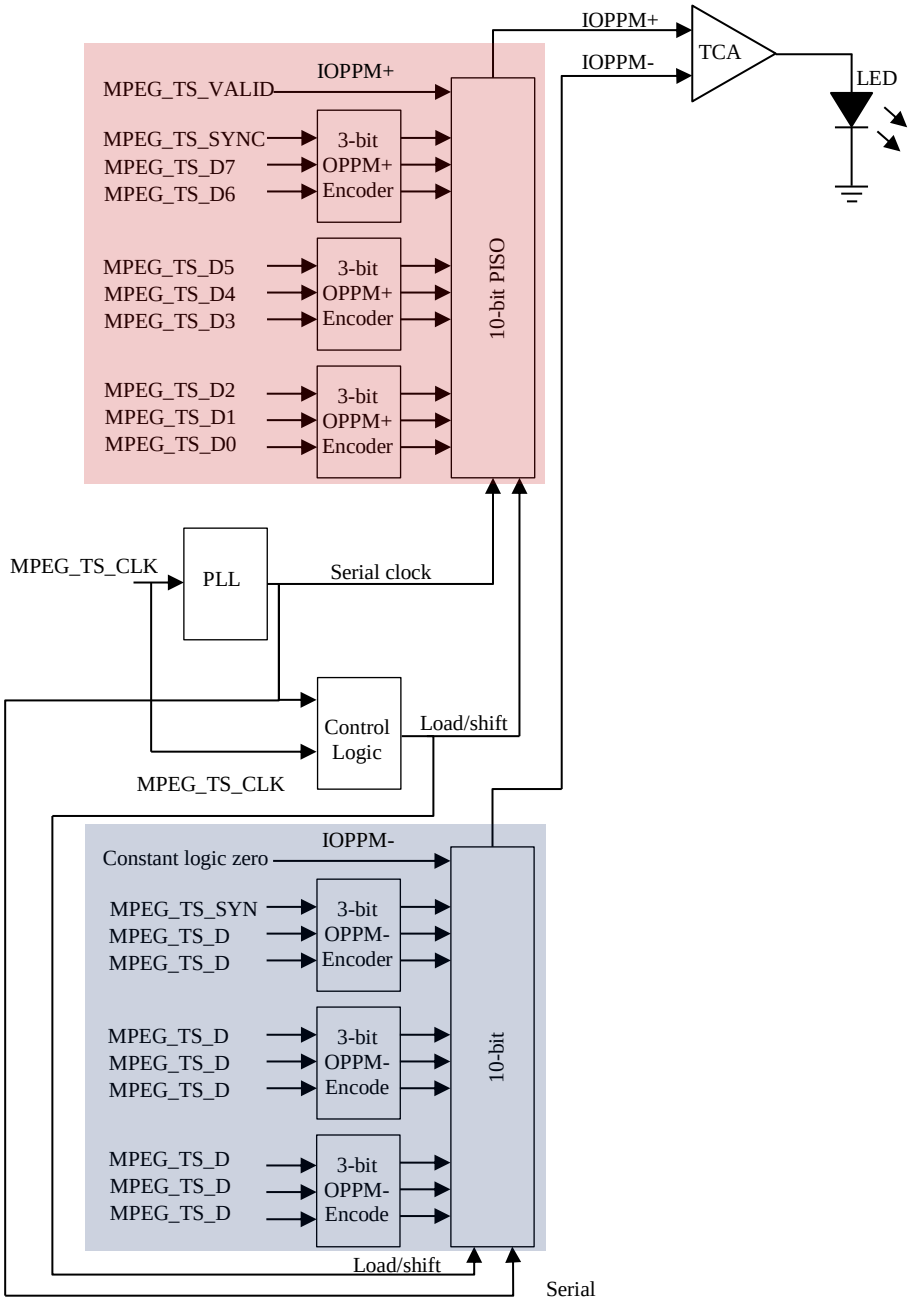


Figure 3-3 IOPPM MPEG TS encoder/transmitter

3.1.4 IOPPM On/Off Driver (Single LED)

The LED driver required by the single LED IOPPM architecture is more complicated than the topologies presented in Chapter 2, section 2.6.1; therefore a new driver topology is needed. It was mentioned in the previous section, that the pseudorandom characteristic of the MPEG TS generates a zero mean for the composite IOPPM signal, which translates into a zero mean radiant intensity of the LED light emission. This concept is realised using the circuit topology shown in Figure 3-4, where two FETs are used to drive the LED. In this topology, the LED has a quiescent bias current that is set by the resistor R3, and which also sets the LED at a mid-point radiant intensity. Referring to Figure 3-4, the intensity of the LED is varied about this mid-point thus: with Q2 turned off (Q2 gate at zero volts/logic zero) and no current flowing through R2, the intensity of the LED is increased above the mid-point by applying a bias voltage (logic one) at the gate of Q1, which causes Q1 to turn on and allow current to flow through R1 to ground via the LED. The sum of the current flowing through R1 and R3, results in an increase in the radiant intensity of the LED. Now, with reference to Figure 3-5, with Q1 turned off (Q1 gate at zero volts/logic zero) and no current flowing through R1, the intensity of the LED is decreased below the mid-point by applying a bias voltage (logic one) at the gate of Q2, which causes Q2 to turn on and allows all, or a partial amount, of the quiescent current set by R3 to flow to ground via R2, thereby reducing the radiant intensity of LED. The optimal bias currents can be established in the composite driver circuit by adjusting the values of the variable resistors.

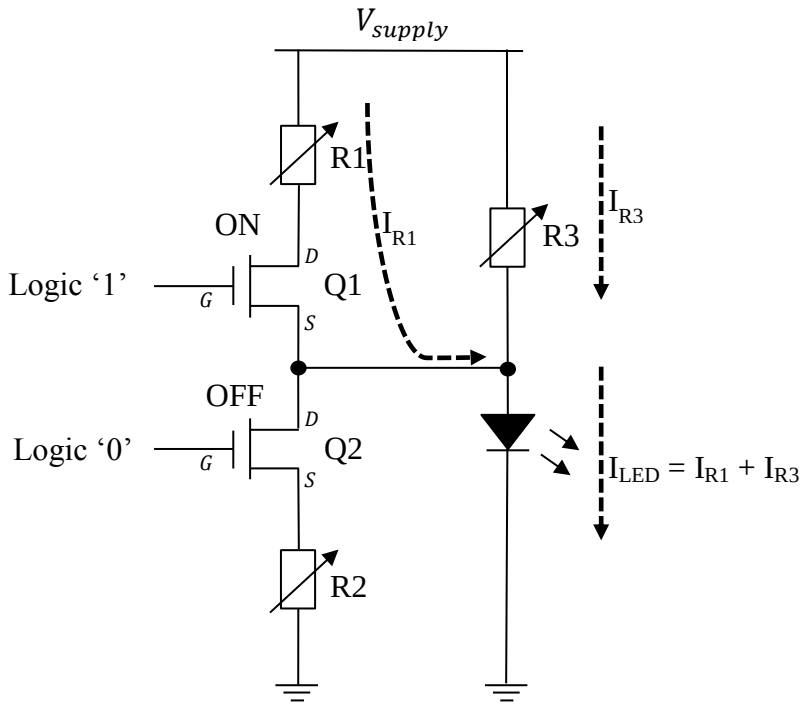


Figure 3-4 IOPPM LED composite driver (increasing intensity)

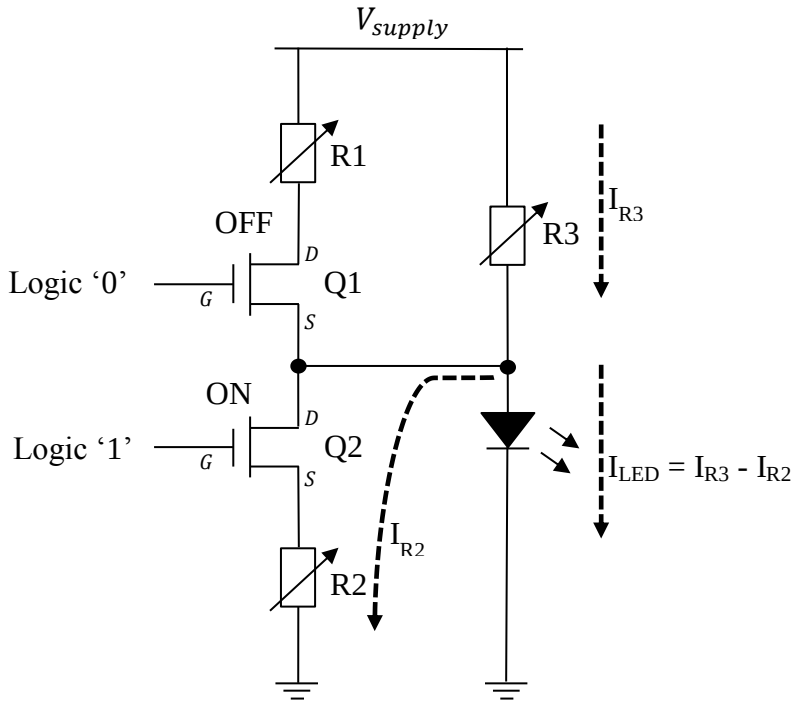


Figure 3-5 IOPPM LED composite driver (decreasing intensity)

The dual FET LED driver topology enables the IOPPM+ and IOPPM- codewords to be directly applied to the gates of the FETs in order to generate the composite drive current through the LED, and thereby vary the LEDs radiant intensity about the mid-point set by R3. Figure 3-6 illustrates the application of IOPPM+ and IOPPM- codewords to the composite driver. In this case, 000_{PCM} is IOPPM encoded and the resultant 100_{IOPPM+} and 001_{IOPPM-} codewords are applied to the gates of Q1 and Q2, respectively. At time, t_1, Q1 is turned off and Q2 is turned on, and the intensity of the LED is increased above the mid-point bias setting, as illustrated in the radiant intensity diagram to the right of the LED, where the increased intensity is indicated by the red pulse.

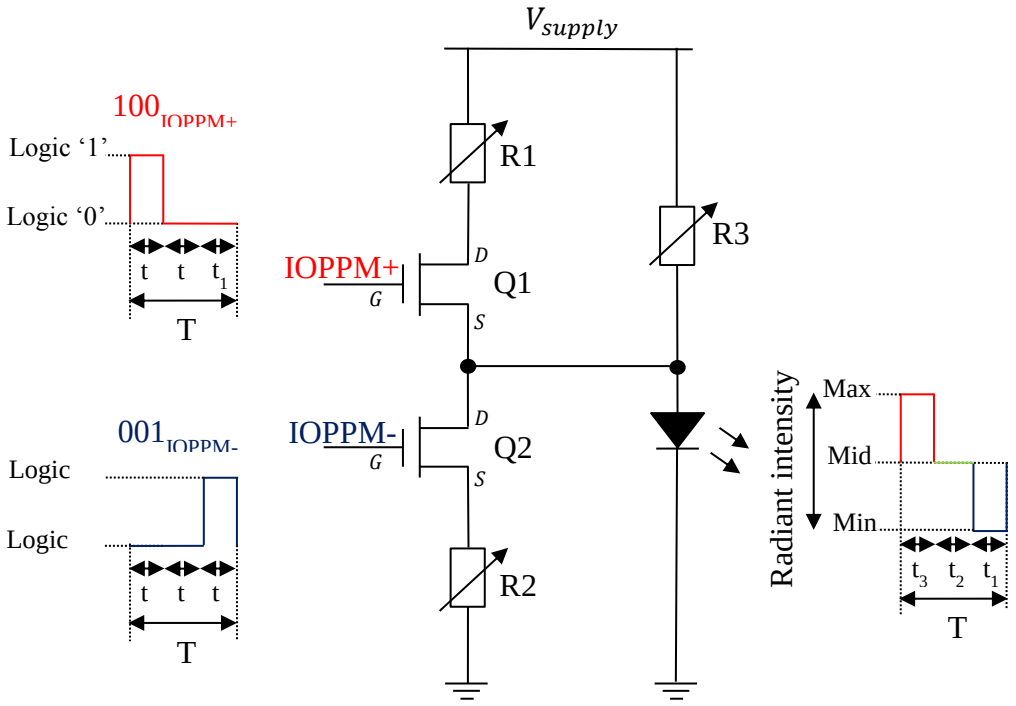


Figure 3-6 IOPPM LED composite driver

At time, t_2, both Q1 and Q2 are turned off, and the LED is set to its quiescent mid-point radiant intensity; as illustrated in the intensity diagram by the green line. At time, t_3, Q2 is turned off and Q1 is turned on, and the intensity of the LED is decreased below the

mid-point bias setting, as illustrated in the radiant intensity diagram, where the decreased intensity is indicated by the blue pulse.

In effect, the IOPPM+ and IOPPM- streams propagate over the FSO channel, with variation about a mean level in radiant intensity, which appears at the receiver as a DC term. This is used to differentiate between the IOPPM+ and IOPPM- levels, enabling detection and decoding. The complete set of 3-bit radiant intensity waveforms generated by the composite driver is shown in the right-hand-side column of Table 3-4.

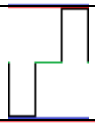
PCM 3-bit MPEG TS	**OPPM codeword**	**IOPPM codewords** $\frac{\text{IOPPM}^{+}}{\text{IOPPM}^{-}}$	**IOPPM 3-bit Radiant Intensity Waveforms**
000	**0**000	**100** **001**	
001	**0**001	**001** **000**	
010	**0**010	**010** **000**	
011	**0**100	**100** **000**	
100	**1**000	**001** **100**	
101	**1**001	**000** **001**	
110	**1**010	**000** **010**	
111	**1**100	**000** **100**	

Table 3-4 MPEG TS to IOPPM coding and LED radiant intensity waveforms

3.1.5 IOPPM Receiver/Decoder (Single LED)

The IOPPM receiver/decoder architecture required to process the composite IOPPM transmission is shown in Figure 3-7.

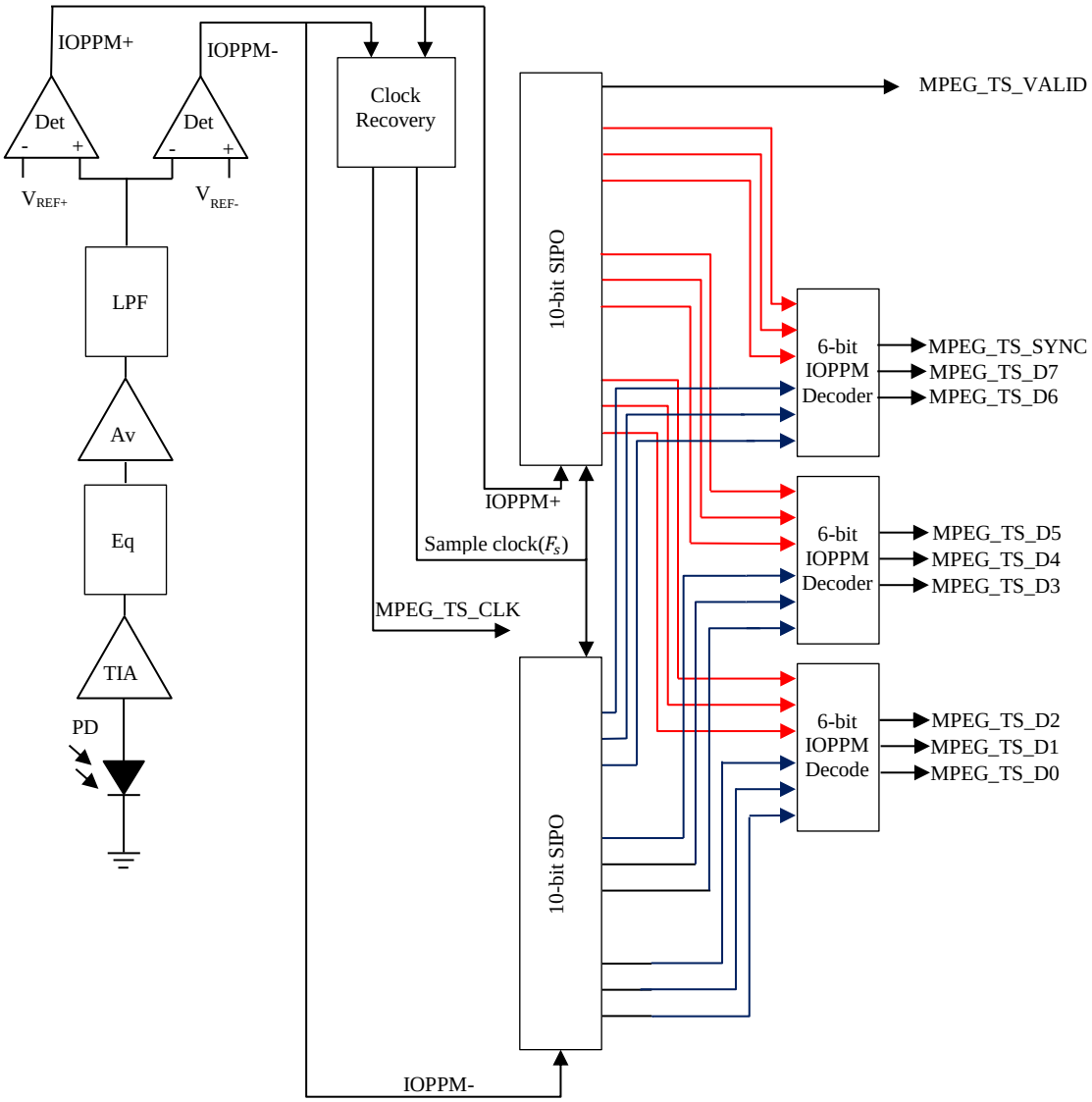


Figure 3-7 IOPPM MPEG TS receiver and decoder (single LED)

In this architecture, the analogue front-end is identical to the OPPM receiver/decoder, except for the voltage comparator topology. The composite IOPPM signal input to the comparator is split into the two component paths of IOPPM+ and IOPPM-. This is achieved by AC coupling the composite signal into the split junction using a capacitor

which removes the DC term set by the IOPPM composite LED drivers quiescent bias point. This results in the IOPPM+ pulses being represented by a positive voltage and IOPPM- pulses represented by a negative voltage, as illustrated in Figure 3-2. The detection of the positive and negative pulses is performed by a window voltage comparator (Pallás-Areny & Webster, 1999), which is constructed from two comparators. One of the comparators is configured as a non-inverting comparator with a positive reference voltage (V_{REF+}), and is used to detect the IOPPM+ pulses The second comparator, which is configured as an inverting comparator with a negative reference voltage (V_{REF-}), is used to detect the IOPPM- pulses. The digital outputs of the comparators are defined by Equation 3-2 and Equation 3-3.

$$V_{D\,IOPPM+} = \begin{cases} 1, & if\ V_{A\,IOPPM+} \geq V_{REF+} \\ 0, & if\ V_{A\,IOPPM+} < V_{REF+} \end{cases} \qquad \text{Equation 3-2}$$

$$V_{D\,IOPPM-} = \begin{cases} 1, & if\ V_{A\,IOPPM-} \leq V_{REF-} \\ 0, & if\ V_{A\,IOPPM-} > V_{REF-} \end{cases} \qquad \text{Equation 3-3}$$

Where $V_{A\,IOPPM+}$ and $V_{A\,IOPPM-}$ are the positive and negative analogue pulses within the composite signal, and V_{REF+} and V_{REF-} are the threshold references.

The circuit topology of the window voltage comparator is shown in Figure 3-8. The capacitor, which is used to remove the DC term from the composite signal, is represented by C_1. Following the capacitor is a potential divider, formed by R_1 and R_2, and which is used to apply a DC offset to the IOPPM composite signal in order to remove the negative excursion from the IOPPM- path; this offset is necessary if the comparators used in the hardware implementation are only able to handle positive voltages. Following the potential divider, the composite signal is split and fed to the two

comparators. IOPPM+ pulses are detected by the non-inverting comparator using the threshold set by $V_{REF}+$, and the IOPPM- pulses are detected by the inverting comparator using the threshold set by $V_{REF}-$. Potential dividers are used to set the threshold voltages: $V_{REF}+$ is set by R_3 and R_4; and $V_{REF}-$ is set by R_5 and R_6.

Note: the polarity of the IOPPM composite signal must be considered when designing the pre- and post-amplifier stages, and the overall cascade of the front-end to ensure that IOPPM+ pulse are positive and the IOPPM- pulses are negative upon arrival at the window comparator. Failure to input the correct polarity, set by the transmitter, results in incorrect path decoding at the receiver.

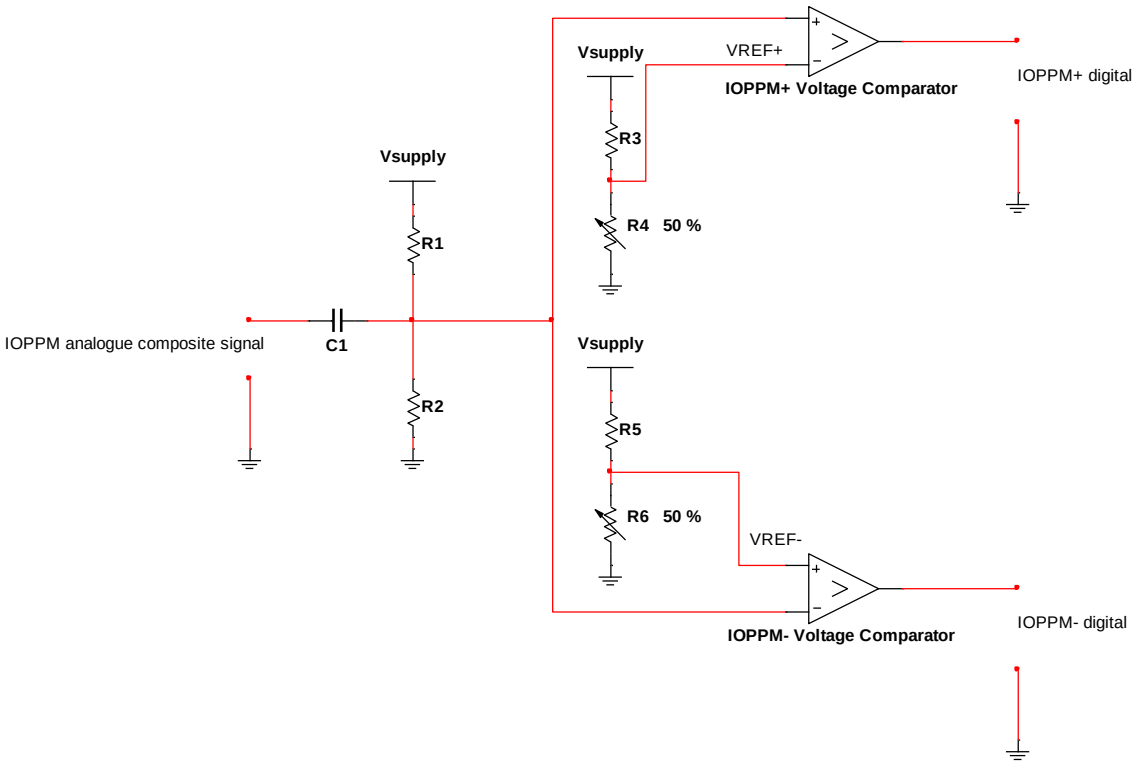


Figure 3-8 Window voltage comparator

The operation of the window comparator is demonstrated using IOPPM codewords $100_{\text{IOPPM+}}$ and $001_{\text{IOPPM-}}$, which represent the transmission of a 000_{PCM} word, as

described in Table 3-1. Figure 3-9 illustrates the composite waveform for the 3-bit codewords, which are presented at the input of the window comparator of Figure 3-8. In this case, it is assumed that the inverting comparator can deal with negative voltages, therefore no DC offset is applied by the potential divider formed by R_1 and R_2, so IOPPM+ are positive and IOPPM- pulses negative about the zero line. The pulses are shown with Gaussian shapes, as expected following transmission over the FSO channel. The positive pulse has a peak voltage of +1 V and represents the IOPPM+ codeword, and the negative pulse has a peak voltage of -1 V and represents the IOPPM- codeword. The bit period (τ) of the waveform is 10 ns and the individual bit periods are represented by t_1, t_2 and t_3. The total period of waveform is 30 ns.

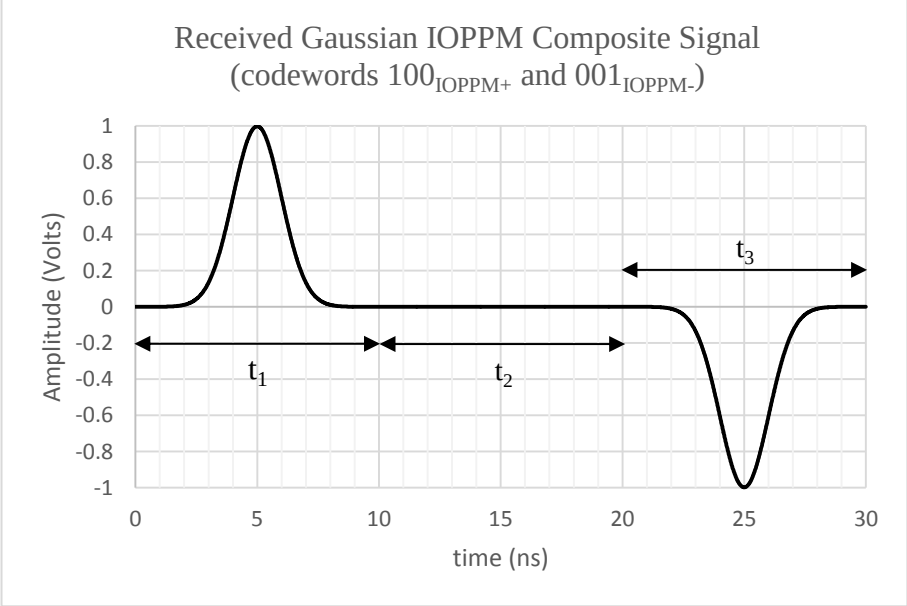


Figure 3-9 IOPPM composite signal for codewords 100_{IOPPM+} and 001_{IOPPM-}

The positive IOPPM+ pulse is detected by the non-inverting comparator, whose threshold ($V_{REF}+$) is set to 50% of the positive pulse peak voltage, and is set at +0.5 V. The negative IOPPM- pulse is detected by the inverting comparator, whose threshold ($V_{REF}-$) is set to 50% of the negative pulse peak voltage, and is set at -0.5 V. Figure

3-10 shows the comparator thresholds for the IOPPM+ and IOPPM- comparators overlaid over the composite signal. In the case of IOPPM+ detection, when the composite signal is below $V_{REF}+$ (highlighted in red), the non-inverting comparator outputs a logic zero, and when it is above $V_{REF}+$, the comparator outputs a logic one. In the case of the IOPPM- detection, when the composite signal is above $V_{REF}-$ (shown in blue), the inverting comparator outputs a logic zero, and when it is below $V_{REF}-$, the comparator outputs a logic one.

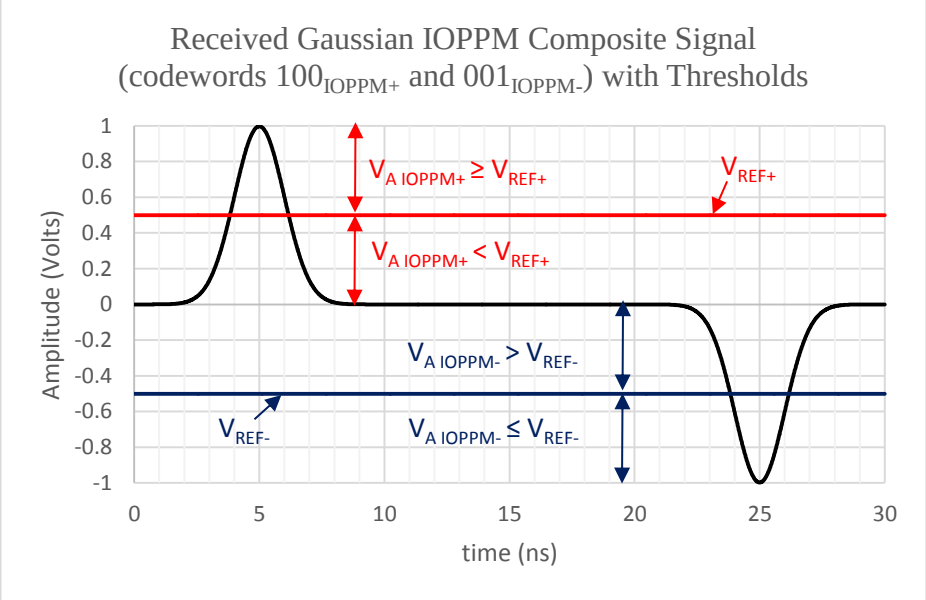


Figure 3-10 IOPPM composite signal detection thresholds

Figure 3-11 shows the threshold crossings for the IOPPM+ and IOPPM- pulses (highlighted in brown), which translate into the digital outputs of the IOPPM+ and IOPPM- comparators, which are shown, respectively, in Figure 3-12 and Figure 3-13. The two digital outputs show the logic levels for the detected codewords:100_{IOPPM+} and 001_{IOPPM-}.

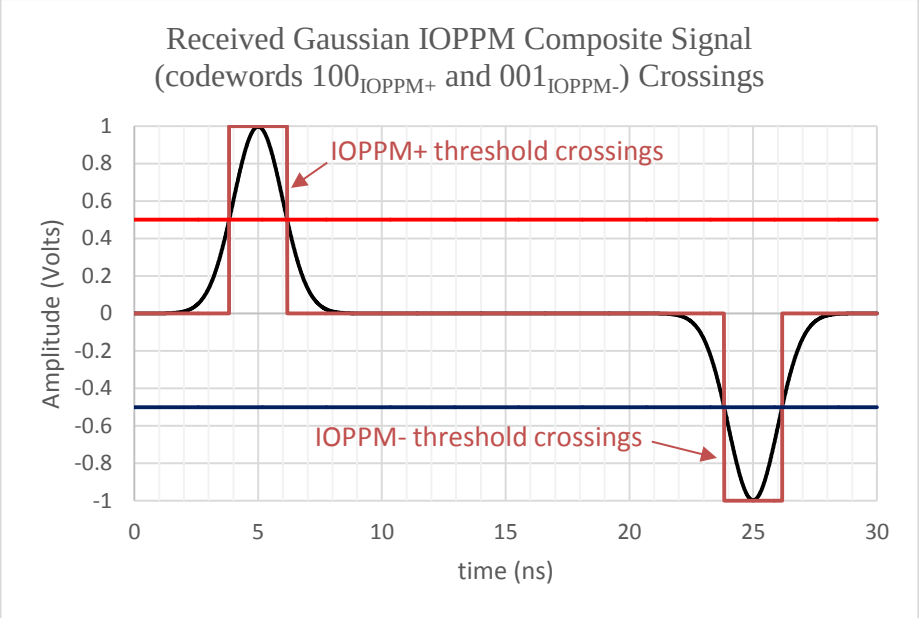


Figure 3-11 IOPPM composite signal threshold crossings

Figure 3-12 shows the detected pulses of the received IOPPM+ codeword and these correspond directly to the transmitted bits for 100_{IOPPM+}. Similarly, Figure 3-13 shows the detected pulses of the received IOPPM- codeword and these correspond directly to the transmitted bits for 001_{IOPPM-}. Both received codewords occupy the same time period, meaning that t_1, t_2, and t_3 time slots for the IOPPM+ codeword, correspond to the same time slots for the IOPPM- codeword, therefore both codewords must be decoded at the same time to generate the 000_{PCM} word encoded at the transmitter. Prior to decoding, central decision detection must be applied to the output of the window comparators, and the decision times for the IOPPM+ codewords, must occur at the same time as the IOPPM- codewords. The decision time is illustrated in Figure 3-12 and Figure 3-13 by the vertical dotted lines which are shown at 5 ns, 15 ns and 25 ns. The decision times are generated by the serial clock ($\frac{1}{\tau}$) of the VLC system, which is shifted by half a time slot period ($\frac{\tau}{2}$), in this case is 5 ns. This generates the sample clock ($F_s = \frac{1}{\tau}$) which

effectively clocks the received bits into the dual SIPOs (Figure 3-7) at the decision times.

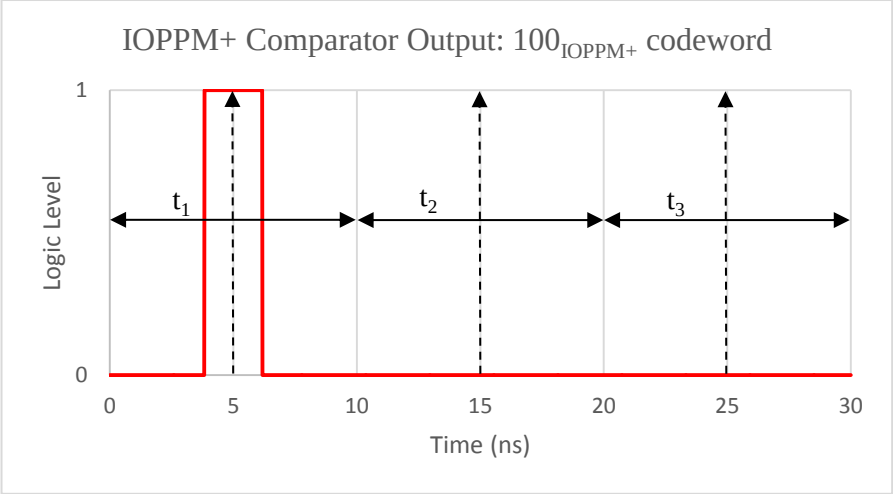


Figure 3-12 IOPPM+ comparator digital output

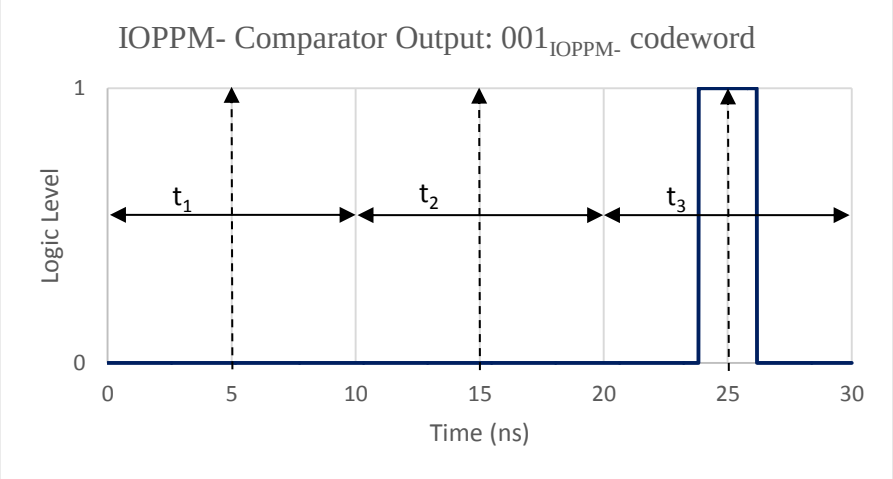


Figure 3-13 IOPPM- comparator digital output

In order to clock the SIPOs, a clock recovery block (Figure 3-7) is required to synchronise the receivers serial and parallel MPEG TS PPL generated clocks. The clock recovery block also applies half time slot shift to the serial clock to generate the sample clock which enables central decision detection. In addition, an IOPPM frame synchronisation logic block (not shown in Figure 3-7 for clarity) is needed to locate the

start of each IOPPM frame to enable correct decoding. The clock recovery and frame synchronisation sub-systems are complicated sub-systems, and beyond the scope of this work, so instead of generating these sub-systems, the transmitters serial and parallel MPEG TS clocks will be hardwired to the receiver to enable IOPPM frame synchronisation and serial and parallel clocking identical to the transmitter.

The operation of the IOPPM SIPOs and decoders, assuming correct serial and parallel clocking and frame synchronisation, is performed when both IOPPM+ and IOPPM- SIPOs are clocked with a 10-bit IOPPM frame from the window comparator. Figure 3-7 shows 9-bits of the SIPO are fed to three, 6-bit IOPPM decoders; the IOPPM+ paths to decoder are highlighted in red, and the IOPPM- paths are highlighted in blue. The 6-bit IOPPM decoder blocks, implemented using combinational logic circuits based on the Boolean expressions presented in section 3.1.2, decode the IOPPM+ and IOPPM- paths simultaneously and output the MPEG TS bits for D0 through D7, and the synchronisation bit. The tenth bit output by the IOPPM+ SIPO is the un-encoded valid bit which is ready for immediate processing in the STB processor. However, the tenth bit of the IOPPM- SIPO, is left unused, as its only purpose is to maintain bit symmetry between the paths. Following decoding, the MPEG TS are available for parallel clocking into the STB processor, where MPEG decoding is performed.

3.1.6 IOPPM Encoder/Transmitter (Dual LEDs)

The second approach to realising the IOPPM scheme uses dual LEDs, each of which is driven by one of the independent IOPPM paths as illustrated in Figure 3-14. This approach increases the system cost, since the transmitter requires two pairs of TCA drivers and LEDs, and the receiver requires two pairs of PDs and independent analogue

signal processing paths. Other than the duplication of the front-end paths, the operation of this architecture is identical to the single LED IOPPM architecture.

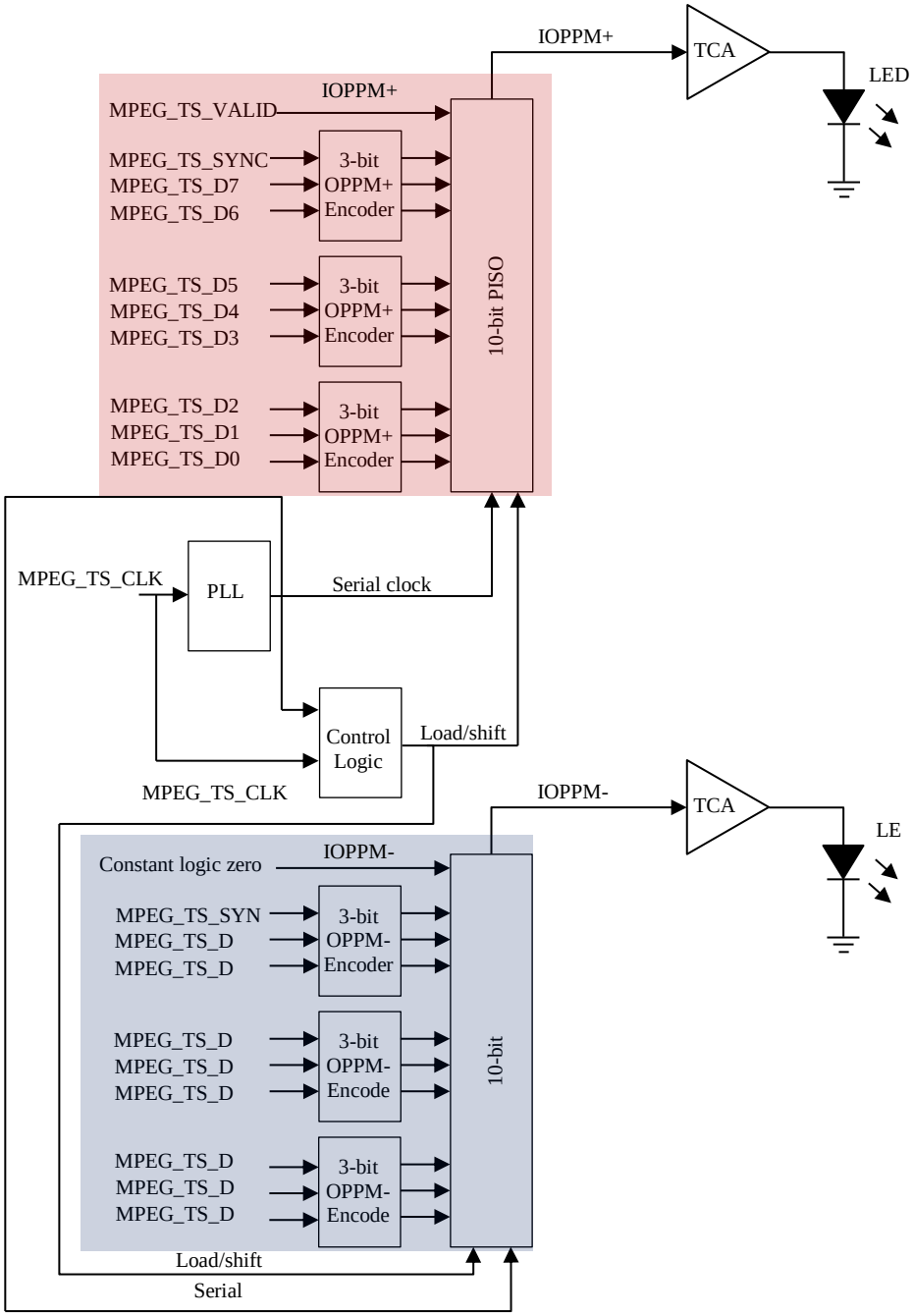


Figure 3-14 IOPPM MPEG TS encoder/transmitter (dual LEDs)

3.1.7 IOPPM On/LED Drive (Dual LEDs)

The TCA driver used in both IOPPM paths in the architecture shown in Figure 3-14 is identical in topology and operation to that used in the OPPM encoder/transmitter introduced in Chapter 2, section 2.7.4. In this case, the IOPPM+ and IOPPM- codewords are used to drive separate TCA and LED stages as illustrated in Figure 3-15a and Figure 3-15b. In Figure 3-15a, the IOPPM+ codeword 100_{IOPPM+} is applied to the gate of the FET, at t_1, a logic zero applied to the gate, switches the FET off. In this condition, there is no current flowing through R or the LED; the LED is switched off. This condition is repeated at t_2 when another logic zero is applied to the gate. However, at t_3, a logic one is applied to the gate, thus switching it on and allowing current to flow through R and the LED to ground via the drain-source junction of the FET. In this condition, the LED is switched on and the logic one is transmitted over the FSO channel. Figure 3-15b shows the corresponding IOPPM- codeword 001_{IOPPM-} being applied at the gate of the second TCA and LED pair. The operation is identical to the IOPPM+ path. Both figures illustrate the radiant intensity by the LEDs.

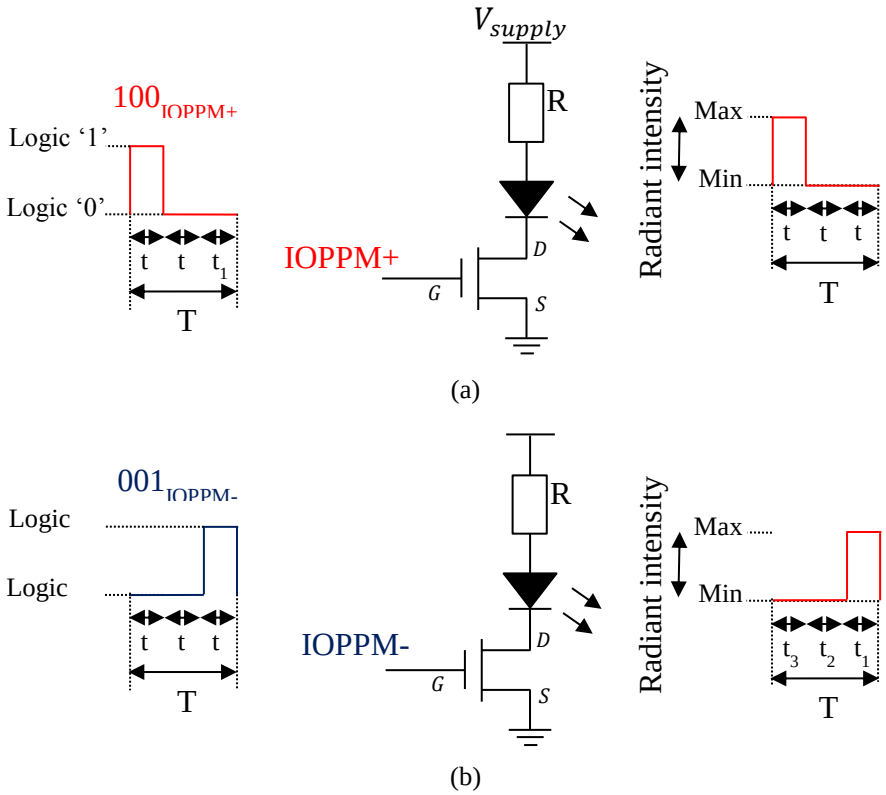


Figure 3-15 IOPPM LED driver (dual LED)

Since this architecture uses identical LEDs and PDs, spatial separation of the optical channels is necessary to eliminate crosstalk between the optical channels, and this is achieved using cowlings over the LEDs and PDs, and increasing the physical separation between the LEDs at the transmitter, and the PDs at the receiver.

3.1.8 IOPPM Receiver/Decoder (Dual LEDs)

The dual LED receiver/decoder architecture is shown in Figure 3-16.

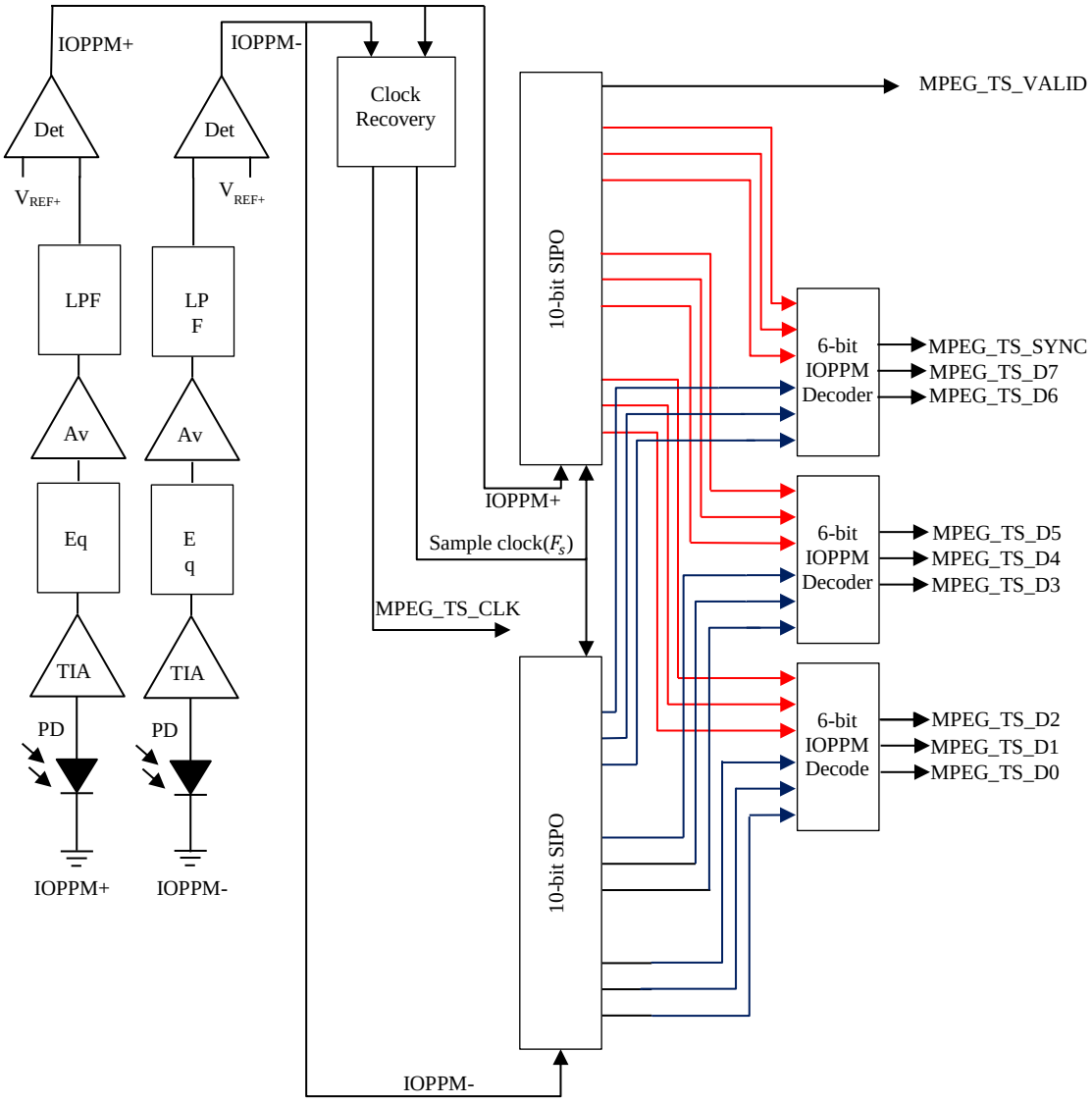


Figure 3-16 IOPPM MPEG TS receiver and decoder (dual LED)

The architecture uses dual PDs and two independent analogue signal processing paths to detect the independent IOPPM+ and IOPPM- transmissions. The comparators used are identical to those used in the OPPM receiver/decoder, introduced in Chapter 2, section 2.7.4. Since the IOPPM paths use identical processing, ideally, the threshold voltages ($V_{REF}+$) used for both comparator should be identical, however, there will be variation in the voltages due to differences in LED bias, and gain and loss levels in the analogue processing stages.

Other than the duplication of the front-end paths, operation of this architecture is identical to the single LED architecture introduced in section 3.1.5.

3.1.9 IOPPM Path Calibration

Path calibration is necessary in both the single and dual LED IOPPM architectures, to compensate for asymmetrical time delays in each path. Propagation delays in both the analogue and digital processing circuits of the IOPPM architectures can lead to timing errors in the system which lead to non-optimal central decision detection in the receiver and, in extreme case, reduced receiver sensitivity. Incorrect timing can lead to IOPPM+ and IOPPM- frames corrupting each other resulting in either complete loss of data or increased error rate.

Calibration can be performed using the FPGA platform that the IOPPM encoder and decoder blocks are implemented upon. One simple method of calibrating the paths that will be investigated is the transmission of known bit sequences in the IOPPM+ and IOPPM- paths and measuring the timing offsets at the receiver.

3.1.10 Conclusions

In this chapter, a new modulation scheme called IOPPM, which is based on a modification to the OPPM scheme introduced in Chapter 2, was presented.

It was concluded in this chapter that:

- IOPPM reduces the encoded serialised bit stream of OPPM from 13-bits to 10-bits, through the elimination of the time slot required by OPPMs sign bit. Instead, IOPPM encodes the sign in the polarity of two codewords.

- IOPPM generates only a single pulse in each positive and negative frame and has a low mark-to-space ratio enabling the 3rd order Butterworth pre-detection filter described in Chapter 2 to be used in the receiver.
- The IOPPM schemes encoder and decoder can be implemented on an FPGA using simple combinational logic circuits which interface easily with the parallel MPEG TS sourced and sinked by a STB.
- Two IOPPM architectures were presented which can be used to realise the VLC system. The first uses a single LED which is intensity modulated by a single composite IOPPM signal that carries both positive and negative codewords. This approach reduces cost and complexity of the system, but results in a 3 dB reduction in sensitivity at the receiver due to the composite signal carrying two data streams. The second uses two LEDs, each of which is intensity modulated by one of the IOPPM streams. This approach increases the cost and complexity of the system, but recovers the 3 dB sensitivity.
- The bandwidth of the IOPPM based VLC system is determined by multiplying the parallel MPEG TS clock frequency by a factor of eleven, where eleven is derived from the serial clocking of 10-bits out of the PISO shift-register, and an additional clock cycle of the serial clock which is needed to load the PISO.
- The composite IOPPM architecture required a new FET based LED driver topology which enabled the LEDs radiant intensity to be varied about a mid-point. The IOPPM+ codewords are used to increase the radiant intensity of the LED and the IOPPM- signal to reduce it. The mid-point intensity of the LED generates a DC term which enables the IOPPM streams to be distinguished from one another at the receiver.

- A window voltage comparator can be used to detect the IOPPM+ and IOPPM- pulses.
- The clock recovery system for IOPPM scheme will not be investigated due to limited timeframe for the work, and instead hardwiring of the parallel MPEG TS clock, serial clock and load pulses for the shift-register from the transmitter to receiver to enable synchronisation and clocking of the whole system.
- Path calibration for the IOPPM+ and IOPPM- paths is necessary to eliminate asymmetrical timing delays in each path, in order to avoid decoding errors in the receiver. Calibration techniques using the transmission of known bit sequences in the IOPPM+ and IOPPM- paths and measuring the timing offsets at the receiver will be explored in Chapter 6.

Two IOPPM architectures have been presented which can be used to realise the VLC system. The single LED architecture offers lower-cost and simplicity compared to the dual LED architecture, but with the penalty of a 3 dB reduction in sensitivity at the receiver; both architectures will investigated. Before the system can be synthesised, characterisation and analyses of STB platforms is necessary to determine the logic levels used for the MPEG TS and also to determine the parallel clock frequency used, which ultimately determines the minimum serial clock and bandwidth of the VLC system. Characterisation and analyses of white and blue LEDs is also necessary to determine the device with the widest bandwidth, and the amount of post-equalisation necessary in the receiver. This works is presented in Chapter 4.

Note: Error correcting codes will not be explored in this work, due to time constraints.

4 Device Characterisation and Analysis

This chapter presents the characterisation measurements and analyses of the MPEG TS source and sink devices selected for use in the hardware implementation of the VLC system. Characterisation of the parallel MPEG TS clock frequency of the devices was necessary to determine the VLC systems serial clock frequency and bandwidth. Characterisation of the MPEG TS signals was also necessary to establish optimal settings to ensure their compatibility within the VLC system. In particular, the logic levels and clocking requirements needed to interface between the devices and the FPGA implementations of the IOPPM encoder and decoder were established.

Also presented in this chapter, is the characterisation and analyses of two LEDs used in SSL applications. This characterisation was necessary to determine the device with the widest bandwidth needed to support MPEG TS transmission over the FSO channel.

The findings of this chapter were key to determining the serial clock and bandwidth requirements of the entire system, and the type and amount of bandwidth compensation needed for the LED. The findings were used in the design and modelling of the system presented in Chapter 5.

4.1 MPEG TS Data Source and Sink Characterisation and Analysis

Set-top-box (STB) platforms were selected to act as the data source and sink devices in the VLC system. Figure 4-1 shows the source devices (highlighted in pink), which consists of tuner that is required to select an off-air DVB-T or DVB-T2 broadcast, and a digital demodulator that is required to demodulate the broadcast and produce the MPEG TS bus. Figure 4-1 also shows the sink device for the MPEG TS, which is a processor

device found in terrestrial STB receivers, and is capable of performing MPEG TS decoding and outputting video and audio content on an HDMI interface, thereby enabling reproduction on an HD monitor.

A fully software configurable Silicon Labs tuner and DVB-T/T2/C demodulator evaluation board (EVB) was selected as the data source, and a Bush DH2636 DVB-T/T2 STB, specifically its internal processor device, as the data sink; note that the DH2636 was configured by firmware at manufacture, and therefore was only configurable using the IR remote control and on-screen menus. The platforms were chosen because of the author's previous experience of working on similar platforms in industry, and also because both used a parallel MPEG TS bus. As described in Chapter 3, parallel MPEG TS was preferred for the implementation of IOPPM encoder and decoder using combinational logic circuits.

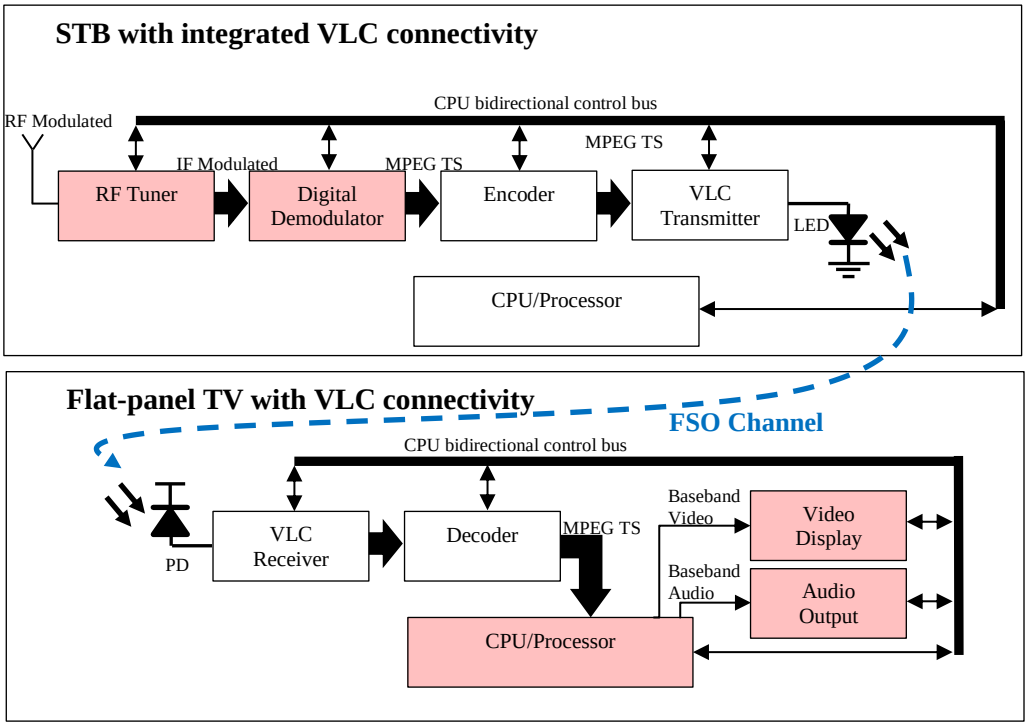


Figure 4-1 VLC MPEG TS source and sink devices (author generated image)

The following section presents the technical overview, characterisation and analyses of the EVB and STB MPEG TS. Based on the characterisation, settings are determined which enabled the two platforms to operate as data source and sink devices in the VLC system. End-to-end testing to confirm compatibility of the platforms MPEG TS is presented at the end of the chapter.

4.1.1 Silicon Labs Evaluation Board Overview

The Silicon Labs worldwide digital tuner and DVB-T/T2/C demodulator EVB is a consumer grade, industry standard evaluation board that uses leading-edge CMOS semiconductor devices for the reception and demodulation of DVB terrestrial and cable based content. The EVB is intended for TV and STB original equipment manufacturers (OEM) to perform device evaluation of the EVBs ICs. The EVB consists of a digital tuner which is capable of receiving off-air DVB-T and DVB-T2 channels via an antenna, and a demodulator capable of outputting MPEG TS. The EVB is fully programmable via a USB bus using Silicon Labs proprietary software, and an on-board microcontroller interfaces with the USB bus and translates instructions, sent by the software, into I^2C commands used to configure the tuner and demodulator.

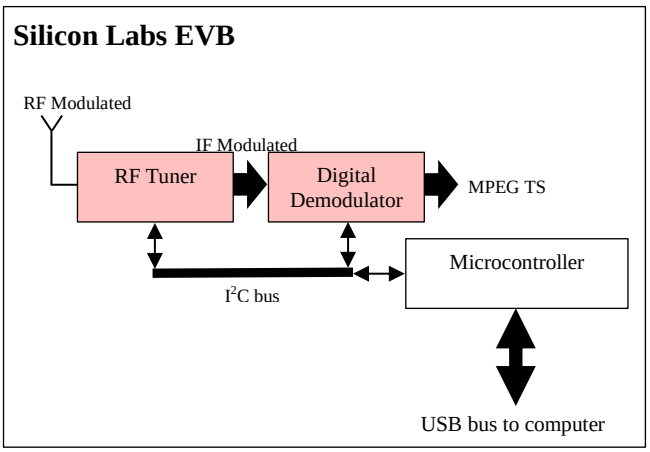


Figure 4-2 Silicon Labs EVB core devices (author generated image)

For a more detailed technical overview of the EVB, refer to Appendix D.

4.1.2 EVB MPEG TS Characterisation and Analysis

During the characterisation, the EVBs tuner was connected to a roof-top Yagi array antenna, which received an RF TV channel spectrum transmitted by Emley Moor transmitter in West Yorkshire, UK. From the received spectrum, Channel C41 was selected, because it was a DVB-T2 broadcast and contained both SDTV and HDTV multiplexed programme streams. The channel consisted of C86 More4 +1; C101 BBC One HD (England no regional news); C102 BBC Two HD (England); C103 ITV HD (ITV Granada); C104 Channel 4 HD North ads; C105 Channel 5 HD; and C204 CBBC HD (Butterworth, 2004). The channel had a centre frequency of 634 MHz and bandwidth of 8 MHz, and was modulated using COFDM and a 256 QAM constellation. The transmissions code rate was 2/3 with a guard interval of 1/128, and an FFT of 32 k.

The EVB was programmed using the Silicon Labs software. The tuner was tuned to the 634 MHz centre frequency of the channel, and the demodulator was configured for the DVB-T2 reception, and parallel MPEG TS mode using a 6 MHz, non-inverted clock. The MPEG TS was output from the demodulator on twelve output lines; eight lines for data TS_DATA [$D0_{LSB}$ to $D7_{MSB}$]; one line each for the MPEG clock (TS_CLK), valid (TS_VALID), synchronisation (TS_SYNC), and error (TS_ERR). The error line was not characterised due to its redundancy, as described in section 2.1.6, where it was described that the 1-bit transport error indicator in the TS header is set to one when errors are uncorrectable, and notifies the demultiplexer and decoding block in the processor of the TS packet error. Due to the elimination of the error line, effectively only ten lines (10-bits) of the MPEG TS bus required characterisation.

Following the configuration of the tuner and demodulator, the software was then used report receive status of channel C41. The carrier-to-noise of the received channel was approximately 31.75 dB, and the estimated bit-rate MPEG TS bit was 40.21 Mbit/s. The BER of the signal was approximately 9.9×10^{-8}; well below the QEF limit of 2.4×10^{-4}, therefore the received signal was considered error free. The forward error-rate (FER) and uncorrected TS packets of the received signal were monitored during the measurements which presented in the following sections, and no uncorrected errors were reported by the software during the measurement periods. For more detailed information relating to the EVB configuration, refer to Appendix G.1.

4.1.3 EVB MPEG TS Clock (TS_CLK)

The clock signal (Figure 4-3) was measured and found to have a frequency of 6.008 MHz, and a 50% duty cycle. A frequency error of approximately +0.13% between the software setting of 6 MHz (period 166.6 ns) and measurement of 6.008 MHz (period 166.4 ns) was observed.

The rise and fall times of the clock were measured between the 10% and 90% points. The rise- and fall time of the clock was measured at approximately 5 ns. This information is needed to ensure that the rise- and fall-times in the simulated VLC system closely correlated with measured data to ensure correct timing.

The logic levels of the clock were measured at 3.0 V (logic one) and 0V (logic zero), compensating for 0.4 V offset from the 0 V line, which was attributed to the under and overshoots of the signal. It was concluded that LVCMOS logic levels were being used. This information is necessary to configure the FPGA input interfaces during implementation of the VLC system.

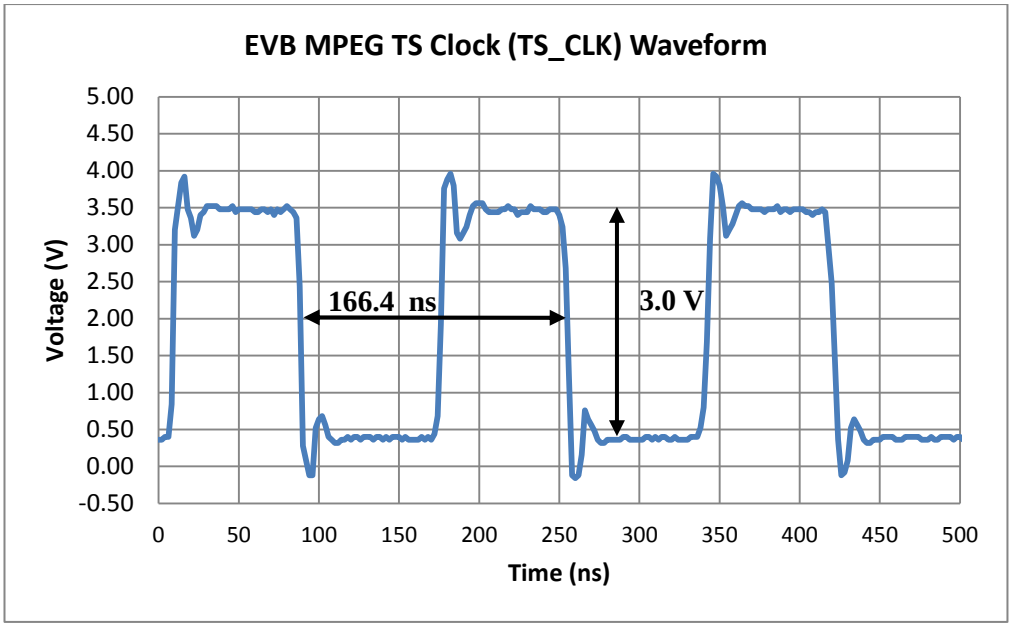


Figure 4-3 EVB MPEG TS clock (6.008 MHz, 50% duty cycle)
(author generated image)

Based on the parallel MPEG TS clock, the serial clock frequency and bandwidth required by the VLC system was calculated at 66 MHz. This was calculated by multiplying the parallel clock frequency of 6 MHz by the 10-bits of the MPEG TS, and then adding one parallel clock cycle to enable serial loading of the PISOs, as described in Chapter 3.

4.1.4 EVB MPEG TS Synchronisation (TS_SYNC)

The frequency of the synchronisation pulses (Figure 4-4) was measured at 26.74 kHz, resulting in a period of 37.4 μs.

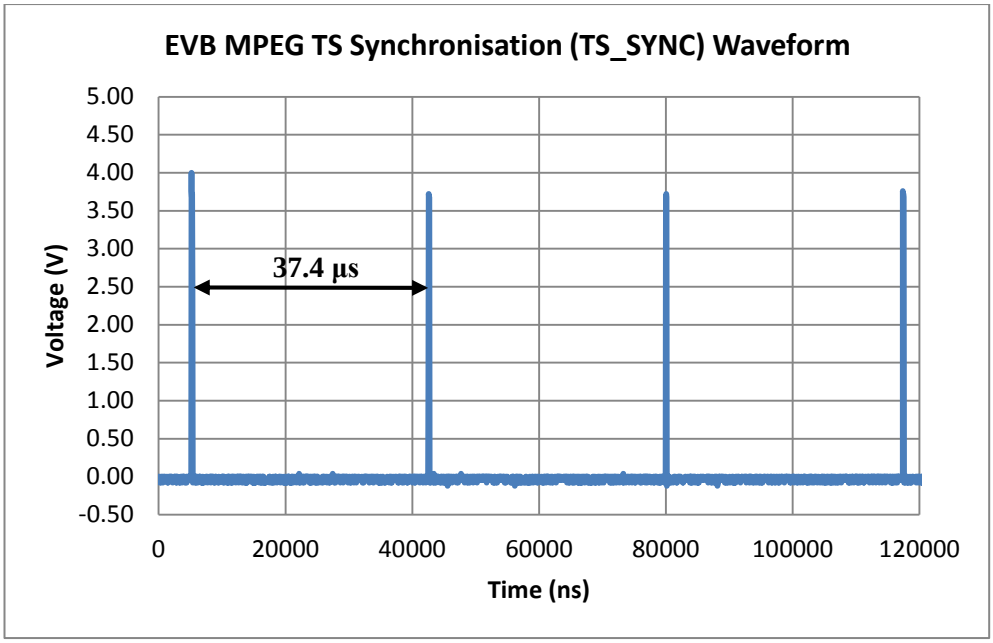


Figure 4-4 EVB MPEG TS synchronisation (author generated image)

The 37.4 µs period was at variance with Equation 2-11, stated in Chapter 2.

$$T_{TS\_SYNC} = \left(188\frac{1}{f_{TS_{CLK}}}\right) + T_{offset}\ (s) \qquad \text{Equation 2-11}$$

The expected period of the synchronisation pulses was 31.33 µs, based on a zero offset (T_{offset}) and a clock frequency of 6 MHz. The difference indicated that the MPEG TS clock of the EVB was running faster than the broadcast transmitter MPEG TS clock. The difference in clock frequency was calculated using Equation 2-13, stated in Chapter 2.

$$f'_{TS\_CLK} = 188\frac{1}{T_{TS\_SYNC}}\ (Hz) \qquad \text{Equation 2-13}$$

Applying 37.4 µs to Equation 2-13 yielded a transmitter MPEG TS clock running at approximately 5.03 MHz. This meant there was a 1 MHz difference between the transmitted clock and demodulator clock, resulting in 6.07 µs period between TS

packets where no content was output on the MPEG TS bus. This is inefficient for the VLC systems bandwidth, since empty slots need to be transmitted by the VLC system that could be used for content. However, this does mean that there is additional data capacity in the system; effectively 10 Mbits/s. If the data sink MPEG TS clock frequency were reconfigurable, it would be possible to run the MPEG TS clock on both devices at 5 MHz, providing the opportunity to run the serial clock of the VLC system at 56 MHz, instead of 66 MHz. Unfortunately the data sink STB has a fixed and non-reconfigurable MPEG TS clock frequency of 6 MHz, meaning that the minimum bandwidth of the VLC system is fixed at 66 MHz.

The duration of a single synchronisation pulse (Figure 4-5) was measured at 166.4 ns.

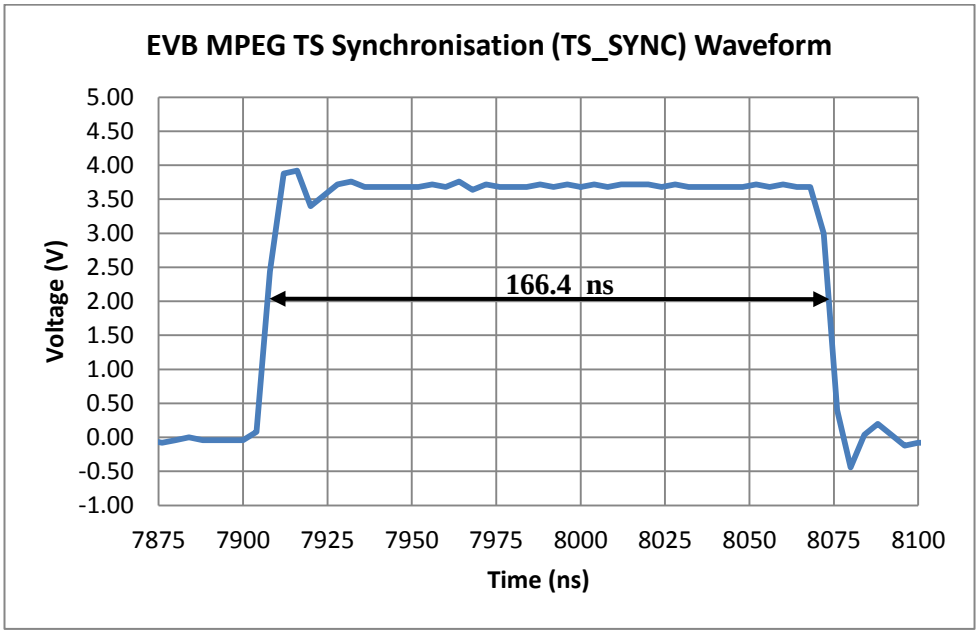


Figure 4-5 EVB MPEG TS MPEG TS synchronisation (single pulse)
(author generated image)

A synchronisation pulse duration was measured relative to the clock (Figure 4-6), and was found to have a duration equal to one cycle of the 6.008 MHz clock at 166.4 ns. Clocking of the synchronisation pulse occurred on the rising-edge of the clock (non-

inverted) as expected. However, an offset of 20 ns was also observed between the clock and the synchronisation signal which was unexpected. The offset was zeroed using the Silicon Labs software in order to ensure compatibility with the data sink device; it will be demonstrated later in this chapter, that the parallel clock used by the system needs to be inverted.

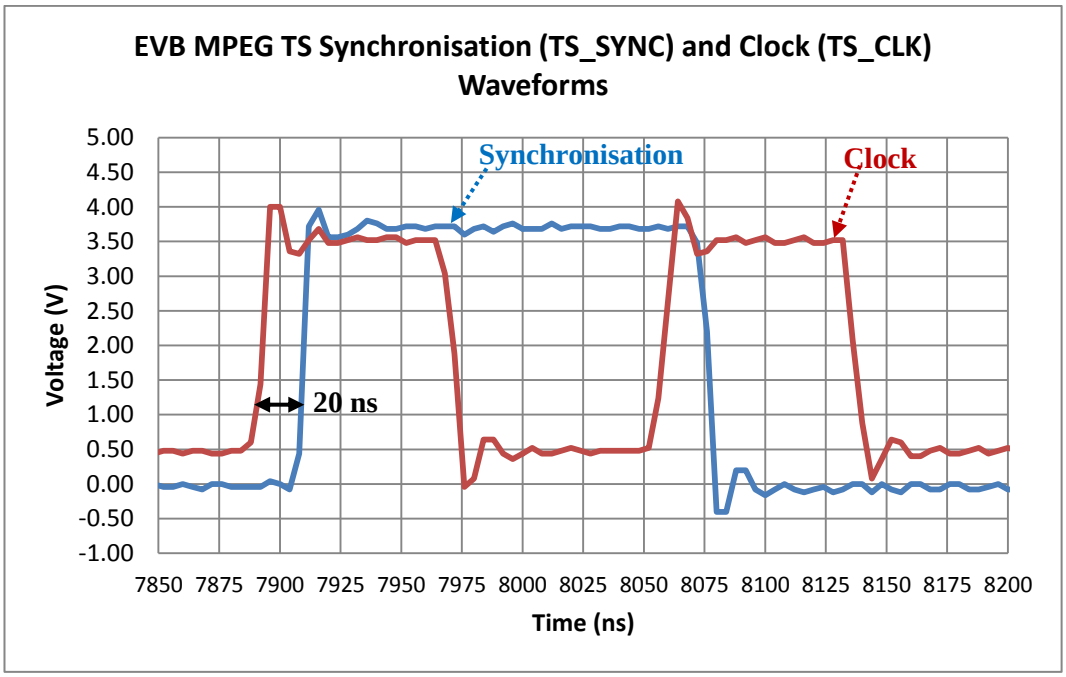


Figure 4-6 EVB MPEG TS synchronisation (single pulse) and clock (author generated image)

4.1.5 EVB MPEG TS Valid (TS_VALID)

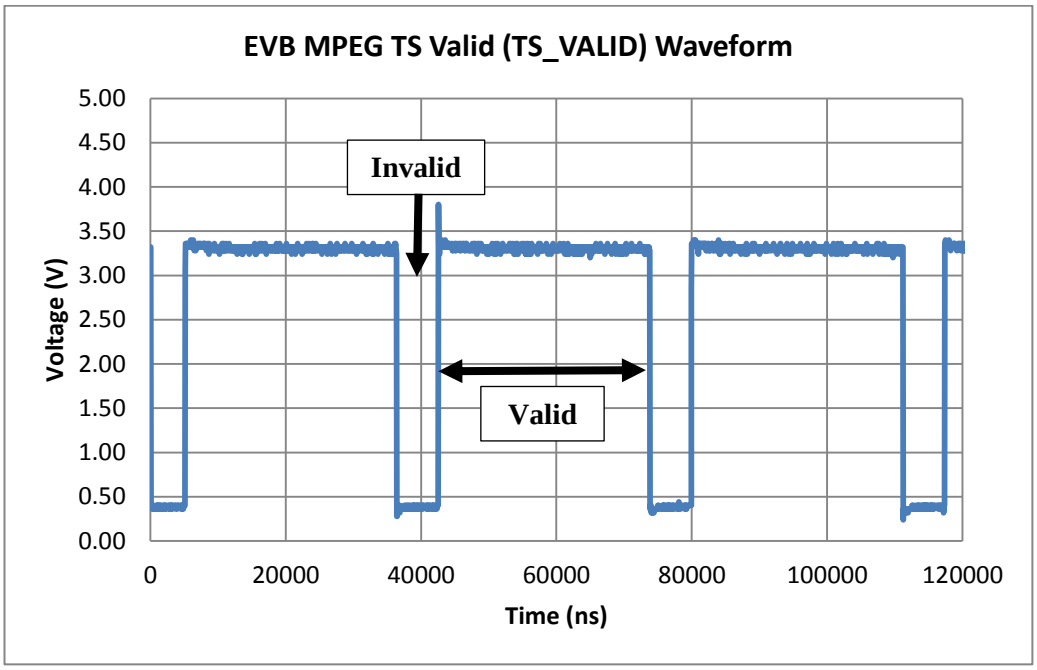


Figure 4-7 EVB MPEG TS valid (author generated image)

The duration of the valid and invalid periods (Figure 4-7) was measured at 31.2 µs and 6.2 µs, respectively, resulting in a total period of 37.4 µs or 26.7 kHz. This result also confirmed that the transmitter MPEG TS clock was running at a lower frequency than the demodulator MPEG TS clock, since the invalid period of 6.2 µs is where no content is transmitted.

The measured period of the TS_VALID signal, when the data is valid, was supported by Equation 2-10, as stated in Chapter 2.

$$T_{TS\_VALID} = 188\frac{1}{f_{TS\_CLK}}\ (s) \qquad \text{Equation 2-10}$$

4.1.6 EVB MPEG TS Data (TS_DATA[1])

Data lines D0 to D7 were measured and found to have similar waveforms. The waveform of the MPEG TS D1 data line is shown Figure 4-8.

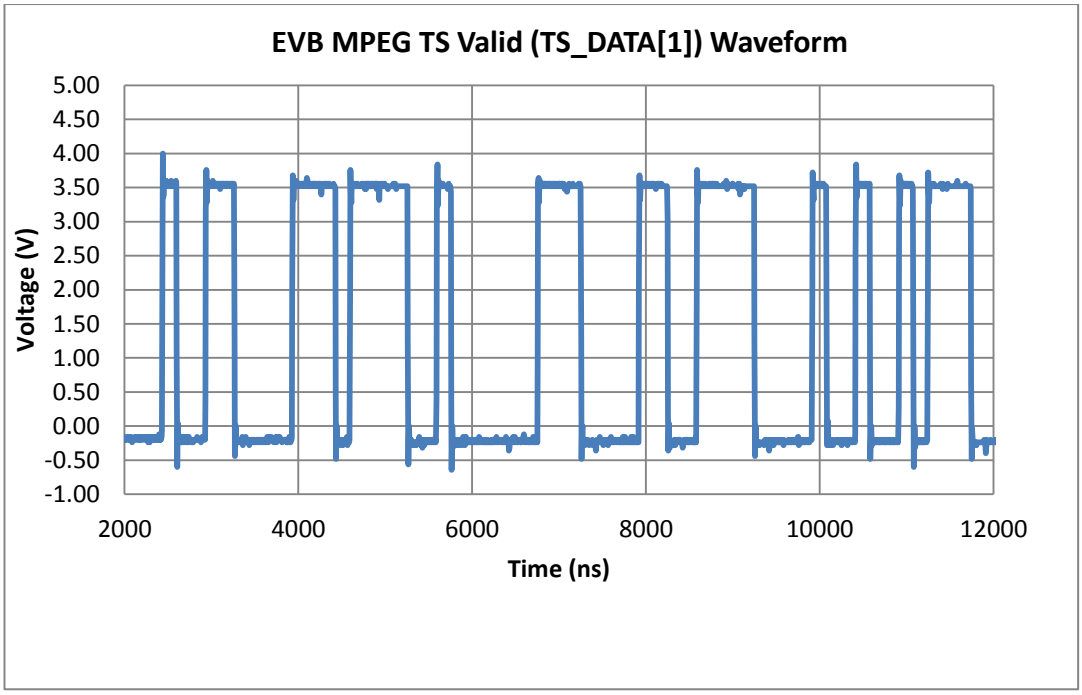


Figure 4-8 EVB MPEG TS data (Data line D1) (author generated image)

Analyses of the data lines relative to the clock, synchronisation and valid signals revealed that all data bits were clocked at 6.008 MHz, and therefore had a bit period of 166.4 ns. Also, blocks of data occurred within the 31.2 µs valid period of the valid signal.

The period of a single data bit [D7...0] is given by Equation 2-9 as stated in Chapter 2.

$$T_{TS\_DATA[7...0]} = \frac{1}{f_{TS\_CLK}} \ (s)$$

Equation 2-9

4.1.7 EVB MPEG TS Summary

An MPEG non-inverted clock frequency of 6 MHz, set by the Silicon Labs software, produced a measured clock frequency of 6.008 MHz (period 166.4 ns), representing a very small error of approximately +0.13% relative to the software setting of 6 MHz (period 166.4 ns).

The rise- and fall time of the clock was measured at approximately 5 ns. This information is needed to ensure that the rise- and fall-times in the simulated VLC system closely correlated with measured data to ensure correct timing.

The logic levels of the clock were measured at 3.0 V (logic one) and 0V (logic zero), implying that LVCMOS logic levels are used. This information is important when interfacing the EVB to the FPGA during implementation of the VLC system.

The serial clock frequency and bandwidth required by the VLC system was calculated at 66 MHz, based on multiplying the parallel clock frequency of 6 MHz by the 10-bits of the MPEG TS, and then adding one parallel clock cycle to enable serial loading of the PISOs.

The clocking of the parallel MPEG bus lines for synchronisation, valid and data (D0 to D7) was confirmed on the rising-edge (non-inverting) of the MPEG clock as expected. However, a 20 ns offset between the rising-rising edge of the clock and the bus signal edges was observed, which is both unexpected and undesirable, since the clock edge should coincide with the bus edges. This offset was zeroed using the Silicon Labs application software.

The synchronisation pulse duration and data bit periods were confirmed at 166.4 ns, identical to the MPEG clock period. The valid data period was confirmed as a function of the MPEG clock period multiplied by the TS packet size of 188 bytes, resulting in a 31.2 μs valid period. However, the synchronisation pulse period was 6.07 μs longer expect due to the demodulator MPEG TS clock running 1 MHz higher than the transmitters MPEG TS clock, and no content is transmitted during this period. It was concluded that there is additional data capacity in the system; effectively 10 Mbits/s.

4.1.8 Bush DH2636 STB Overview

The Bush DH2636 is a low-cost consumer grade STB receiver capable of receiving DVB-T and DVB-T2 broadcasts. The key difference between the Bush DH2636 STB and the Silicon Labs EVB, is that the STB contains a processor IC, which is capable of decoding the MPEG TS and outputting baseband digital video to an HD monitor via its HDMI interface. Figure 4-9 shows the core blocks of the STB, relevant to the tuner, demodulator and processor. The processors MPEG TS to HDMI function is key to the data sink of the VLC system. A detailed overview and product specification of the STB is provided in Appendix E.

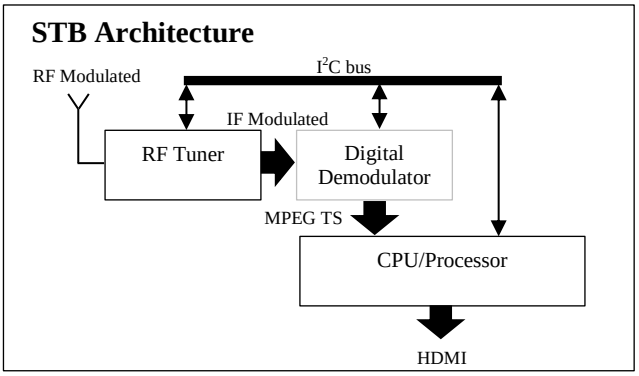


Figure 4-9 Bush DH2636 STB core blocks (author generated image)

In order to ensure the parallel MPEG TS of the EVB was compatible with the STB processor, characterisation of the STB MPEG TS was performed, and the results used to determine the correct configuration for the EVBs MPEG TS to enable its interfacing to the STB processor. Confirmation of correct interfacing was established using end-to-end RF to HDMI testing.

The STB is hardware and firmware configured for MPEG TS parallel mode. In this case, the MPEG TS is not directly available at an output of the STB, and is instead accessed at the output of the STBs internal demodulator. As with the EVB, the demodulator has

twelve output lines; eight lines for data TS_DATA [$D0_{LSB}$ to $D7_{MSB}$]; one line each for the MPEG clock (TS_CLK), valid (TS_VALID), synchronisation (TS_SYNC), and error (TS_ERR). Note: The error line is not required, and therefore is not characterised. Effectively, the parallel bus has ten data lines (10-bits).

4.1.9 STB MPEG TS Characterisation and Analysis

The characterisation of the STB was performed almost identically to the Silicon Labs EVB. The configuration of the STB was different to that of the EVB, in that the parametric configuration of the tuner and demodulator was performed by STB processor and its built-in firmware. Only the STB user menus were accessible using the remote control, therefore tuning to Channel C41 was achieved by performing a channel scan of the RF spectrum presented to the STBs RF input. Upon completion of the scan, the discovered channels were saved to the STBs channel look-up table, and then the channel C101 BBC One HD, which is an elementary programme stream within the channel C41 broadcast, was selected using the remote control. In effect, selecting this elementary stream from the look-up table resulted in the tuner being tuned to 634 MHz; (C41 centre frequency), and the demodulator being configured for DVB-T2 reception. Once locked, the demodulator output a 6 MHz clocked parallel MPEG TS.

4.1.10 STB MPEG TS Clock (TS_CLK)

The clock signal (Figure 4-10) was measured and found to have a frequency of 6.017 MHz, and a 50% duty cycle. Assuming the clock was set to exactly 6 MHz (period 166.6 ns) by the firmware, a frequency error of approximately +0.28% between the firmware setting and measurement of 6.017 MHz (period 166.2 ns) was observed. The logic levels of the clock were measured at 4.0 V (logic one) and 0V (logic zero), compensating for 0.2 V offset from the 0 V line, which was attributed to the under and

overshoots of the signal. It was concluded that the MPEG TS was using TTL logic levels. Logic translation is therefore necessary in the VLC systems. Logic translation is therefore necessary in the VLC systems.

The rise and fall times of the clock were measured between the 10% and 90% points, and were found to be approximately 9 ns. The EVB rise and fall times are faster that the EVB by 4 ns, so the STBs sets the maximum rise- and fall-times acceptable in the VLC system at 9 ns, since the STB MPEG TS can operate with these slow times.

Overall, and with the exception of the rise- and fall-time and TTL logic levels, the STB clock signal behaviour is similar to the EVB.

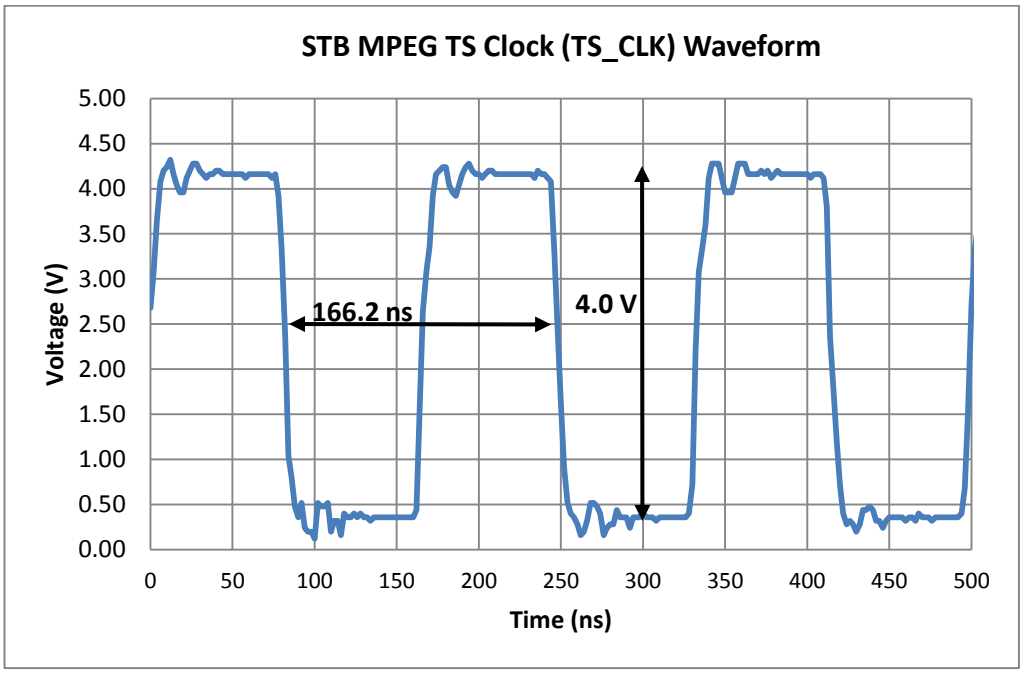


Figure 4-10 STB MPEG TS clock (6.017 MHz, 50% duty cycle)
(author generated image)

4.1.11 STB MPEG TS Synchronisation (TS_SYNC)

The frequency of the synchronisation pulses (Figure 4-11) was measured at 26.44 kHz, resulting in a period of 37.8 µs. The 37. 8 µs period was also at variance with Equation

2-11, as stated in Chapter 2, confirming that the MPEG TS clock of the STB was running faster than the transmitters MPEG TS clock. The difference in clock frequency was again calculated using Equation 2-13, stated in Chapter 2, and it was found that the transmitter MPEG TS clock running at approximately 4.97 MHz, approximately 1 MHz below the demodulator clock; this correlates with the analysis of the EVB synchronisation signal, and confirms that the transmitters MPEG TS clock is responsible for the 1 MHz clock difference.

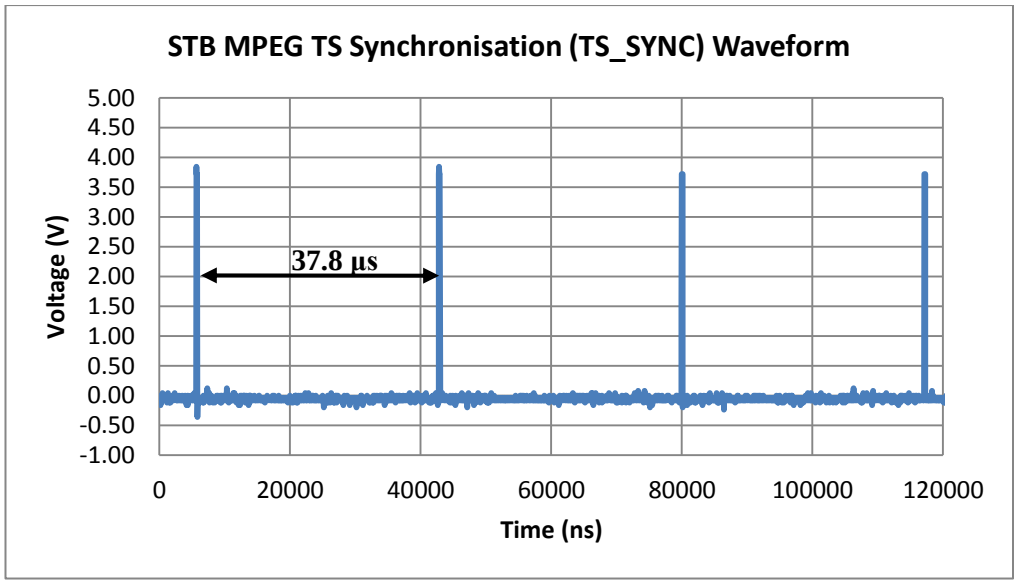


Figure 4-11 STB MPEG TS synchronisation (author generated image)

The duration of a single synchronisation pulse (Figure 4-12) was measured at 166.2 ns.

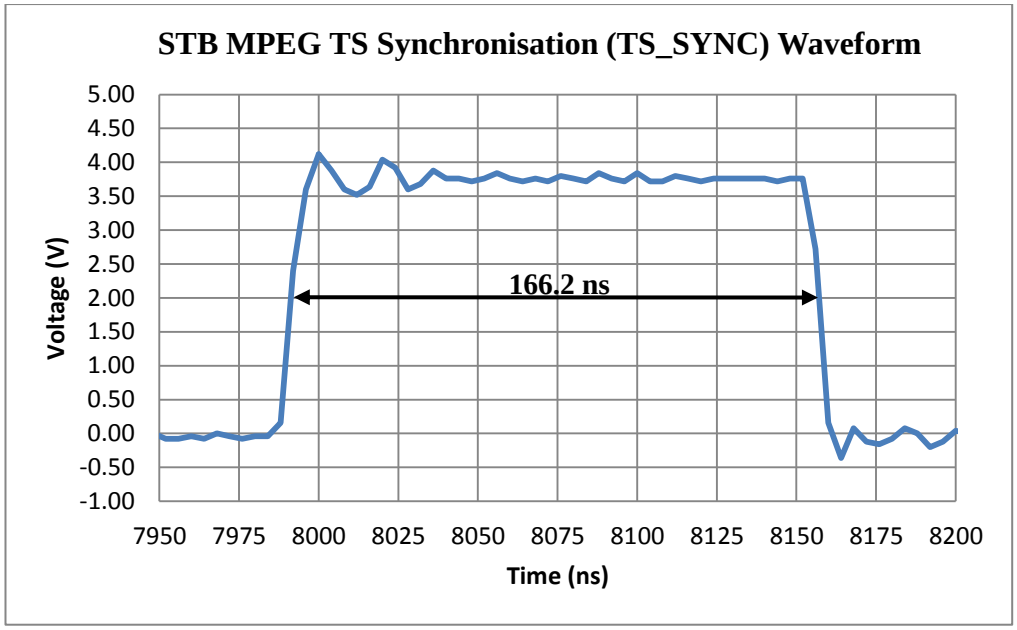


Figure 4-12 STB MPEG TS synchronisation (single pulse) (author generated image)

A single synchronisation pulse duration was measured relative to the clock (Figure 4-13), and was found to have a duration equal to one cycle of the 6.017 MHz clock at 166.2 ns. Clocking of the synchronisation pulse occurred on the falling-edge of the clock (inverted). It was also noted that no timing offset between the falling-edge of the clock and the signal edges of the synchronisation, valid and data lines D7 to D0 was observed.

Comparing STB clock with that of the Silicon Labs EVB, indicated that the STB clock was inverted relative to the EVB clock. In order to ensure MPEG TS compatibility between the devices, the EVB clock needed changing from the non-inverted to the inverted setting. This finding is confirmed in section 4.1.15.

Overall, and with the exception of the clock inversion, the synchronisation signal behaviour is similar to the EVB.

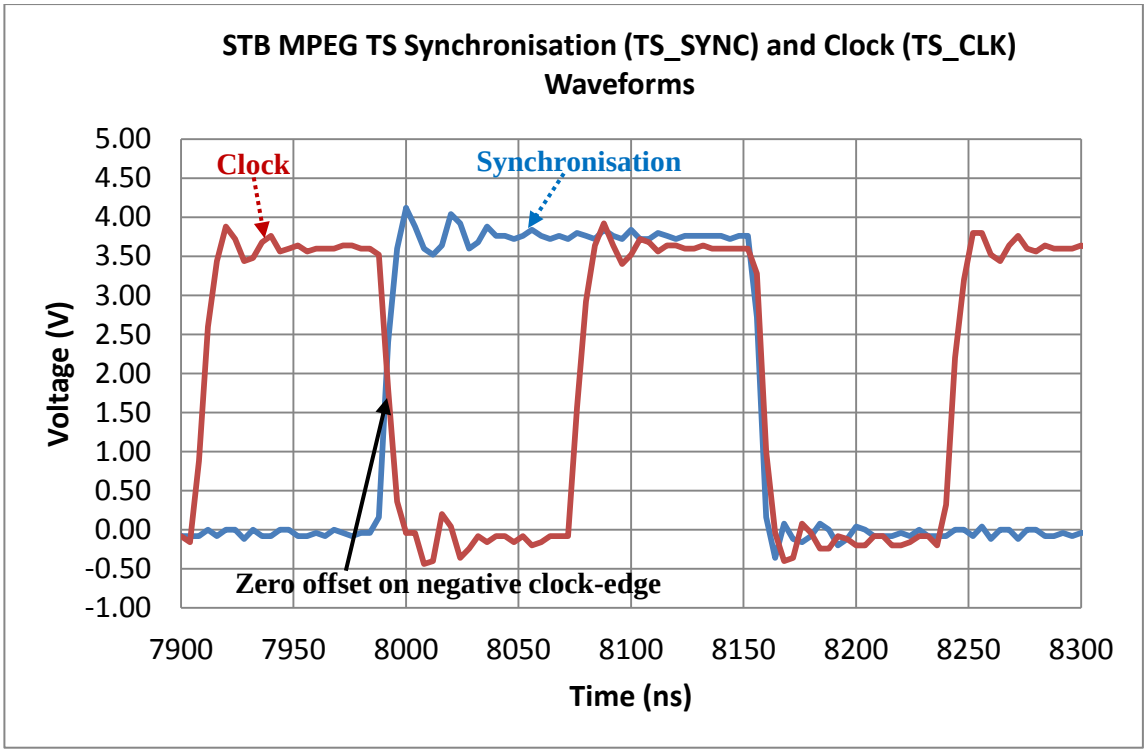


Figure 4-13 STB MPEG TS synchronisation (single pulse) and clock (author generated image)

4.1.12 STB MPEG TS Valid (TS_VALID)

The duration of the valid and invalid periods (Figure 4-14) was measured at 31.4 µs and 5.7 µs, respectively, resulting in a total period of 37.1 µs or 27.0 kHz.

The measured period of the TS_VALID signal, when the data is valid, was again supported by Equation 2-10, as stated in Chapter 2.

Overall, the STB valid signal behaviour is similar to the EVB.

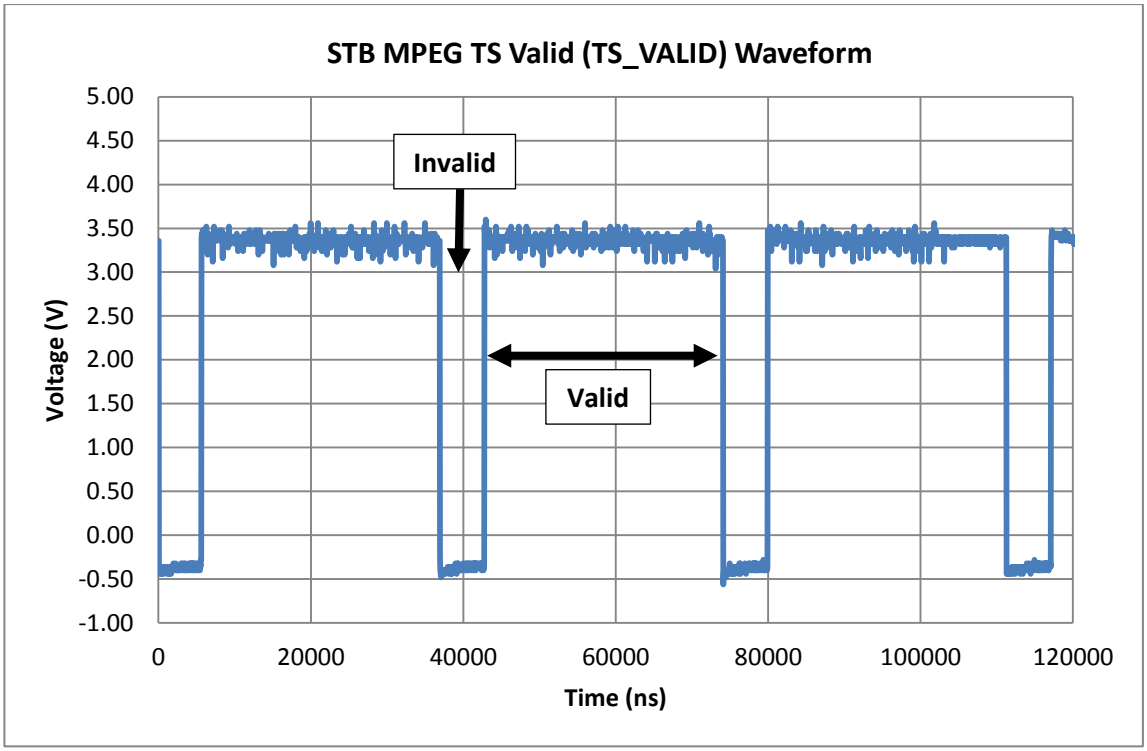


Figure 4-14 STB MPEG TS valid (author generated image)

4.1.13 STB MPEG TS Data (TS_DATA[1])

Data lines D0 to D7were measured and found to have similar waveforms. The waveform of the MPEG TS D1 data line is shown Figure 4-15.

Analyses of the data lines relative to the clock, synchronisation and valid signals revealed that all data bits were clocked at 6.017 MHz, and therefore had a bit period of 166.2 ns. Also, blocks of data occurred within the 31.4 µs valid period of the valid signal.

The period of a single data bit [D0...D7] is given by Equation 2-9 as stated in Chapter 2.

Overall, the STB data signals behaviour is similar to the EVB.

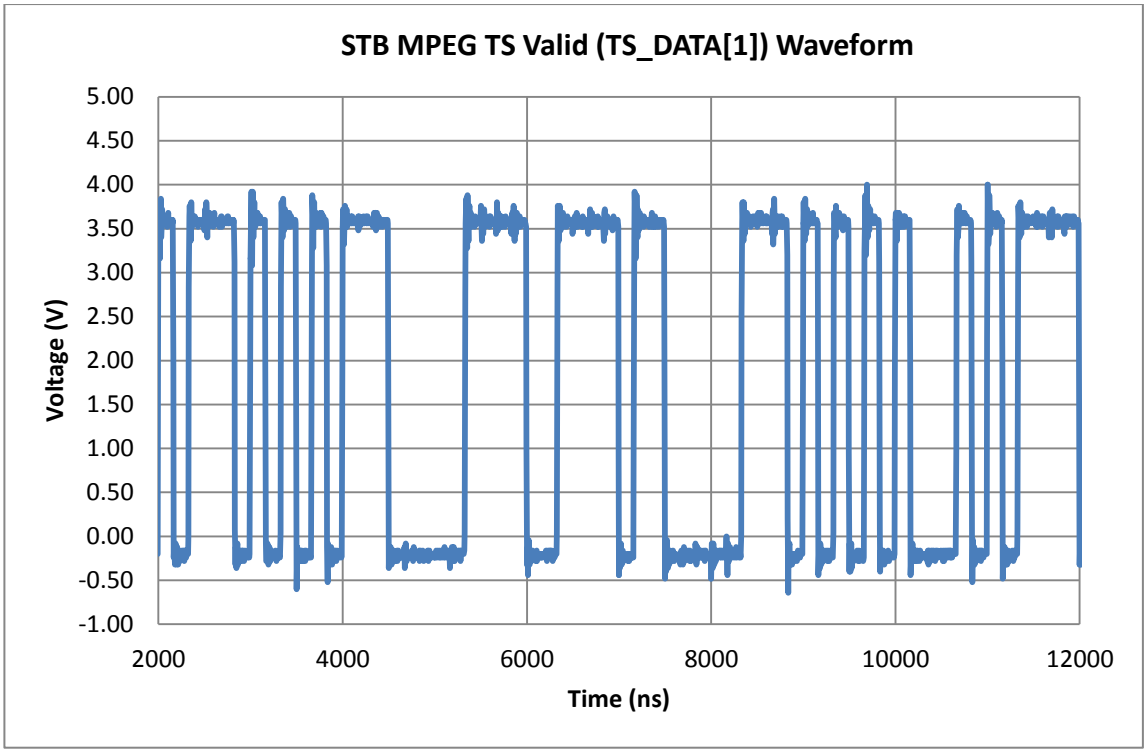


Figure 4-15 STB MPEG TS DATA (Data line D1) (author generated image)

4.1.14 STB MPEG TS Summary

An MPEG inverted clock frequency of 6 MHz (period 166.4 ns), assumed set by the firmware of the STB platform, produced a measured clock frequency of 6.017 MHz (period 166.2 ns), representing a very small error of approximately +0.28% relative to the firmware setting.

The rise- and fall time of the clock was measured at approximately 9 ns. And it was determined that this slower rise- and fall-time is the maximum tolerated in the VLC system.

The logic levels of the clock were measured at 4.0 V (logic one) and 0V (logic zero), implying that TTL logic levels are used. Logic translation is therefore necessary in the VLC system.

The 6 MHz clock and 10-bits of the MPEG TS bus used by the EVB and STB confirmed that a serial clock frequency and bandwidth required of 66 MHz was required by the VLC system.

Overall, and with the exception of the rise- and fall-times and TTL logic levels, the STB clock signal behaviour was found to be similar to the EVB.

The clocking of the parallel MPEG bus lines for synchronisation, valid and data (D0 to D7) was confirmed on the falling-edge (inverting) of the MPEG clock, which meant that the EVB clock needed changing from non-inverting to inverting to enable compatibility with the STB processor. No offset between the falling-rising edge of the clock and the bus signal edges was observed on the STB, meaning that 20 ns offset found on the EVB must be zeroed to ensure compatibility.

The synchronisation pulse duration and data bit periods were confirmed at 166.2 ns, identical to the MPEG clock period. The valid data period was confirmed as a function of the MPEG clock period multiplied by the TS packet size of 188 bytes, resulting in a 31.4 μs valid period. The synchronisation pulse period was again found to be longer expected, due to the demodulator MPEG TS clock running 1 MHz higher than the transmitters MPEG TS clock, and no content is transmitted during this period. It was again concluded that there is additional data capacity in the system; effectively 10 Mbits/s.

Overall, the behaviour of the synchronisation, valid and data signals of the STB were similar to the EVB.

4.1.15 Data Source and Sink End-to-End Compatibility

An essential check before designing and implementing the VLC system was to confirm MPEG TS compatibility between the EVB and the STB processor. In order to do this check, a bypass board, was constructed to enable switching of the STB demodulator or EVB MPEG TS into the STB processor. A logic level translator circuit was used to translate the LVCMOS logic levels of the EVB to the TTL levels required by the STB. Figure 4-16 shows the physical test setup of the platforms and Figure 4-17 shows block diagram of the end-to-end test configuration of the EVB and STB. The precise pin assignments and switching circuit schematic for the end-to-end test configuration are show in Appendix G.1 and G.2, respectively.

In the first test configuration, the EVB MPEG TS was switched into the STB processor, and its RF input connected to a roof-top Yagi array. The EVB was then tuned to Channel C41 (634 MHz), and configured for parallel MPEG TS output. The parallel clock was inverted, and set to 6 MHz with the 20 ns offset zeroed, as described in section 4.1.11. The STB was then used to select BBC One HD ES from the MPEG TS of the EVB; note that the STB performed a channel scan prior to this test to ensure all available channels were stored in the STBs channel look-up table. The STB processor performed MPEG decoding of the MPEG TS and presented the baseband BBC One HD content on the HDMI interface, which was connected to an HD monitor to facilitate reproduction. The reproduced content was monitored for a period 24 hour without error. Following this test, all other ESs were tested in the multiplex: C86 More4 +1; C102 BBC Two HD (England); C103 ITV HD (ITV Granada); C104 Channel 4 HD North ads; C105 Channel 5 HD; and C204 CBBC HD. All the streams were successfully decoded and produced error-free reproduction.

In the second test configuration, the STB internal demodulators MPEG TS was switched into STB processor. The STB was tuned to Channel 41 (634 MHz) and all the ESs of the multiplex were tested. All the streams were successfully decoded and produced error-free reproduction. This test configuration was used during the FPGA implementation of the IOPPM encoder and decoder, to confirm that the FPGAs MPEG TS matched the STB internal demodulators signal levels and timing.

The tests confirmed end-to-end compatibility of the data source and sink devices required by the hardware implementation of the VLC system.

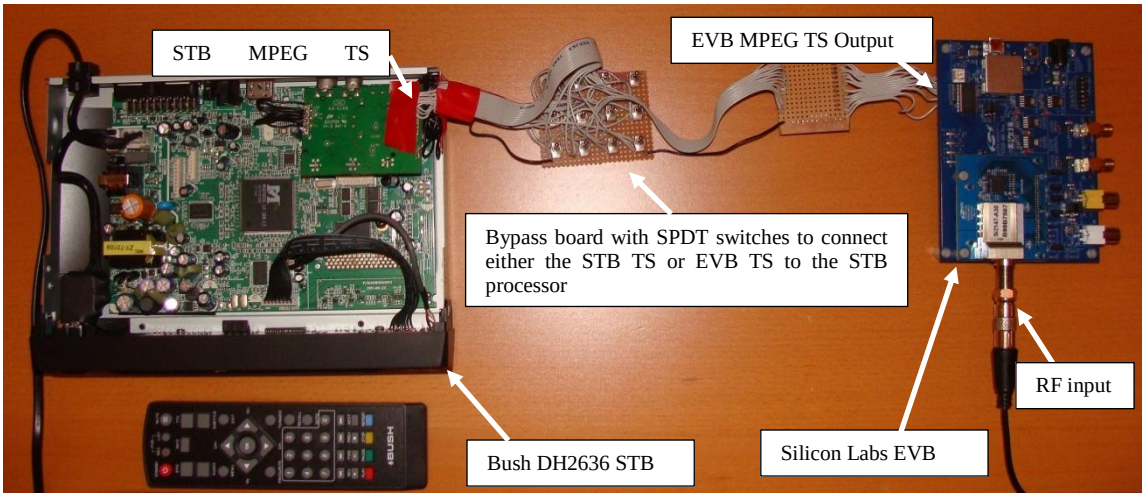


Figure 4-16 Si2168 MPEG TS to MSD7853L physical test setup
(author generated image)

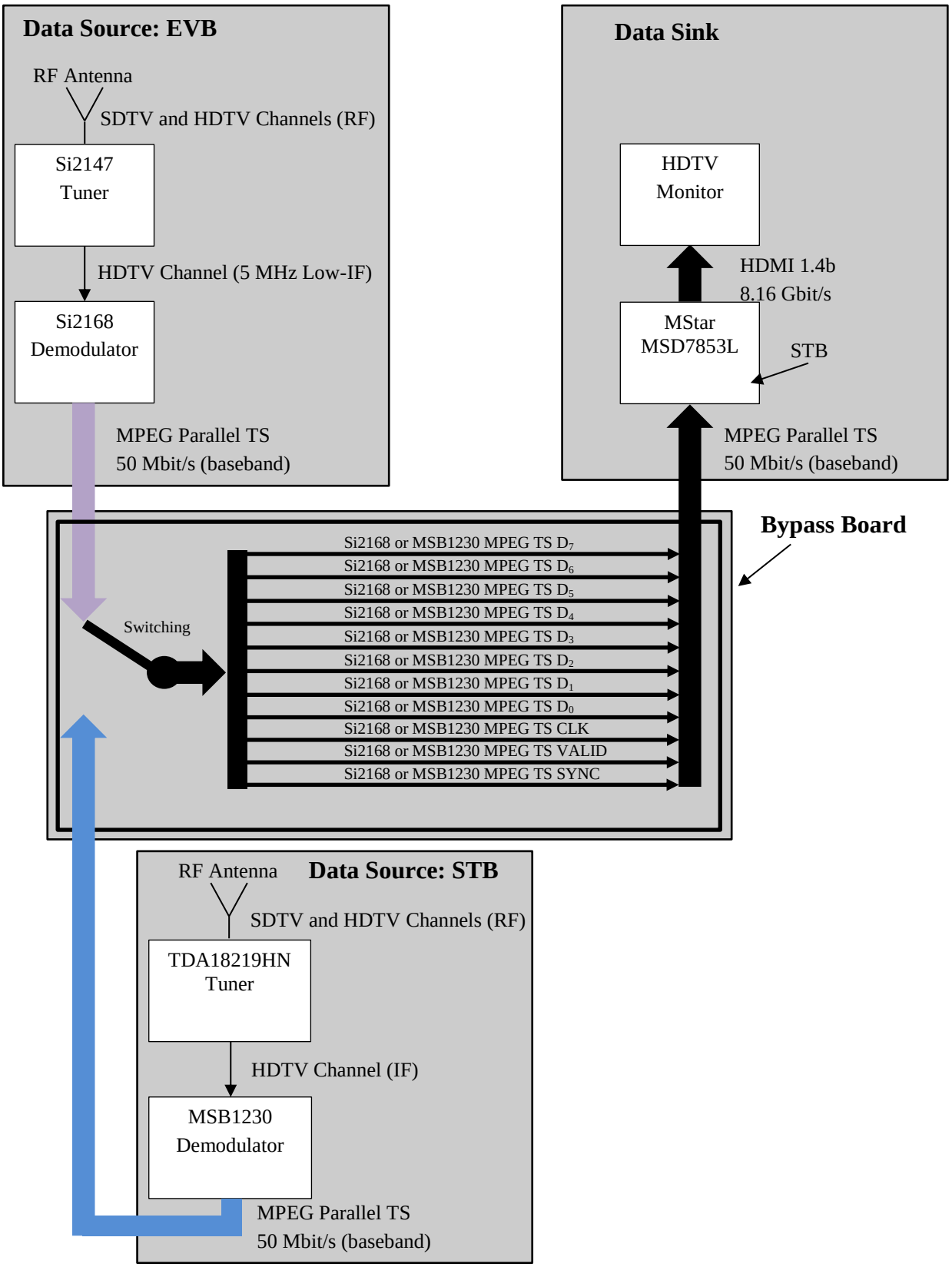


Figure 4-17 Data source and sink end-to-end test configuration (author generated image)

4.1.16 Conclusions

In this section of Chapter 4, the characterisation measurements and analyses of the MPEG TS source and sink devices, selected for use in the hardware implementation of the VLC system, were presented. The characterisation of the parallel MPEG TS clock frequency of the devices was used to calculate the VLC systems serial clock frequency and bandwidth. The other signals of the MPEG TS were also characterised, in order to establish optimal settings to ensure their compatibility within the VLC system. In particular, the logic levels and clocking requirements needed to interface between the devices and the FPGA implementations of the IOPPM encoder and decoder were established.

It was concluded in this section that:

- A Silicon Labs worldwide digital tuner and DVB-T/T2/C demodulator EVB will be used as the data source in the VLC system, and will receive off-air DVB-T and DVB-T2 broadcasts and generate the 10-bit MPEG TS bus that will be used for IOPPM re-encoding.
- A Bush DH2636, low-cost consumer grade DVB-T and DVB-T2 STB receiver will be used as the data sink in the VLC system, and will decode the IOPPM decoded 10-bit MPEG TS bus and provide HDMI output to enable reproduction of content on an HD monitor.
- The serial clock frequency and bandwidth required by the VLC system is 66 MHz, based on the 6 MHz parallel clock frequency and 10-bit MPEG TS used by both source and sink devices. Multiplying the clock frequency and number of bits in the MPEG TS bus, and then adding one parallel clock cycle to enable serial loading of the PISOs, yielded the 66 MHz frequency. This parameter is

key to the VLC system, since the LED must be able to support this bandwidth. The characterisation of a white and blue LED will be performed in the next section.

- Overall, the MPEG TS of the EVB and STB were similar, with the exception of:
    - The MPEG TS logic levels. The EVB outputs LVCMOS levels and the STB outputs TTL levels. A logic translator is therefore necessary to convert the EVB output to TTL levels.
    - The STB parallel MPEG TS uses falling-edge clocking (inverted) of the MPEG TS bus, therefore the EVB clock needs setting to inverted clocking to ensure compatibility between the source and sink.
- Correction of the differences in the MPEG TS of the EVB compared to the STB enabled compatibility of the MPEG TS bus. This was confirmed with end-to-end testing.
- Additional capacity in the bit rate of the VLC system is possible, given that the MPEG TS clock of the EVB and STB is running higher than the MPEG TS clock of the broadcast transmitter by 1 MHz. The parallel clock at the transmitter for Channel C 41 is actually running at 5 MHz versus 6 MHz at the EVB and STB, meaning that the actually effective bit rate of the broadcast is 50 Mbits/s versus 60 Mbits/s in the EVB and STB – a difference of 10 Mbits/s. Unfortunately, the clock frequency of the STB is fixed at 6 MHz, so lowering the serial clock frequency to 56 MHz to reduce the bandwidth demand on the VLC systems LED is not possible.

Characterisation of white and blue LED candidates is presented in the following section. The chosen LED must be able to support the 66 MHz serial clocking

frequency of the IOPPM PISOs. The first zero crossing bandwidth of the IOPPM pulses is also 66 MHz as described by the theory in Chapter 2, section 2.5.4. The IOPPM pulse period (τ) is 15.1515 ns, based on the inverse of the serial clock frequency.

4.2 LED Characterisation and Analysis

Two consumer grade SSL LEDs were selected for characterisation. The first an Osram Oslon1 PowerStar ILH-ON01-NUWH-SC201-WIR200 white LED, which is based on the OSLON SSL ceramic package LCW CP7P device (Osram, 2010a), and the second, an Osram Oslon LB CP7P-GYHY-35 SSL blue (470 nm) LED (Osram, 2010b, 2013). These devices were chosen by the author due to wide availability and proven use in VLC systems (Dimitrov, 2015). The devices were characterised at a number of forward bias current settings, and the resulting frequency responses and 3 dB bandwidths analysed.

4.2.1 White LED Overview

The Osram white LED, is fabricated using a GaN semiconductor device and a YAG:Ce phosphor, and relies on the partial conversion process to produce a white emission. The device is a SMD device and is mounted on heat-sink as shown in Figure 4-18. The data sheet stated that the device is normally driven using a constant DC current in the range 100 to 1000 mA at a forward bias voltage in the range 2.75 to 3.75 V (Osram, 2010a). The device is also stated as having an irradiance angle of ± 40°.

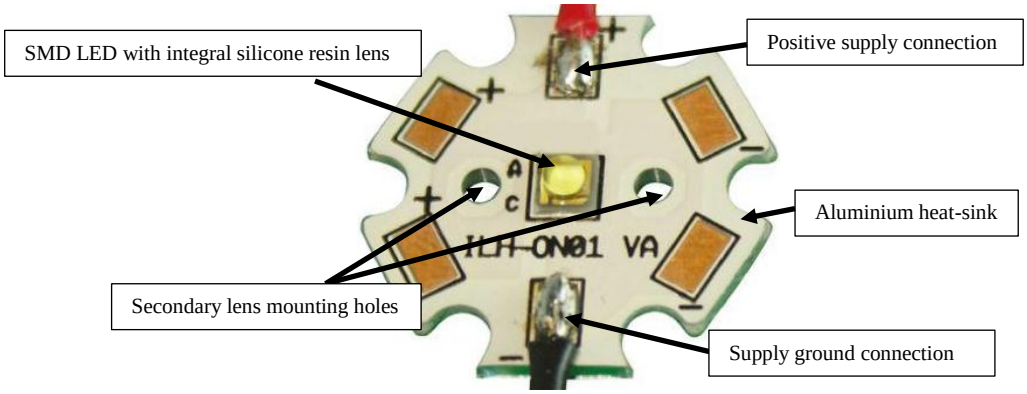


Figure 4-18 Osram White LED (author generated image)

Note that during all tests a secondary Tina-Pin-OSL real spot concentrator, also manufactured by Osram, was mounted over the LED. This concentrator provides a semi-angle of ± 4°, effectively reducing the irradiance angle and concentrating the LED emission into a narrow beam, which is desirable for DLOS transmission.

4.2.2 White LED Characterisation and Analysis

The frequency response of the white LED was measured at five bias currents: 99.1 mA, 80.5 mA, 59 mA, 28.4 mA and 13.1 mA. These currents, which were below the minimum operating current of 100 mA stated in the data sheet, were selected to reduce the power consumption of the transmitter. An additional benefit of operating the LED at a lower power was to increase life expectancy of the device in the VLC system.

Figure 4-19 shows the normalised frequency responses of the device from DC to 200 MHz at all five forward bias currents. It is important to note that roll-off of the received power between DC and 2 MHz was caused by the capacitive reactance of a 1 nF coupling capacitor used in the test circuit; the primary purpose of the capacitor was to act as a DC block, preventing the LEDs bias current flowing into the front-end of the RF signal generator. For more information regarding the DLOS test setup and conditions, refer to Appendix I.1.

Further analysis of the frequency responses of Figure 4-19 showed that there was a resonance at approximately 24 MHz, limiting the devices usable range from DC to slightly above 20 MHz. Negating the resonance, the device exhibited similar responses from DC to 90 MHz at all forward bias currents, although the noise level increased significantly from 40 to 80 MHz. Beyond 80 MHz the device exhibited inconsistent behaviour.

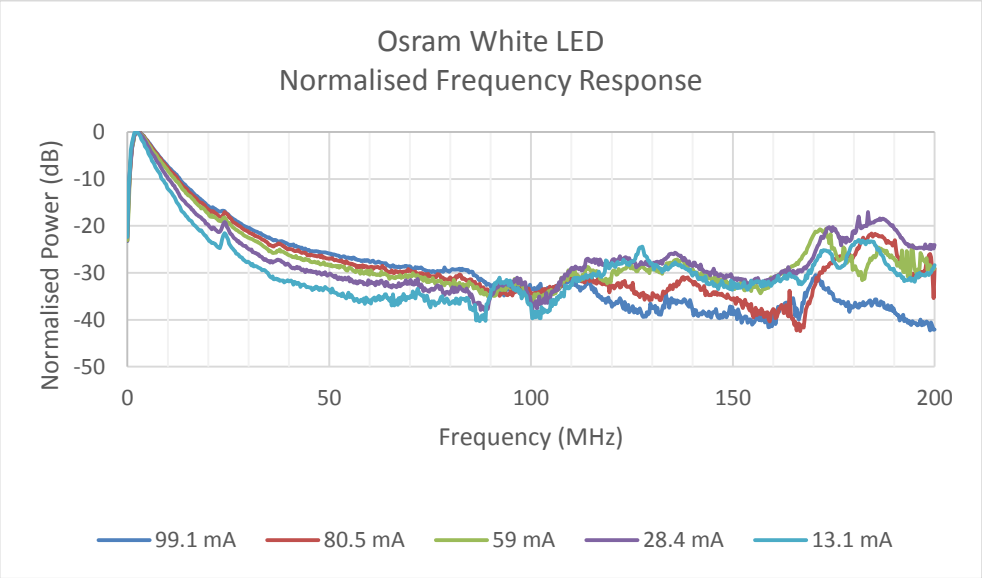


Figure 4-19 White LED normalised frequency response (DC to 200 MHz) (author generated image)

The 3 dB bandwidth of the device was determined by analysing the frequency responses from DC to 10 MHz at all five forward bias currents, as shown in Figure 4-20; note the -3 dB point is highlighted by the dotted line.

In addition to the 3dB bandwidth, Figure 4-20 also highlights a frequency offset when the LED is biased at 13.1 mA. This offset is approximately 100 kHz relative to the other forward bias currents, and is indicative of an increase in impedance within the device at low bias current.

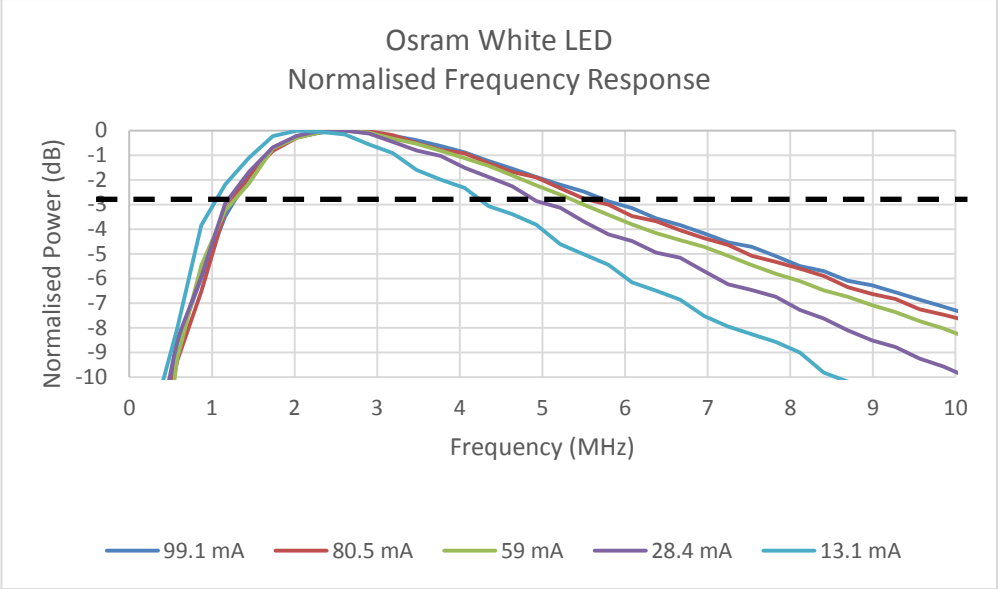


Figure 4-20 White LED normalised frequency response (DC to 10 MHz) (author generated image)

Figure 4-21 shows a plot of LEDs 3 dB bandwidth versus forward bias current. The bandwidth of the device increases as the forward bias current increases. The rate at which the bandwidth increases is 17.7 kHz/mA, as estimated by the dotted trend line.

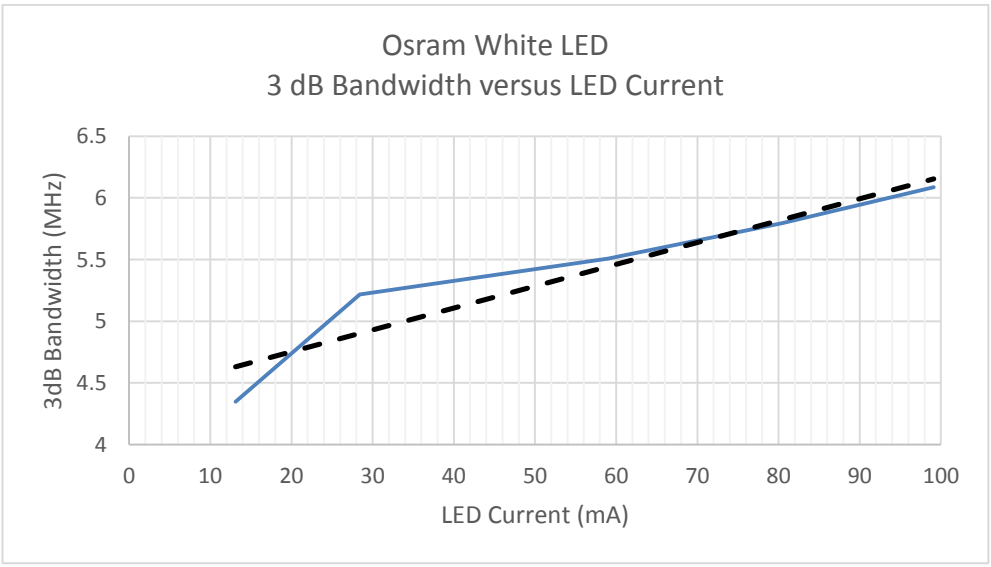


Figure 4-21 White LED 3 dB bandwidth versus forward bias current (author generated image)

The forward bias currents versus 3 dB bandwidths are also tabulated in Table 4-1. The table shows that even at the lowest bias current of 13.1 mA, the LED has a 3 dB

bandwidth of 4.35 MHz, which is almost twice the bandwidth of an Osram Ostar phosphor based LED that was reported by Ghassemlooy et al as, which had a bandwidth of 2.5 MHz (Z. e. Ghassemlooy et al., 2013). This indicates that Osram Oslon1 device has higher bandwidth than the Osram Ostar device discussed in Chapter 2, even at forward bias currents below the 100 mA minimum stated in the data sheet.

Forward Bias Current (mA)	**3 dB Bandwidth (MHz)**
13.1	4.35
28.4	5.22
59.0	5.51
80.5	5.80
99.1	6.09

Table 4-1 White LED forward bias current versus 3 dB bandwidth

Further bandwidth extension is possible using optical blue filter at the receiver, but at the cost of lower received power due to the attenuation of the filter. Additional equalisation is also possible using post-equalisation at the receiver as described in Chapter 2.

A received power measurement was also made using collimation lens and a separation of 95 cm between the LED and a reference PD. For more information regarding the test setup, refer to Appendix I.2.

The LED forward bias current was swept over the values used in previous measurements. Figure 4-22 shows the plot of received power versus forward bias current, and illustrates a linear increase of the received power with increasing forward bias current; the rate of increase is 39.8 μW/mA, as indicated by the dotted trend line. The results are also shown tabulated in Table 4-2, which shows that the received power at the forward bias current of 99.1 mA is almost eight times larger than the minimum

bias current of 13.1 mA. However, operating the LED at the higher bias current increases the range of the LED transmitter, but also increases power consumption in the transmitter.

Forward Bias Current (mA)	Received Power (mW)
13.1	0.52
28.4	1.17
59.0	2.27
80.5	3.14
99.1	4.01

Table 4-2 White LED forward bias current versus received power

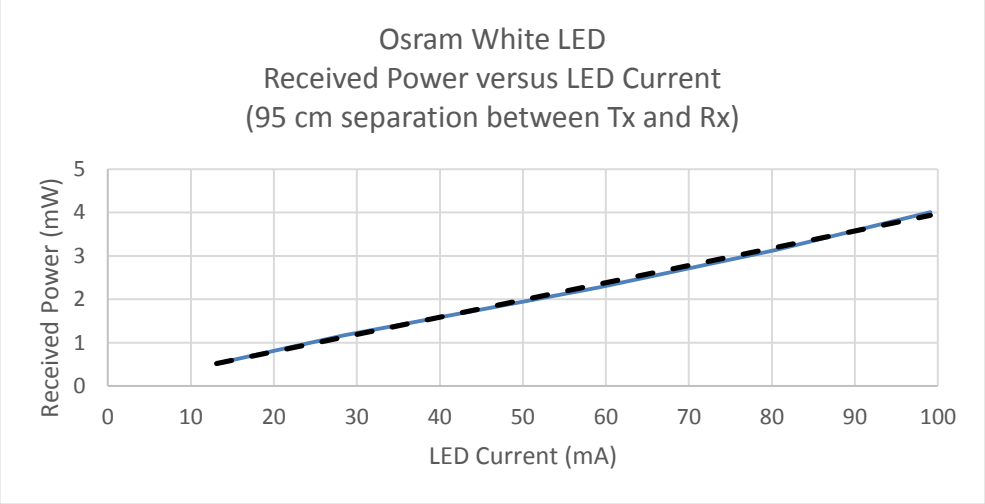


Figure 4-22 White LED received power versus forward bias current
(author generated image)

4.2.3 Blue (470 nm) LED Overview

The Osram blue LED is fabricated using a GaN semiconductor device and produces an almost monochromatic blue emission centred at a wavelength of 470 nm. The device is also mounted on a heat-sink identical to that shown in Figure 4-18 . The data sheet stated that the device is normally driven using a constant DC current in the range 20 to 1000 mA at a forward bias voltage in the range 2.75 to 3.50 V (Osram, 2010b, 2013). The device is also stated as having an irradiance angle of ± 40°.

4.2.4 Blue (470 nm) LED Characterisation and Analysis

Characterisation of the blue LED was performed using the same setup as described in Appendix I.1. The frequency response of the blue LED was measured at six bias currents: 106.3 mA, 102 mA, 80 mA, 55 mA, 27.2 mA, 13 mA. These currents, which were largely above the operating current of 20 mA stated in the data sheet, were selected again to reduce the power consumption of the transmitter. Figure 4-23 shows the normalised frequency responses of the device from DC to 200 MHz at all six forward bias currents. Again, it is important to note that roll-off of the received power between DC and 2 MHz was caused by the capacitive reactance of a 1 nF coupling capacitor used in the test circuit.

Further analysis of the frequency responses of Figure 4-23 showed that bias currents at, or above 27.2 mA, exhibited consistent responses from DC to 125 MHz, and beyond 125 MHz the device exhibited inconsistent behaviour. At a bias current of 13 mA, the device exhibited consistent behaviour from DC to 116 MHz.

The 3 dB bandwidth of the device was determined by analysing the frequency responses from DC to 20 MHz at all five forward bias currents, as shown in Figure 4-24; note the -3 dB point is highlighted by the dotted line.

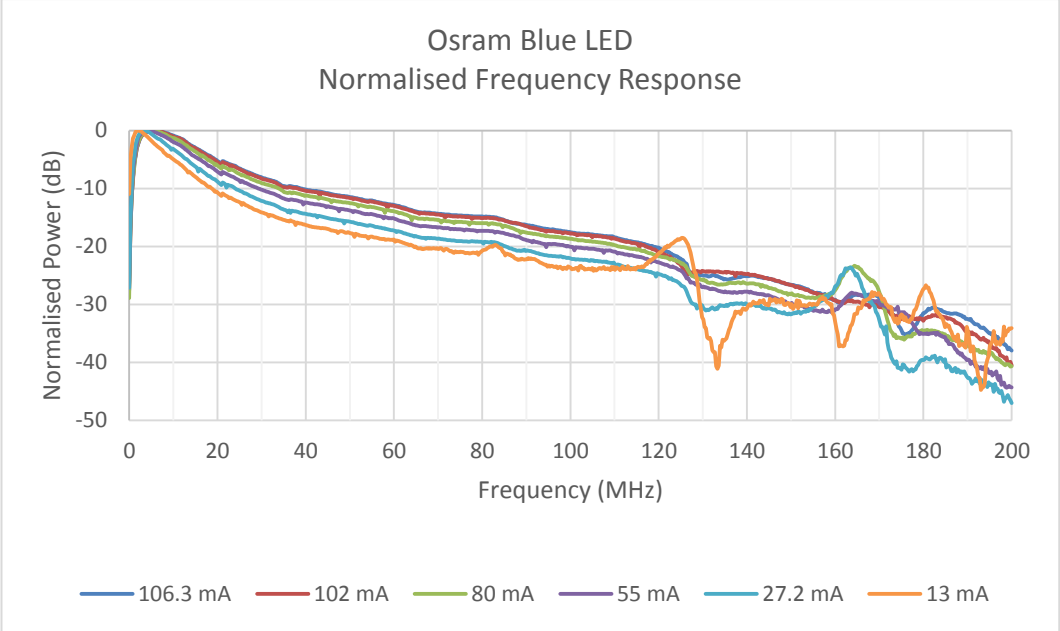


Figure 4-23 Blue LED normalised frequency response (DC to 200 MHz) (author generated image)

In addition to the 3dB bandwidth, Figure 4-24 also highlights a frequency offset when the LED is biased at 13 mA. This offset is approximately 860 kHz relative to the other forward bias currents, and is indicative of an increase in impedance within the device at low bias current.

Figure 4-25 shows a plot of LEDs 3 dB bandwidth versus forward bias current. The bandwidth of the device increases as the forward bias current increases. The rate at which the bandwidth increases is 85.7 kHz/mA, as estimated by the dotted trend line.

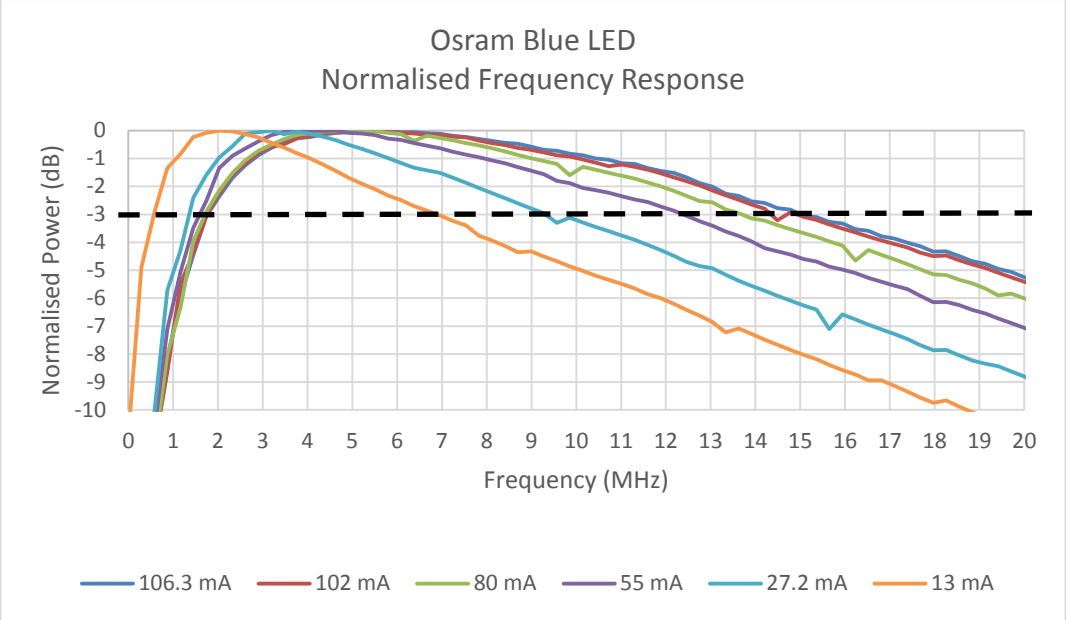


Figure 4-24 Blue LED normalised frequency response (DC to 20 MHz) (author generated image)

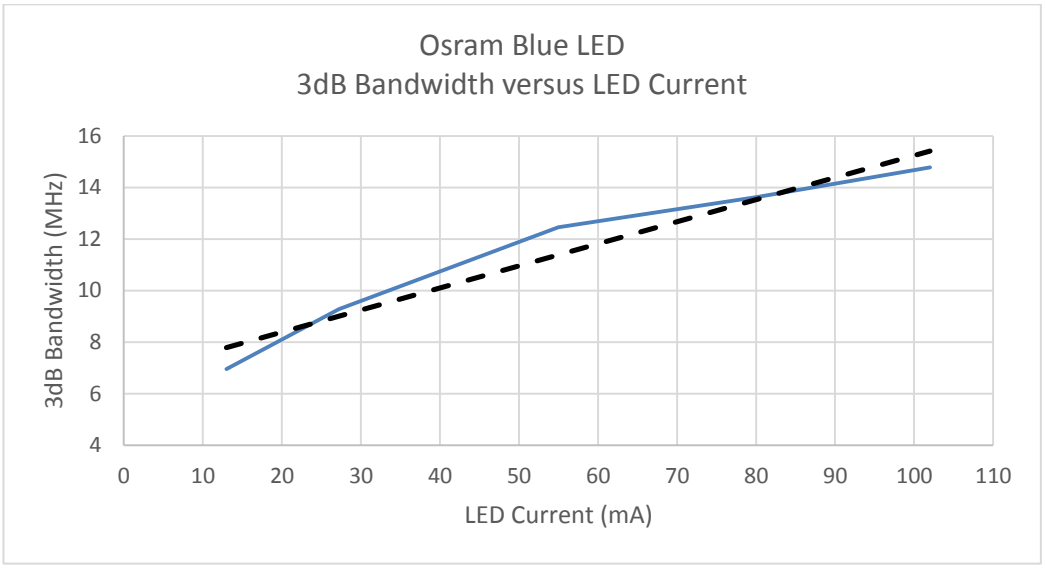


Figure 4-25 Blue LED 3 dB bandwidth versus forward bias current (author generated image)

The 3 dB bandwidth versus the forward bias current is also tabulated in Table 4-3. It can be seen that at the forward bias current of 13 mA, which is below the data sheet stated minimum current of 20 mA, the bandwidth is 6.96 MHz. However, at 27.2 mA, the bandwidth is at almost 10 MHz, which was reported by Cossu for single colour LEDs

(Cossu, 2012), as described in Chapter 2. The blue LED offers wider bandwidths than the white LED at the same forward bias currents.

Forward Bias Current (mA)	3 dB Bandwidth (MHz)
13.0	6.96
27.2	9.28
55.0	12.46
80.0	13.62
102.2	14.78
106.1	15.07

Table 4-3 Blue LED forward bias current versus 3 dB bandwidth

In the case of the blue LED, only post-equalisation in the receiver is necessary to extend the bandwidth, therefore no received power reduction is incurred by the attenuation introduced by an optical filter.

A received power measurement was again made using characterisation setup described in Appendix I.2, where the received power versus forward bias current is shown in Figure 4-26. The plot shows a linear increase of 48.8 μW/mA, as indicated by the dotted trend line, in the received power versus forward bias current. The results are also shown tabulated in Table 4-4, which shows that the received power at the forward bias current of 106.1mA is almost nine times larger than the minimum bias current of 13 mA. The blue LED has similar received power to that of the white LED, and again, at higher bias currents the range of the LED transmitter is increased, but so too is power consumption in the transmitter. The aim during implementation of the VLC system is to reduce the power consumption in the transmitter, so the lower forward bias current of 13 mA is desirable. The blue LED, as already mentioned, has both a received power and bandwidth advantages over the white LED, since the white LED requires the blue optical filter to extend its bandwidth, but which reduces received power.

Forward Bias Current (mA)	Received Power (mW)
13.0	0.60
27.2	1.39
55.0	2.83
80.0	4.06
102.2	4.93
106.1	5.18

Table 4-4 Blue LED forward bias current versus received power

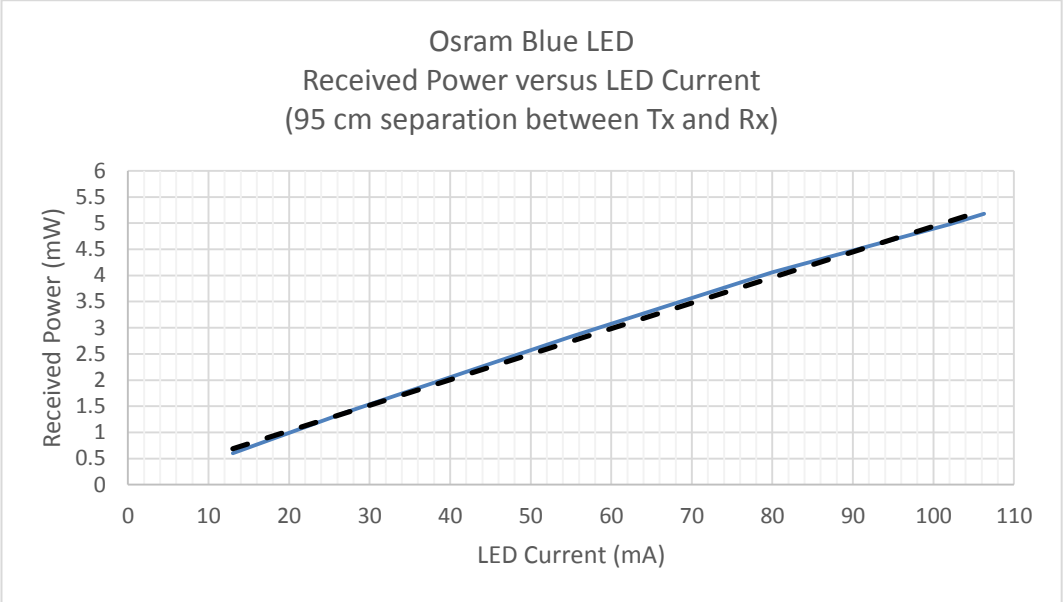


Figure 4-26 Blue LED received power versus forward bias current
(author generated image)

4.2.5 Conclusions

In this section of Chapter 4, the forward bias and 3 dB bandwidth of two LEDs was characterised and analysed. The candidate devices were the Osram Oslon1 PowerStar ILH-ON01-NUWH-SC201-WIR200 white LED and the Osram Oslon LB CP7P-GYHY-35 SSL blue (470 nm) LED.

It was concluded in this section that:

- The Osram Oslon LB CP7P-GYHY-35 SSL blue (470 nm) LED was the most suitable LED for the VLC system. The reasons for the selection were:

- The blue LED exhibits the widest bandwidth across all forward bias currents, compared to the white LED. At 13 mA, the blue LED has a bandwidth of 7 MHz, which is 159% wider than the white LED at the same forward bias current. At approximately 100 mA, the blue LEDs bandwidth is 250% wider. The straight line approximation of the bandwidth versus forward bias current shows a 85.7 kHz/mA rate of increase for the blue LED, compared to a 17.7 kHz/mA for the white LED.
- The usable range frequency of the blue LED is also significantly wider and flatter than the white LED, extending from DC to 125 MHz, except at 13 mA where it extends from DC to 116 MHz. In contrast, the white LED is limited to a DC to 40 MHz range, and exhibits higher noise level from 40 to 80 MHz; beyond 80 MHz the response is inconsistent.
- The absolute received power for both the white and blue devices, is very similar, where the received power versus forward bias current straight line approximation for the blue LED is 48.8 μW/mA and 39.8 μW/mA for the white LED. However, the addition of a blue optical filter to increase the white LEDs bandwidth would result in lower received power due to the attenuation incurred by the filter. The blue filter requires no filtering and therefore has a higher received power.

- The blue LEDs lowest forward bias current will be used by the transmitters drive circuit to reduce power consumption. This will compromise the range of the optical link, since the received power will also be reduced; 13 mA bias achieves a received power of 0.6 mW with a 95 cm separation between transmitter and receiver.

- A secondary Osram Tina-Pin-OSL real spot concentrator, will be mounted over the LED during implementation of the VLC system to reduce the semi-angle to ± 4°, effectively reducing the irradiance angle and concentrating the LED emission into a narrow beam, which is desirable for DLOS transmission.

Using suitable post-equalisation, it is expected that the blue LEDs bandwidth can be extended to support the serial clock frequency of 66 MHz required by the VLC system. Post-equalisation will be explored during the design and simulation work presented in Chapter 5.

5 System: Design and Simulation

In this chapter, the definition, design and simulation of the VLC system is presented, the first section presents the systems top-level architecture, including a block diagram and an explanation of the operation. The subsequent sections detail the design and simulation of the subsystems contained in the top-level architecture using a top-down, modularised approach.

All electrical modelling and simulation were performed using NI Multisim, industry standard PSPICE simulation software.

5.1 Top-level Architecture (IOPPM Single LED)

The first phase of the design process was to define the top-level block diagram of the overall VLC system, which was achieved by integrating the block diagram of the single LED IOPPM encoder/transmitter and the receiver/decoder defined in Chapter 3, with the data source and data sink subsystems and LED device defined in Chapter 4; the resulting system architecture is shown in Figure 5-1. The Silicon Labs EVB is integrated into the transmitter of the VLC system, and acts as the data source for the IOPPM encoder, providing the encoder with the 10-bit MPEG TS generated by the received off-air DVB-T and DVB-T2 broadcast. At the receiver, the Bush DH2636 STB is integrated into the system, and acts as the data sink for the 10-bit MPEG TS, providing MPEG TS decoding and HDMI output, and thus enabling reproduction of the video and audio content on an HD monitor. The EVB and STB MPEG TS buses interface directly with the IOPPM encoding and decoding functions (highlighted in pink), and use the 6 MHz parallel MPEG TS clock to drive a PLL and load pulse block (also highlighted in pink). The function of the PLL is to generate the 66 MHz serial clock required by the VLC

system. The PLL phase-locks to the 6 MHz parallel MPEG TS clock, scaling it by a factor of eleven in order to generate the 66 MHz frequency. As discussed in Chapter 4, clock recovery is not used in the receiver, and instead the 6 MHz and 66 MHz clocks, along with the load pulse generated in the transmitter, are shared with the receiver using hardwired connections. At the transmitter, ten cycles of 66 MHz clock are used to serialise the 10-bit IOPPM encoded MPEG TS, resulting in a 15.1515 ns slot time for each bit of the encoded IOPPM stream; this is calculated by taking the inverse of 66 MHz. At the receiver, ten cycles of the serial clock are used to clock-in the 10-bits into the SIPO. The eleventh cycle of the serial clock is used to load the IOPPM encoder PISOs and unload the decoder SIPOs. The load pulse which is used to perform the loading and unloading operations is generated by the pulse load block, which uses the 6 MHz parallel MPEG TS and 66 MHz serial clock to generate the load/unload pulse. The operation of the load pulse block will be discussed in more detail in the next section.

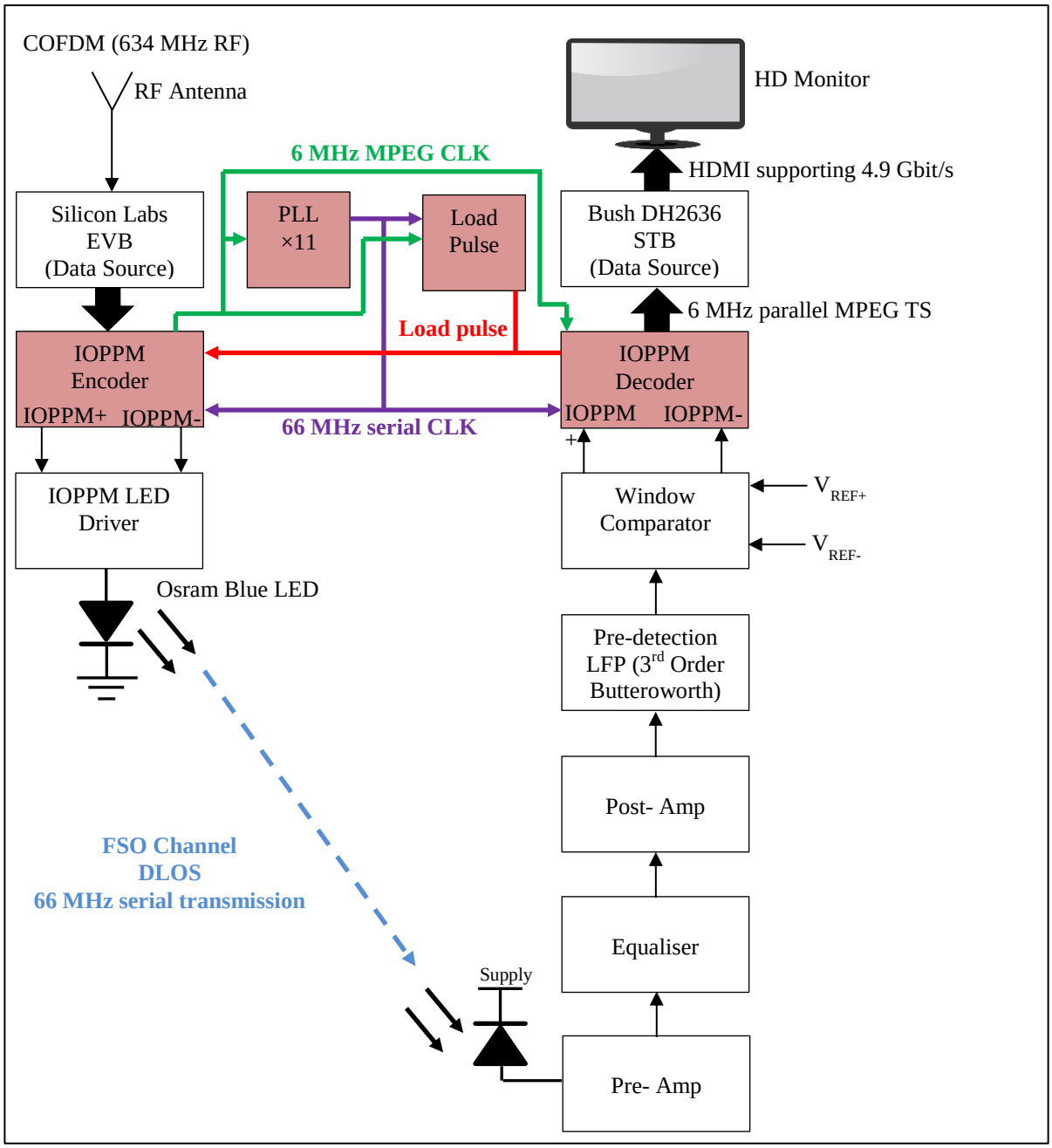


Figure 5-1 Top-level block diagram of proof-of-concept system

5.1.1 System Operation

Expansion of the block diagram shown in Figure 5-1 is necessary to explain the operation of the system in more detail. Figure 5-2 shows the expanded block diagram of the transmitter/encoder of the VLC system. In the diagram, the MPEG TS bus from the Silicon Labs EVB is input to a 1-bit buffer stage, which is used to store the 10-bits of

the MPEG TS bus, and is loaded on the rising-edge of the 6 MHz parallel MPEG TS; note that the EVB updates the MPEG TS output on every falling-edge of the MPEG TS clock (inverted clock) as established in Chapter 4, therefore, the rising-edge represents the half-cycle of the MPEG TS clock.

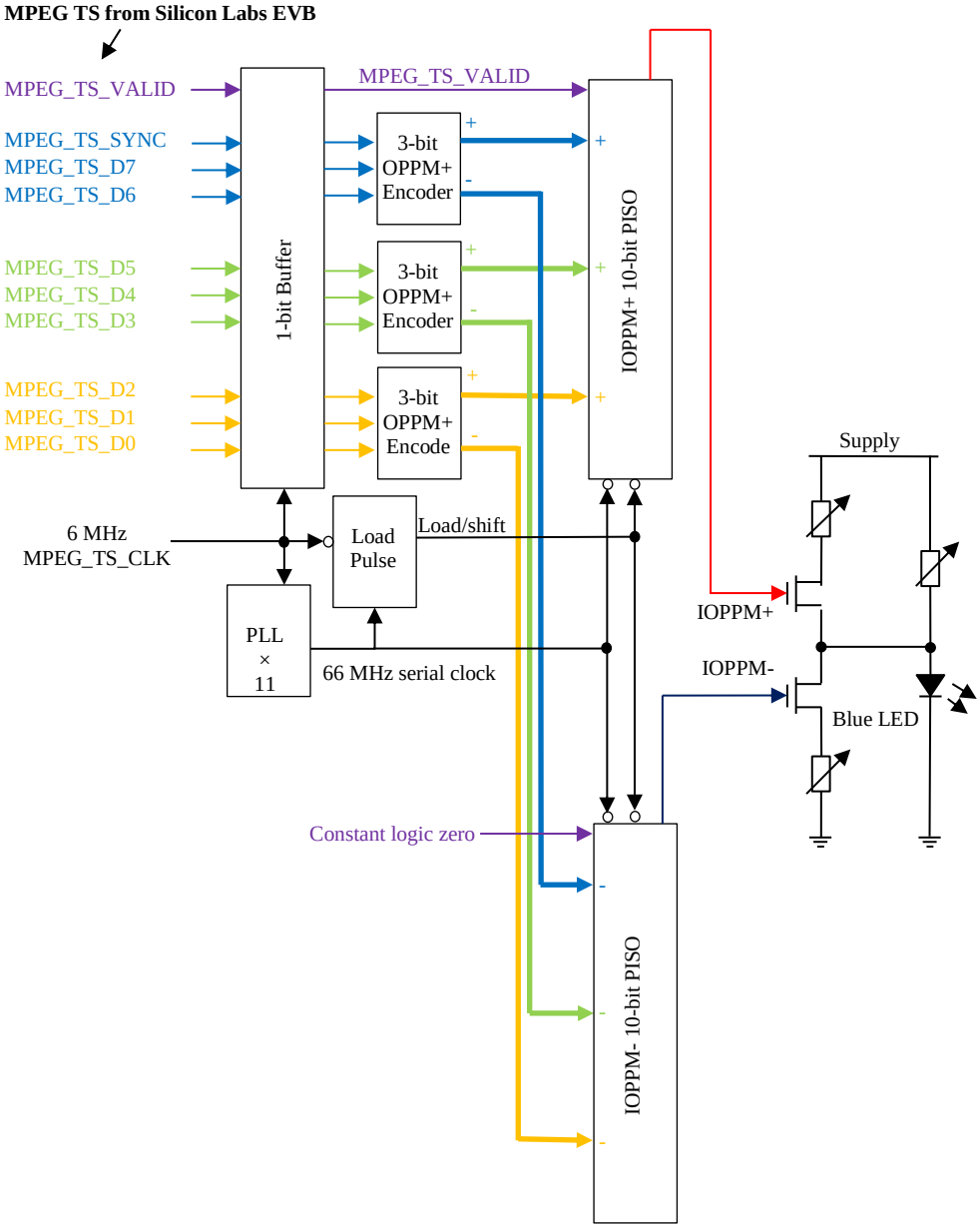


Figure 5-2 Detailed IOPPM MPEG TS encoder/transmitter architecture (Single LED)

Referring to Figure 5-2, after the buffer is clocked, the stored bits are available at the buffers output, nine of the bits are subdivided into 3-bits blocks which are presented to the IOPPM encoders: bits D0, D1 and D2 (highlighted in yellow) are presented to the first 3-bit IOPPM encoder; D3, D4 and D5 (highlighted in green) to the second; and D6, D7 and the synchronisation bit (highlighted in light blue) to the third. The valid bit (highlighted in light purple), which is not encoded since it only changes state every 31.33 μs (31.9 kHz), and is therefore directly input to the IOPPM+ PISO; note that the valid bit is not input to the IOPPM- PISO, and instead a constant logic zero is input, which maintains symmetry between the IOPPM+ and IOPPM- PISOs. Following IOPPM encoding, the IOPPM+ and IOPPM- bits are presented to the respective IOPPM+ and IOPPM- PISOs in three pairs of 3-bit buses, as shown in Figure 5-2 by the bold highlighted yellow, green and light blue paths. The load pulse signal is now required to parallel load the bits into both PISOs simultaneously.

The load pulse block generates the PISO load and shift signals using the 6 MHz parallel MPEG TS and 66 MHz serial clocks. As already mentioned, the 66 MHz clock is generated by the PLL block, which phase-locks to the 6 MHz clock, therefore the rising- and falling-edges of the 6 MHz and 66 MHz clocks coincide with each other, due to the phase-lock provided by the PLL. The load pulse block generates a logic zero output, representing the load mode for the PISO, when the falling-edge of the 6 MHz clock is detected. The pulse has a duration of 22.7272 ns, representing one and half cycles of the 66 MHz clock, and is determined by counting two rising-edges of the 66 MHz clock following the detection of the falling-edge of the 6 MHz clock. Upon detection of the second rising-edge of the 66 MHz clock, the load pulse generator is reset, and outputs a logic one, which sets the shift mode of the PISO and remains in this state until the next 6

MHz falling-edge is detected. During the shift mode, ten falling-edge clock cycles of the 66 MHz clock are used to clock out the 10-bits held in the IOPPM+ and IOPPM- PISOs; note that when the PISO bits are clocked out, the valid bit emerges from the PISO first and the D0 bit last. Figure 5-6 shows the timing of the load pulse relative to the 6 MHz and 66 MHz clocks.

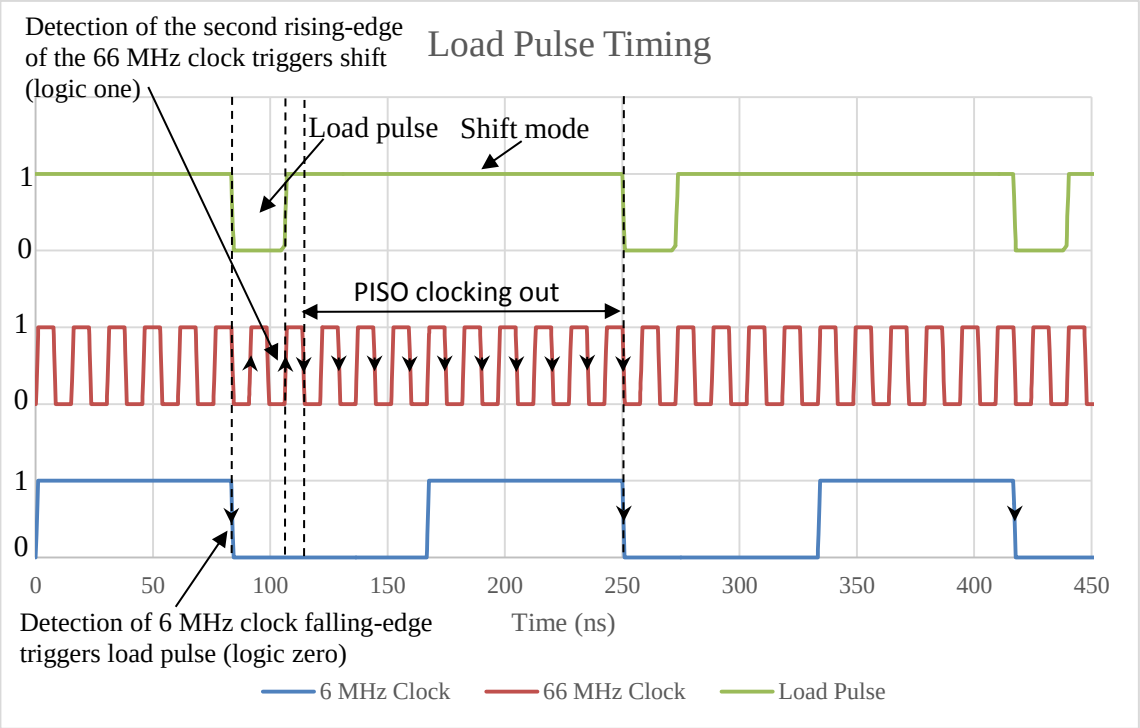


Figure 5-3 PISO load pulse timing relative to the 6 MHz and 66 MHz clocks

The clocked out bits of the PISOs are used to drive the IOPPM composite LED driver, which varies the radiant intensity of the blue LED based on the transmitted IOPPM codewords: IOPPM+ codewords increase intensity and IOPPM- codewords reduce intensity. The IOPPM composite signal generated by the LED driver circuit is transmitted over the FSO optical channel to the receiver.

The VLC systems detailed receiver/decoder block diagram is shown in Figure 5-4. At the direct-detection receiver, the composite IOPPM signal is received by the PD and the

optical transmission is converted to electrical signal in the form of a photocurrent. The PD is required to have sufficient bandwidth to receive the serialised 66 MHz IOPPM transmission.

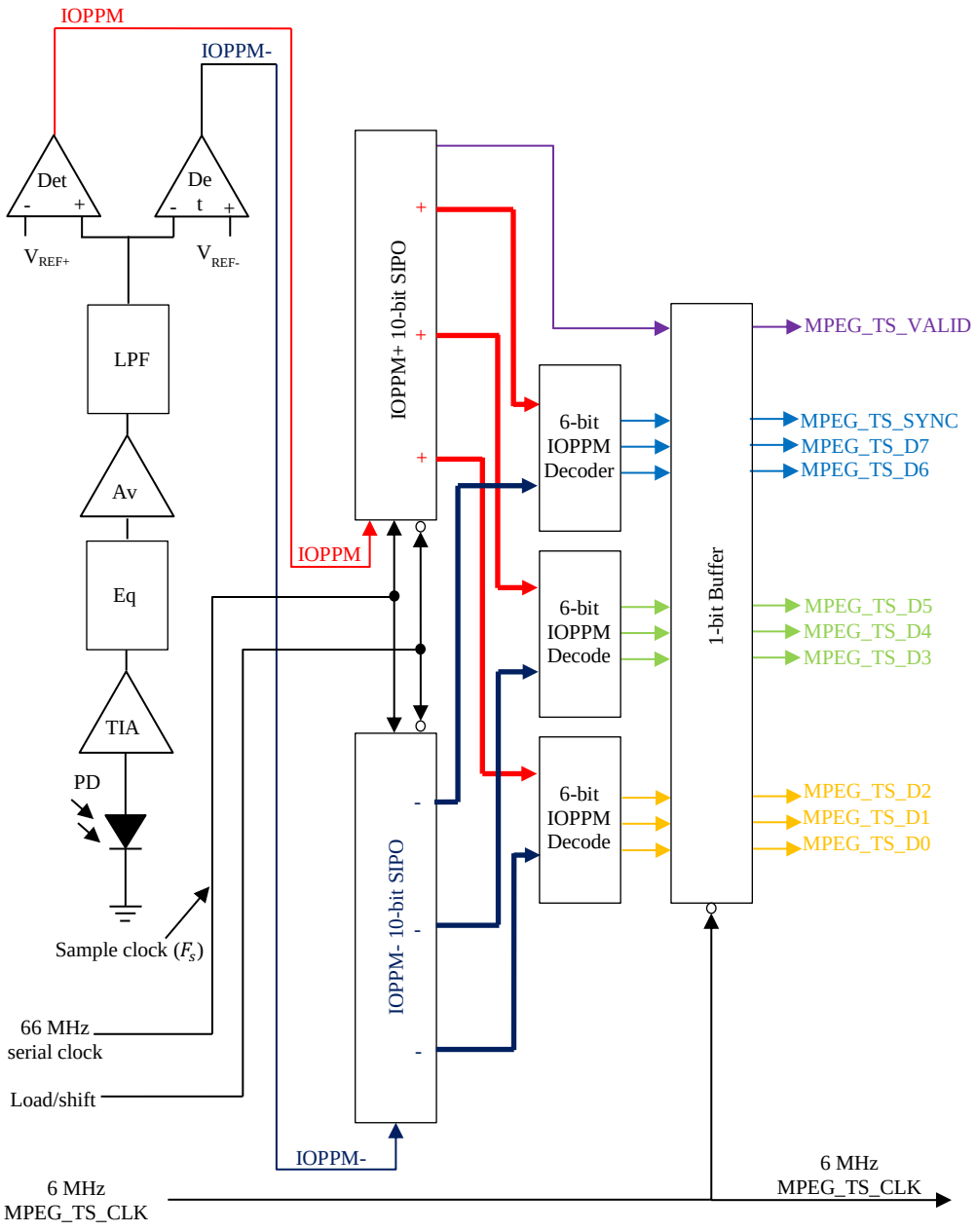


Figure 5-4 Detailed IOPPM MPEG TS receiver/decoder architecture (Single LED)

The photocurrent is amplified and converted to a voltage by the pre-amplifier (TIA), which is required to have a 3 dB bandwidth of 50% of the transmission bandwidth, as

stated in Chapter 2, section 2.6.4. Given that the transmission bandwidth is 66 MHz, the 3 dB cut-off of the pre-amplifier is 33 MHz. The pre-amplified signal is then equalised (Eq) to compensate for channel and LED roll-off using a passive, 2nd order RC equaliser circuit, as stated in Chapter 2, section 2.6.5. Following equalisation, voltage amplification (Av) is applied to the signal, which is then filtered by a 3rd order Butterworth low-pass pre-detection filter (LPF). The filter is required to have a 3 dB bandwidth of 70% of the transmission bandwidth, as stated in Chapter 2, section 2.6.7. The cut-off frequency of the filter is therefore 46.2 MHz. The IOPPM composite signal, which varies about a fixed DC point, is then detected by a window comparator (Det), which is constructed using two comparators: a non-inverting comparator to detect positive IOPPM codewords, using a crossing threshold defined by V_{REF+}; and an inverting amplifier to detect negative codewords, using a crossing threshold defined by V_{REF-}, as described in Chapter 3, section 3.1.5. The digital outputs of the comparators are then input to two SIPOs: an IOPPM+ SIPO which stores positive codewords, and an IOPPM- SIPO which stores negative codewords; note that when the SIPO bits are clocked in, the valid bit enters first and the D0 bit last. The 10-bits of the IOPPM transmission are clocked into the SIPOs using central decision detection, which is achieved using the rising-edge of the 66 MHz serial clock which is hardwired from the transmitter; note that the clock must be delayed by the same amount of propagation delay introduced by the FSO channel and receiver analogue processing stages in order to correctly align the rising-edge of the clock with the centre of the received IOPPM+ and IOPPM- bit streams– effectively, the 66 MHz clock becomes the sample clock (F_s) described in Chapter 3, section 3.1.5. The load/shift signals from the transmitters load pulse generator is also hardwired to the receiver, and must also be delayed by the same amount as the 66 MHz clock to ensure correct timing. During clocking in of the 10-bit

stream, both PISOs are in shift mode, and once all 10-bits are clocked in, the serial bits are then loaded into a parallel register when the load pulse occurs; note that the load pulse is falling-edge triggered at the PISOs. Nine positive and nine negative codewords emerging from the parallel register are input to three 6-bit IOPPM decoders, which then simultaneously decode the received codewords in order to recover the 9-bit MPEG TS; the tenth bit, which is the valid bit, is read directly out of the IOPPM+ PISO and its complementary bit in the IOPPM- PISO is unread. The 3-bit buses emerging from the decoders and colour coded identically to the IOPPM encoders at the transmitter. The 10-bit parallel MPEG TS is then clocked into the 1-bit register, using the 6 MHz parallel MPEG TS, which is also subject to the same delay correction as the 66 MHz serial clock and load/shift signal. The 1-bit register is falling-edge triggered.

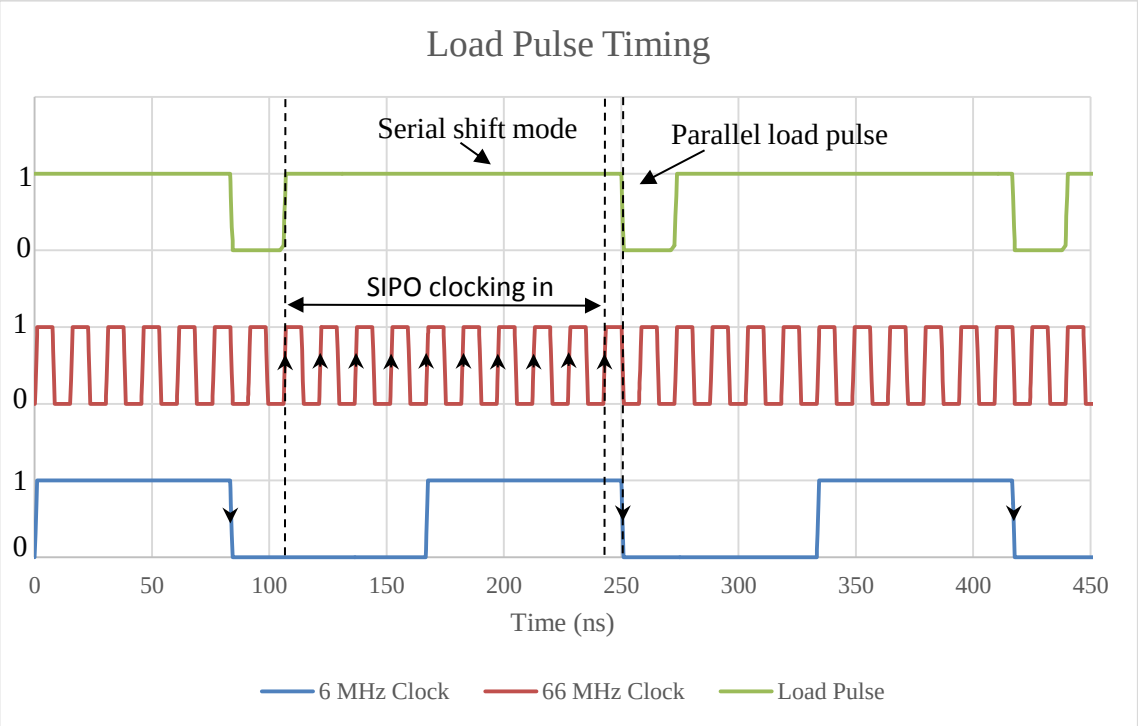


Figure 5-5 SIPO parallel load pulse timing relative to the 6 MHz and 66 MHz clocks

The 10-bit parallel MPEG TS is then clocked into the STB processor using the 6 MHz clock. Following MPEG decoding in the processor, the STB outputs content on an HDMI interface, enabling reproduction on an HD monitor.

5.2 Digital Subsystems

Having established the top-level architecture for the encoder/transmitter (Figure 5-2) and receiver decoder (Figure 5-4), and specified a number of key parameters for each subsystem, it was possible to move to the design and simulation phase. The digital circuits required by the IOPPM encoder and decoder were designed first, because these were the simplest to synthesise. Simple combination and sequential logic circuits are used throughout the digital design.

5.2.1 1-bit Buffer (Tx)

The first digital subsystem encountered in the encoder/transmitter is the 1-bit buffer which is used to store 10-bits of the MPEG TS prior to IOPPM encoding. The buffer was designed using ten D-type flip-flops, which enabled parallel loading of 10-bits of the MPEG TS on the rising-edge of the 6 MHz clock. The purpose of the buffer was to isolate the EVB MPEG TS from the IOPPM encoder. Appendix J.1 shows the circuit for the 10-bit buffer.

5.2.2 IOPPM Encoder (Tx)

The IOPPM encoder was designed using the Karnaugh mapping techniques. The resultant SOP 3-bit encoder equations are shown below.

IOPPM + terms:

$$Y_0(D_2, D_1, D_0) = \sum(\overline{D_2}.\overline{D_1}.D_0 + D_2.\overline{D_1}.\overline{D_0}) \qquad \text{Equation B.1-1}$$

$$Y_1(D_2, D_1, D_0) = \sum(\overline{D_2}.D_1.\overline{D_0}) \qquad \text{Equation B.1-2}$$

$$Y_2(D_2, D_1, D_0) = \sum(\overline{D_2}.\overline{D_1}.\overline{D_0} + \overline{D_2}.D_1.D_0) \qquad \text{Equation B.1-3}$$

IOPPM- terms:

$$Z_0(D_2, D_1, D_0) = \sum(\overline{D_2}.\overline{D_1}.\overline{D_0} + D_2.\overline{D_1}.D_0) \qquad \text{Equation B.1-4}$$

$$Z_1(D_2, D_1, D_0) = \sum(D_2.D_1.\overline{D_0}) \qquad \text{Equation B.1-5}$$

$$Z_2(D_2, D_1, D_0) = \sum(D_2.\overline{D_1}.\overline{D_0} + D_2.D_1.D_0) \qquad \text{Equation B.1-6}$$

The equations were used to synthesis the 3-bit encoder combinational logic circuit shown in Figure 5-6.

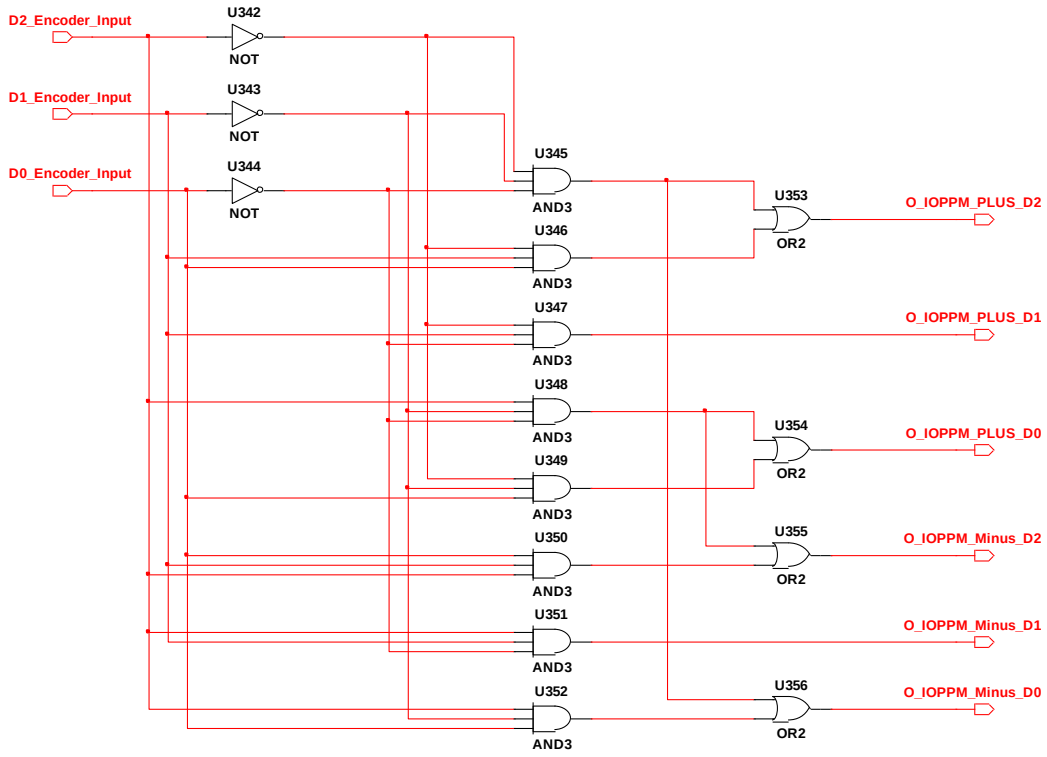


Figure 5-6 3-bit IOPPM encoder

The circuit use three inverters, eight AND gates, and four OR gates. The circuit was optimised for minimum gate count using Karnaugh mapping techniques. This circuit is used in each of the three, 3-bit encoders shown in Figure 5-2, resulting in a complete encoder gate count of forty five gates. The complete design, optimisation and simulation of the encoder is shown in Appendix B.

5.2.3 10-bit PISO (Tx)

Serialisation of the IOPPM+ and IOPPM- streams was achieved using two, 10-bit PISOs constructed using D-type flip-flops which are clocked on the falling-edge of the 66 MHz clock. In addition, combinational logic circuits, connecting the cascaded flip-flops together, provided selection of the load and shift operations; the PISO circuit is shown in Appendix J.2. The load (trigger by logic zero) and shift (trigger by logic one) mode of the PISO were selected using the signal generated by load pulse block shown in Figure 5-2. The load pulse circuit was designed to detect and count the edges of the 6 MHz MPEG TS clock and the 66 MHz serial clock and at the appropriate moment load the PISOs. The circuit, shown in Figure 5-7, is constructed using two, 2-bit counters, one of which is used to detect and count a single falling-edge of the 6 MHz MPEG clock, and a second which detects and counts two rising-edges of the 66 MHz serial clock. As discussed in section 5.1.1, the load pulse is necessary to load the parallel output of the IOPPM encoders into the PISO, and then trigger the serial clock-out of the 10-bits.

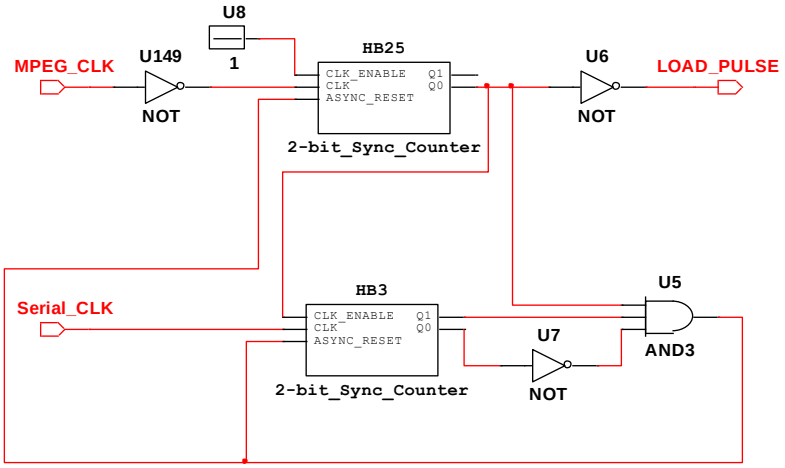


Figure 5-7 Load pulse generator

The load pulse circuit operation is explained using the circuit diagram of Figure 5-7 and the timing diagram shown in Figure 5-8. The initial condition of the circuit is defined following an asynchronous reset of both 2-bit counters, after which all counter outputs are set low. The LOAD_PULSE output is set high by the inverter at the output of the 6 MHz counter (HB25). The output of the AND gate (U5), the input of which is connected to Q1 of the 66 MHz counter (HB3), is set low. Both counters are no longer held in reset because the asynchronous reset pins of both counters are low, set by the output of the AND gate (U5). The 6 MHz counter clock is enabled, since its clock enable pin is set permanently high. The 66 MHz counter is disabled, since its clock enable pin is set low by the Q0 output of the 6 MHz counter. With the 6 MHz clock applied to the MPEG_CLK input, and the 66 MHz clock to the Serial_CLK input, at time ‘A’, shown in the timing diagram, the falling-edge of the 6 MHz causes the 6 MHz clock counter (HB25) to increment by one, resulting in the Q0 output going high and the LOAD_PULSE output going low. The PULSE_LOAD change from high to low is indicated at time ‘B’. Since Q0 output of the 6 MHz counter is now high, the clock enable of the 66 MHz clock is also high, enabling the counter. At time ‘C’, the first

rising-edge of the 66 MHz clock is detected and the 66 MHz counter increments by one, so the counters Q0 output goes high, whilst its Q1 remains low; the output of the AND gate (U5) also remains low. At time ‘D’, the second rising-edge of the 66 MHz clock is detected, and the 66 MHz counter increments again, resulting in its Q0 going low and Q1 going high. Since all the inputs to the AND gate (U5) are now high, the output of the gate also goes high, and applies an asynchronous reset to all the counters. The PULSE_LOAD now reverts back to logic high, and between the times ‘E’ and ‘F’, the PISO serially clocks out the 10-bits on the falling-edge of the 66 MHz clock, until the next falling-edge of the 6 MHz clock occurs, at which point the pulse load generators cycle repeats. The load pulse has a total period of 22.7272 ns, since it covers one and half cycles of the 66 MHz clock.

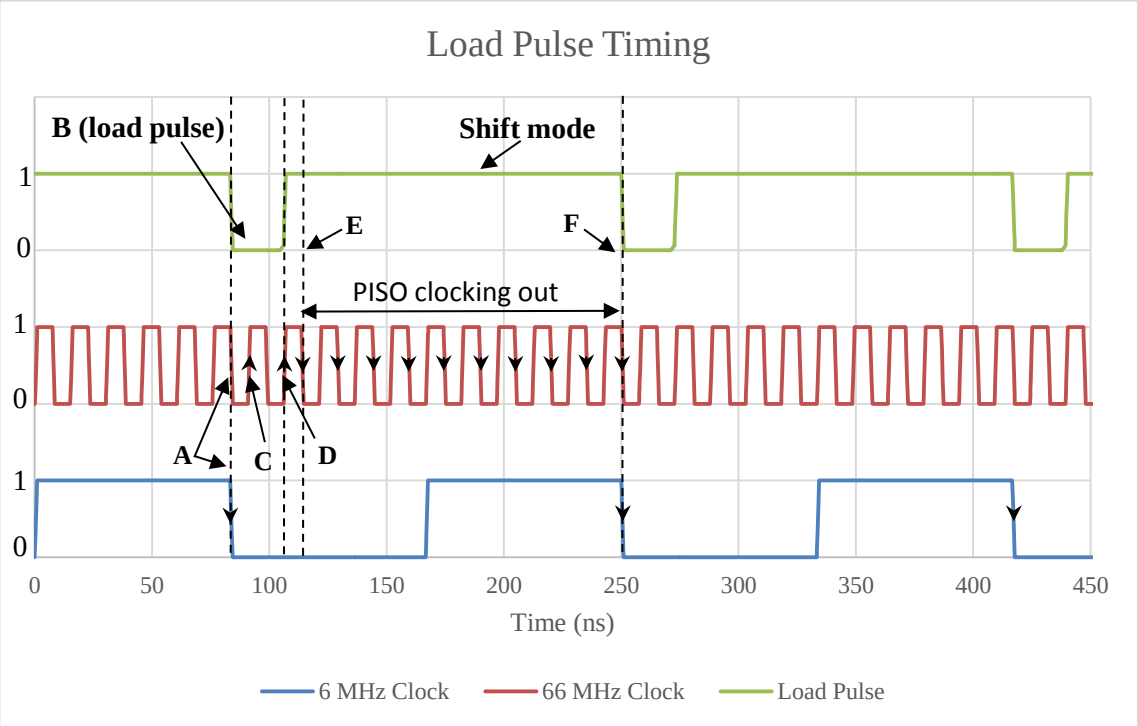


Figure 5-8 PISO load pulse timing relative to the 6 MHz and 66 MHz clocks

The pulse load block is a simple circuit, but is critical to the timing of the VLC system, in particular the slot time of the IOPPM codewords, which must be maintained at 15.1515 ns to reduce the effects of ISI.

5.2.4 10-bit SIPO (Rx)

At the receiver, following detection of the IOPPM+ and IOPPM- streams, the two independent streams are clocked into the SIPOs by the rising-edge of the 66 MHz clock. The circuit is constructed using ten D-type flip-flops which serially shifts in and stores a 10-bits IOPPM frame. Upon clocking-in the tenth bit, a parallel-in parallel-out (PIPO) circuit, which is also constructed using ten D-type flip-flops, is used to de-serialise the 10-bit frame. Load and shift selection is applied to the PIPO, which is performed by the load pulse signal generated in the transmitter and hardwired to the receiver. Figure 5-9 shows the block diagram of the IOPPM+ and IOPPM- SIPOs and PIPOs. The SIPO blocks are shown containing ten bits, represented by b0 through b9, and which have been serially shifted simultaneously into the SIPOs using the rising-edge of the 66 MHz clock, where b9 was the first bit shifted in to the SIPO and b0 was the last. The shift and load timing is shown in Figure 5-10, where the bit timings are shown for b0 through b9, relative to the 66 MHz and 6 MHz clocks and the load pulse waveform. The timing diagram shows that on the rising-edge of the 66 MHz clock, bit b9 is the first bit clocked into the SIPO and bit b0 is the last. Following the rising-edge that clocks in b0, the load pulse goes low, triggering the parallel load of the PIPO, at which point the PIPO output is available to the IOPPM decoder. The SIPO shifting cycle repeats when the load pulse goes high and the first rising-edge of the 66 MHz clock occurs. The transmitter and receiver IOPPM 10-bit frame synchronisation is set by the load pulse, the 66 MHz and 6 MHz clock.

The SIPO serial shift and parallel load (PIPO) circuits are shown, respectively, in Appendix J.3 and J.4.

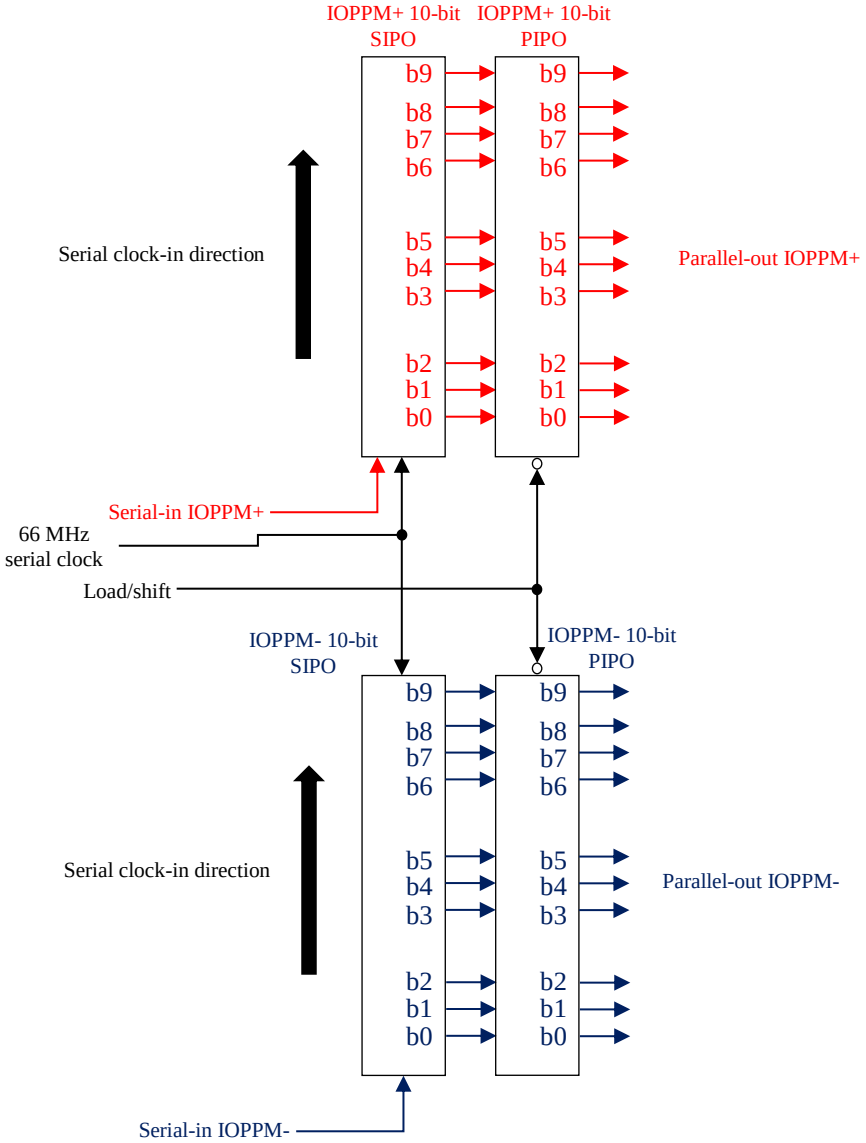


Figure 5-9 SIPO and PIPO block diagram

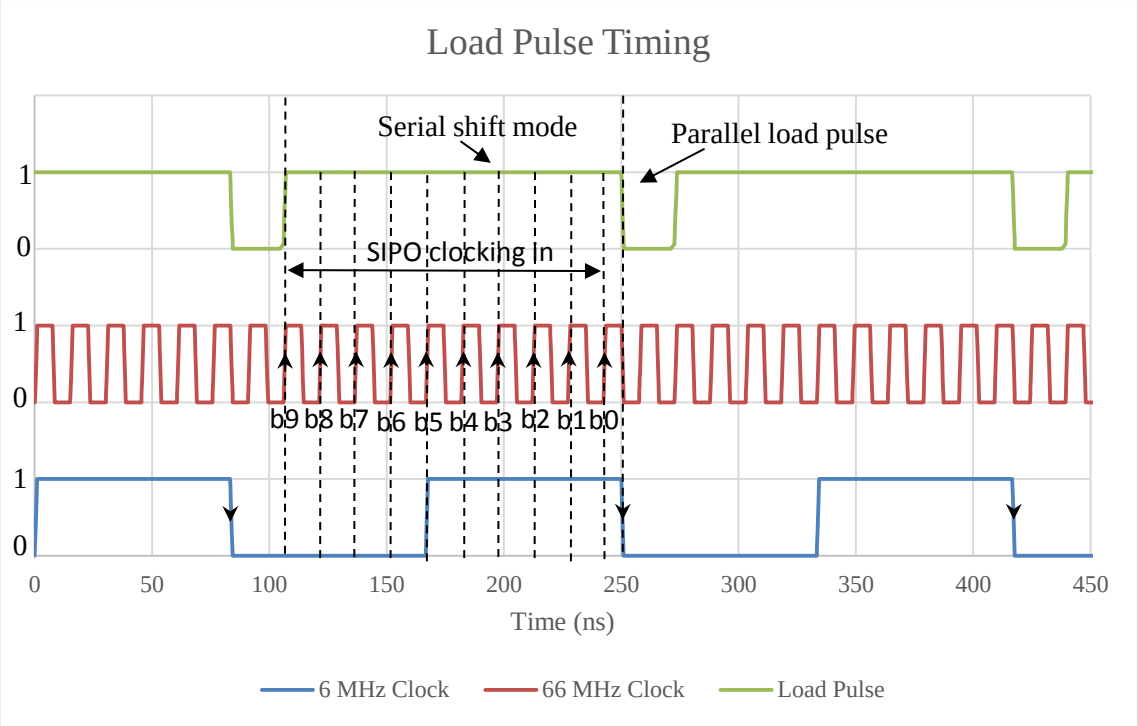


Figure 5-10 SIPO/PIPO parallel load pulse timing relative to the 6 MHz and 66 MHz clocks

5.2.5 IOPPM Decoder (Rx)

The IOPPM decoder was also designed using the Karnaugh mapping techniques. The resultant SOP 6-bit decoder equations are shown below.

$$D_0(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.Z_0 + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.Z_2.\overline{Z_1}.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.Y_0.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} + \\ Y_2.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} \end{pmatrix} \qquad \text{Equation B.5-7}$$

$$D_1(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.Z_1.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.Z_2.\overline{Z_1}.\overline{Z_0} + \\ \overline{Y_2}.Y_1.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} + \\ Y_2.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} \end{pmatrix} \qquad \text{Equation B.5-8}$$

$$D_2(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.Z_0 + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.Z_1.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.Z_2.\overline{Z_1}.\overline{Z_0} \end{pmatrix}$$ Equation B.5-10

The equations were used to synthesis the 6-bit decoder combinational logic circuit shown in Figure 5-11.

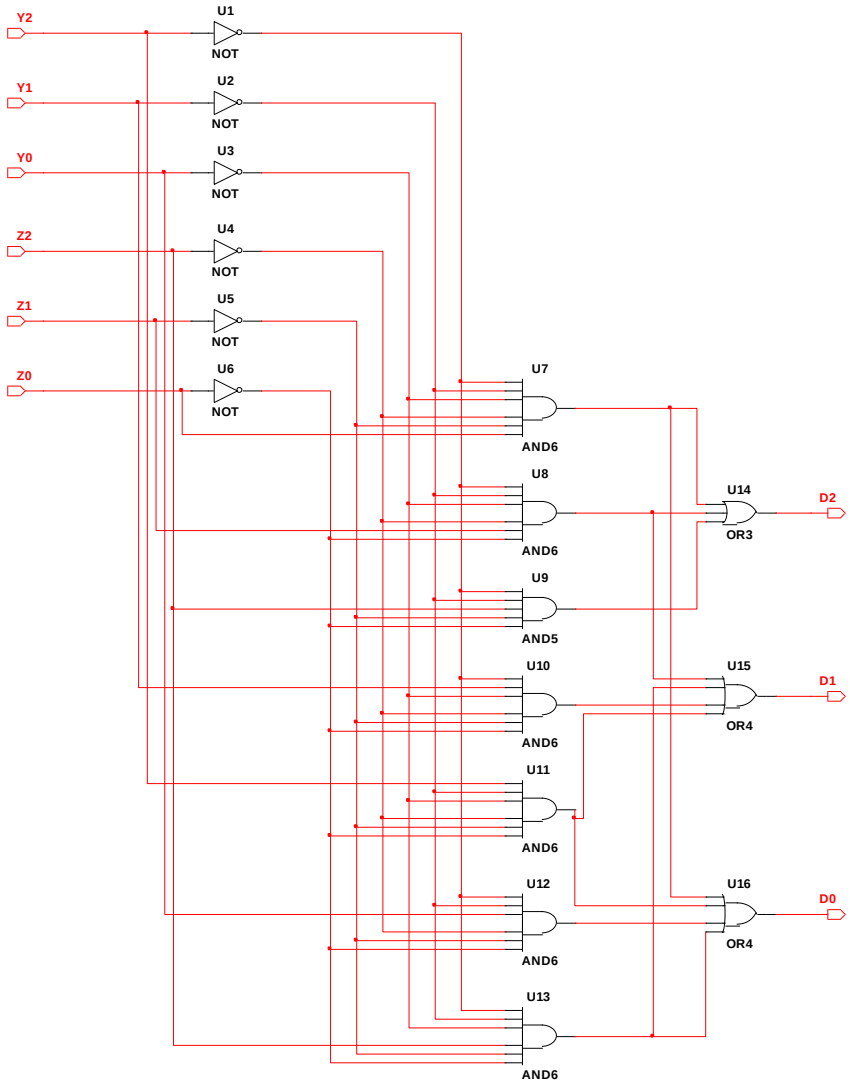


Figure 5-11 6-bit IOPPM decoder

The circuit use six inverters, seven AND gates, and three OR gates. The circuit was optimised for minimum gate count using Karnaugh mapping techniques. This circuit is used in each of the three, 6-bit decoders shown in Figure 5-2, resulting in a complete

decoder gate count of forty eight gates. The complete design, optimisation and simulation of the encoder is shown in Appendix B.

5.2.6 1-bit Buffer (Rx)

Following IOPPM decoding, the parallel MPEG TS is loaded into a 1-bit buffer which is identical to the one used in the first stage of the encoder/transmitter. Again, the buffer is used to store 10-bits of the MPEG TS prior following IOPPM decoding and was designed using ten D-type flip-flops. However, the parallel unloading of 10-bits onto the MPEG TS bus of the STB is performed on the falling-edge of the 6 MHz clock, instead of the rising-edge in the encoder/transmitter. Again, the purpose of the buffer was to isolate the IOPPM decoder from the STB. Appendix J.1 shows the circuit for the 10-bit buffer, but the inverter required to provide falling-edge clocking is not shown.

The circuits described in this section were later transferred into the Altera Quartus II IDE so that they could be implemented on an FPGA platform.

5.3 Analogue Subsystems

The analogue subsystems were designed and simulated, where possible, using commercially available devices which had readily available SPICE models. This approach was taken to ensure ease of transition from simulated circuits to physical hardware implementations, and to improve the correlation between simulated and physically measured results. The receiver chain was designed using an unbalanced characteristic impedance of 50Ω, and device supply rails of 5V and 3V since these rails are common in real-world STB platforms.

5.3.1 IOPPM Composite LED Driver (Tx)

The IOPPM composite LED driver was designed using two FDG1024NZ dual N-channel MOSFET devices (ON, 2010). An ISL55110 dual high speed MOSFET driver (Renesas, 2015) was used in conjunction with the FDG1024NZ devices to provide the required V_{GS} drive voltages. The FDG1024NZ and ISL55110 were simulated using the manufacturers SPICE models.

The FDG1024NZ was selected as the switching device in the LED driver, due to its fast 1.5 ns rise- and fall-times, and also because of its low $R_{DS\,ON}$ (175 mΩ) and high I_D (1.2 A) when operated with at a V_{GS} of 5 V.

The ISL55110 driver was selected to enable interfacing with LVCMOS logic (3V) output of the FPGA implemented IOPPM encoder, and also because it could provide the necessary V_{GS} (5 V) drive voltage required by the gates of the FETs. Furthermore, the drivers 1.4 ns rise- and fall-times facilitates the generation of pulses with 6 ns duration, which is significantly shorter than the 15.1515 ns pulses generated by the IOPPM encoder.

The circuit topology of the IOPPM composite LED driver is shown in Figure 5-12, and is based on the circuit introduced in Chapter 3, section 3.1.4. The circuit of Figure 5-12 also shows the dual FET driver circuit, which provides interfacing between the IOPPM encoder implemented in an FPGA and the gates of the IOPPM drivers FETs. The FET driver has two supply voltages: $V_{Digital}$ and V_{FET}. The $V_{Digital}$ supply is used to power the digital circuitry of the driver, and the V_{FET} supply is used to drive the FETs. The circuit effectively translates 0V to 3V LVCMOS logic levels to 0 V to 5 V to drive the FETs. The IOPPM composite driver is shown to the right of the FET drive and consists

of an LED and two FET devices represented by Q1 and Q2. Q1 is used to injected current into the LED via R1, when 5 V (logic high) is applied to its gate, and Q2 is used to divert current from the LED to ground via R2, when 5 V (logic high) is applied to its gate; note that Q1 and Q2 are never switched on simultaneously as specified by the IOPPM coding scheme. In effect, when Q1 is switched on, the radiant intensity of the LED emission increases and when Q2 is switched on it reduces.

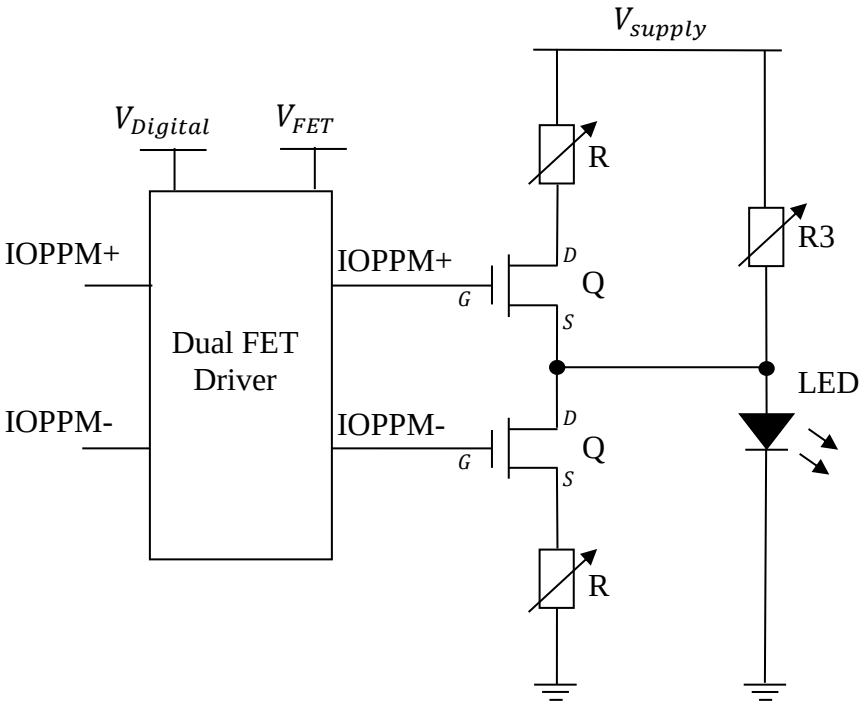


Figure 5-12 IOPPM composite LED driver

The radiant intensity of the LED emission is thus determined by IOPPM+ and IOPPM- codeword pulses applied to the gates of the FETs. When both Q1 and Q2 are switched off, the LED radiant intensity is determined by R3 which sets the quiescent forward bias current of the LED. Figure 5-13 illustrates the forward bias current applied to the LED when IOPPM codewords 100_{IOPPM+} and 100_{IOPPM-} are input to their respective FETs. At t_1, Q1 is off and Q2 is on, causing the bias current to the LED to be bypassed to ground

via R2 – effectively switching the LED off - as shown by the blue pulse in the bias plot shown to the right of the driver circuit. At t_2, both Q1 and Q2 are off and the bias to the LED is set by R3 at 13 mA (quiescent current), as shown by the green line in the bias plot. At t_3, Q1 is on and Q2 is off, causing the bias current to increase to 26 mA, due to the currents flowing through R1 and R2 to sum at the junction with the LED, as shown by the red pulse in the bias plot.

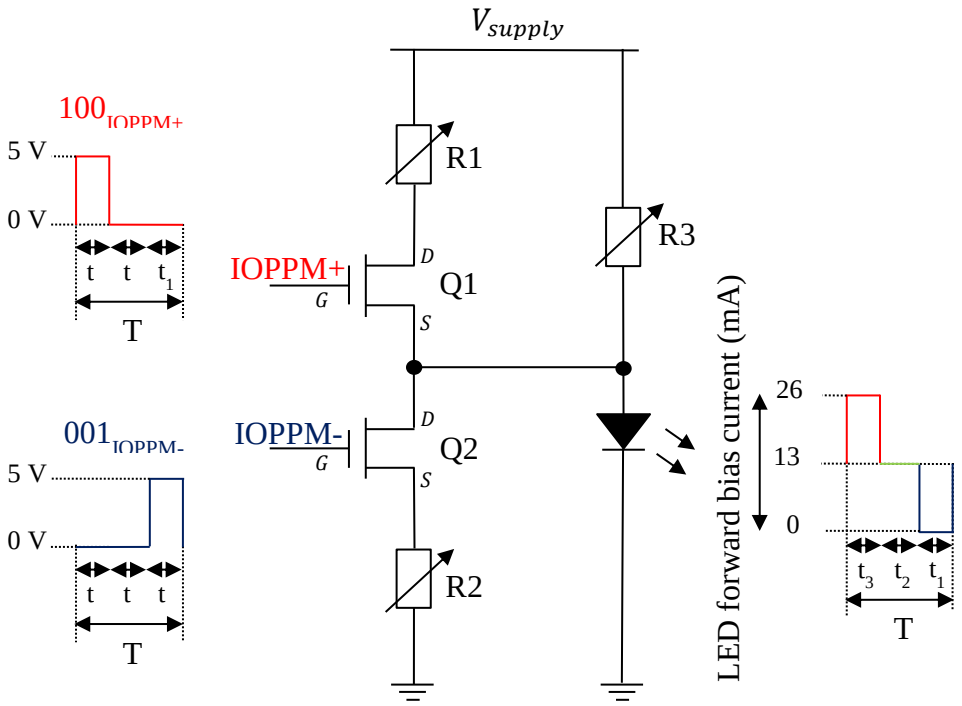


Figure 5-13 IOPPM LED composite driver (codeword versus driver current)

The quiescent current of the blue LED was set by the lowest bias current of 13 mA, which was determined by characterisation presented in Chapter 4. This bias setting was selected because the LED consumed the least power at this setting, and also because the lower power consumption increases lifetime of the LED. The LED was simulated using the model presented in Chapter 2, section 2.6.2, and circuit of which is shown in Figure 5-14. The electrical circuit parameters of the device were determined by overlaying the

measured frequency response of the blue LED (13 mA bias applied) with the modelled response, and adjusting the circuit parameters of the model until the two responses coincided, as shown in Figure 5-15. The measured (red trace) and modelled (blue trace) responses closely match, with a deviation of ±1 dB. The sharp roll-off of the blue LEDs measured response at DC is attributed to the 1 nF DC blocking capacitor used in the measurement setup, and is not present during normal biasing and switching of the device. The approximate modelled values for the blue LED were: series resistance (R2) = 0.9 Ω, inductance (L1) = 24 nH and diode capacitance (C1) = 4 nF.

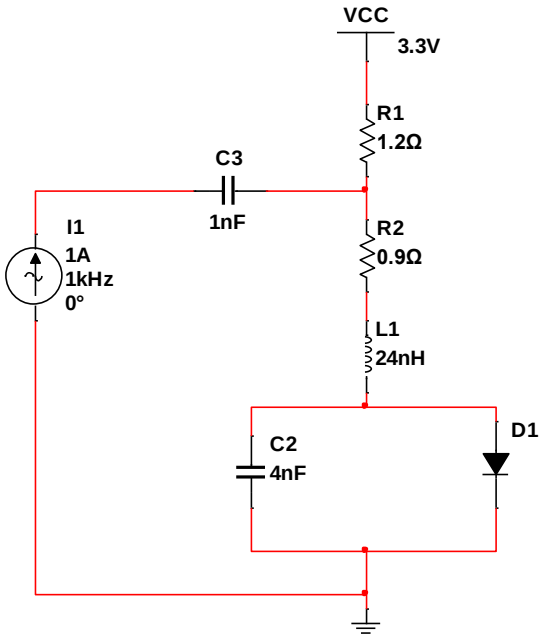


Figure 5-14 Osram Blue LED model

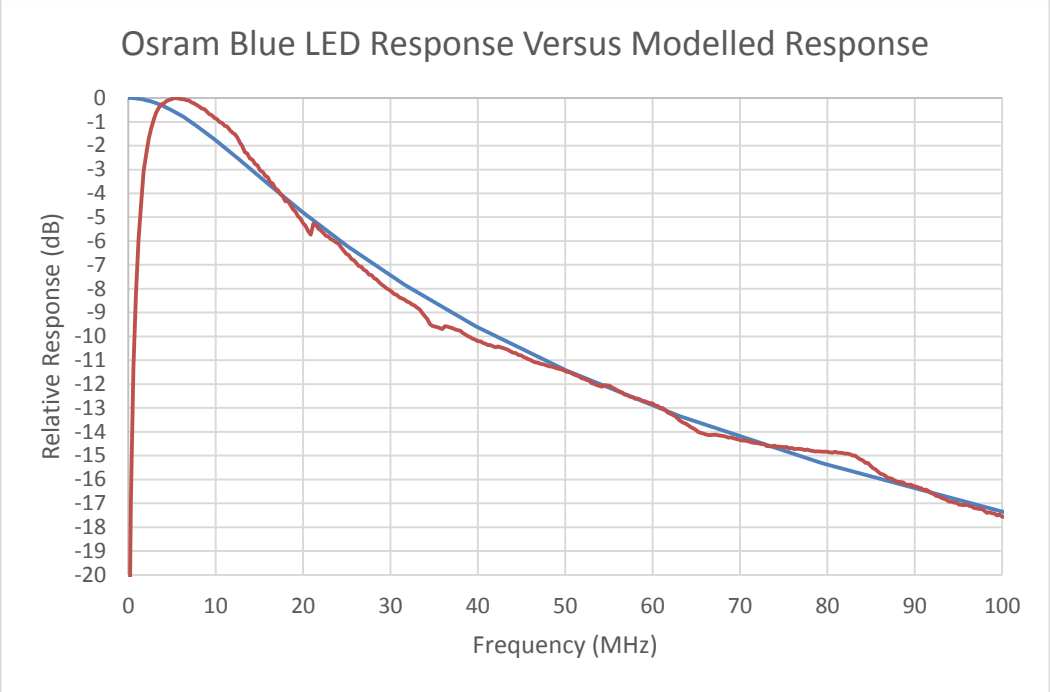


Figure 5-15 Osram Blue LED measured response versus modelled response

Using the IOPPM composite circuit and LED circuit models to perform circuit simulation, it was possible to determine the quiescent operating point and switching limits for IOPPM+ and IOPPM- codewords. Referring Figure 5-12, and starting with the quiescent bias current, which occurs when the when 0 V (logic low) is applied to the gate of both FETs, the forward bias current of 13 mA was achieved with a supply voltage (V_{supply}) of 3V3 and R3 value of 54 Ω, where the forward bias voltage of the LED was at 2.6 V; note that at the quiescent point, the LED consumes a total power of 34 mW. The IOPPM switching limits were then defined. IOPPM+ logic high pulses (5 V) were set to provide an increase in the LED forward bias current from 13 mA to 26 mA, effectively doubling the bias, and the IOPPM- logic high pulses (5 V) were set to reduce the bias from 13 mA to 0 mA, effectively turning the LED off. In order to achieve the 26 mA LED bias for IOPPM+ pulses, R1 was set at 40 Ω, so that when Q1 is switched on, R1 and R3 are connected in parallel resulting in a total resistance of 23

Ω and a 13 mA increase in current through the LED; note that the forward bias current of the LED increased to 2.65V. Conversely, to switch the LED off for IOPPM- pulses, R2 was set at 80 Ω which reduced the current through the LED to 1 μA and the forward bias voltage across the LED to 1.9 V. The transconductance of the IOPPM+ and IOPPM- switches is calculated at 2.6 mS, based on a 5 V peak pulse V_{GS} voltage and I_{DS} of 13 mA. The switching parameters were set to provide symmetrical pulses centred on the quiescent current of the LED, and thereby achieve symmetry about the DC term at receiver. This was to ensure that the composite waveform was centred correctly in the window comparator to enable balanced detection.

Figure 5-16 shows the IOPPM composite LED circuit with the key devices and component values identified. This circuit was used in the first iteration of the VLC systems hardware implementation.

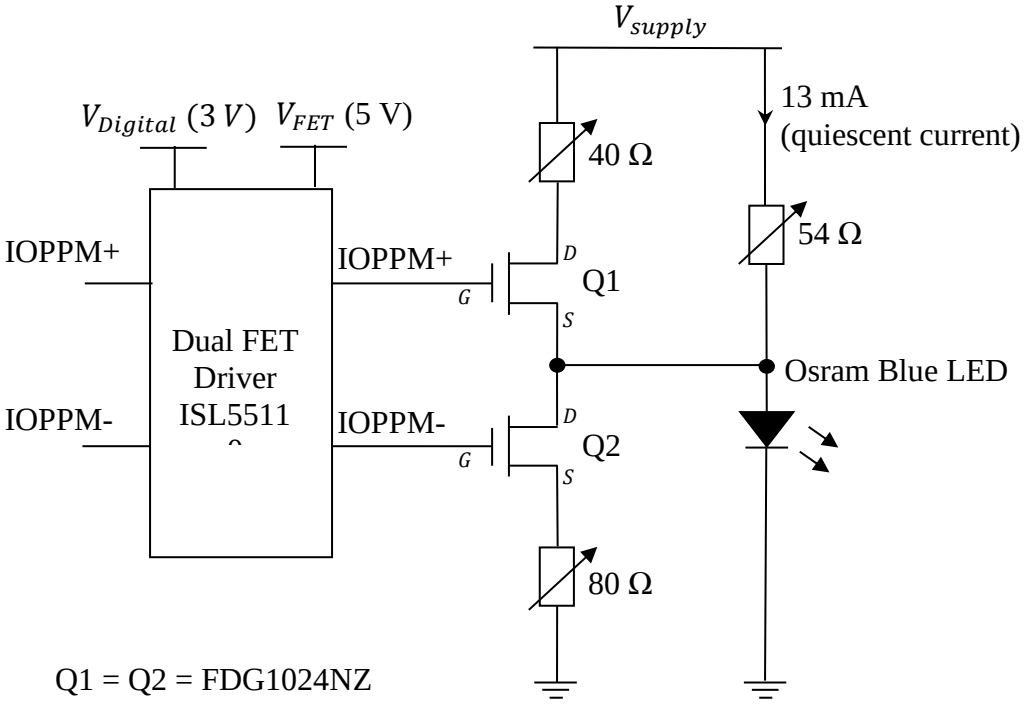


Figure 5-16 IOPPM composite LED driver circuit and component values

5.3.2 Pre-Amplifier (Rx)

The receivers PD and pre-amplifier was designed using a combination of simulation and empirical measurements of a prototype circuit. The prototype was designed using a Vishay Semiconductors BPV10 silicon PIN PD (Vishay, 2011) and a Texas Instruments (TI) OPA847 wideband operational amplifier (op-amp) (TI, 2019). The BPV10 device was selected because of its wide 250 MHz bandwidth, which was enabled by its small detection surface area of 0.78 mm, and operating the device with a 12V reverse voltage (V_R) to provide a diode capacitance (C_D) of 3pF. The device also exhibited a fast, 2.5 ns rise- and fall-times, and had a half sensitivity angle of ± 20° that limited multipath effects. The device also generated a very small, 5nA dark current. The TI OPA847 op-amp was selected because of its high gain bandwidth product (GBP) of 3.9 GHz, its low input noise voltage and current (0.85 $nV/\sqrt{Hz}$, 3 $pA/\sqrt{Hz}$), and its fast, 1.2 ns rise- and fall-time. The OPA847 was modelled using the manufacturers SPICE model.

The op-amp was configured as a transimpedance amplifier, as defined in Chapter 2, section 2.6.4, the circuit topology of which is shown in Figure 5-17. The gain and frequency response of the circuit is defined by the op-amps GBP; the feedback resistor (R_f), which sets the transimpedance gain; and the PDs diode capacitance (C_D) in parallel with op-amps internal common-mode (C_{CM}) and differential-mode (C_{DM}) parasitic input capacitances; effectively all three capacitances are summed. These parameters are used to determine the feedback capacitor, C_f, and ultimately the frequency response of the op-amp (TI, 2019).

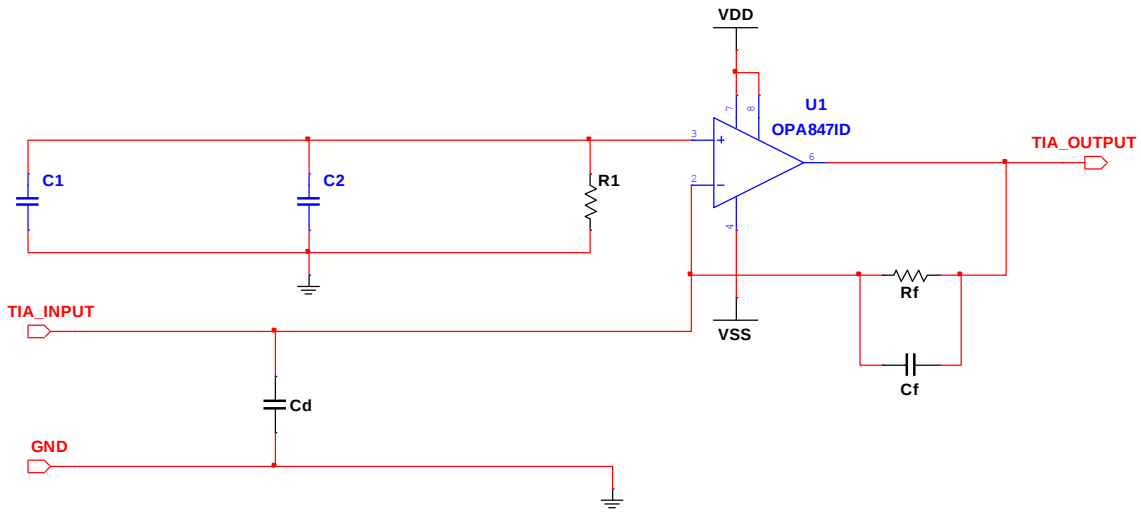


Figure 5-17 TI OPA847 op-amp transimpedance amplifier

The circuit shown Figure 5-17 generates a 2nd-order Butterworth, maximally flat, frequency response, which is set by the feedback pole determined by expression on the right-hand-side of Equation 2-40 (Chapter 2).

$$\frac{1}{2\pi R_f C_f} = \sqrt{\frac{GBP}{4\pi R_f (C_D + C_{CM} + C_{DM})}} \quad (Hz) \qquad \text{Equation 2-40}$$

Where GBP is 3.9 GHz, C_{CM} is 1.2 pF and C_{DM} is 2.5 pF, as stated in the OPA847 op-amps data sheet (TI, 2019), and C_D is 3 pF as stated in the BPV10 data sheet (Vishay, 2011). The value of R_f, and also R_1 which is equal to R_f, was chosen arbitrarily by the author at 12 kΩ. Using these component values, the pole is located at approximately 62 MHz. The feedback capacitance required to set the pole is now calculated by substituting the pole location into the right-hand-side of Equation 2-40 and transposing for C_f, which results in a capacitance of 0.214 pF. Since 0.214 pF is very close to the parasitic capacitance of a SMD package, which is approximately 0.2 pF (TI, 2019), the

parasitic capacitance of the feedback resistor provides both feedback resistance and capacitance in the hardware implemented circuit.

The transimpedance gain of the amplifier, where R_f is set to 12 kΩ, is 81.6 dBΩ, as defined by Equation 5-1.

$$G = 20\log(R_f)\,(dB\Omega) \qquad \text{Equation 5-1}$$

The 3 dB bandwidth of the amplifier is approximately 88 MHz as defined by Equation 5-2.

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_f(C_D + C_{CM} + C_{DM})}}\,(Hz) \qquad \text{Equation 5-2}$$

The amplifier circuit, including component values and positive and negative 5 V supply rails is shown in Figure 5-18.

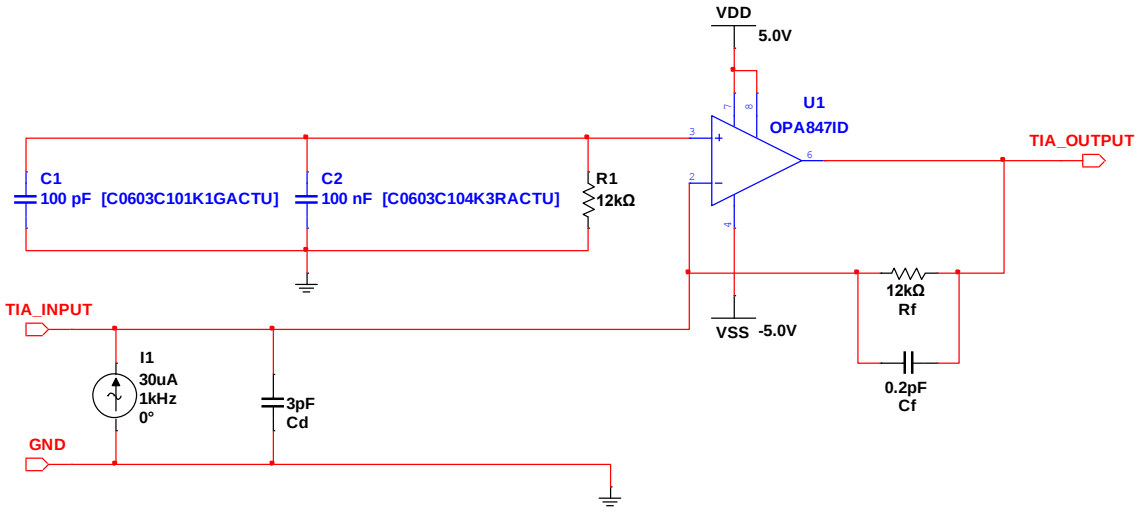


Figure 5-18 TI OPA847 op-amp transimpedance amplifier circuit (component values)

The circuit of Figure 5-18 was simulated and generated the response shown in Figure 5-19.

The transimpedance gain of the circuit is 81.6 dBΩ from 1 Hz to approximately 10 MHz, and then peaks at 86.5 dBΩ around 47 MHz. The 3 dB bandwidth occurs at 84 MHz, which is 4 MHz lower than the design calculation predicted, and is possibly due to slightly higher parasitic capacitances used in the OPA847 SPICE model.

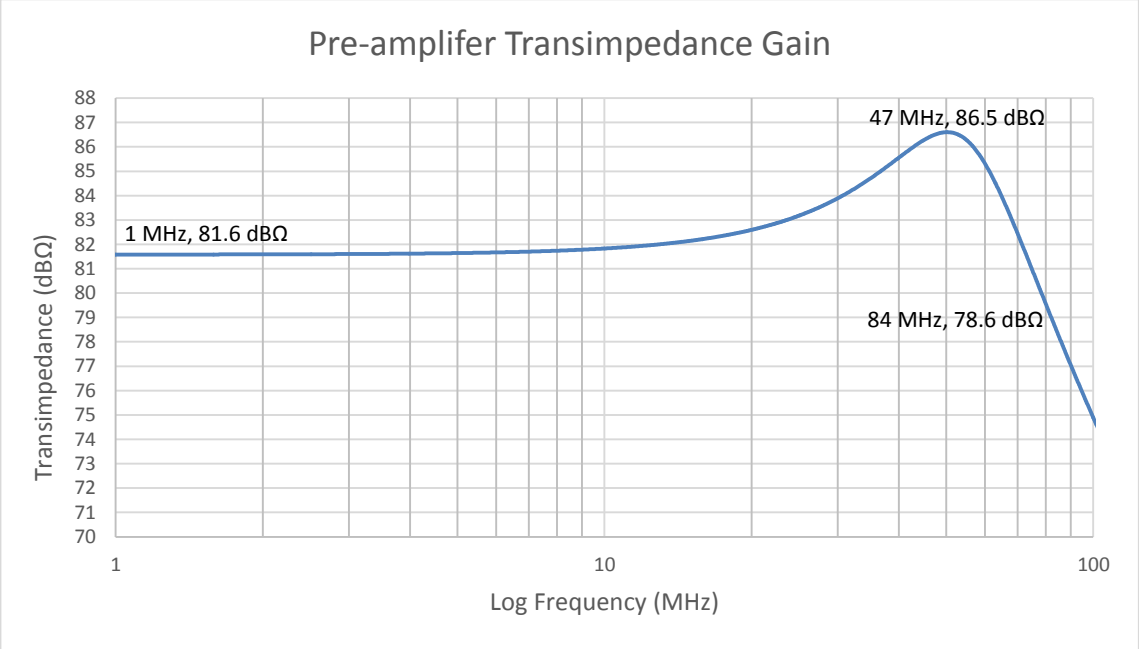


Figure 5-19 TI OPA847 op-amp transimpedance amplifier gain response

Using the OPA847 based pre-amplifier circuit shown in Figure 5-18 and the BPV10 PD, a prototype circuit was built and tested in order to characterise the cascaded behaviour of the pre-amplifier and the PD. The physical implementation of the prototype circuit is shown in Figure 5-20. The PD and op-amp are labelled, as well as the -12 V rail used to bias the PD to achieve the 3 pF capacitance, and the positive and negative 5 V rails used to power the op-amp. The +5 V is derived from LDO regulator fed with a +12 V supply rail.

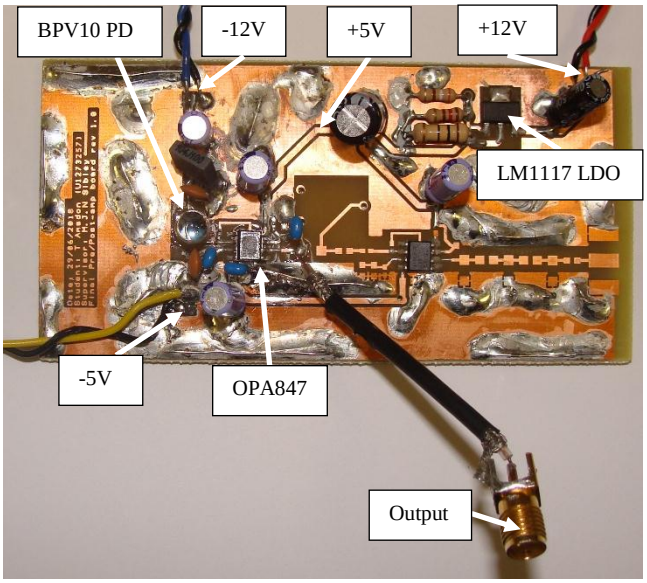


Figure 5-20 BPV10 PIN PD and TI OPA847 pre-amplifier prototype

The prototype circuit was tested using the frequency response and bandwidth test setup and conditions described in Appendix I.1; note that the Thorlabs PDA10A-EC Si amplified PD was replaced with the prototype circuits BPV10 PD as the photo-detecting device. The Osram blue LED, biased at 13 mA, was used as the optical source during testing. The incident optical power measured at the PD detector surface, prior to performing the frequency response measurement, was approximately 0.6 mW.

The resultant frequency response of the cascaded PD and pre-amplifier is shown in Figure 5-21. The response is presented in decibel-milliwatts (dBm), absolute power, measured in a 50 Ω system. The high-frequency roll-off of the LED and channel is evident in the response, and indicates the need for positive slope equalisation following the pre-amplification stage. Based on the design calculation, simulation and measured performance of the PD and pre-amplifier, it was decided to apply the 33 MHz, 3 dB cut-off in the equaliser stage rather than the pre-amplifier in order to increase SNR.

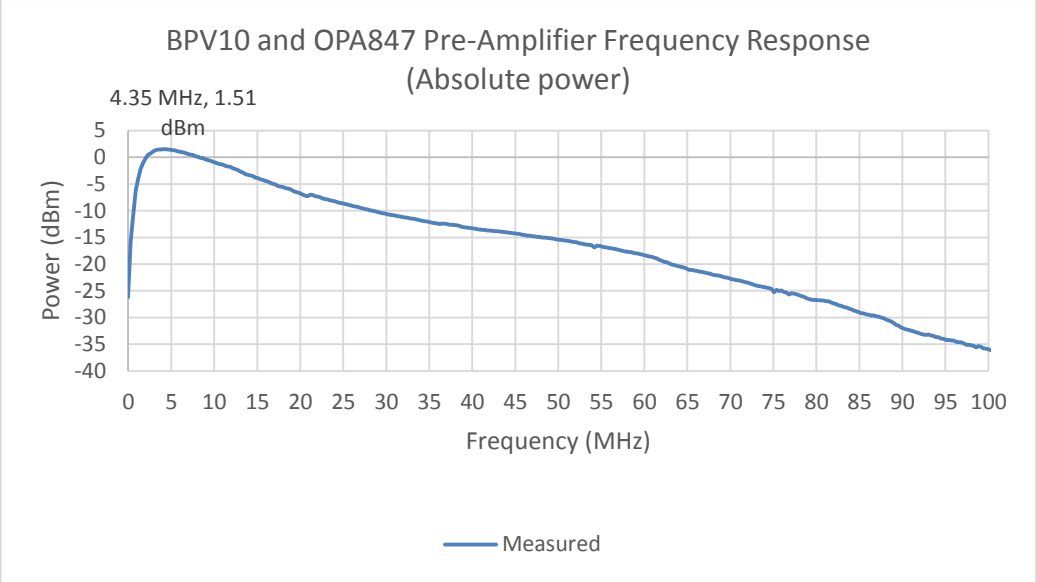


Figure 5-21 BPV10 PIN PD and TI OPA847 op-amp frequency response

In addition to characterising the frequency response of the PD and pre-amplifier, it is possible to estimate the photocurrent flowing in the PD, and use the value to determine the devices responsivity. This is achieved using the maximum power point shown labelled in Figure 5-21, which is 1.51 dBm at 4.35 MHz. This value can be converted to RMS voltage (V_{RMS}) using Equation 5-3, which is derived from Equation 5-4, Equation 5-5 and Equation 5-6; note that Equation 5-6 is shown to highlight the link between system characteristic impedance, R, which is 50 Ω, and the power and voltage.

$$V_{RMS} = \sqrt{\frac{R\ 10^{\left(\frac{P_{dBm}}{10}\right)}}{10^3}} \qquad \text{Equation 5-3}$$

$$P_{dBm} = 10\ Log_{10}\ (P_{mW}) \qquad \text{Equation 5-4}$$

$$P_{mW} = 10^{\left(\frac{P_{dBm}}{10}\right)} \qquad \text{Equation 5-5}$$

$$P_{mW} = \frac{V_{RMS}^2 \, 10^3}{R}$$ Equation 5-6

Applying the equation to the measured power of 1.51 dBm, yields an RMS voltage of approximately 0.27 V. The RMS photocurrent is estimated by dividing the RMS voltage by the amplifiers transimpedance gain of 12 kΩ, which results in a photocurrent of 22.5 μA. The responsivity of the BPV10 PD is approximated by dividing the photocurrent by the optical power measured at the BPV10 PD surface, which is approximately 0.6 mW, and results in a responsivity of approximately 0.04 A/W at the blue LEDs wavelength of 470 nm. This result is of the expected order, but is lower than the 0.14 A/W stated for similar devices operating at 480 nm (Z. e. Ghassemlooy et al., 2013).

5.3.3 Equaliser (Rx)

Using the measured frequency response of the PD and pre-amplifier cascaded, it was possible to determine the amount and type of equalisation required by the system. In Chapter 2, equalisation techniques using passive or active equalisation, or combinations of both, were discussed. Specifically, the work of Li et al. was cited, which described bandwidth extension up to 151 MHz using passive and active circuitry (Li, 2014). However, it was decided that a passive and active approach was excessive, and that the simple passive, 2nd order RC equaliser, proposed by Minh et al. (Minh et al., 2009), was sufficient to provide positive slope compensation and the required bandwidth extension. The 3dB bandwidth required by the system is defined by 50% of the serial clock frequency of 66 MHz, which results in a bandwidth requirement of 33 MHz. The RC equaliser used to achieve this response is shown in Figure 5-22, and is constructed using a 10 MΩ trimming resistor and 47 pF fixed capacitor. The variable resistor was chosen with a large value because it provided a large sweep range, and the capacitor was chosen

in the picofarad range because it has large capacitive reactance at low frequencies (1 kΩ at 1MHz). The preferred value of 47 pF was selected arbitrarily.

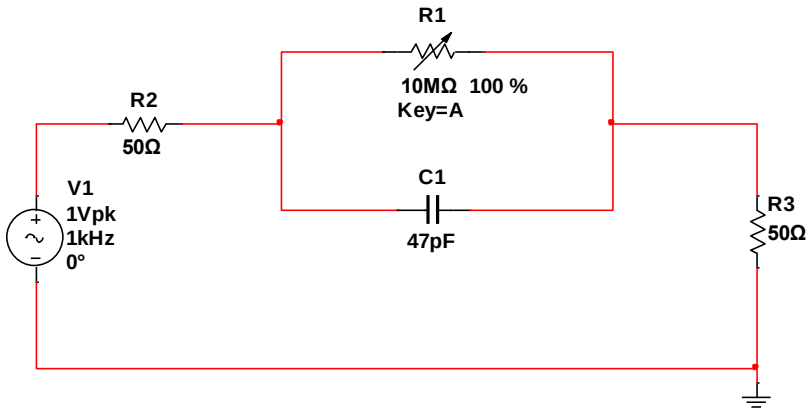


Figure 5-22 2nd order RC equaliser circuit

The equaliser circuit was added after the pre-amplifier in the prototype circuit, and the optimal value of the equalisers resistor (R1) was determined empirically by performing iterative, incremental increases in its value, and then performing a frequency response measurement using the frequency response and bandwidth test setup and conditions described in Appendix I.1. The pre- and post-equalisation frequency responses are shown in absolute power in Figure 5-23. The optimal equalised response was achieved using a resistor value of 4 kΩ. Figure 5-24 shows normalised pre- and post-equalisation responses, and enables comparison of the bandwidth extension and flatness. The pre-equalised response has a 3 dB bandwidth of approximately 7 MHz and has a flatness within 4 dB up to 10 MHz. The post-equalised response exhibits a 3 dB bandwidth at 39.71 MHz, compared to a theoretical requirement of 33 MHz, based on 50 % of the serial clock (66 MHz), resulting in an 18.6% error on the theoretical value; this was deemed acceptable by the author. The flatness of the equalised response is within 4 dB up to 47 MHz.

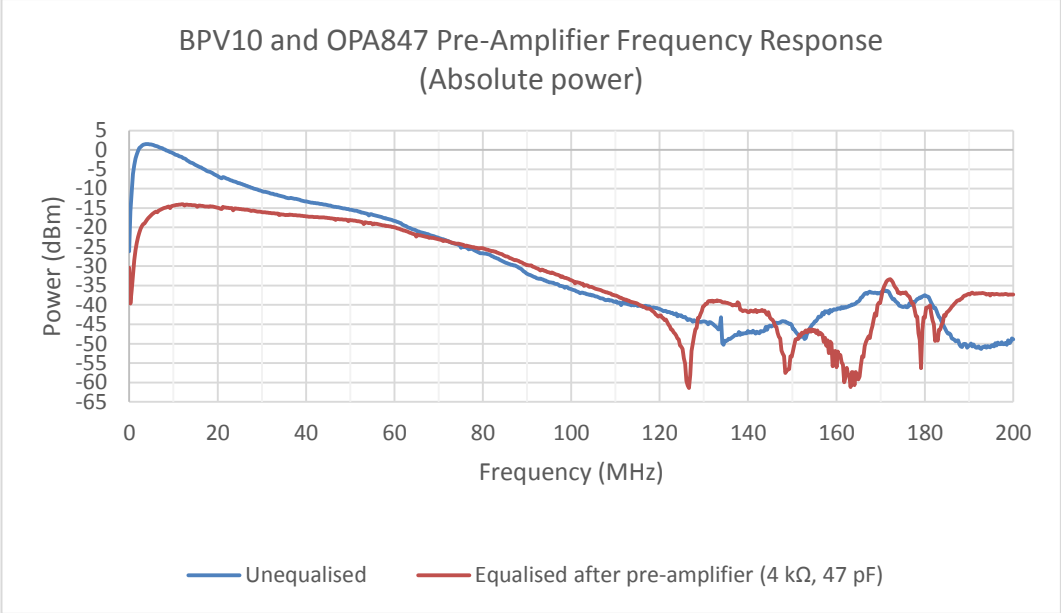


Figure 5-23 BPV10 PIN PD and TI OPA847 op-amp frequency responses

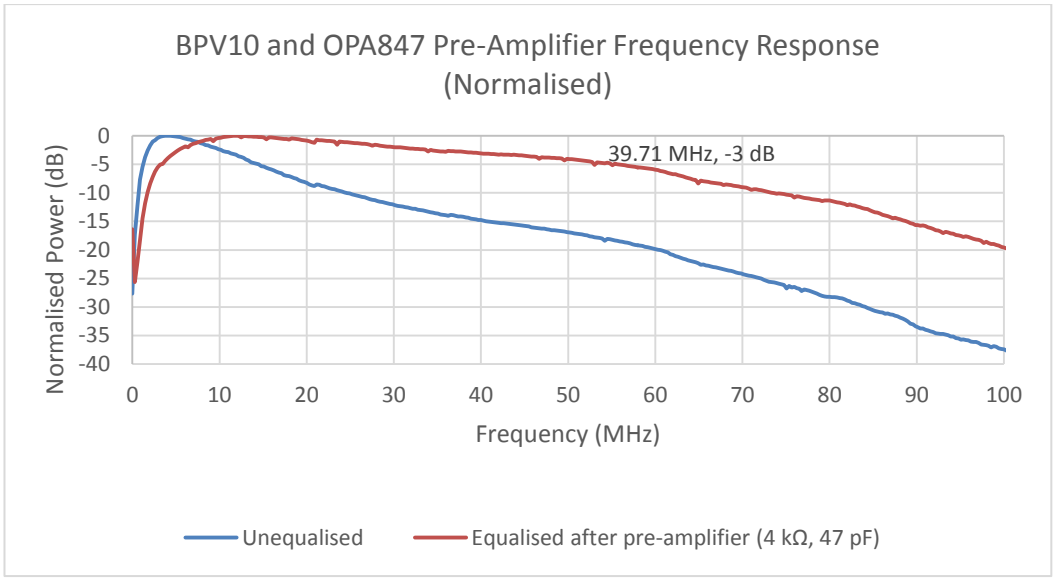


Figure 5-24 BPV10 PIN PD and TI OPA847 op-amp normalised frequency responses

The equaliser circuit was also simulated, and produced the response shown in Figure 5-25, which exhibits a positive slope of 15 dB/decade, with an insertion loss of 35 dB at 1 Hz and 1.6 dB at 100 MHz.

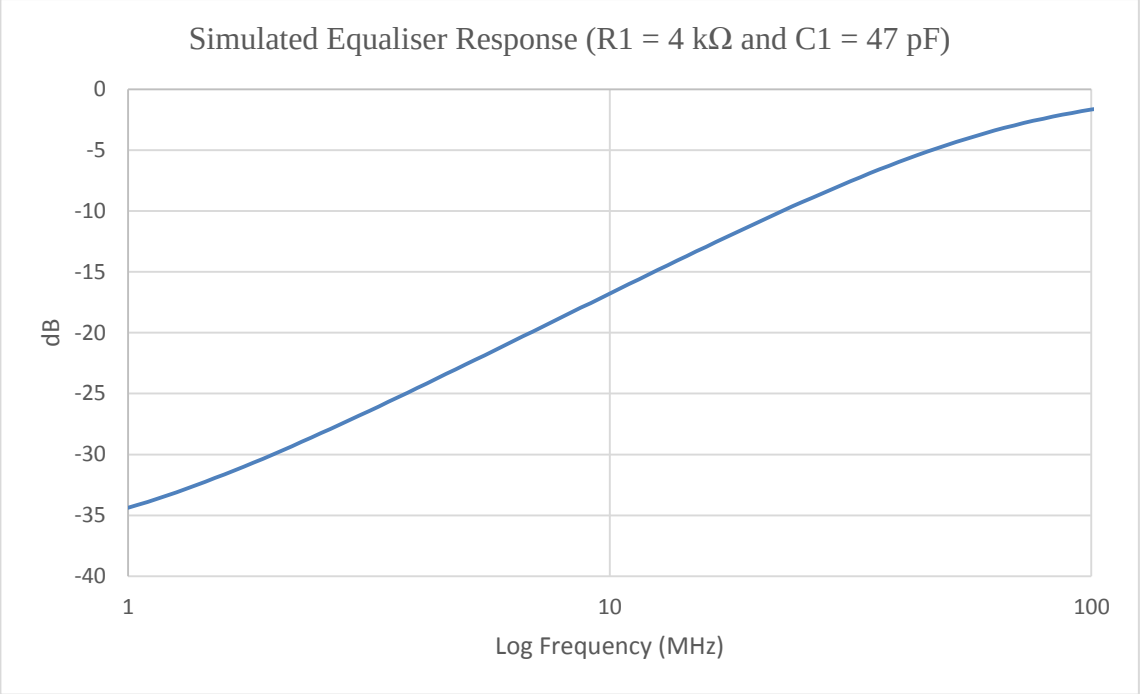


Figure 5-25 Simulated frequency response of the 2nd order equaliser (log frequency)

A 6th order polynomial approximation of the simulated equaliser response was also generated, which is shown graphically in Figure 5-26, where the solid blue trace is the simulated response plotted against linear frequency, and the black dotted trace is the polynomial approximation. Equation 5-7 shows the mathematical expression for the polynomial and Table 5-1 furnishes the values of its coefficients.

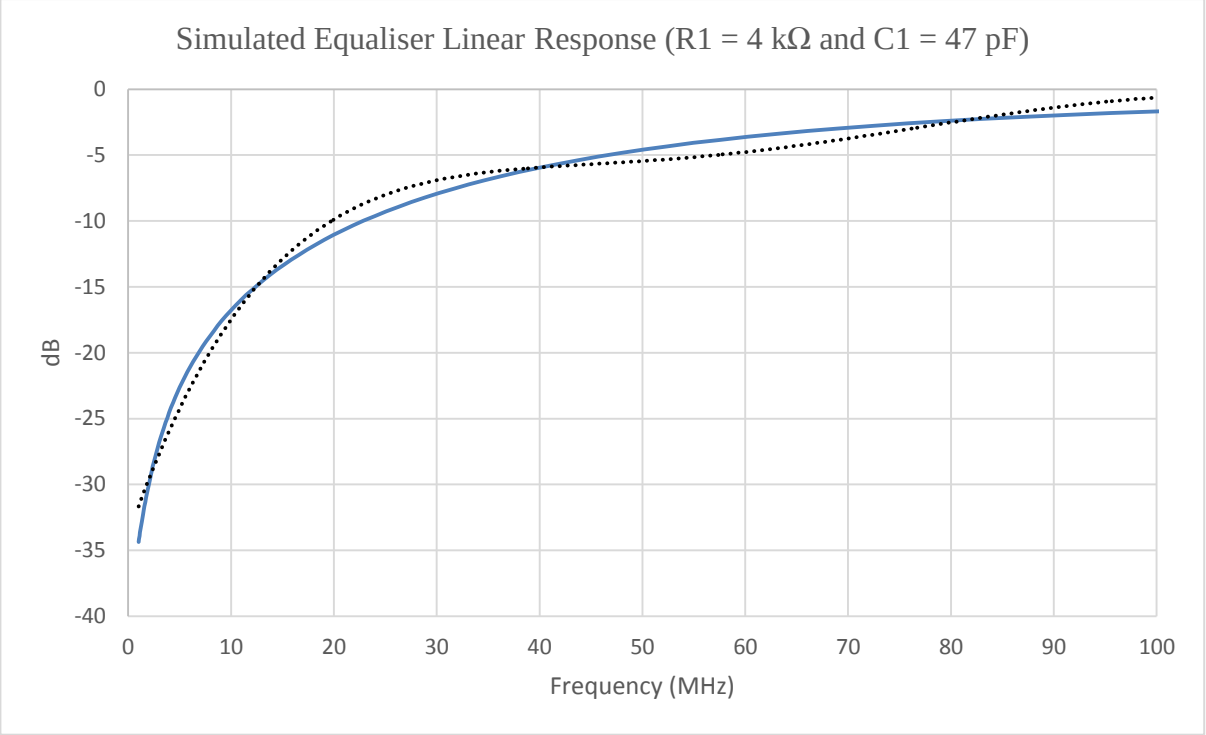


Figure 5-26 Simulated frequency response of the 2nd order equaliser (linear frequency)

$$y = ax^6 + bx^5 + cx^4 + dx^3 + ex^2 + fx + g$$ Equation 5-7

Coefficient	Value
a	$-6.21224131880088\times10^{-11}$
b	$3.96560444854298\times10^{-8}$
c	$-9.79839104331411\times10^{-6}$
d	0.001183038525951
e	-0.0730178867525367
f	2.25758519094501
g	-33.8466565968593

Table 5-1 Equaliser polynomial coefficients

The polynomial approximation was used to evaluate the similarity between the simulated and measured responses, and was performed by summing the equaliser polynomial approximation with the measured unequalised response, as shown in Figure 5-27, where the black trace shows the measured response for the PD and pre-amplifier

prior to equalisation, and the purple trace shows the simulated polynomial response of the equaliser circuit.

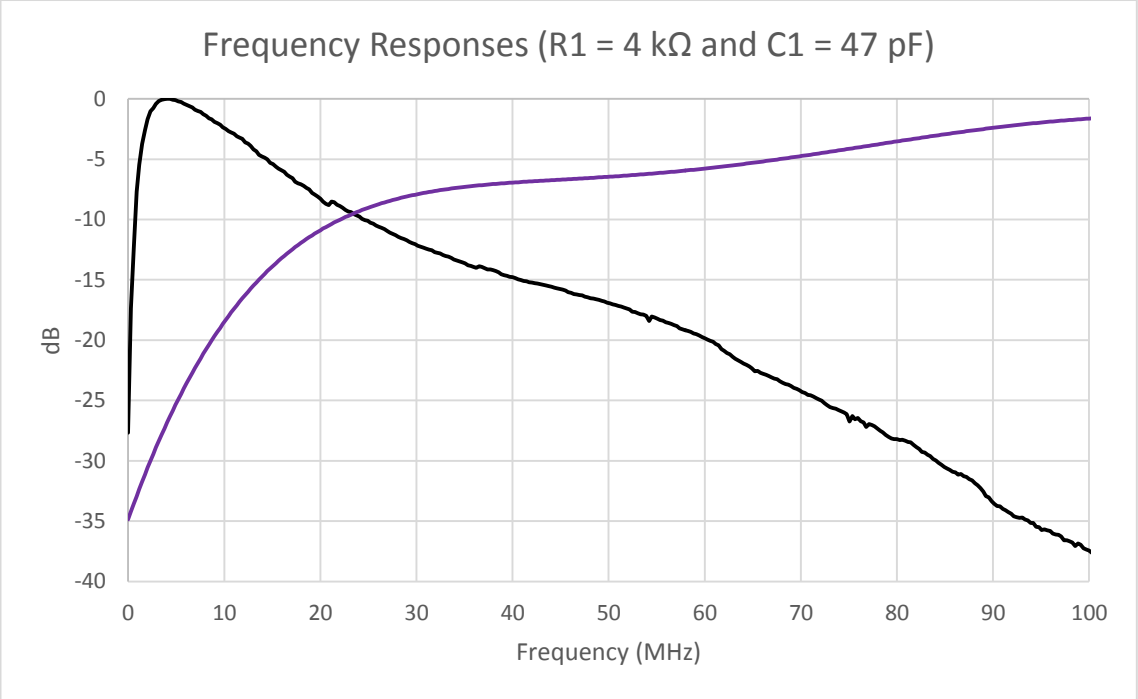


Figure 5-27 Unequalised PD and pre-amplifier (measured) and polynomial approximated equaliser (simulated)

The two traces of Figure 5-27 were then summed, to produce a trace of the unequalised PD and pre-amplifier response, which is equalised by the simulated polynomial approximation of the equaliser circuit. This operation yielded the brown trace shown in Figure 5-28, which is compared against the orange trace in the same figure, which is the actual measured hardware response of the PD, pre-amplifier and equaliser cascade. This graph shows that the simulated and hardware implemented equaliser circuits compare closely, within less ± 1.5 dB separation.

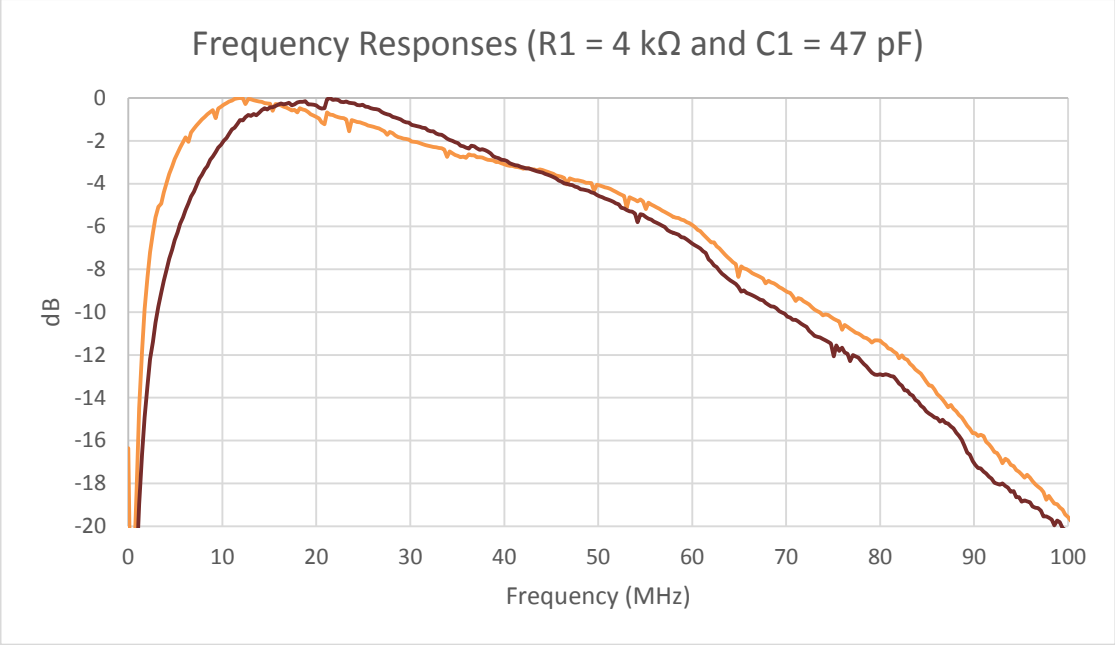


Figure 5-28 Equalised PD and pre-amplifier (measured) and Equalised PD and pre-amplifier (simulated)

This RC equaliser circuit consisting of the 4 kΩ resistor and 47 pF capacitor was used in the first iteration of the VLC systems hardware implementation.

5.3.4 Post-Amplifier (Rx)

The post-amplifier was designed using an inverting op-amp, based on the same OPA847 op-amp and SPICE model used to design and simulate the pre-amplifier stage. In this case, the op-amp was configured as an inverting voltage amplifier, as shown in Figure 5-29, where the gain of the amplifier is defined by Equation 5-8 and Equation 5-9.

$$Av = -\frac{R_f}{R_1} \qquad \text{Equation 5-8}$$

$$G = 20\log\left(\frac{R_f}{R_1}\right) \qquad \text{Equation 5-9}$$

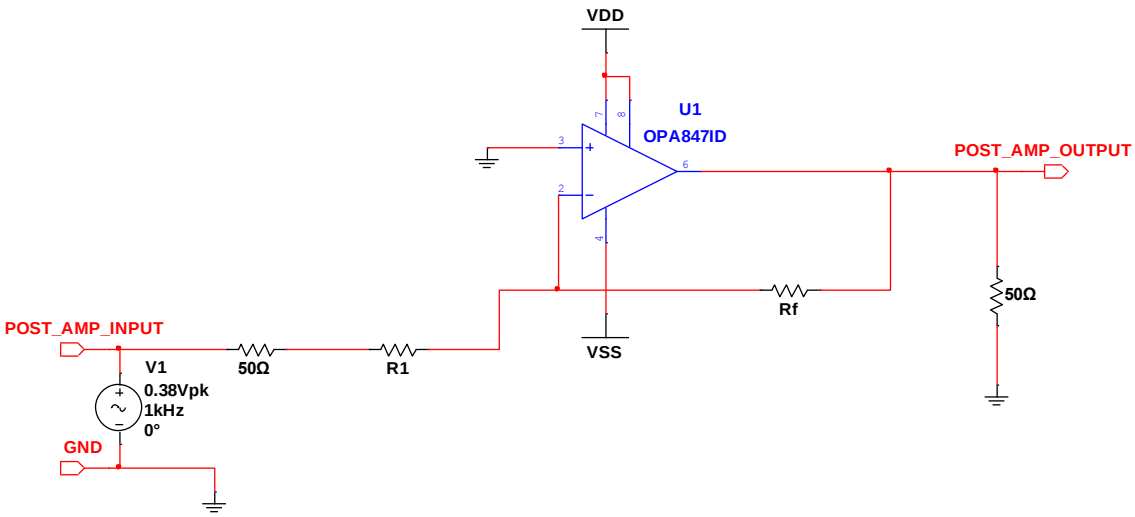


Figure 5-29 Post-amplifier inverting voltage amplifier circuit

The gain of the amplifier was determined using cascade analysis of the pre-amplifier and equaliser signal levels. The peak signal output by the pre-amplifier during frequency response analysis in section 5.3.2 was 1.51 dBm (0.27 V RMS, 0.764 Vpp) at 4.35 MHz, which was then attenuated by the equaliser by 23 dB at the same frequency, resulting in a signal level of -21.49 dBm (19 mV RMS, 53.2 mVpp) at the equalisers output. A design decision was taken to amplify the equaliser output to 4.01 dBm (0.354 V RMS, 1.0 V pp), resulting in a voltage gain of 25.5 dB in the post-amplifier.

Given the voltage gain of 25.5 dB, the post-amplifier was designed by setting R_1 to 50 Ω, which set the input impedance of the amplifier, and then transposing Equation 5-9 for R_f. The resultant R_f is 942 Ω with the closest preferred resistor value at 931 Ω. The component values were to simulate the circuit shown in Figure 5-30; note that positive and negative 5 V supply rails were used to power the OPA846 op-amp.

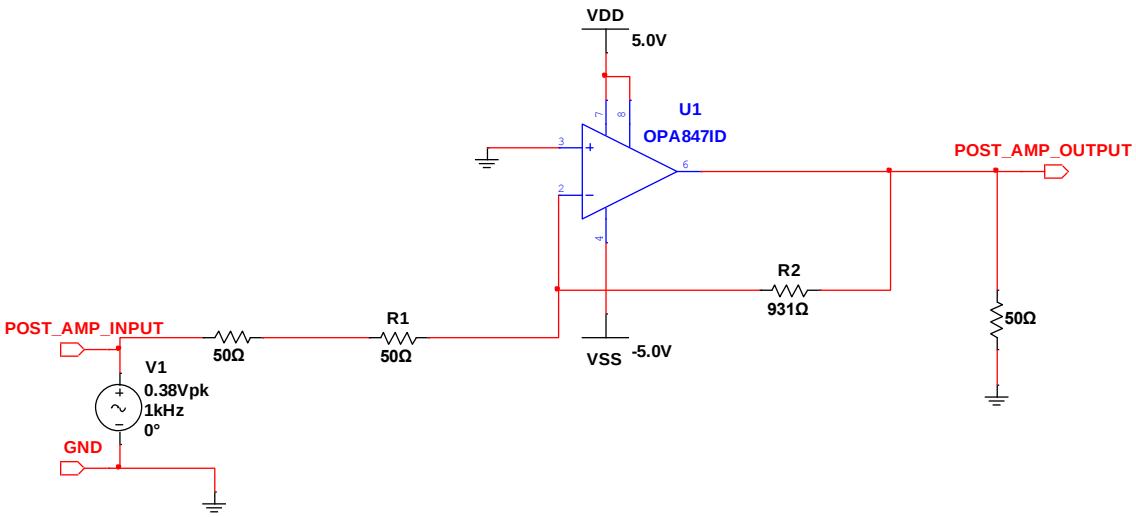


Figure 5-30 Post-amplifier inverting voltage amplifier circuit (component values)

The simulated circuit exhibits a flat response from DC to 10 MHz at a gain of 25.38 dB. The gain is 0.12 dB below the design value of 25.5 dB, due to the lower value of the feedback resistor. The response peaks at 100 MHz at a gain of 26.38 dB.

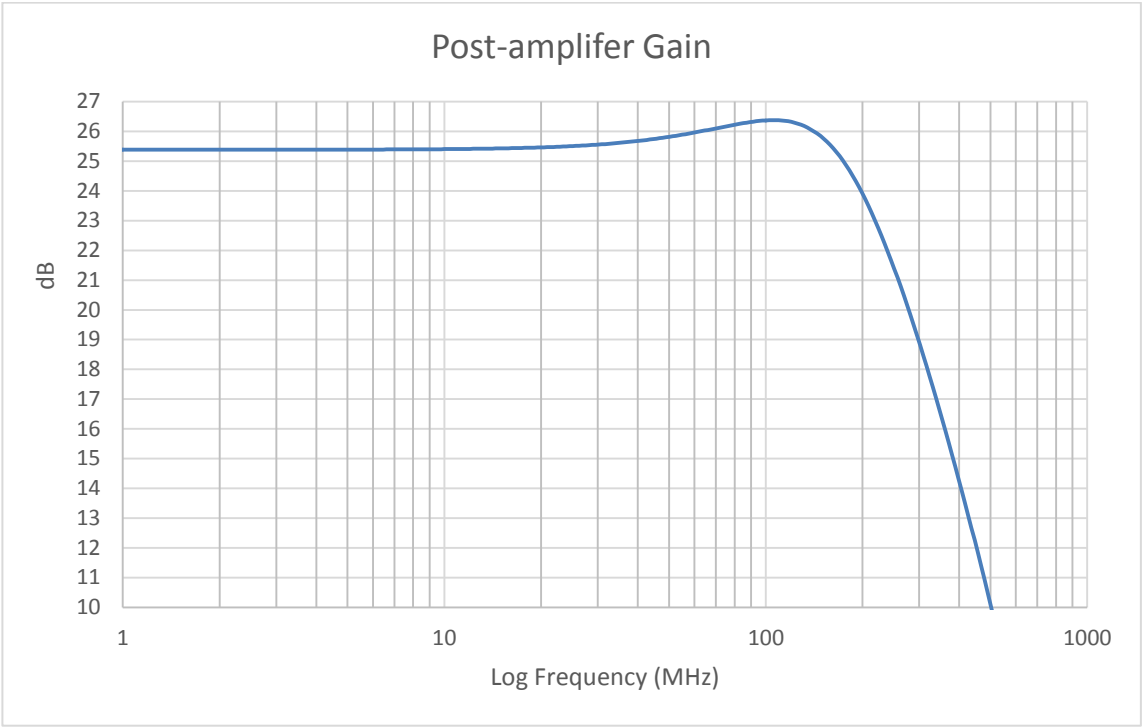


Figure 5-31 Post-amplifier frequency response

The 25.38 dB post-amplifier circuit will be used as the initial gain in the first iteration of the VLC system.

5.3.5 Pre-Detection LPF (Rx)

The pre-detection filter was designed using a 2nd order Butterworth LPF, with a cut-off frequency of 46.2 MHz, which was calculated from 70% of the serial clock frequency of 66 MHz as stated in Chapter 4. The filter was synthesised using a commercial filter synthesis tool (Nuhertz Filter Solutions), and was designed to operate in a 50Ω characteristic impedance. The circuit is shown in Figure 5-32, with ideal component values.

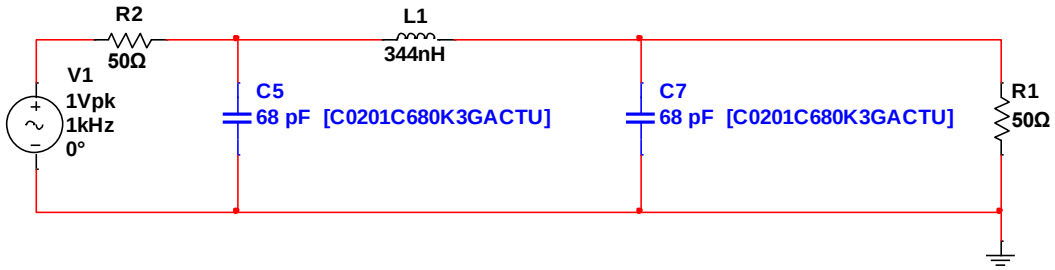


Figure 5-32 2nd order pre-detection LPF circuit

The 344 nH inductor (L1) is not a preferred value, and therefore it was necessary to replace the component with the nearest preferred value, which was 330 nH. Figure 5-33 shows the simulation of the filter with the 344 nH and 330 nH inductors. The blue trace shows the response with the 344 nH inductor, the 3 dB bandwidth is labelled at 45.70 MHz. The red trace shows the response with the 330 nH inductor, and the 3 dB bandwidth is now at 47.86 MHz, indicating an upward shift of 1.66 MHz representing a 3.6% error in the design value of 46.2 MHz. The error is relatively small, and is unavoidable given that preferred inductor value must be used to realise the hardware

implementation. Figure 5-34 shows the skirt and stopband of both responses, and there is little difference shown.

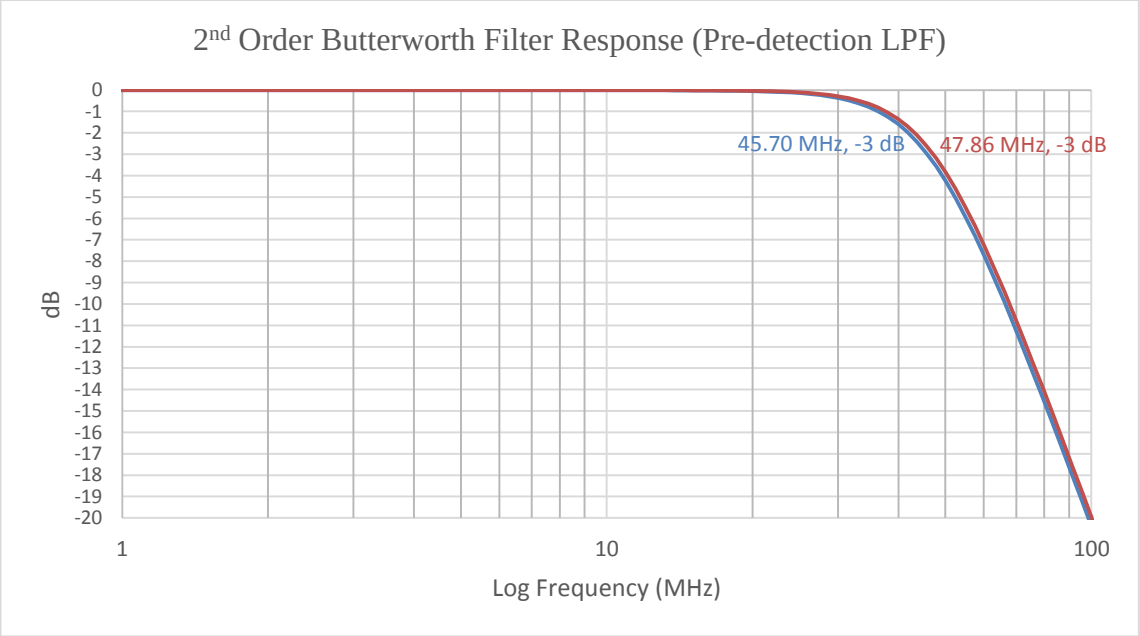


Figure 5-33 2nd order Butterworth LPF frequency response (passband)

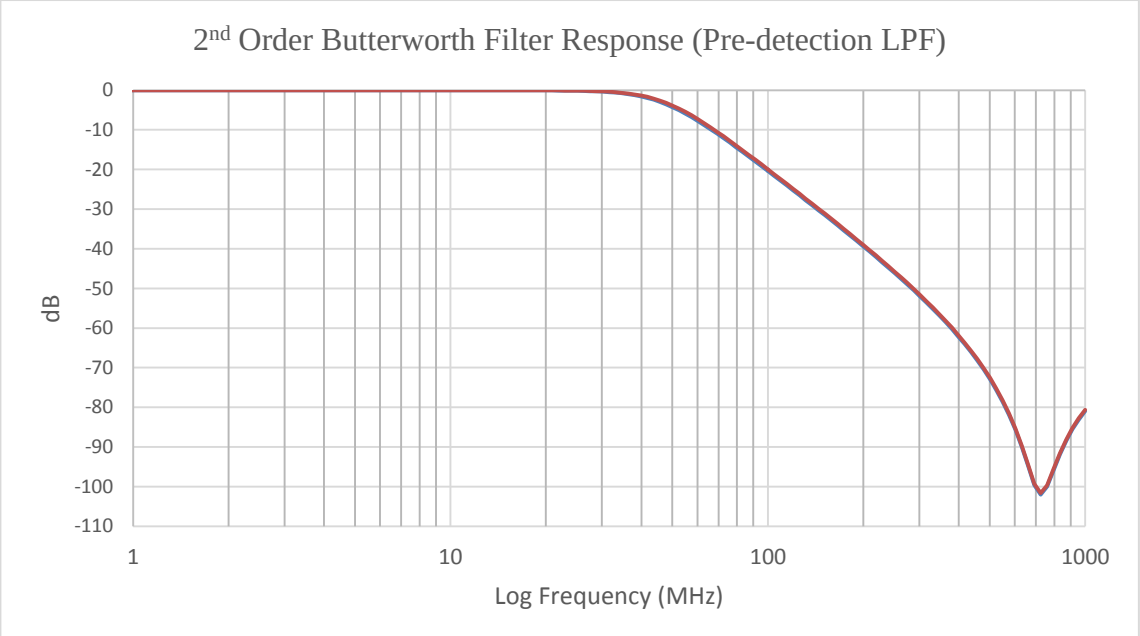


Figure 5-34 2nd order Butterworth LPF frequency response (stopband)

The pre-detection filter using the series 330 nH inductor and two shunt 68 pF capacitors will be used as the initial gain in the first iteration of the VLC system.

5.3.6 Comparator (Rx)

The window comparator, defined in Chapter 3, was designed using an Analog Devices ADCMP551 single-supply, high speed positive emitter-coupled logic (PECL) comparator, and simulated using the manufacturers SPICE model (Analog, 2015). The device was selected because of it high speed threshold detection capabilities, in particular, its ability to process pulse durations of 0.7 ns, which is a fraction of IOPPM pulse duration of 15.1515 ns. The device also has fast 0.5 ns rise- and fall-times and a propagation delay of only 0.5 ns, which ensures fast comparison of detected pulses.

Two ADCMP551 comparators were used to construct the window comparator, one configured as a non-inverting comparator with a positive reference voltage (V_{REF+}), that detects the IOPPM+ pulses, and a second configured as an inverting comparator with a negative reference voltage (V_{REF-}), that detects the IOPPM- pulses. The digital outputs of the comparators are defined by Equation 3-2 and Equation 3-3 that were introduced in Chapter 3.

$$V_{D\,IOPPM+} = \begin{cases} 1, & if\ V_{A\,IOPPM+} \geq V_{REF+} \\ 0, & if\ V_{A\,IOPPM+} < V_{REF+} \end{cases} \quad \text{Equation 3-2}$$

$$V_{D\,IOPPM-} = \begin{cases} 1, & if\ V_{A\,IOPPM-} \leq V_{REF-} \\ 0, & if\ V_{A\,IOPPM-} > V_{REF-} \end{cases} \quad \text{Equation 3-3}$$

Where $V_{A\,IOPPM+}$ and $V_{A\,IOPPM-}$ are the positive and negative analogue pulses within the composite signal, and V_{REF+} and V_{REF-} are the threshold voltage references.

The circuit diagram of the window comparator is shown in Figure 5-35.

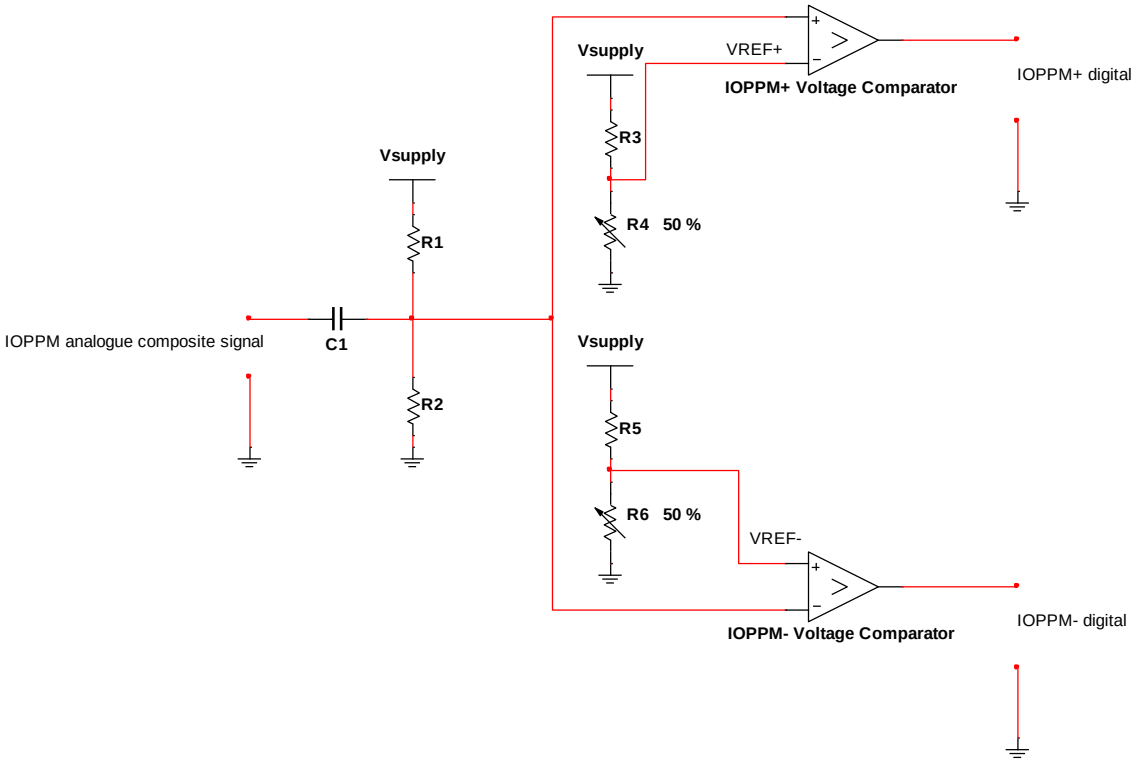


Figure 5-35 Window voltage comparator

Reading the circuit from left to right, the first component is C_1, which is used to couple the IOPPM composite signal into the comparator. The capacitor is required to pass the 66 MHz serialised IOPPM signal, but remove the DC term. This action is achieved using a C_1 value of 1 nF that provides low capacitive reactance at 66 MHz. Following the capacitor is a potential divider, formed by R_1 and R_2, which enables the application of a DC offset to the IOPPM composite signal to enable the removal of negative excursions in the signal; it was explained in Chapter 3, that the removal of negative excursions is necessary when the comparator used only accepts positive input voltages, as is the case with the ADCMP551. The comparator has a single-ended input voltage range of 0 V to 1 V, centred on 0.5 V, which means that the IOPPM composite signal must be shifted into this voltage range to ensure correct detection of the IOPPM+ and IOPPM- codewords. The peak-to-peak amplitude of the IOPPM composite signal

applied to the input of the window comparator is determined by the output voltage of the post-amplifier, which was designed in section 5.3.4 to provide 1 V pp. Since the 1 V pp signal is AC coupled via C_1, it has a positive 0.5 V excursion and a -0.5 V excursion, which will result in corrupted invalid codewords being detected. Using a 3 V supply rail for the potential divider, the negative excursion is removed by setting the R_1 value to 1 k Ω and R_2 value to 200 Ω, which results in offset of 0.5 V being applied to composite signal. The signal now has a ± 0.5 V excursion centred on the 0.5 V offset, which fits into the 0 V to 1 V input range of the comparator. Figure 5-36 illustrates the voltage levels resulting from the application of the 0.5 V DC offset to the AC coupled 1 V pp input composite signal, which in this example consists of IOPPM codewords $100_{\text{IOPPM+}}$ and $001_{\text{IOPPM-}}$. The pulses are Gaussian shaped and the 3-bit code occupy a slot-time (τ) of 15.1515 ns, which is the inverse of the 66 MHz serial clock. The 0.5 V offset is highlighted in green, and the maximum and minimum ranges of the comparator are highlighted, respectively, in red and blue.

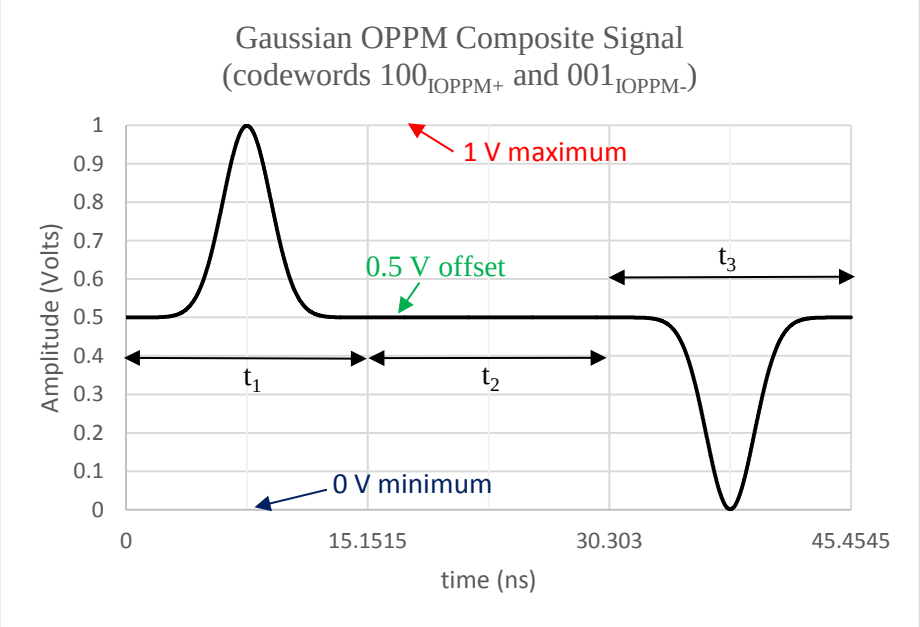


Figure 5-36 IOPPM composite signal with 0.5 V DC offset

After the potential divider, the composite signal is split and fed to the two comparators. IOPPM+ pulses are detected by the non-inverting comparator using the threshold set by V_{REF+}, and the IOPPM- pulses are detected by the inverting comparator using the threshold set by V_{REF-}. In the case of the 1 V pp, 0.5 V offset composite signal, the ideal V_{REF+} is at the mid-point between 0.5 V and 1 V, which is 0.75 V, and the ideal V_{REF-} is at the mid-point between 0 V and 0.5 V, which is 0.25 V. Figure 5-37 illustrates the threshold crossing for the IOPPM+ and IOPPM- pulses, where the IOPPM+ comparator detects a logic one when the composite signal is at or above 0.75 V (red highlight), and a logic zero when it is below 0.75 V, and the IOPPM- comparator detects a logic one when the composite signal is at or below 0.25 V (blue highlight), and a logic zero when it is above 0.25 V.

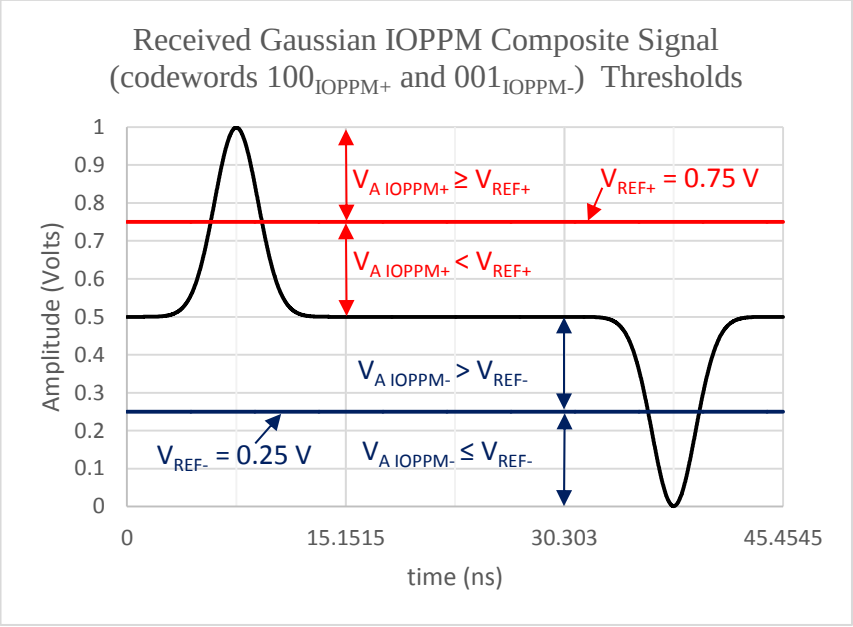


Figure 5-37 IOPPM composite signal threshold crossings (1 Vpp, 0.5 V offset)

Given the threshold voltages, it is possible to establish values for the V_{REF+} potential divider formed by R_3 and R_4 and the V_{REF-} potential divider formed by R_5 and R_6. Using a supply voltage of 3 V for both potential dividers, the V_{REF+} of 0.75 V is

provided using an R_3 value of 1 kΩ and an R_4 value of 333.33 Ω, and the V_{REF-} of 0.25 V is provided using an R_5 value of 1 kΩ and an R_6 value of 90.90 Ω. Figure 5-38 shows the window comparator threshold crossings for the IOPPM+ and IOPPM- pulses (brown highlight), which are used to generate the digital outputs for the IOPPM+ comparator (Figure 5-39) and IOPPM- comparator (Figure 5-40). Both figures for the digital outputs show the central decision times indicated by the vertical dotted lines, which are determine by the 66 MHz serial clock ($\frac{1}{\tau}$) of the VLC system, shifted by half a time slot period ($\frac{\tau}{2}$). The IOPPM decoders sample clock ($F_s = \frac{1}{\tau}$) is used to clock the received bits into the decoders dual SIPOs, which produce parallel outputs that are used by the combinational logic based decoder circuits.

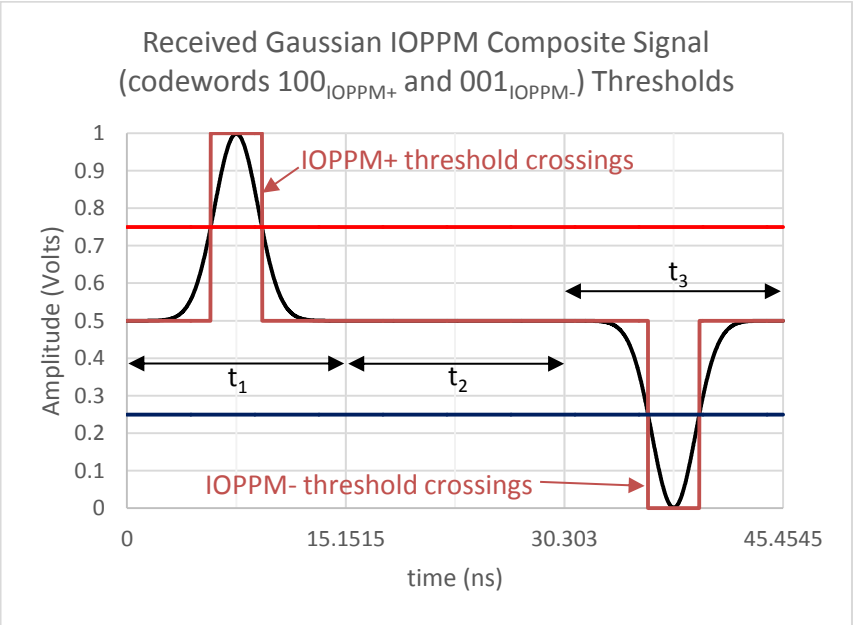


Figure 5-38 IOPPM composite signal threshold crossings (1 Vpp, 0.5 V offset)

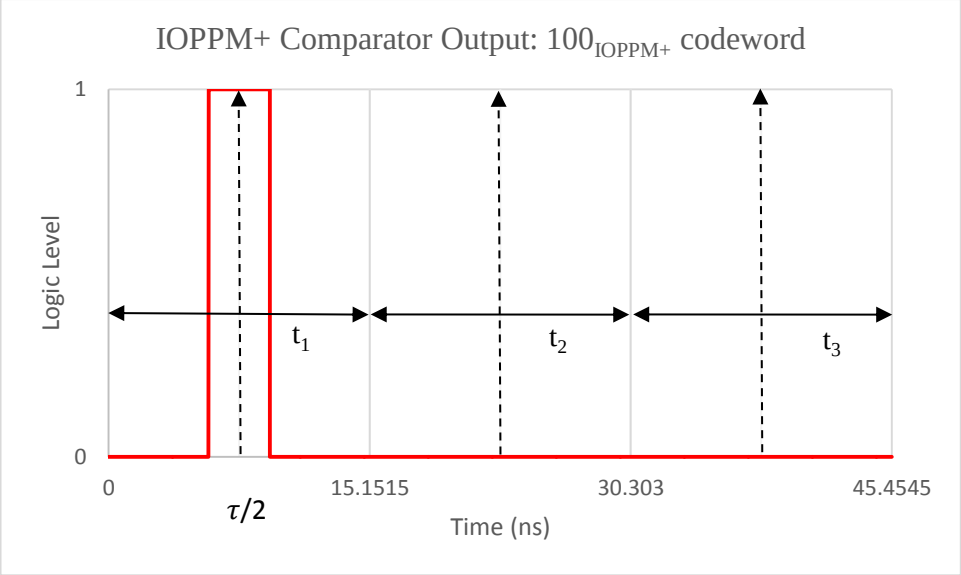


Figure 5-39 IOPPM+ comparator digital output

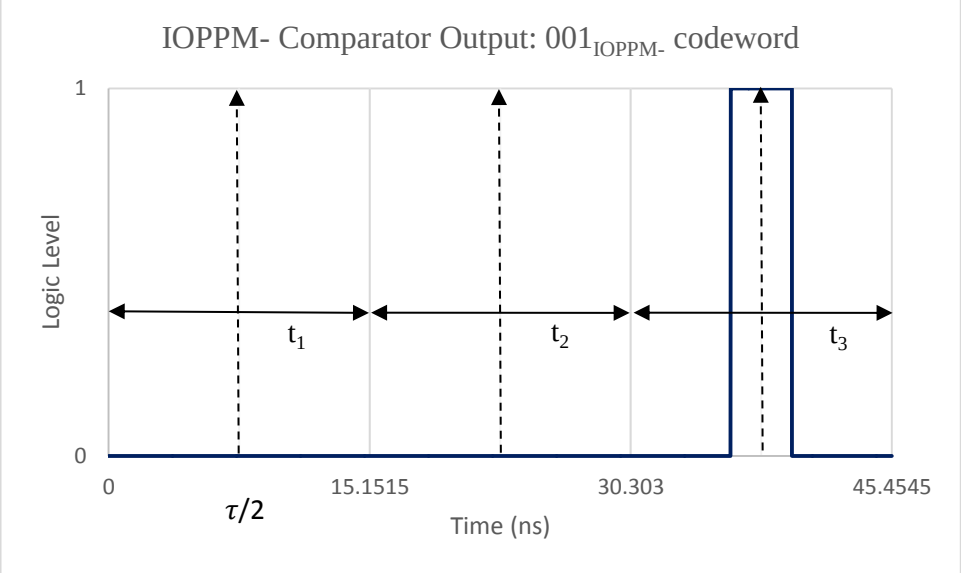


Figure 5-40 IOPPM- comparator digital output

The window comparator circuit, shown in Figure 5-41, was simulated using the ADCMP551 SPICE model for the non-inverting and inverting comparators, and the component values established for the input capacitor, and potential divider circuits used for the DC offset and threshold reference voltages.

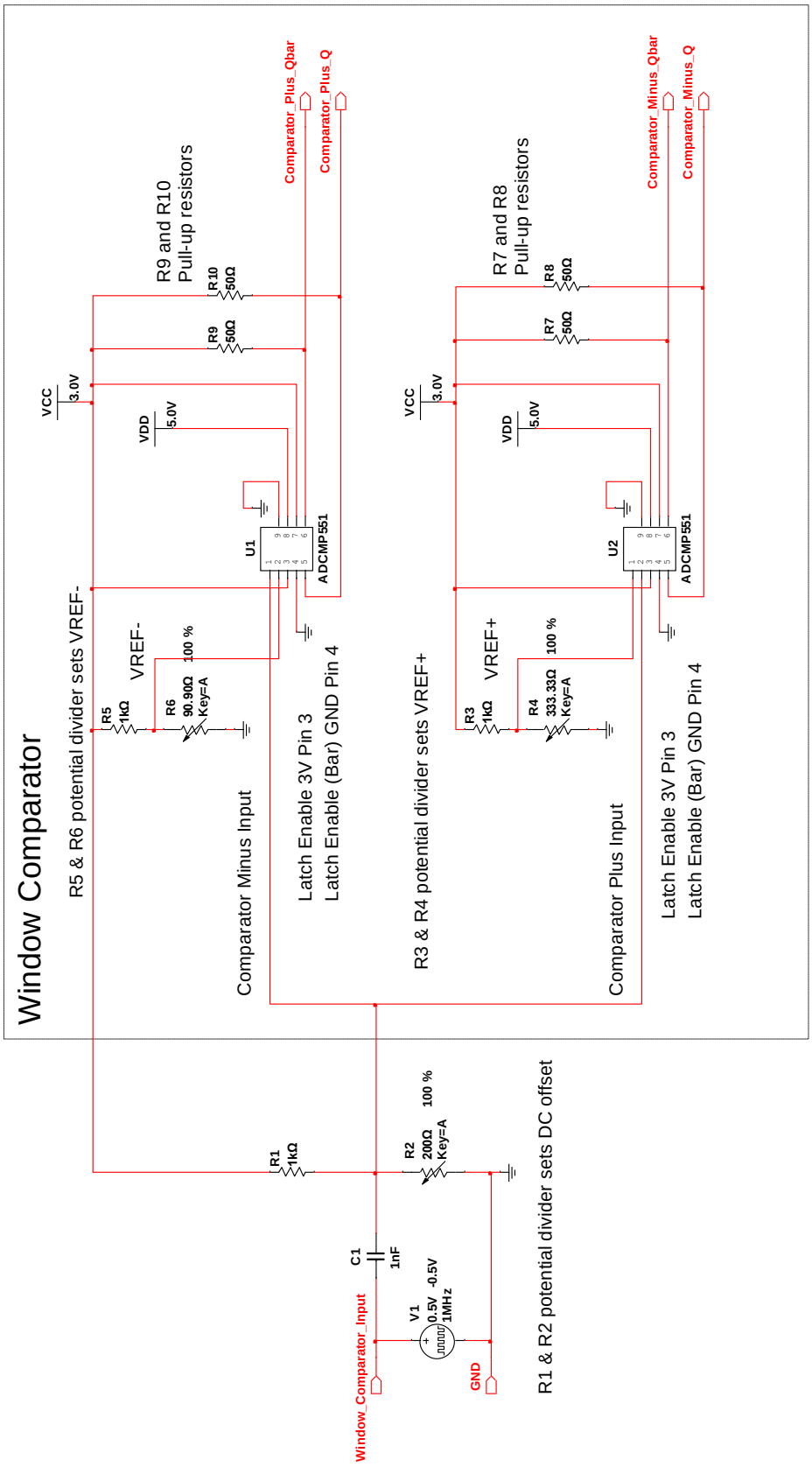


Figure 5-41 Window comparator simulation circuit

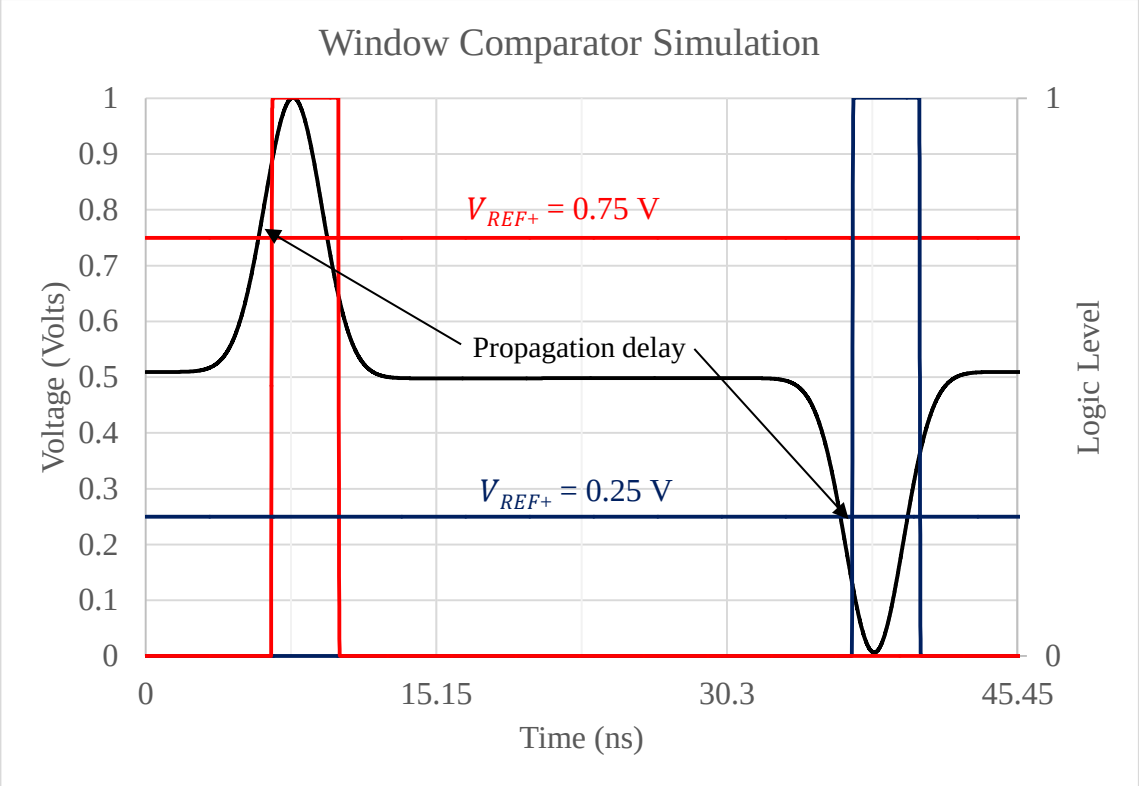


Figure 5-42 Window comparator simulation

The circuit was simulated using an IOPPM composite signal composed of IOPPM codewords $100_{\text{IOPPM+}}$ and $001_{\text{IOPPM-}}$, as shown in Figure 5-42. The pulses are shown by the black trace, and have Gaussian approximated shapes. Referring to the left-hand-side vertical axis, the signal is centred on a 0.5 V DC level, set by the window comparators input potential divider, and the crossing thresholds are shown by the red solid horizontal line for IOPPM+ ($V_{REF+} = 0.75\,V$) and the blue solid line for IOPPM- ($V_{REF-} = 0.25\,V$). The IOPPM+ and IOPPM- digital outputs of the comparator are shown overlaid, respectively, in solid red and blue traces, and their logic levels are shown on the right-hand-side axis (logic one/zero). The simulated waveforms are almost identical to the theoretical predictions, with the exception of the 0.5 ns propagation delay introduce by the ADCMP551 device SPICE model. The simulation demonstrates that

detection of the IOPPM composite signal is possible using the window comparator architecture.

The ADCMP551 comparator was proven in terms of speed and input voltage range, however, the digital outputs of the device not readily compatible with FPGA inputs. Figure 5-41 shows that the digital outputs of the ADCMP551 comparators are powered from a 5 V rail and use differential PECL logic. In order to make interfacing with an FPGA easier, the outputs were translated to single-ended TTL logic using comparators configured with the device parameters of an ON Semiconductor MC100ELT23 differential PECL to single-ended TTL translator (ON, 2015). Figure 5-43 shows the comparator circuits used in the simulator to achieve differential PECL to single-end TTL translation.

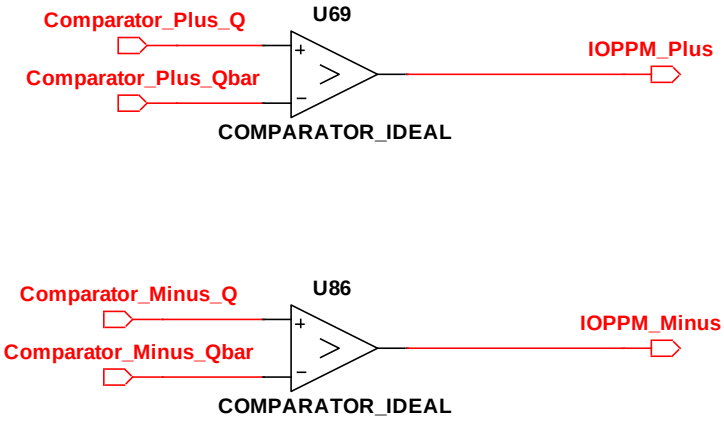


Figure 5-43 Differential PECL to single-ended TTL translator

The ADCMP551 based window comparator circuit and MC100ELT23 PECL to TTL translator will be used in the implementation of the VLC system.

5.3.7 VLC System Electrical Model

The individual subsystem blocks were cascaded into a complete electrical model for the VLC system. Figure 5-44 shows the block diagram of the cascaded transmitter and

receiver subsystems. The blocks highlighted in pink are required by the simulation environment to provide input stimuli to the system.

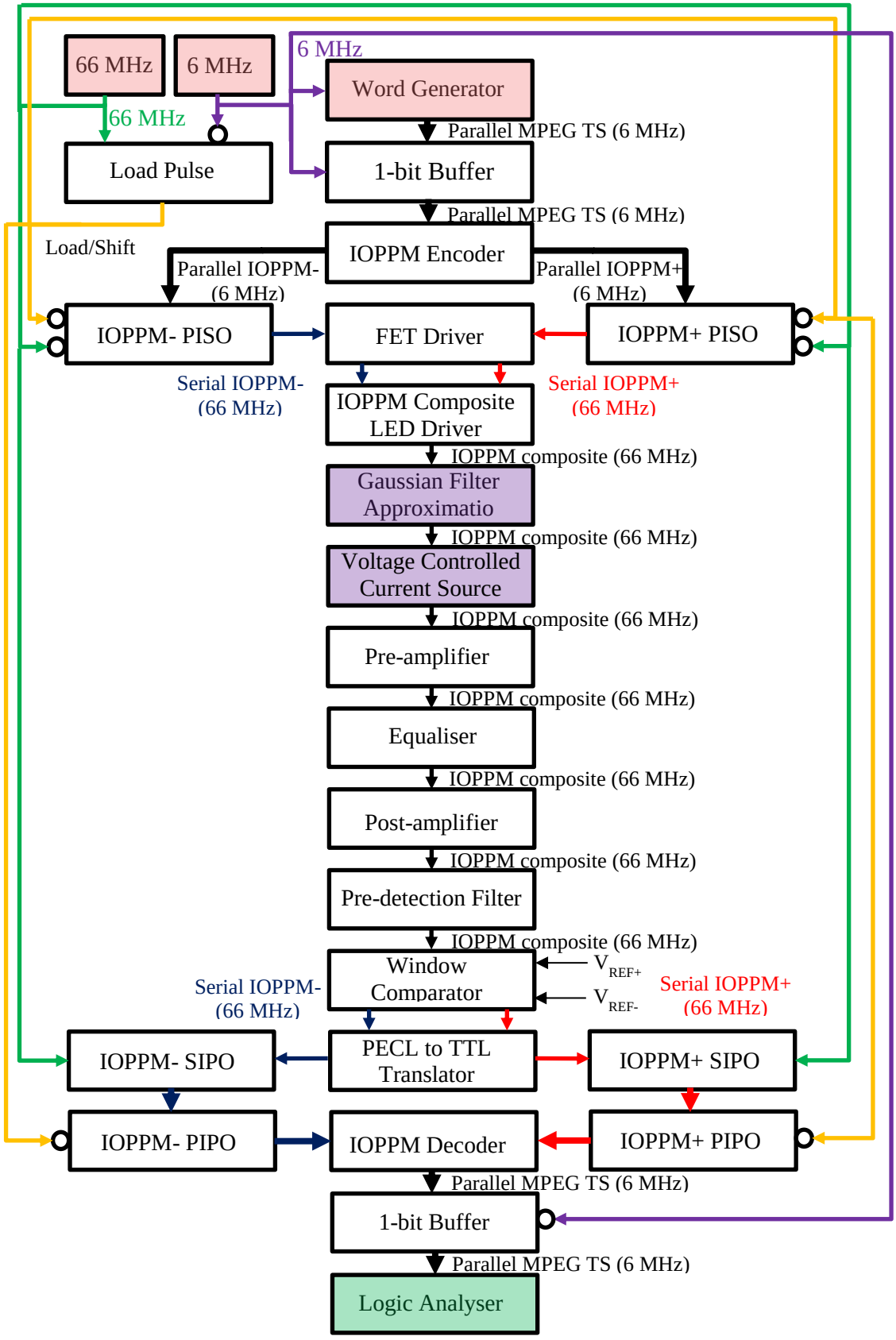


Figure 5-44 VLC Electrical System Model

The input stimuli consists of the 6 MHz MPEG TS and 66 MHz serial clocks, which are provided by synchronised reference clocks, and the system data source provided by a 10-bit word generator clocked at 6 MHz.

The key measurement devices used in the system consists of the logic analyser block, highlighted in green, and time and frequency domain measurement functions which can be placed anywhere along the signal paths; note these function are not shown in the diagram for clarity.

The most critical blocks added to the system model, which enable approximation the optical channel in the electrical domain, are the Gaussian filter approximation and voltage controlled current source.

The Gaussian impulse response of the optical channel was approximated using a 10^{th} order Butterworth LPF, which has a cut-off frequency of 70 MHz. The filter design is based on measurements taken from the prototype PD and pre-amplifier circuit shown in section 5.3.2. The synthesised filter circuit is shown in Figure 5-45, and uses a shunt component first topology, and is designed to operate in a 50Ω characteristic impedance.

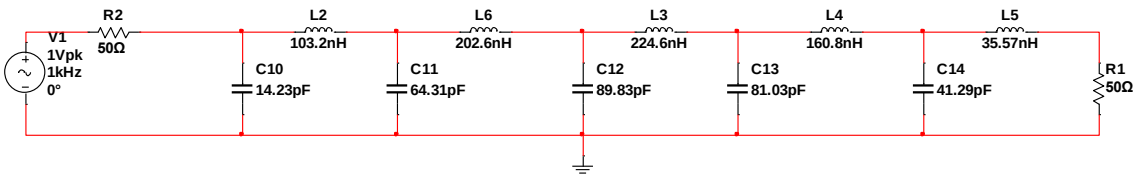


Figure 5-45 10^{th} order Butterworth LPF circuit

The frequency response of the filter is shown in Figure 5-46, and approximates the Gaussian shaping of the IOPPM pulses introduced by the optical channel. The output voltage pulses of the IOPPM composite LED driver are presented to the input of the filter which reduces the bandwidth of the pulses to 70 MHz, resulting in the pulses

approximating a Gaussian shape. The pulses are then presented to a voltage controlled current source which converts voltage pulses output by the filter into current pulses that simulate the photocurrent of the PD. The transfer function between the voltage and current is given by a frequency invariant transconductance coefficient. These stages effectively enable the optical channel to be modelled purely in the electrical domain, eliminating the optical components from the circuit .i.e. the LED and PD. The pulse shaping also enable more accurate modelling of the IOPPM composite signals propagation through the analogue processing stages of the receiver.

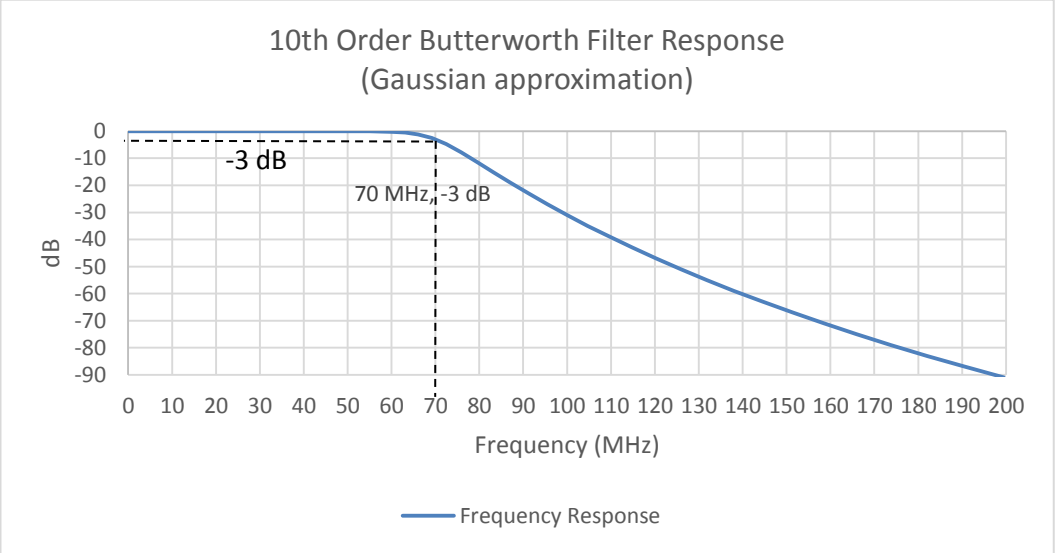


Figure 5-46 10th order Butterworth LPF frequency response

The simulated and measured hardware implemented system results are presented and analysed in Chapter 7.

5.3.8 Conclusions

In this chapter, the VLC systems top-level architecture and operation was defined. Using a top-down, modularised approach, the digital and analogue subsystems needed to realise the top-level architecture were specified, designed and simulated.

It was concluded in this chapter that:

- The digital IOPPM encoder and decoder circuits were realisable using simple combinational logic: AND, OR and NOT gates, and the sequential circuits using D-type flip-flops to realise the required buffers, PISOs, SIPOs and PIPOs.
- A PLL is required to generate the 66 MHz serial clock, which is phase-locked and scaled (×11) to the 6 MHz MPEG TS clock.
- The timing of the loading and shifting of the encoders PISO and decoders SIPO/PIPO blocks required a load pulse which detects and counts the clock transitions of the 6 MHz and 66 MHz clocks, outputting a load pulse (or shift) which simultaneous drives the encoder and decoder. The entire VLC system is timed and controlled by these three signals, and since no clock-recovery is used in the proof-of-concept system, the clocks and load pulse are hardwired into the receiver.
- The IOPPM composite LED driver is realisable using a FET driver to interface the IOPPM encoder logic with two FETs, one of which is used to increase the drive current of the LED by 13 mA and the second which is used to reduce it to zero. The quiescent current of the LED was set at 13 mA, to reduce power consumption in the transmitter and also increase the lifetime of the LED.
- A PD with a wide bandwidth (250 MHz) is suitable for the system. The device has a small detection surface area (0.78 mm) and operates with a reverse voltage of 12 V, which achieves a small diode capacitance of 3pF.
- A pre-amplifier with a transimpedance gain of 12 kΩ (81.6 dBΩ) and 84 MHz bandwidth is suitable for the initial iteration of the system. Based on the measured performance of the cascaded PD and pre-amplifier prototype circuit,

the responsivity of the PD was approximated at 0.04 A/W at a wavelength of 470 nm.

- A 2nd order passive RC equaliser is sufficient to provide the necessary positive slope to compensate for the LED and channel roll-off. The 33 MHz 3 dB bandwidth, based on 50 % of the serial clock, was also applied in the equaliser rather than pre-amplifier, its 3dB point measured at 39.71 MHz; note this was measured with the equaliser connected at the output of the pre-amplifier in the PD and pre-amplifier prototype circuit.
- A post-amplifier with a voltage gain of 25.5 dB is required to achieve an output voltage of 1 V pp; note this output voltage is dependent on the received power.
- A 3rd order Butterworth pre-detection filter with a 47.86 MHz 3 dB bandwidth is suitable for the system. The filter bandwidth is based on 70% of the serial clock frequency, and the filter is realisable using preferred component values.
- The window comparator is realisable using a commercially available comparator. Simulation using Gaussian approximated IOPPM pulses demonstrated that detection of the IOPPM composite signal is possible using the window comparator architecture. DC offset correction for the comparator window and threshold voltages were established.
- A 10th order Butterworth low-pass filter, with a bandwidth or 70 MHz, is able to approximate the Gaussian shaping required by the IOPPM pulses, and ,in conjunction with a voltage controlled current source, can be used to electrical model the end-to-end performance of the VLC system.

6 System: Implementation

This chapter presents the proposed physical implementation of the VLC system, which is based on the subsystem design and simulation presented in Chapter 5. The digital subsystems are recreated in an FPGA design environment to enable their implementation on a commercially available FPGA, and the analogue subsystems are fabricated on PCBs, and populated with the commercially available devices which were presented and simulated in Chapter 5. All subsystems, including the Silicon Labs EVB (data source) and Bush DH2636STB (data sink), are then integrated into the complete end-to-end VLC system. A directed LOS transmission optical rail system, fitted with concentrators (lenses) to collimate the light and maximise the received power at the receiver is used to facilitate testing of the overall system.

6.1 End-to-End VLC System Architecture (Single LED)

Figure 6-1 shows the proposed end-to-end architecture for the single LED VLC system, and is based on the electrical system model presented in Chapter 5, Figure 5-44. The architecture differs from the electrical model in that the word generator block, which was used as the data source in the model, is replaced with the Silicon Labs EVB that provides the parallel MPEG TS input to the IOPPM encoder; note that the MPEG TS is derived from a live off-air DVB-T2 broadcast. The independent 66 MHz clock, used in the model, is now replaced with a 66 MHz PLL which phase-locks to the 6 MHz MPEG TS parallel clock; note that the 6 MHz clock also acts as the master reference clock for the entire system. At the optical interfaces of the transmitter and receiver, the Gaussian filter approximation and voltage controlled current source blocks, which were used to electrically model the optical channel, are replaced with the LED and PD devices. The

logic analyser, which in the model acted as the data sink enabling the analysis of the system digital logic levels, is replaced with the Bush DH2636 STB that provides MPEG TS decoding and HDMI connectivity to the HD monitor. Figure 6-1 also highlights the key semiconductor devices used to realise each subsystem (shown in bold black text), and introduces a 'time delay' block, indicated by the grey blocks containing the initials 'TD', which provides fixed time delays in the IOPPM, 6 MHz, 66 MHz and load pulse paths that are hardwired between the transmitter and receiver. The purpose of the delay blocks is to compensate for asymmetrical propagation delays introduced by the digital circuits, and ensures that the optical transmission and hardwired paths are synchronised, thus enabling correct clocking and decoding at the receiver. The delays are realised in the digital domain, and are therefore implemented in the FPGA, along with the rest of the digital subsystems blocks (highlighted in pink) in the architecture.

In terms of the order of implementation, the digital subsystems are implemented first, followed by the analogue subsystems. The reason for this approach is that testing and optimisation of the analogue subsystems is completely dependent on IOPPM+ and IOPPM- signal paths generated by the FPGA. The sequence of implementation is to first generate the FPGA logic circuitry for the IOPPM encoder and decoder, and secondly, generate the transmitter and receiver analogue circuitry.

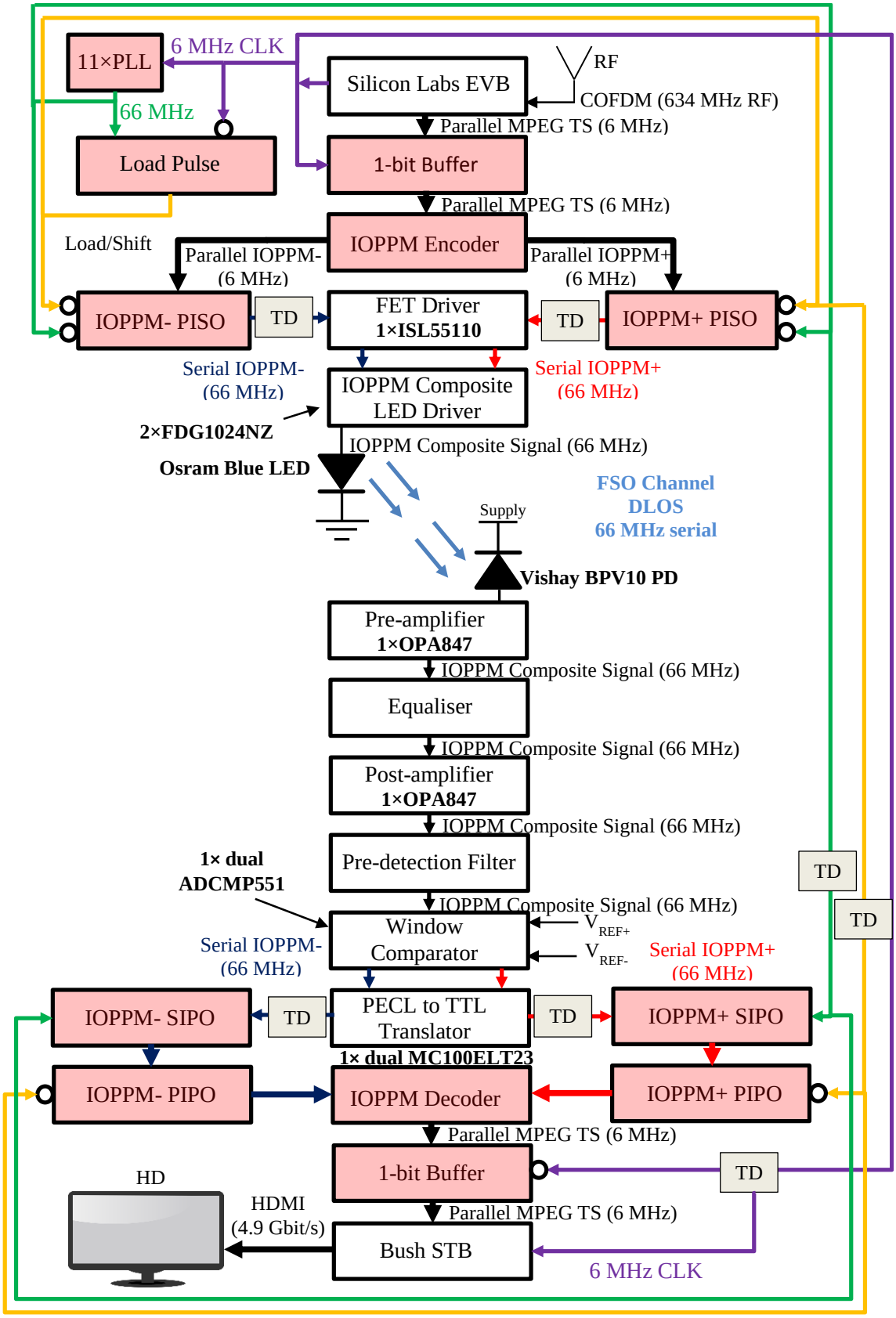


Figure 6-1 Final end-to-end system architecture

6.2 Digital Subsystem Implementation

The digital subsystems designed in Chapter 5 were transferred to a commercial FPGA design environment called Altera Quartus II. The IOPPM encoder and decoder combination logic circuits and sequential buffer, PISO, SISO and PIPO circuits designed in Chapter 5, were all recreated in the Quartus II environment using schematic based logic primitives for AND, OR and NOT gates, and the D-type flip-flop schematic primitive for the sequential circuits. The subsystems were constructed using hierarchical blocks which enabled the modularised testing and verification of the individual subsystems, prior to their assembly in the overall system. Figure 6-2 shows the hierarchical end-to-end digital subsystems constructed within the Quartus II environment. The IOPPM encoder and IOPPM decoder, which are partitioned by dotted boxes in the figure, are connected together by the serialised IOPPM+ and IOPPM- paths and the 6 MHz, 66 MHz and load pulse signals; note that the time delay blocks are shown in each of the signal paths that cross partitions. Testing of the end-to-end system is possible by applying a 10-bit stimulus/pattern at the input to the encoders buffer, and monitoring the 10-bit bus that emerges at output of the decoders buffer.

Note that all circuit construction and simulation was performed using Altera Quartus II 64-bit Version 13.1.0, build 162 23/10/2013 SJ Web Edition.

The intention was to implement the IOPPM encoder and decoder digital subsystems in separate FPGAs to completely separate the transmitter and receiver systems, however, in order to simplify the hardwiring of the 6 MHz, 66 MHz and load pulse paths, both digital subsystems were implemented in the same FPGA; in this case an Altera Cyclone III FPGA development board, fitted with an EP3C120F7807N device. This approach

reduced the external wiring required by the system, and thereby reduced signal degradation from cable loses and ingress of noise and interference signals.

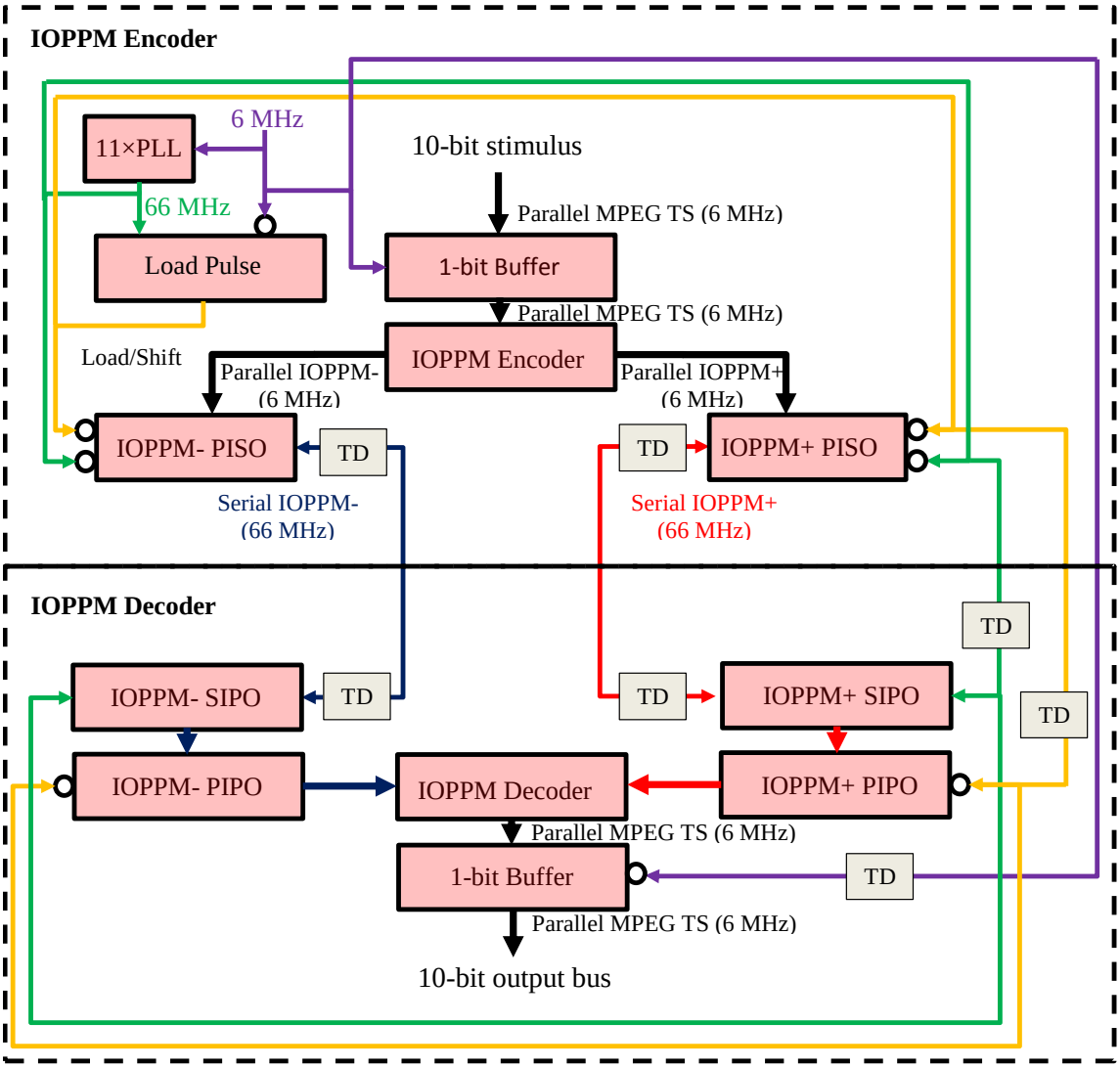


Figure 6-2 Quartus II hierarchical IOPPM encoder/decoder end-to-end system

6.2.1 PLL

The 66 MHz serial clock was also designed as a hierarchical block using the Quartus II ALTPLL megafunction. The 6 MHz MPEG TS clock from the Silicon Labs EVB was used as the input reference to the PLL, and scaled by a factor of eleven, resulting in an output of 66 MHz. The clock was also configured to have a 50% duty cycle and zero phase shift relative to the 6 MHz reference. The hierarchical block of the 66 MHz PPL

is shown in Figure 6-3, and the complete design settings for the PLL are shown in Appendix K.

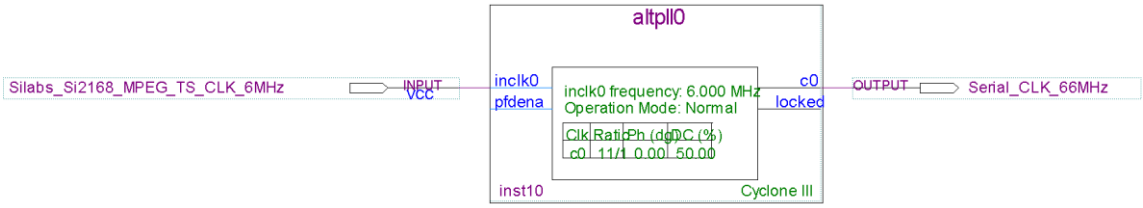


Figure 6-3 66 MHz PLL block

6.2.2 Digital Path Delay Calibration

The time delay hierarchical block (Figure 6-4), which was used to calibrate the transmitter and receivers IOPPM, 6 MHz, 66 MHz and load pulse paths, was designed using the LCELL primitive (Figure 6-5), which is a buffer that has a fixed propagation delay of approximately 197 ps. By cascading multiple LCELL buffers together, it is possible to create fixed length delays in the system in multiples of its 197 ps propagation delay. Note, that the 197 ps propagation was based on the average delay of a pulse propagating through a cascade of three hundred LCELLs.

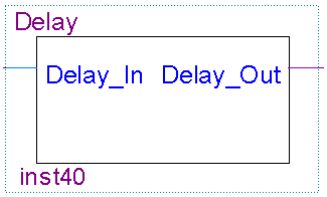


Figure 6-4 Time delay block

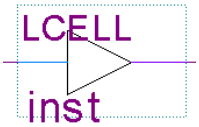


Figure 6-5 single LCELL primitive

6.2.3 Parallel MPEG TS and FPGA Compatibility

The FPGA implementation of the IOPPM encoder and decoder end-to-end system, was tested using the Silicon Labs EVB (data source) and Bush DH2636 STB (data sink). Interfacing of the MPEG TS buses to the FPGA was established using TTL logic levels described in Chapter 4. Figure 6-6 illustrates the end-to-end test configuration, where the pink and grey blocks are implemented inside the FPGA, and white blocks, representing the EVB and STB, are external devices interfaced to the FPGA via 10-bit parallel buses.

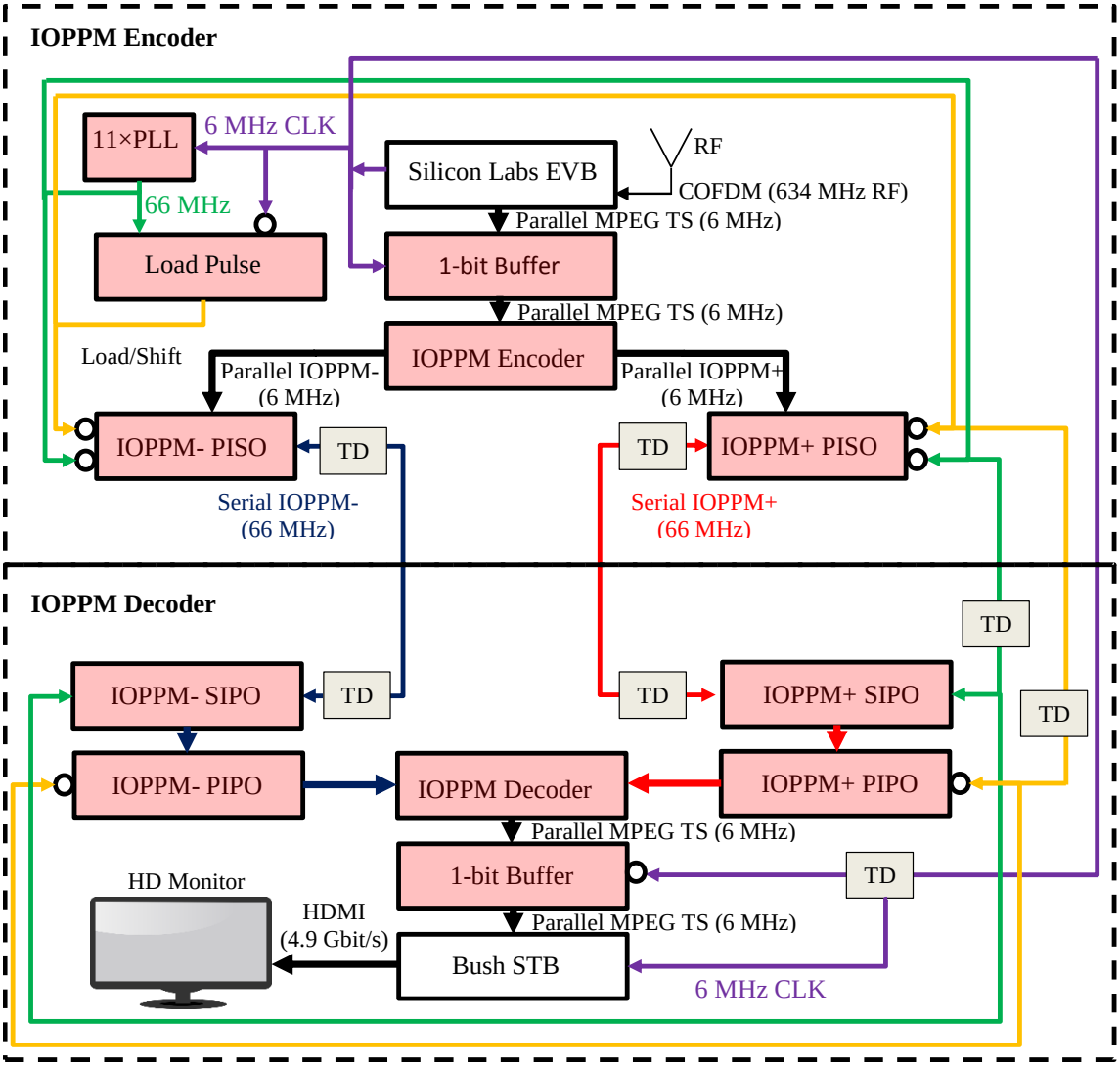


Figure 6-6 Digital only end-to-end test configuration

The serialised IOPPM+ and IOPPM- paths, and 6 MHz, 66 MHz and load pulse paths, are all routed between the encoder and decoder inside the FPGA.

The physical test configuration of the digital subsystems is shown in Figure 6-7. The RF signal carrying the off-air DVB-T2 channel is applied at the 'RF input' of the Silicon Labs EVB, and is down-converted and demodulated to recover the 6 MHz parallel MPEG TS (pre-IOPPM encoded). The 6 MHz parallel clock and 10-bit MPEG TS are input to the FPGA where the MPEG TS is IOPPM encoded and serialised. The hardwired buses connecting the encoder to the decoder, enabled conducted transmission of the IOPPM streams and other signals to the decoder. At the decoder the IOPPM streams are deserialised, IOPPM decoded, and the recovered 10-bit MPEG TS and 6 MHz parallel clock (post-IOPPM decoded) presented to the Bush DH2636 STB where the required programme ID is selected, MPEG decoded, and output in HDMI format to enable reproduction on the HD monitor.

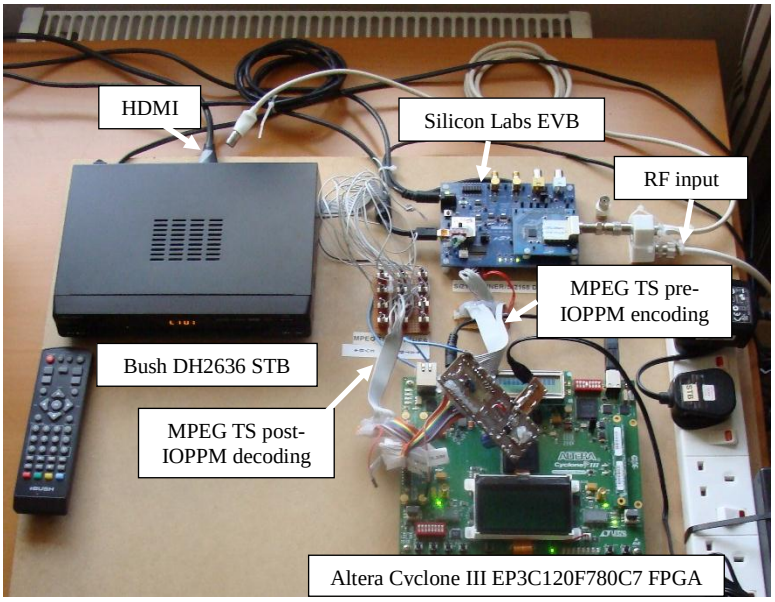


Figure 6-7 Digital only end-to-end physical test configuration

The test configuration was used to successfully IOPPM encode and decode a live off-air DVB-T2 broadcast, confirming the correct operation of the logic interfacing between the EVB and STB and the FPGA implementation of IOPPM subsystems. Verification of the digital architecture permitted implementation of the analogue subsystems to commence.

6.3 Analogue Subsystem Implementation

The analogue subsystems were divided into three modules; the first a transmitter module, containing the LED, FET driver and IOPPM composite LED driver subsystems; the second a receiver module, containing the PD, pre-amplifier, equaliser, post-amplifier and pre-detection filter subsystems; and the third a comparator module, containing the window comparator and differential PECL to TTL translator subsystems. The receiver and comparator modules were specifically kept separate to prevent digital noise and spurious from the comparator circuit from coupling into the sensitive receiver circuits and causing distortion of the low level signals, particularly in the pre-amplifier. The modularised approach also enabled the transmitter and receiver circuits to be housed in shielded boxes to prevent RF radiated coupling between the transmitter and receiver, ensuring that signal transmission was only over the optical channel. The modules were constructed using low-cost, off-the-shelf components, predominantly surface-mount devices (SMD), in order to keep the PCB surface area of the circuits small and the interconnecting traces between circuits short to reduce losses. SMD passive components covering the size ranges of 0402, 0603 and 0805 were also used to reduce parasitic effects. All PCBs were fabricated using FR-4, double-sided copper (35 μm copper thickness) due to its low-cost and availability. Two-layer ground-plane techniques were also used to achieve low impedance ground returns and reduce ground loops.

6.3.1 Transmitter Module

The transmitter circuit, shown in Figure 6-8, consists of two analogue subsystems: the FET driver and the IOPPM composite LED driver, which were designed in Chapter 5, section 5.3.1. Both circuits were constructed in cascade on single PCB, using the initial component values shown in the figure, and additional capacitive decoupling components and linear power supply regulation circuitry, which are not shown for clarity. Using a single +12 V supply rail to power the transmitter module, two linear voltage regulators were used to provide a +5V and a +3V3 rails to power FET driver and IOPPM composite LED driver. The use of a single +12 V supply reduced the number of laboratory power supplies needed to power the VLC system, and also reduced the effect of earth loops. The complete transmitter circuit schematic, PCB layout and bill-of-materials (BOM) is provided in Appendix L.1.

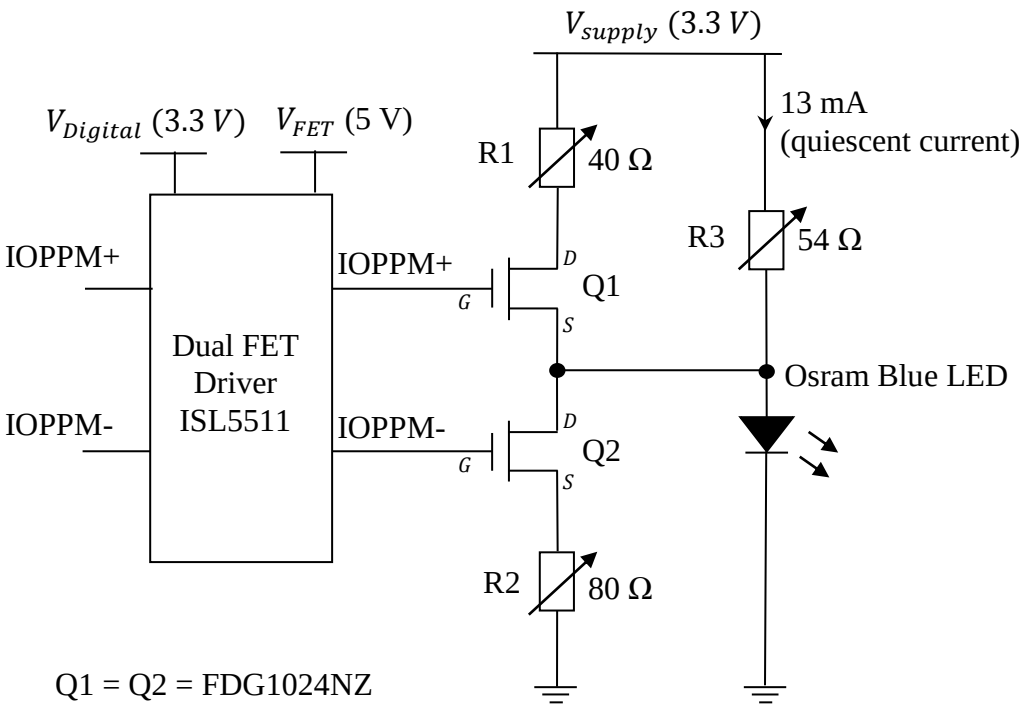


Figure 6-8 Transmitter schematic

The physical implementation of the transmitter circuit is shown in Figure 6-9. The IOPPM+ and IOPPM- signals are input to the transmitter circuit via SMA connectors, which are connected to the output of the FPGAs IOPPM encoder via coaxial cables (50 Ω characteristic impedance); coaxial cable interconnection reduces unwanted signal ingress and egress. The IOPPM signals are then applied to the FET driver via orthogonal, short, equal length transmission lines, where the orthogonality reduces crosstalk between paths, the short traces reduces insertion loss, and equi-length traces ensures synchronisation. The outputs of the FET driver are then fed to their respective FETs: IOPPM+ is fed to Q1 with bias control provided by R1, and IOPPM- is fed to Q2 with bias control provided by R2. The output bias of the FETs is connected to the LED anode at a common junction. The quiescent current of the LED is set by R3.

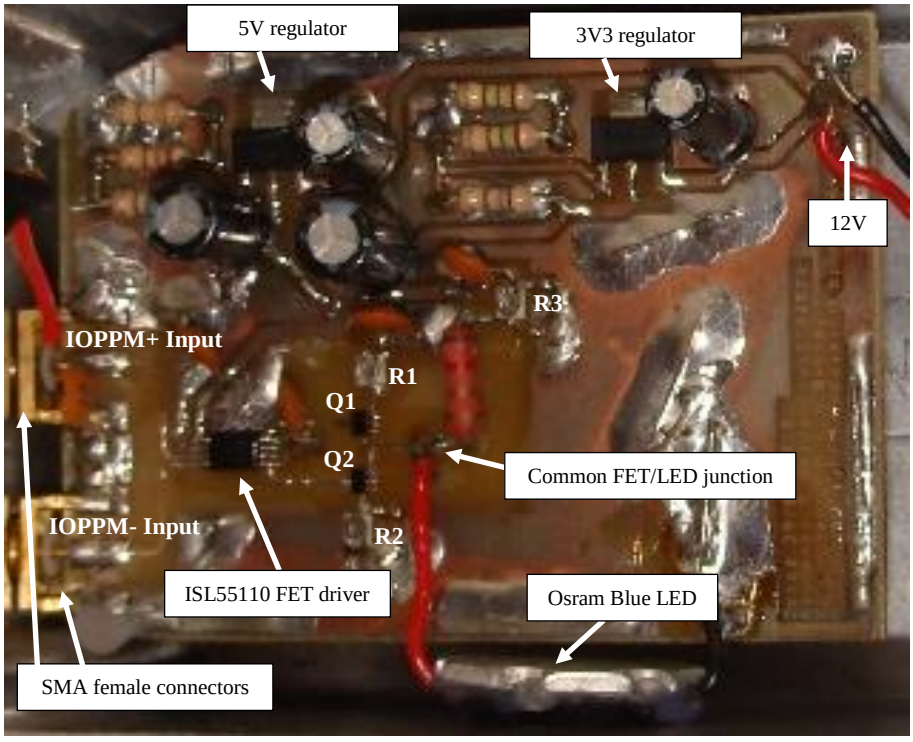


Figure 6-9 Transmitter physical circuit

Using the initial component values shown in Figure 6-8, the transmitter circuit was aligned to provide the necessary bias currents for the LED, as determined in Chapter 5: 26 mA for IOPPM+ pulses, zero current for IOPPM- pulses, and 13 mA for the quiescent state. The quiescent current was determined by applying logic zeroes to both IOPPM inputs, switching both Q1 and Q2 off, and adjusting R3 until a 13 mA current flowed through the LED; this occurred with an R3 value of 52.3 Ω. The bias for an IOPPM+ pulses of 26 mA was determined by applying a logic one to the IOPPM+ input and logic zero to the IOPPM- input, turning Q1 on and Q2 off, and adjusting R1 until a 26 mA current flowed through the LED; this occurred with an R1 value of 39.1 Ω. Finally, the bias for the IOPPM- pulses of zero current was determined by applying a logic zero to the IOPPM+ input and logic one to the IOPPM- input, turning Q1 off and Q2 on, and adjusting R2 until zero current flowed through the LED; this occurred with an R2 value of 82.5 Ω - note that a slight leakage current of 15 μA was measured flowing through the LED at this setting. Figure 6-10 shows the final bias resistor values applied to the transmitter circuit. The values closely match the design values determined in Chapter 5, and the differences were attributed to imperfect regulated value of the +3V3 rail and variations in the FET and LED characteristics.

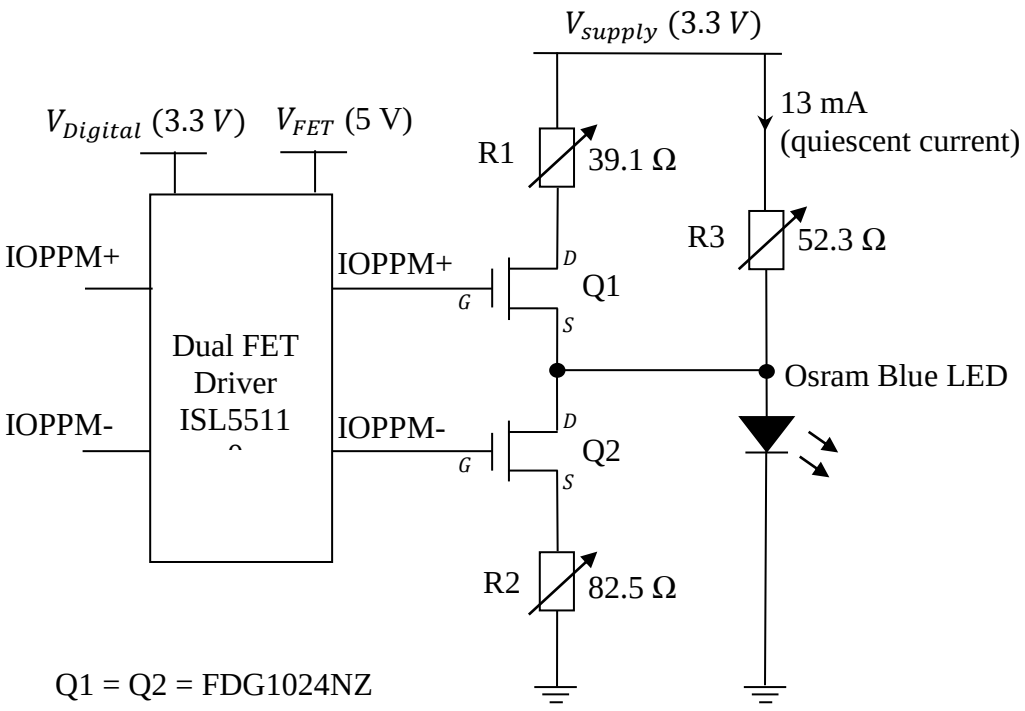


Figure 6-10 Final transmitter schematic

The optimised transmitter circuit was fitted into a shielded housing and mounted on to the optical rail as shown in Figure 6-11. A lens, having a focal length of 135 mm, was placed in front of the transmitting LED, forming part of the DLOS collimation arrangement between the transmitter and receiver described in Chapter 2, section 2.4.2.

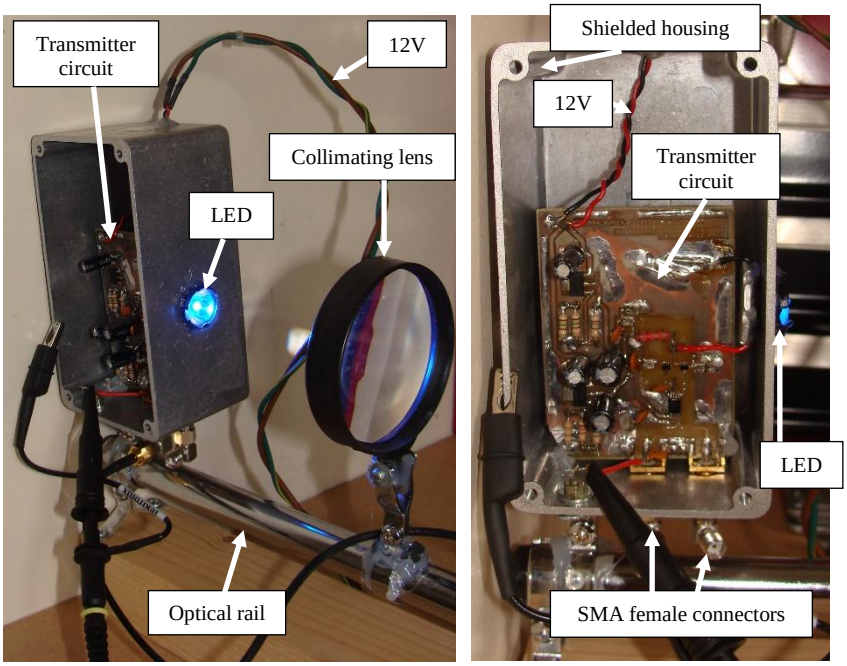


Figure 6-11 Optical rail mounted transmitter module

6.3.2 Receiver Module

The receiver circuit, shown in Figure 6-12, consists of four analogue subsystems: the pre-amplifier, equaliser, post-amplifier and pre-detection filter, which were designed in Chapter 5. All four subsystems were constructed in cascade on single PCB, using the initial component values shown in the figure, and additional capacitive decoupling components and linear power supply regulation circuitry, which are not shown for clarity. In this case, the module uses two power supply rails: a -12 V rail, which reverse biases (V_R) the PD, setting its capacitance to 3 pF, in order to achieve the pre-amplifiers frequency response determined in Chapter 5; and a +12 V supply rail, which using two linear regulators, is used to generate the +5 V and the -5 rails required by the op-amps. The complete receiver circuit schematic, PCB layout and bill-of-materials (BOM) is provided in Appendix L.2.

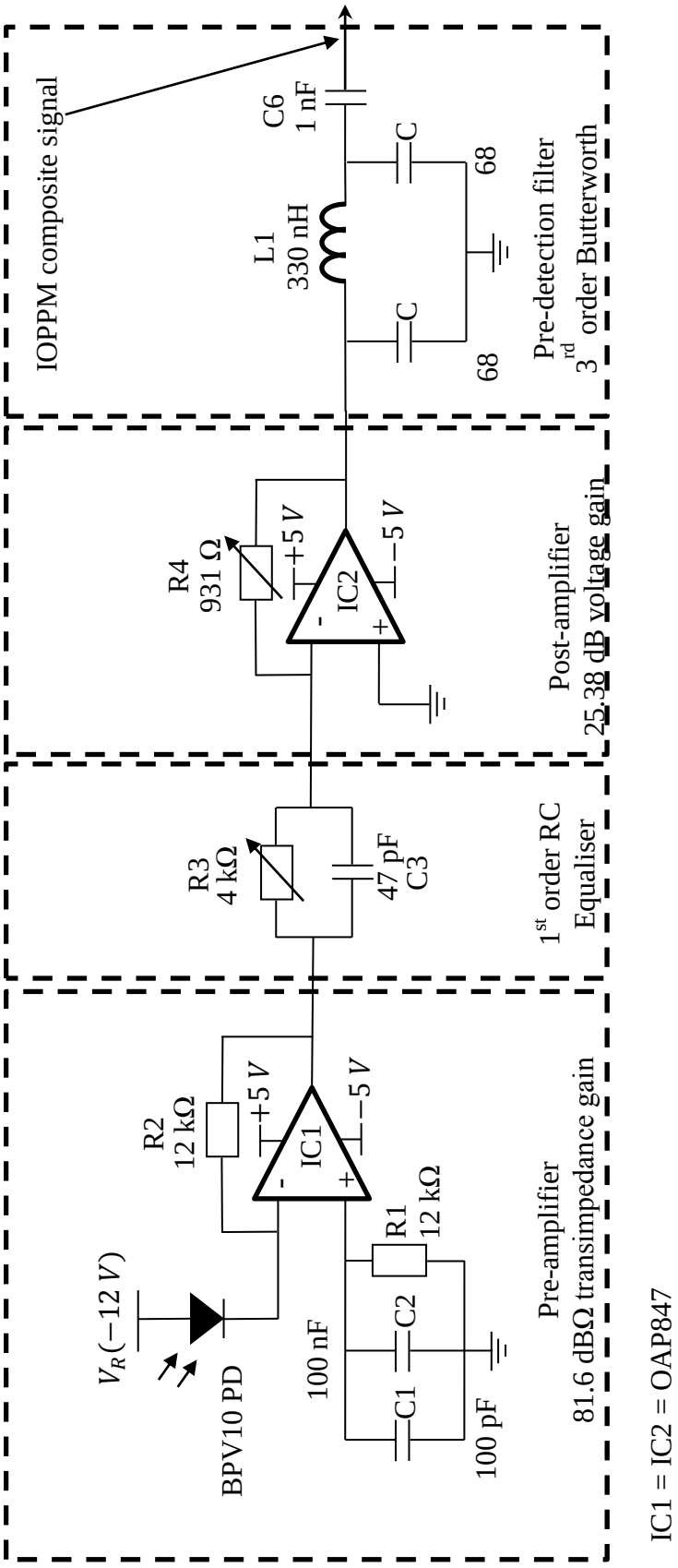


Figure 6-12 Receiver schematic

The physical implementation of the receiver circuit is shown in Figure 6-13. The optical IOPPM signal is received by the PD, which produces the photocurrent that feds the pre-amplifier (IC1); a short length of transmission line is used between the PD and pre-amplifier to ensure minimal insertion loss. The pre-amplifier provides a transimpedance gain of 81.6 dBΩ, and converts the photocurrent into a voltage which is fed to the passive 2nd order RC equaliser formed by R3 and C3, where R3 is variable to enable optimisation during testing. Following equalisation, the signal is passed to the post-amplifier (IC2) which provides voltage gain of 25.38 dB, set by R4 (931 Ω) feedback resistor and Rin (50 Ω not shown in the schematic); note that R4 is variable to enable gain optimisation during testing. Finally, the signal is low-pass filtered by the pre-detection filter formed by L1, C4 and C5. The signal is then AC coupled through C6 to the SMA connector (50 Ω characteristic impedance). A male-to-male SMA adaptor is then used to interconnect the receiver and comparator modules.

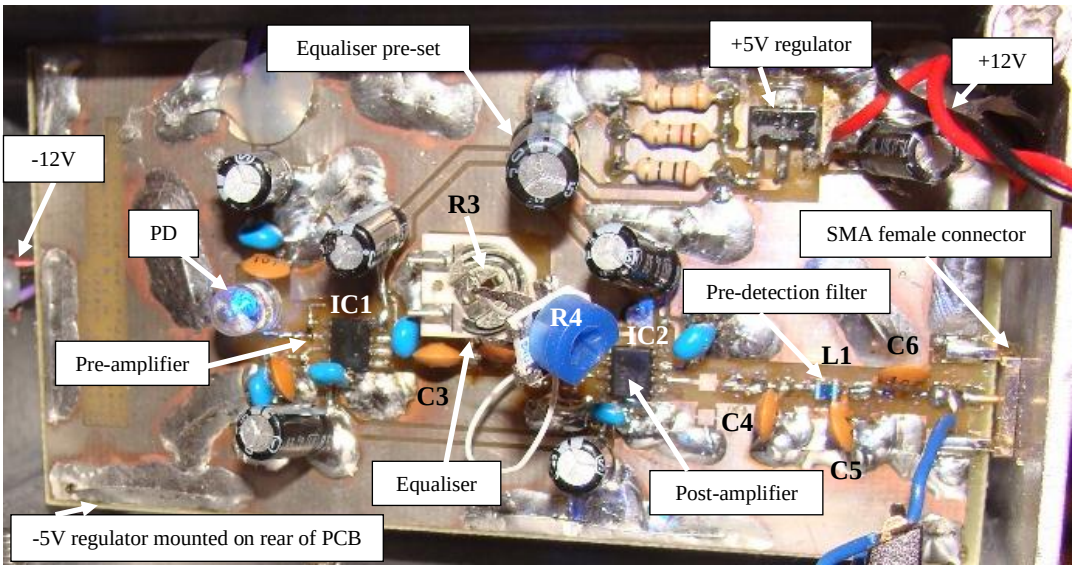


Figure 6-13 Receiver physical circuit

In terms of aligning the receiver circuit, the PD, pre-amplifier and equaliser cascade were already aligned using the prototype circuit described in Chapter 5, therefore the

component values of these three stages did not require further alignment. However, the voltage gain of the post-amplifier, which ensures that the IOPPM composite signal is centred correctly in window comparators input range of 0 V to 1 V, is adjusted using R4 to compensate for changes in the received optical power. If the gain is not set correctly, the input to the window comparator will either be too large resulting in distortion, or too small resulting in low SNR, both of which can lead to pulse detection errors. Usually, receiver systems of this type use automatic-gain control (AGC) to ensure that the input voltage to comparator is maintained, but since additional power detection and decision circuitry is required to provide AGC, this was not employed since it was beyond the scope of this work. Instead manual adjustment of the post-amplifier stage is used, with the initial value gain set at 25.38 dB.

Following alignment, the receiver circuit was fitted into a shielded housing and mounted on to the optical rail as shown in Figure 6-14. A lens, also having a focal length of 135 mm, was placed in front of the receiving PD to complete the DLOS collimation arrangement between the transmitter and receiver.

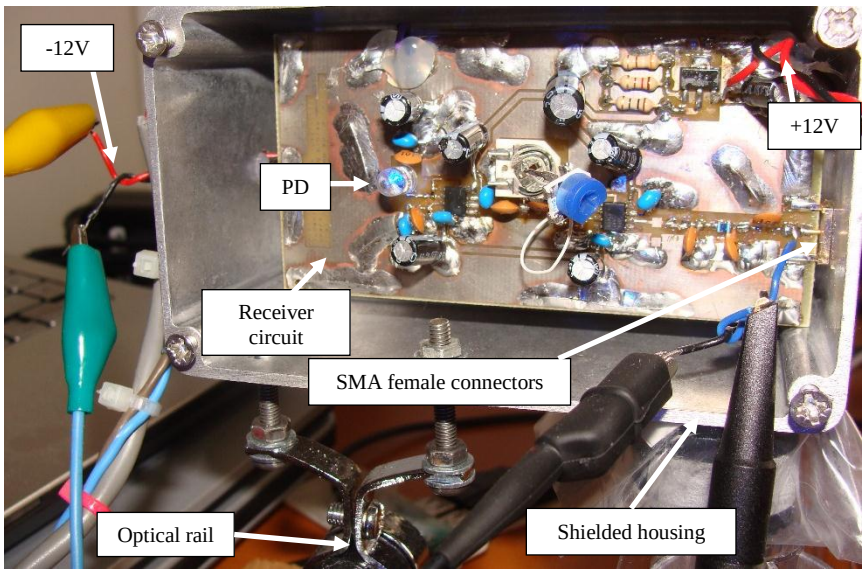
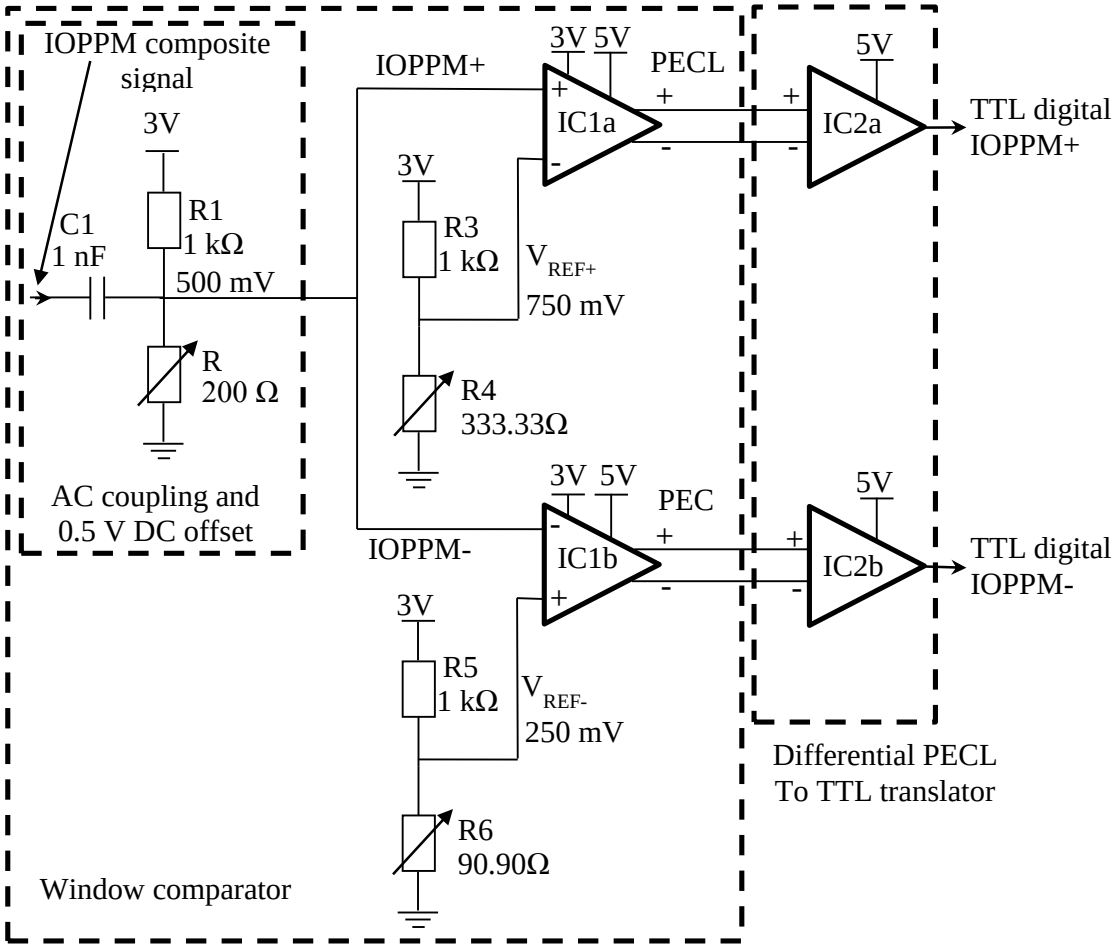


Figure 6-14 Optical rail mounted receiver module

6.3.3 Comparator Module

The comparator circuit, shown in Figure 6-15, consists of two analogue subsystems: the window comparator and the differential PECL to TTL logic translator, which were designed in Chapter 5.



IC1a/IC1b = ADCMP551 (dual comparators in single package)

IC2a/IC2b = MC100ELT23 (dual translators in single package)

Figure 6-15 Comparator schematic

The IOPPM composite signal is applied to the AC coupling and 0.5 V DC offset circuit which centres the IOPPM signal in the 0 V to 1 V range of the window comparator. The window comparator is is formed by IC1, a dual comparator IC, where the IOPPM+ comparator is formed by IC1a and IOPPM- comparator is formed by IC1b. The

IOPPM+ pulse threshold detection voltage ($V_{REF+} = 0.75\,V$) is set by R3 and R4, and IOPPM- voltage ($V_{REF-} = 0.25\,V$) by R5 and R6. Following dectection, the differential PECL outputs of the window comparators are fed to the PECL to TTL translator IC (IC2), which contains dual comparators. IC2a translates the IOPPM+ path and IC2b the IOPPM- path. The translated signals are then output from the module and are made available at the FPGA for IOPPM decoding.

Both subsystems were constructed in cascade on single PCB, using the initial component values shown in the figure, and additional capacitive decoupling components and linear power supply regulation circuitry, which are not shown for clarity. In this case, the module uses two power supply rails: a +3 V rail, used to set the window comparator (IC1) input range, and a +5 V rail to set the comparator PECL output voltage (IC2). The rails are derived using two linear regulators which are supplied by a +12 V rail. The complete comparator circuit schematic, PCB layout and bill-of-materials (BOM) is provided in Appendix L.3.

Figure 6-16 shows the physical implementation of the circuit. The IOPPM composite signal enters the comparator via an SMA female connector shown on the right-hand-side of the figure, and is coupled into the circuit via C1. The 0.5 V DC bias is applied to the signal by R1 and R2 potential divider and is then applied to the IOPPM+ and IOPPM- comparators contained within IC1. The comparator threshold voltages of which are set by R4 and R6, respectively. Following detection, the digital IOPPM+ and IOPPM- streams emerge from IC1 in differential PECL format and then are applied to IC2 which performs PECL to TTL translation. Finally, the TTL logic levels emerge from IC2 and are output from the module via two SMA female connectors which are then connected to the FPGA IOPPM decoder inputs via coaxial cable (50 Ω characteristic impedance).

A 50 Ω terminating termination was used at the input to the FPGA to impedance match the coaxial cable.

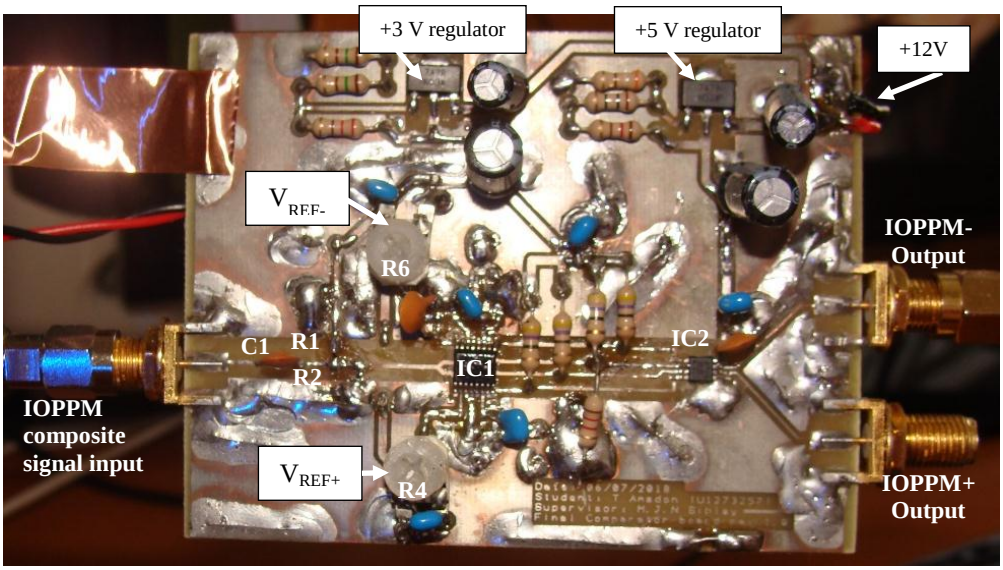


Figure 6-16 Comparator module

The circuit was aligned using the initial component values established in the design described in Chapter 5. The 0.5 V mid-point of the window comparators input range was set by adjusting R2, and was achieved with an R2 value of 198.4 Ω, versus an ideal of 200 Ω. The V_{REF+} of 0.75 V was set by adjusting R4, and was achieved with an R4 value of 335.1 Ω, versus an ideal of 333.33 Ω. The V_{REF-} of 0.25 V was set by adjusting R6, and was achieved with an R6 value of 90.6 Ω, versus an ideal of 90.90 Ω. The variations in the final resistor values were attributed to component tolerances and +3 V supply variations.

The aligned comparator board was not fitted inside a shielded housing, as it was deemed by the author as unnecessary given that both the transmitter and receiver modules were already shielded.

6.4 Physical VLC System Integration

Following the implementation of the digital subsystems on the FPGA, and the construction and alignment of the analogue modules, it was possible to integrate all the subsystems to form the overall VLC system. Figure 6-17 shows the physical integration of the digital subsystems. In the figure, the DVB-T2 channel is received via a Yagi array antenna, and is input to the Silicon Labs EVB at the 'RF input'. The EVB provides tuning and demodulation of the DVB-T2 channel, and outputs the 10-bit parallel MPEG TS bus and 6 MHz clock, which are fed to the IOPPM encoder via a ribbon cable, labelled 'MPEG TS pre-IOPPM encoding'. The MPEG TS is encoded in the FPGA, and the 66 MHz serialised IOPPM output is transferred via coaxial cable, labelled 'IOPPM encoder output', to the transmitter module. Following transmission of the signal over the FSO channel and its reception and detection by the respective receiver and comparator modules, the digital output of the comparator is fed back into the FPGA for decoding via another coaxial cable, labelled 'IOPPM decoder input'; note the 50 Ω termination provides impedance matching for the coaxial cable. The serialised digital pulses are clocked into the FPGA using a 66 MHz clock which is aligned with the centre of the received pulses to facilitate central decision sampling. After decoding, the recovered parallel MPEG TS is fed into the Bush DH2636 STB via another ribbon cable, labelled 'MPEG TS post-IOPPM decoding', where the MPEG TS is decoded and the desired PID is selected using the STB remote control channel selection. The raw video and audio content is output on the HDMI interface, enabling its reproduction on an HD monitor.

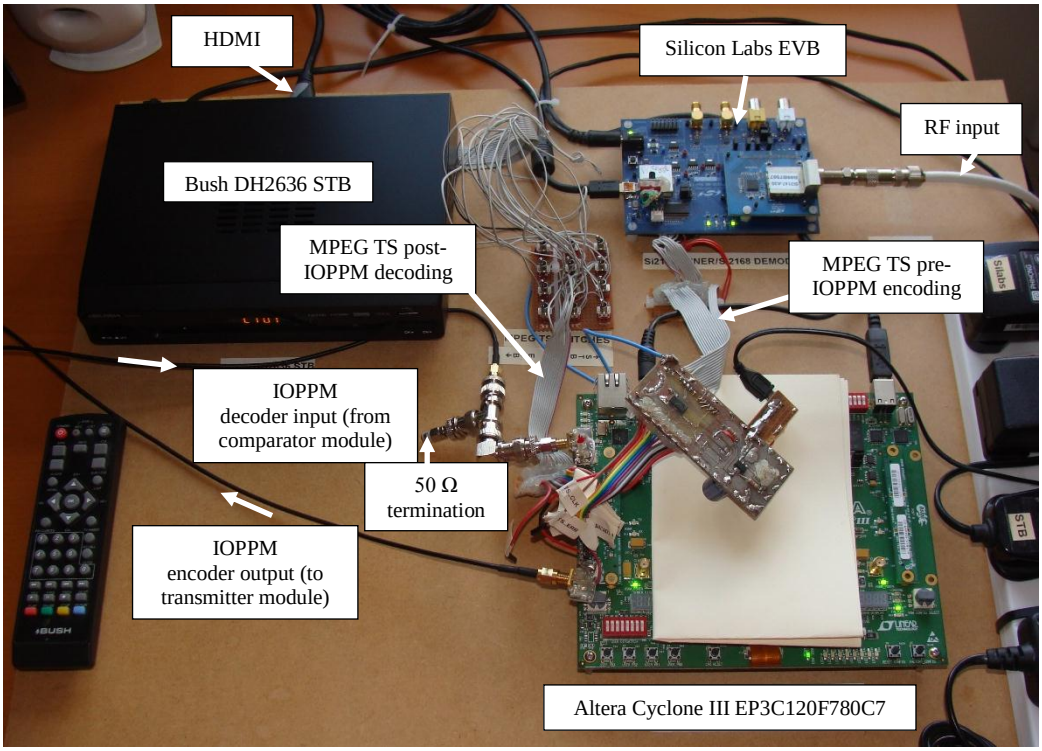


Figure 6-17 Digital modules

It is important to note that Figure 6-17 only shows a single serialised IOPPM stream flowing out of and then back into the FPGA, this is because there was only sufficient space on the FPGA development board to accommodate two SMA interfaces, and not the desired four i.e. one pair of IOPPM encoder outputs, and one pair of IOPPM decoder inputs. The encoder output and decoder input SMA connectors were separated by a distance of 8 cm to reduce crosstalk caused by radiated coupling. Since only one IOPPM channel is transmitted over the FSO, the other IOPPM channel is hardwired between the IOPPM encoder and decoder inside the FPGA as shown in Figure 6-18. The figure shows that the IOPPM+ stream propagates over the FSO channel, whilst the IOPPM- channel is hardwired inside the FPGA in identical arrangement to the 6 MHz, 66 MHz, and load pulse hardwired signals. The IOPPM- path is also delayed in time by the same amount as the other hardwired signals to ensure synchronisation with the IOPPM+ at the receiver. This arrangement means that only one single IOPPM channel can be tested at a

time, and that simultaneous transmission of the IOPPM+ and IOPPM- stream in the composite signal is not possible. However, this arrangement does enable verification of the two LED IOPPM architecture described in Chapter 3, and a partial verification of the single LED IOPPM architecture, since the IOPPM+ and IOPPM- paths are interchangeable within the FPGA, and at the transmitter and comparator interfaces.

6.5 DLOS Optical Rail

The shielded analogue transmitter and receiver modules were mounted on a DLOS optical rail, as shown in Figure 6-19, and the transmitting LED and receiving PD positioned at a distance of 1.2 m apart; this distance was set arbitrarily by the author. The collimation lens, also mounted on the rail, were positioned to enabled sharp focusing of the transmitted light onto the surface of the PD, thus maximising received optical power, and also limiting the irradiance and FOV angles in order to reduce unwanted reflections. The first lens, mounted closest to the LED, is positioned 8.5 cm away from the LEDs surface, and the second, closest to the PD, is positioned 18.5 cm away from the PD surface. The lenses, which have a focal length of 135 mm, are separated by a distance of 93 cm.

6.6 Path Calibration

Prior to testing the system, it was necessary to determine the time delays required by the TD blocks within the system to ensure correct synchronisation of the transmitter and receiver, and in particular, the correct central decision timing needed to clock data output by the comparator module into the decoders SIPO. Path calibration of the system was performed by measuring the propagation delay between the encoder output and the decoder input. This was achieved by loading the encoders 10-bit IOPPM+ PISO with a fixed 10-bit pattern containing a single logic one, clocking it out of the encoder at 66

MHz; and transmitting it over the 1.2 m FSO channel. The received pulse (15.1515 ns duration) was processed by the receiver and comparator modules and input to the FPGA decoder. The propagation delay between the logic one emerging from the encoder and it terminating at the decoder input was measured at approximately 54 ns. The time delay for the IOPPM-, 6 MHz, 66 MHz and load pulse hardwired paths was then calculated by dividing the 54 ns propagation delay by the propagation delay of a single LCELL (197 ps) buffer, which is used to generate the delay in the time delay blocks. This calculation was used to determine the number of LCELL buffers which must be connected in cascade to achieve the required delay. In this case the number of buffers required is 274 to the nearest integer value, which results in a time delay of 53.97 ns. The time delay blocks used to delay hardwired paths between the encoder and decoder inside the FPGA are labelled with the 53.97 ns delays in Figure 6-18; note that no delays are applied to the IOPPM+ encoder or decoder paths, and these are labelled 0 ns in the figure.

The physical arrangements shown in Figure 6-17 and Figure 6-19 constituted the overall VLC system used to perform the proof-of-concept video distribution function described in Chapter 1. The performance of the system was determined by interchanging the data source in the system with either fixed logic sequences generated within the FPGA, or the Silicon Lab EVB and live off-air DVB-T2 content; note that the EVBs 6 MHz clock reference was used to synchronise the system for both FPGA internally generated logic sequences and live off-air distribution.

The results and analysis of the VLC system testing is presented in Chapter 7.

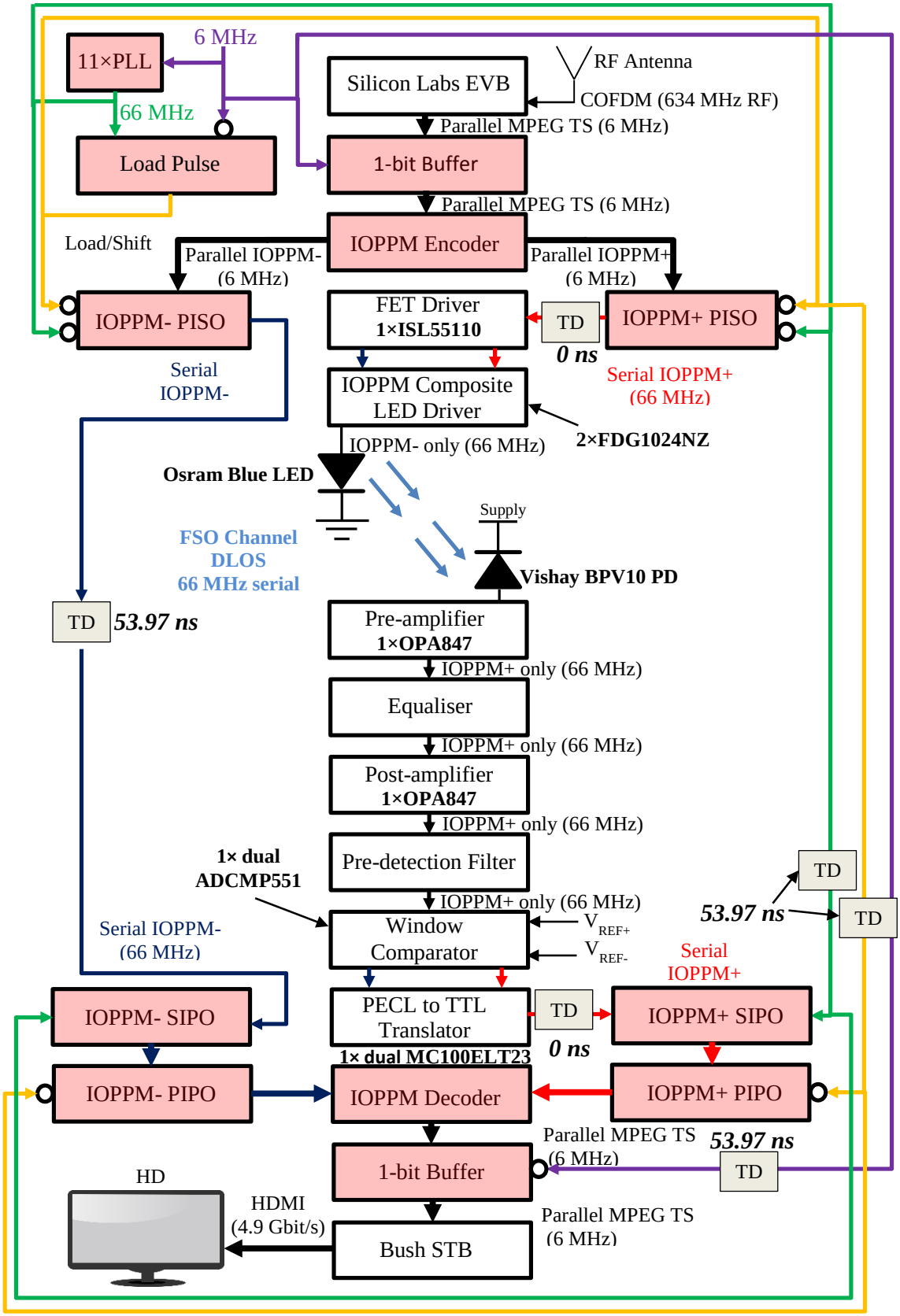


Figure 6-18 End-to-end VLC test system

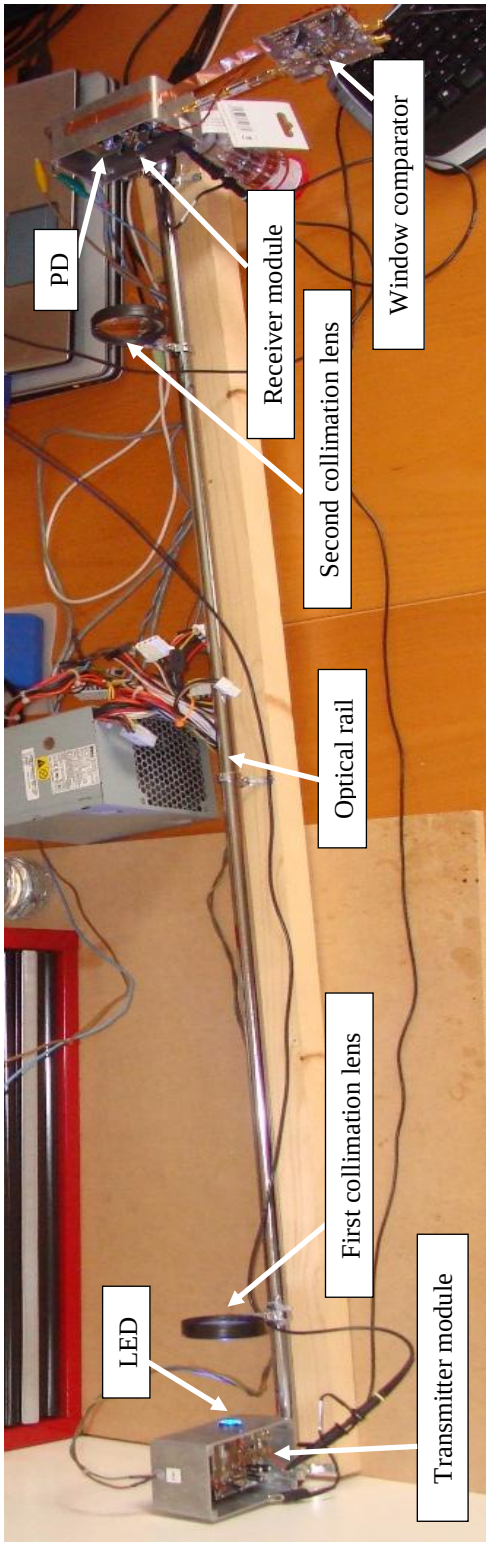


Figure 6-19 Analogue modules and DLOS optical rail

6.7 Conclusions

In this chapter, the implementation of the digital and analogue subsystems, followed by the integration of the subsystems into the overall VLC, was presented.

It was concluded in this chapter that:

- The IOPPM encoder and decoder should be implemented on a single FPGA platform to enable the hardwired IOPPM-, 6 MHz, 66 MHz and load pulse signals from being routed inside the same FPGA, thereby reducing signal loss and exposure to interference.
- A PLL, phase-locked to the 6 MHz MPEG TS clock was necessary to generate the 66 MHz serial clock required by the system. The 6 MHz MPEG TS is the master reference clock for the entire VLC system.
- The implementing the analogue circuitry in three modules: transmitter, receiver and comparator reduced signal ingress and egress. In particular, the transmitter and receiver modules were placed in shielded housings to prevent radiated coupling between the two modules.
- The component values of the aligned physical hardware closely matched the simulated circuit component values, and that variations were most likely attributed to component tolerances and power supply variations.
- Due to a lack of space on the FPGA development board, only one IOPPM channel could be ported out of and back into the FPGA at a time, meaning that simultaneous transmission of the IOPPM+ and IOPPM- stream in the composite signal is not possible. Complete verification of the two LED IOPPM architecture described in Chapter 3 is possible, along with a partial verification of the single LED IOPPM architecture, since the IOPPM+ and IOPPM- paths are

interchangeable within the FPGA, and at the transmitter and comparator interfaces.

- Time delay blocks having a delay of 53.97 ns were necessary to synchronise the hardwired IOPPM-, 6 MHz, 66 MHz and load pulse hardwired signals implemented inside FPGA with the OPPM+ signal propagated over the FSO channel.
- The transmitter and receiver modules were mounted on an optical rail and separated by a distance of 1.2 m. Two collimating lens between the transmitter and receiver were used to sharply focus the transmitted light onto the surface of the PD, thus maximising received optical power, and also limiting the irradiance and FOV angles in order to reduce unwanted reflections. One lens was positioned 8.5 cm from the LED, and a second, 18.5 cm from the PD. Both lenses had a focal length of 135 mm, and were separated by 93 cm.

7 Results and Analysis

This chapter presents the parametric and system level performance of the VLC system. Predominantly, the results presented are in the time domain and are based on parametric measurements of each subsystem. Comparison between the simulated electrical model and hardware results are presented and analysed.

7.1 Time Domain Measurements and Analyses

The time domain measurements were performed using the electrically simulated model, described in Chapter 5, and the physical hardware described in Chapter 6. The measurements were taken at specific test points in the electrical model and physical system configurations and analysed. The measurement points used in the electrical model are shown in Figure 7-1, and are indicated by the red circles which are labelled alphabetically. The hardware test points are also indicated using the same labelling convention in Figure 7-2 and Figure 7-3, and map directly to the equivalent test points in the electrical model. Two physical hardware configurations are required, since the FPGA development board only permits the optical transmission of a single IOPPM channel at a time, as discussed in Chapter 6. Figure 7-2 shows the configuration used when the IOPPM+ channel is transmitted optically and the IOPPM- channel is hardwired from the encoder to the decoder inside the FPGA. Conversely, Figure 7-3 shows the configuration used when the IOPPM- channel is transmitted optically and the IOPPM+ channel is hardwired.

In the electrical model (Figure 7-1), the encoder/transmitter has four test points: A and C, corresponding, respectively, to the IOPPM+ and IOPPM- PISO outputs, and B and D, corresponding, respectively, to the IOPPM+ and IOPPM- FET driver outputs. The

receiver/decoder has six test points: E at the preamplifier output, F at the equaliser output, G at the post-amplifier output, H at the pre-detection filter output, and I and J corresponding, respectively, to the IOPPM+ and IOPPM- comparator outputs.

The hardware test points used in the IOPPM+ optical transmission configuration are identical to the electrical model, except that C, D and J are omitted since the IOPPM- path is hardwired from the encoder to decoder inside the FPGA. Similarly, in the IOPPM- optical transmission configuration, the test points are identical to the electrical model, except that A, B and I are omitted since the IOPPM+ path is hardwired in the FPGA.

Parametric measurements of the simulated model and physical hardware were performed using fixed binary patterns applied at specific points in the encoder circuitry; note that in the physical hardware, the 6 MHz MPEG clock of the EVB was used as the master clock for the FPGA even during fixed binary sequence testing.

Testing of the physical hardware was also performed using live off-air DVB-T2 broadcast to generate an MPEG TS, and this was approximated in the simulated model using a pseudo-random bit sequence to simulate the MPEG TS from a live off-air broadcast. The live off-air DVB-T2 broadcast channel used during testing was Channel 41 (634 MHz) multiplex, received from Emley Moor transmitter in West Yorkshire, UK; note this channel has a QAM 256 constellation, 2/3 code rate, 1/128 guard interval and 32 K FFT. The MPEG TS bit rate was estimated at 40.21 Mbit/s.

Parametric and system level testing was performed using the DLOS optical rail arrangement described in Chapter 6 (Figure 6-19). The distance between the transmitter modules LED and the receiver modules PD was set at 1.2 m.

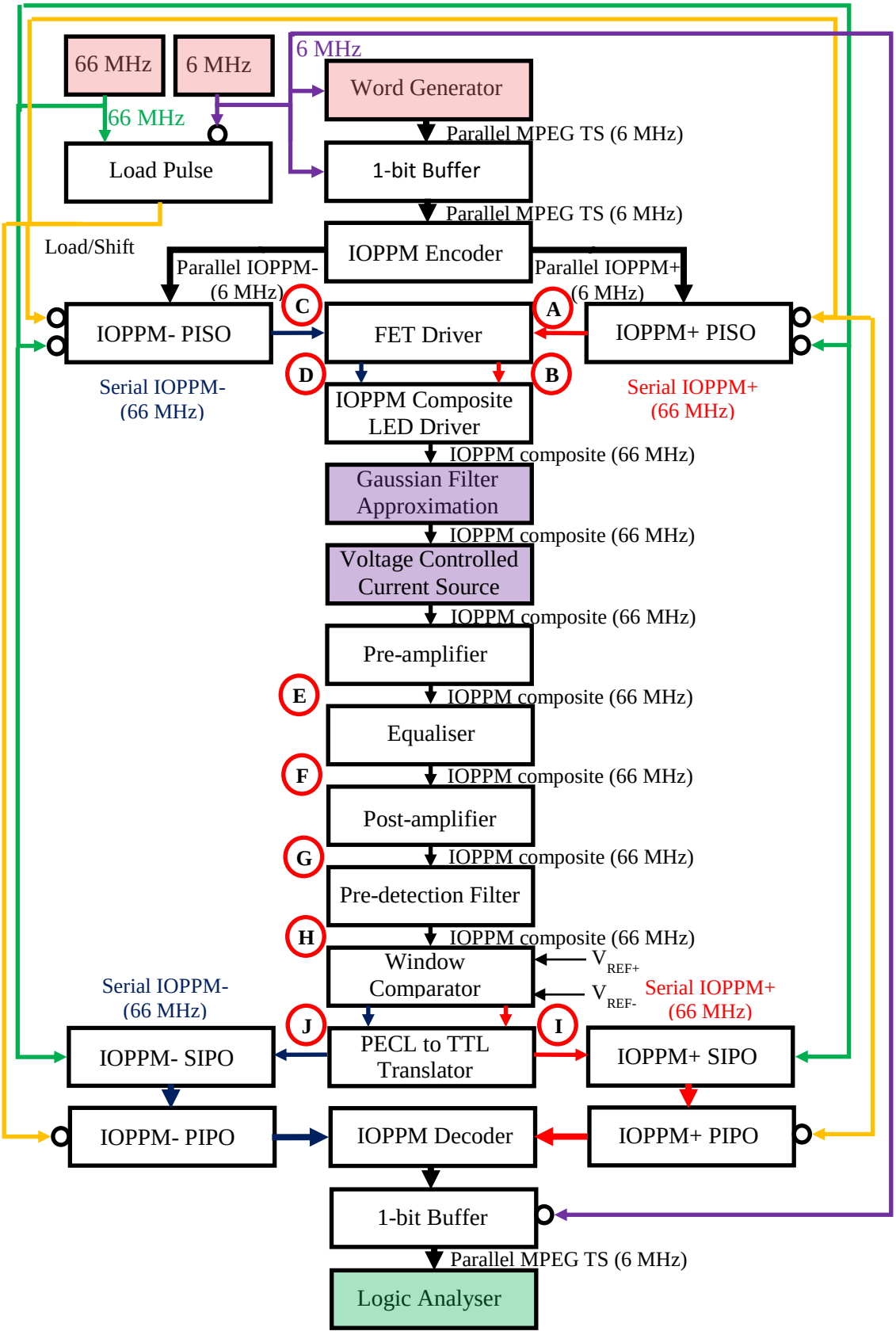


Figure 7-1 VLC electrical model configuration and test points

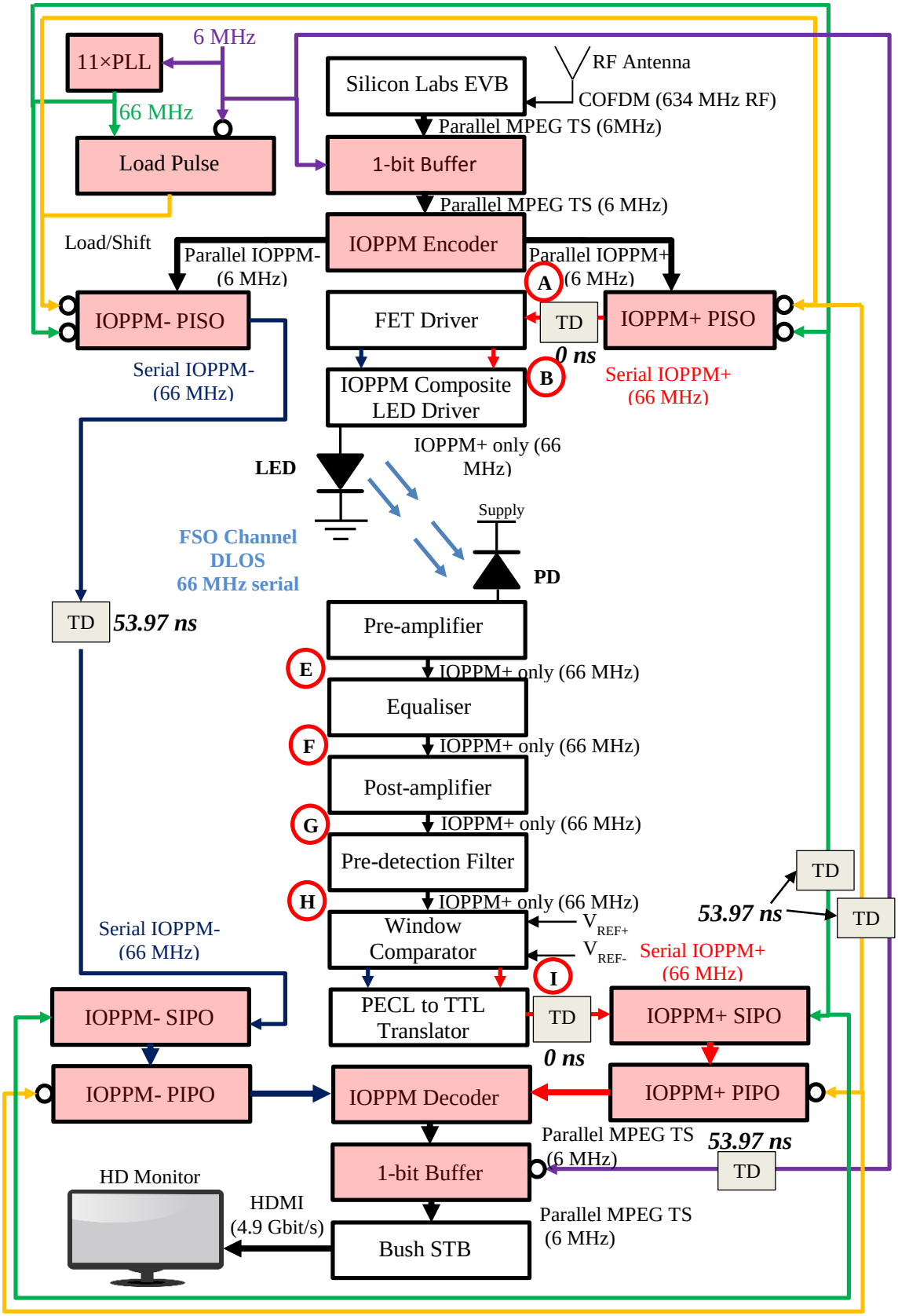


Figure 7-2 VLC IOPPM+ optical transmission configuration and test points

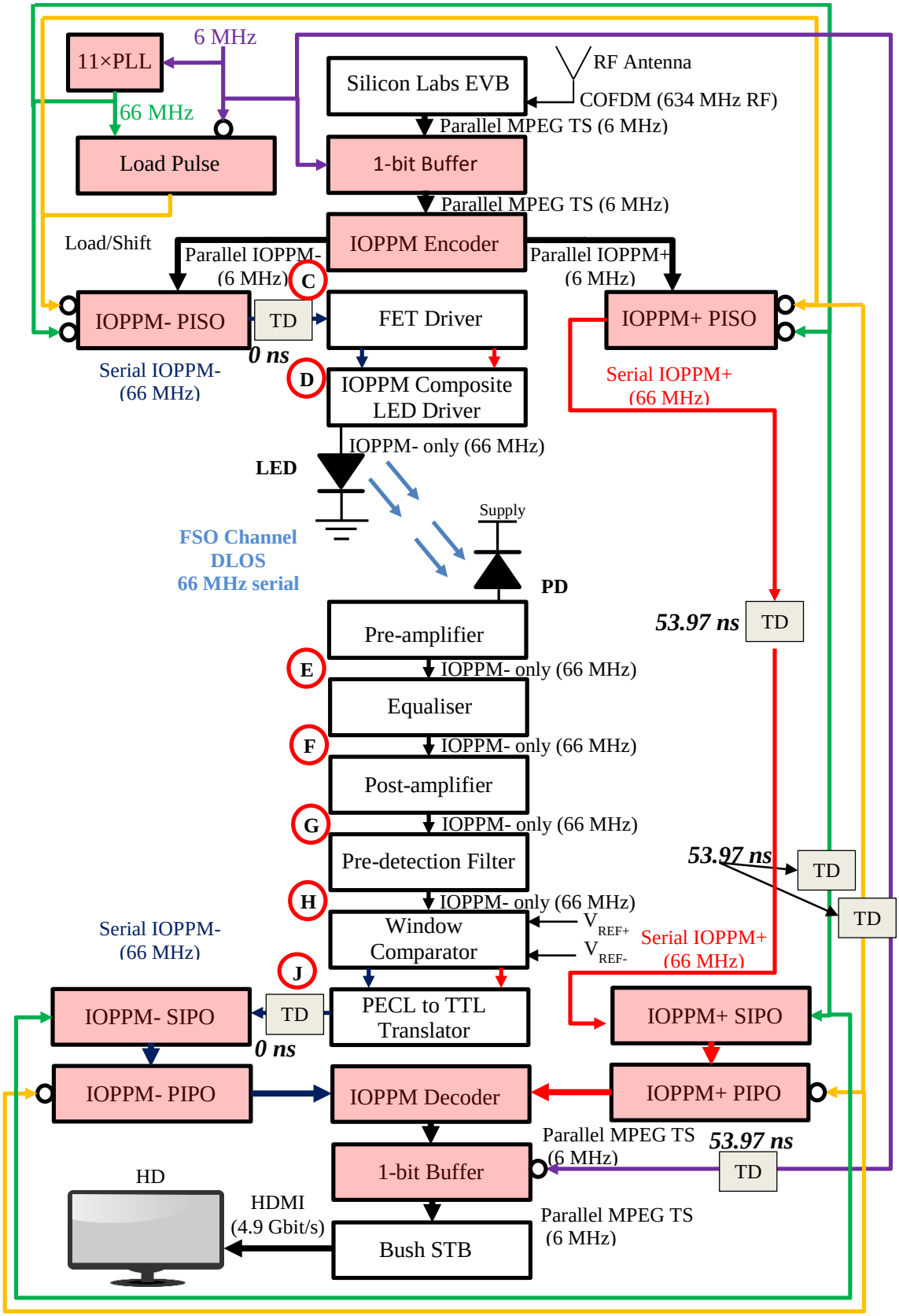


Figure 7-3 VLC IOPPM+ optical transmission configuration and test points

7.1.1 FPGA IOPPM Output Timing (Test points A and C)

The first priority was to measure the timing accuracy of the VLC system, since the timing and duration of pulses in the IOPPM scheme are critical to distinguishing between empty slots and those containing valid pulses. Timing measurements were performed using the electrical model (Figure 7-1) and IOPPM+ hardware configuration (Figure 7-2), in conjunction with a fixed 10-bit binary test pattern which was applied at the parallel input of the transmitters IOPPM+ PISO. The test pattern consisted of a 10-bit sequence arranged thus: $_{MSB}0100100011_{LSB}$. The MSB represented by D9, is the first bit to be clocked out of the PISO, followed in sequence by D8 through D1, until the LSB, represented by D0, is finally clocked out of the PISO; note that the binary test pattern was configured to clock out of the PISO on a continuous repeating cycle. The bit period of the PISO output is defined by the serial clock frequency of 66 MHz, resulting in a slot time of 15.15 ns. Bits D8 and D5 in the test pattern generate single pulses of 15.15 ns duration in the PISO output, whilst D0 and D1 generate a non-return to zero (NRZ) double pulses of 30.30 ns. Figure 7-4 shows the simulated (blue trace) and hardware generated (red trace) outputs measured at test point A in the system. The dotted vertical lines in the figure show the bit periods (D9 through D0) of the test pattern; note that the first time period is the load pulse period which is used to parallel load the PISO. The simulated and hardware timing closely correlates, however, voltage overshoots are present in the single pulses of the hardware output which are due to the 1.52 m length of 50Ω coaxial cable connecting the output of the IOPPM+ PISO to the transmitter module; note that PISO output (test point A) was established at the coaxial cables interface with the transmitter module, and not directly at the output of the FPGA to enable cable degradation to be measured.

Figure 7-5 shows the single pulse, representing one bit period or one slot time (15.15 ns theoretical). The simulated pulse (blue trace) occupies a slot time of 15.2 ns, representing an error of approximately 0.33% on the theoretical value, and the hardware generated pulse (red trace) occupies a slot time of 20 ns, representing an error of approximately 32% on the theoretical value. In effect, approximately 2.4 ns of the hardware generated single pulse overlaps with adjacent slot times. The overlap is insufficient to cause significant ISI in adjacent pulses, since the pulses are centred within the slot time.

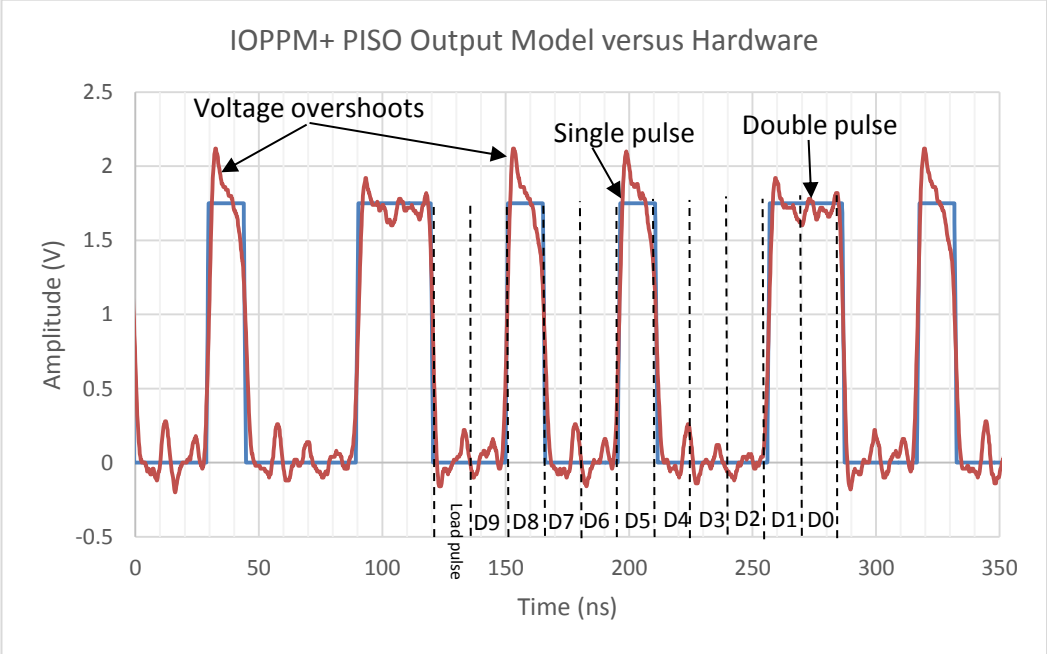


Figure 7-4 IOPPM+ PISO output timing

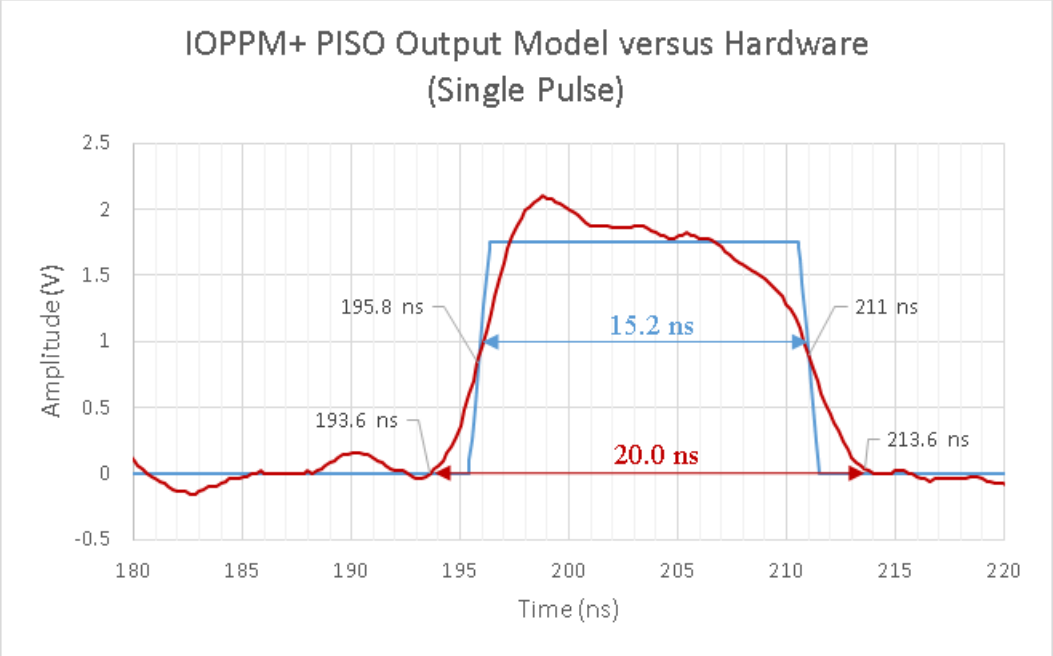


Figure 7-5 IOPPM+ PISO output timing (single pulse)

Figure 7-6 shows the double pulse, representing two bit periods or two slot times (30.30 ns theoretical); note that double pulses occur when two 3-bit IOPPM codewords generate adjacent pulses. In this case, the simulated double pulse (blue trace) occupies two slot times equating to 30.2 ns, which represents an error of approximately -0.33% on the theoretical value. In contrast, the hardware generated pulse (red trace) occupies two slot times equating to 34.4 ns, which represents an error of approximately 13.5% on the theoretical value. In this instance, the double pulse overlaps adjacent slot times by approximately 2 ns, which is again insufficient to cause significant ISI in adjacent pulses. This test verified that the accuracy of the 66 MHz PLL implemented in the FPGA is sufficient to generate IOPPM pulses in the system, and permit central decision detection at the receiver.

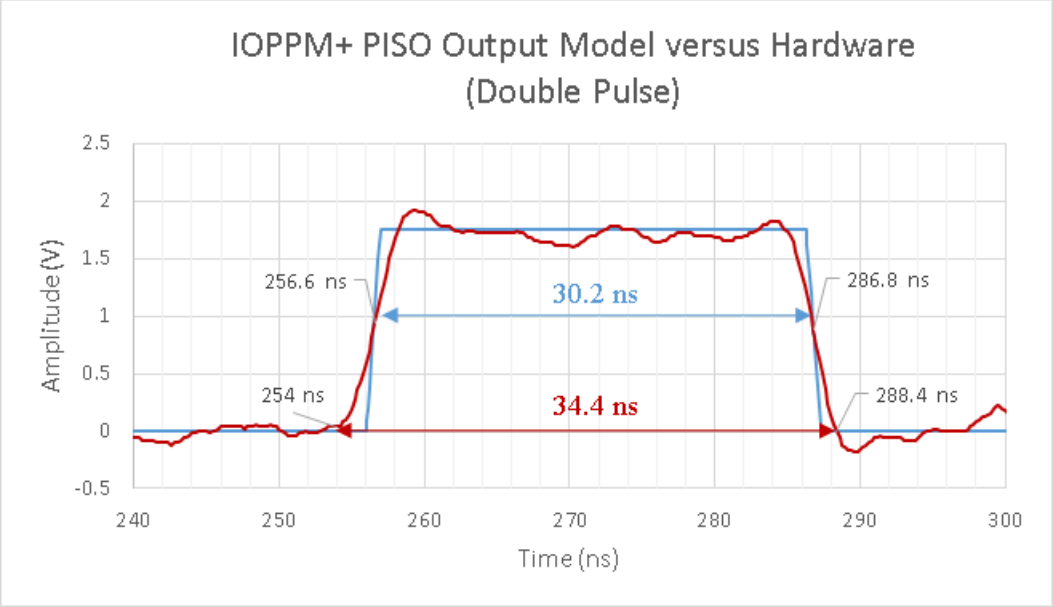


Figure 7-6 IOPPM+ PISO output timing (double pulse)

The timing measurements were then repeated using the electrical model (Figure 7-1), and the IOPPM- hardware configuration (Figure 7-3). The same fixed binary test pattern used to generate single pulses and double pulses in the previous test, were applied at the input to the IOPPM- PISO in the model and hardware configuration and the measurements repeated at test point C. The IOPPM- configuration yielded similar results to the IOPPM+ configuration.

7.1.2 FPGA IOPPM Frequency Domain (Test points A and C)

Following the confirmation of the FPGAs timing accuracy, it was necessary to determine whether the frequency domain response of the IOPPM signal behaved like the sinc function described in Chapter 2. This was achieved in the electrical model (Figure 7-1) by applying a pseudo-random bit sequence at the input of the 1-bit buffer to simulate the MPEG TS of a live off-air DVB-T2 broadcast. In the equivalent IOPPM+ hardware configuration (Figure 7-2), the MPEG TS was derived from the output of the EVB, and applied at the input of the 1-bit buffer. The output of test point A in the model

and hardware was measured in the time domain, and a fast Fourier transform (FFT) applied to enable extraction of the frequency domain response. Figure 7-7 shows the resultant FFT, with the simulated (blue trace) and hardware generated (red trace) responses. The individual frequency components overlay precisely, and as expected, the response behaves like a sinc function. The first zero crossing (null) occurs at the serial clock frequency of 66 MHz and harmonically related nulls at 132 MHz and 197 MHz. The amplitude variations and roll-off above 200 MHz of the hardware generated signal are attributed to coaxial cable, where dispersion causes amplitude variations in frequency components, and the low-pass response of the cable causes the gross roll-off above 200 MHz.

Figure 7-8 shows the zoomed-in overlay of the simulated (blue trace) and hardware generated (red trace) frequency domain responses. In this figure, the individual frequency components are shown equispaced at the parallel MPEG TS clock frequency of 6 MHz; note that the hardware generated frequency domain trace (red trace) appears wider than the simulated trace (blue trace), and is due to the limitation of the measurement instruments FFT resolution.

The FFT measurements were then repeated using the electrical model (Figure 7-1), and the IOPPM- hardware configuration (Figure 7-3) and the same input stimuli. The FFT was derived in this instance from test point C in the model and hardware, and yielded similar results to the IOPPM+ configuration.

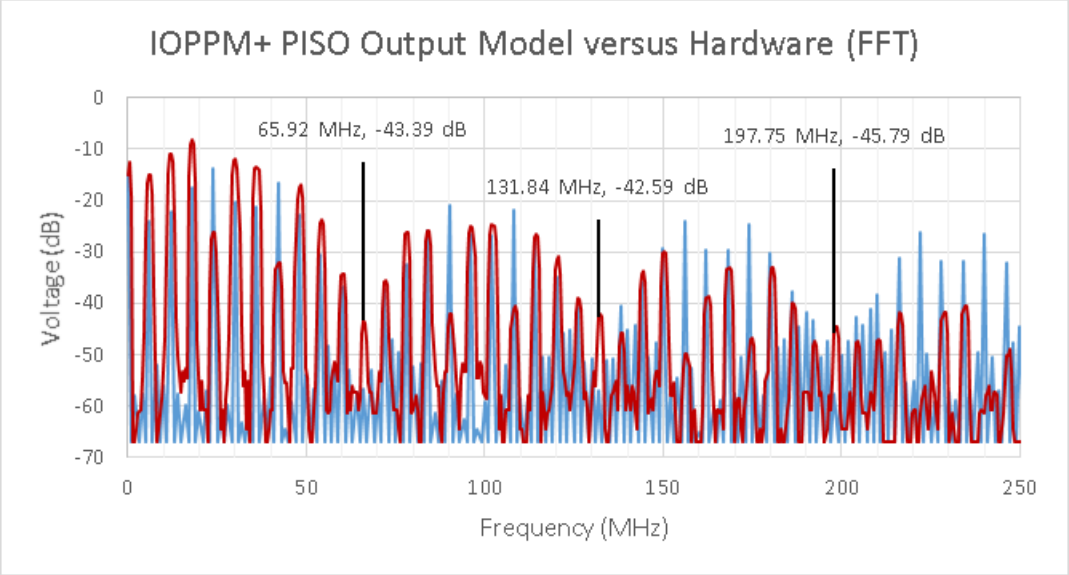


Figure 7-7 IOPPM+ PISO output FFT

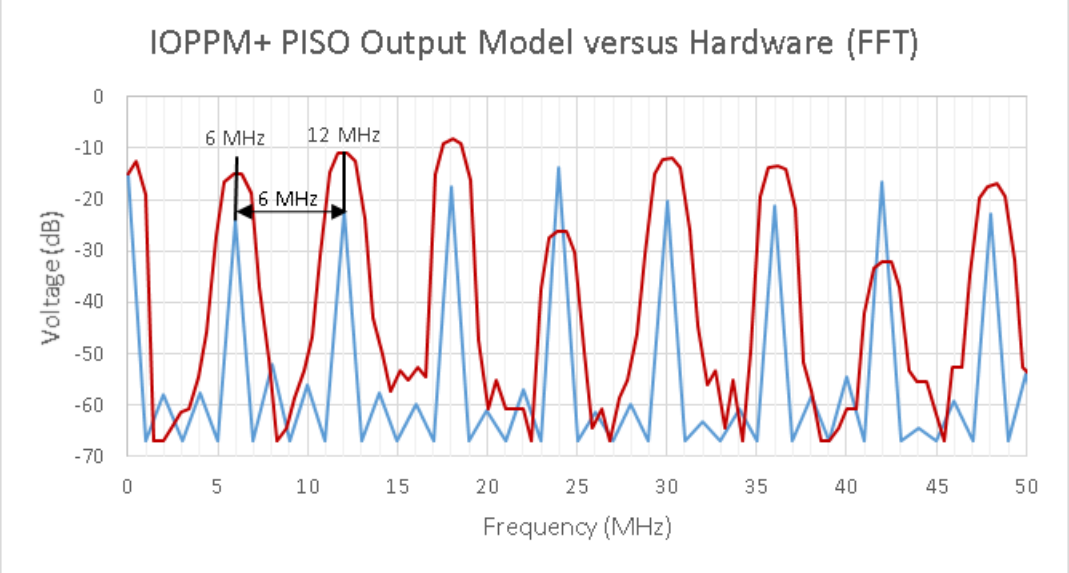


Figure 7-8 IOPPM+ PISO output FFT

In effect, the IOPPM signals first zero crossing, and bandwidth, is defined by the minimum slot time of 15.15 ns (66 MHz), and the spacing of the individual frequency components within the spectrum are defined by the 6 MHz parallel MPEG TS clock frequency. In order to reduce the bandwidth of the VLC system, it is necessary to reduce the parallel MPEG TS clock frequency.

It was demonstrated in Chapter 4 that there is redundancy in the 6 MHz parallel MPEG TS generated by the EVB, when receiving the live off-air DVB-T2 broadcast on Channel C41 (634 MHz). The broadcast MPEG TS clock on Channel C41 was demonstrated to be operating at 1 MHz lower than the parallel MPEG TS clock frequency of the EVB, and that EVB generates padding bits (non-useful data) to increase the clock frequency from 5 MHz to 6 MHz. If the serial clock in the EVB and STB is set to 5 MHz, the serial clock could be reduced to 55 MHz, resulting in a bandwidth reduction of 11 MHz. Unfortunately, the 6 MHz parallel clock used in the proof-of-concept system is set at 6 MHz by the firmware in the STB, so the redundancy is unavoidable. However, the 66 MHz system bandwidth does mean that the system can support a total bit rate capacity of 60 Mbits/s, 30 Mbits/s per IOPPM channel, which exceeds the target bit rate of 50 Mbits/s specified in Chapter 1.

7.1.3 FET Driver Output (Test points B and D)

Using the electrical model and IOPPM+ and IOPPM- hardware configurations, in conjunction with the binary pattern described in section 7.1.1, the FET driver output at test point B was measured. In the electrical model and the IOPPM+ hardware configuration, the IOPPM+ PISO is again loaded with the fixed $_{MSB}0100100011_{LSB}$ binary pattern which feeds the FET and IOPPM composite LED drivers contained within the transmitter module. The FET driver output of the model and hardware were measured, and the results of which are shown Figure 7-9; the dotted vertical lines in the figure show the bit periods of the transmitted binary test pattern, $_{MSB}0100100011_{LSB}$, where the MSB is D9 and the LSB is D0. The simulated (blue trace) and hardware generated (red trace) pulses correlated closely both in amplitude and timing. The design level of 5 V required for the input drive of the FET composite driver was achieved, with

± 0.5 V variation on the pulse peaks. This testing verified that the FET driver output level and timing were correct.

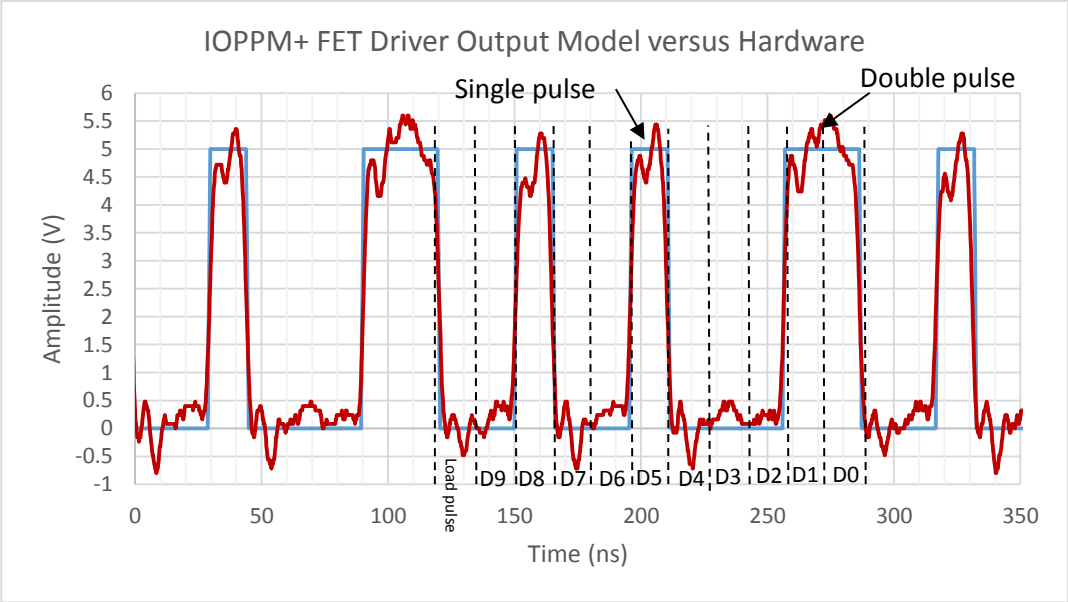


Figure 7-9 IOPPM+ FET driver output

The FET driver measurement was then repeated using the electrical model (Figure 7-1), and the IOPPM- hardware configuration (Figure 7-3) and the same input stimuli. The measurement was performed on test point D in the model and hardware, and yielded similar results to the IOPPM+ configuration.

7.1.4 Pre-amplifier Output (Test point E)

Using the electrical model and IOPPM+ and IOPPM- hardware configurations, in conjunction with the binary test pattern used in section 7.1.1, the pre-amplifier output at test point E was measured. In the electrical model, the IOPPM+ PISO is again loaded with the fixed $_{MSB}0100100011_{LSB}$ binary pattern which feeds the FET and IOPPM composite LED drivers. The output of the IOPPM composite LED driver is electrically coupled into the receivers pre-amplifier via the Gaussian filter approximation (10^{th} order Butterworth LPF) and the voltage controlled current source (transconductance set at -11

μS) blocks which effectively simulate the FSO channel. In the IOPPM+ hardware configuration, the LED is intensity modulated, using the same binary pattern as the model. In this case, the FET composite driver injects the LED with a 13 mA bias for logic zeroes and 26 mA for logic ones, and the resulting light emission from the LED was transmitted over the 1.2 m FSO channel and detected by receivers PD, the photocurrent of which was fed to the pre-amplifier. Figure 7-10 shows the simulated (blue trace) and hardware generated (red trace) output voltage of the pre-amplifier (test point E), and dotted vertical lines are added to show the bit periods of the transmitted binary test pattern, MSB0100100011LSB, where the MSB is D9 and the LSB is D0. The figure shows correlation between the simulated and hardware generated responses. The waveforms have an amplitude of approximately 700 mVpp (resulting from 13 mA current swing in the LED at the transmitter), and the variation between the waveforms is typically ±0.1 V, except for the hardware generated double pulses which, due to their shorter duration, exhibit a larger voltage variation compared to the simulation. Ringing is also observed in the signal below the zero line, as predicted in Chapter 2. The pulses have an amplitude of 400 mV relative to a 300 mV ringing amplitude.

The timing of a single pulse is shown in Figure 7-11. The duration of the simulated (blue trace) and hardware generated (red trace) pulse is measured between the zero crossing points. The simulated pulse duration is 15.6 ns, representing a 2.97% error on the theoretical value of 15.15 ns. The hardware generated pulse duration is approximately 12.4 ns, representing an -18.15% on theoretical value. The shape of the hardware generated pulse is Gaussian, as described in Chapter 2, but is shorter in duration than the simulated pulse by approximately 3.2 ns. The shorter duration single

pulses are still centred in the slot time; therefore central decision detection in the receiver is not degraded.

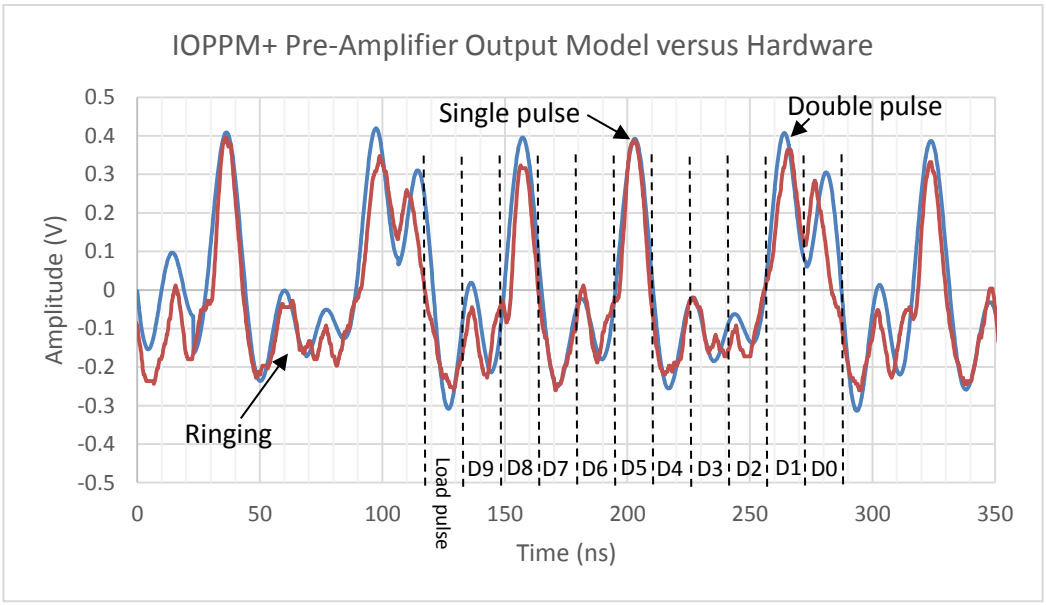


Figure 7-10 IOPPM+ pre-amplifier output

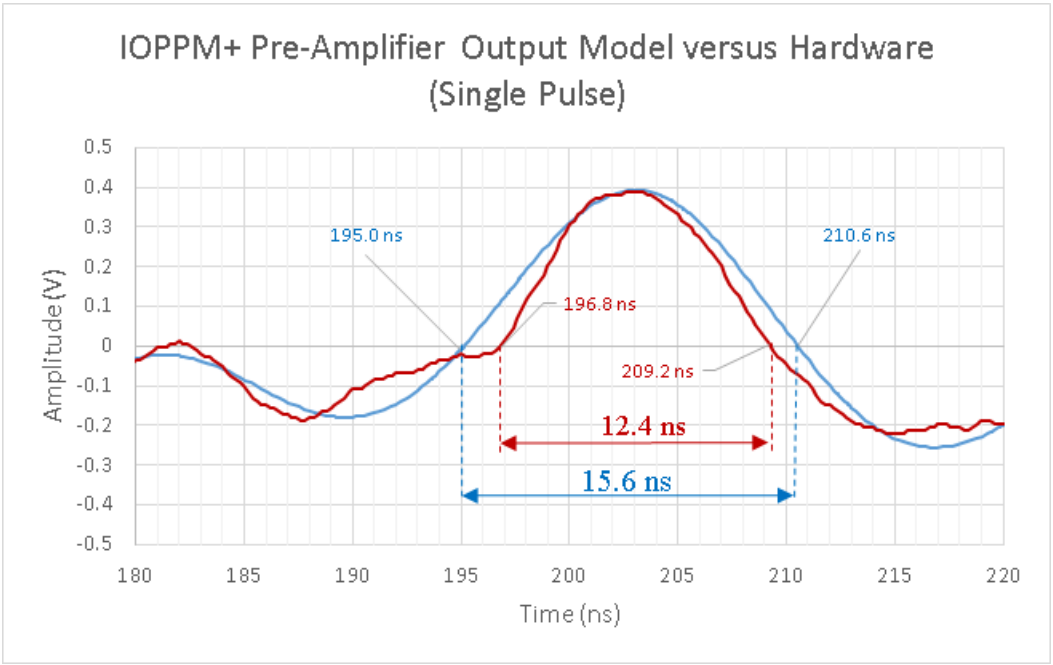


Figure 7-11 IOPPM+ pre-amplifier output (single pulse)

The timing of the double pulse is shown in Figure 7-12, where the duration of the simulated pulse is 31.4 ns, representing a 3.6% error on the theoretical value of 30.30 ns.

The hardware generated pulse duration is approximately 27.2 ns, representing a -10.2% error on the theoretical value. In this case, due to the shorter duration of the hardware double pulse, the leading and trailing peaks, which are labelled in the figure, are shifted off centre, resulting in lower voltage levels at the central decision detection points; the hardware leading pulses is 0.1 V lower than simulated and the trailing pulse 0.2 V lower. Again, the hardware generated pulse is Gaussian in shape, but is shorter in duration than the simulated pulse by approximately 4.2 ns.

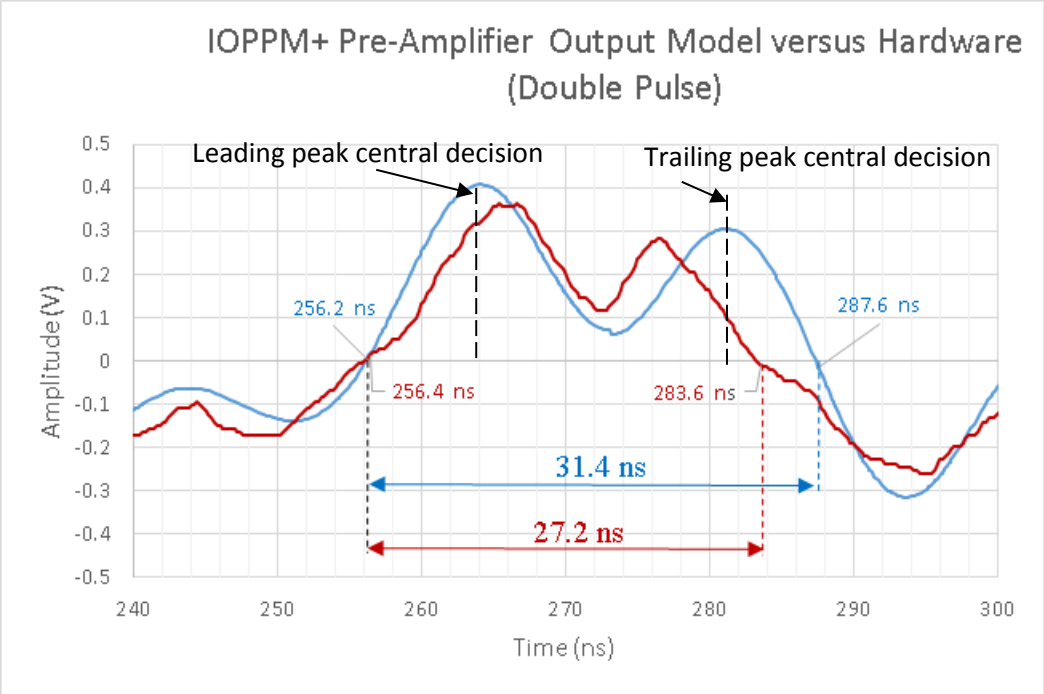


Figure 7-12 IOPPM+ pre-amplifier output (double pulse)

Overall, the simulated Gaussian single pulses are 25.8% longer in duration than the hardware pulses, and the double pulses are 15.4% longer. The peak amplitudes are almost identical between simulated and hardware generated pulses, but the double pulses lower voltages at the decision points, due to their shorter duration. It will be demonstrated later in this chapter that, due to the pre-detection filter, the short duration pulses do not affect central decision detection at the IOPPM decoder. This test verified

that the Gaussian approximation using the 10^{th} order Butterworth LPF was acceptable for modelling the Gaussian pulse shapes.

The test also verified that the pre-amplifiers transimpedance gain of 81.6 dBΩ was capable of producing a significant 700 mVpp output voltage, where empty slot times and pulses could be distinguished from each other and from the ringing.

The pre-amplifier measurement was then repeated using the electrical model (Figure 7-1), and the IOPPM- hardware configuration (Figure 7-3) and the same input stimuli. The measurement was performed again at test point E in the model and hardware. The simulated result was similar to the IOPPM+ simulation, however, the IOPPM- composite LED driver FET, which is required to reduce the LED bias during IOPPM- pulses, did not provide sufficient voltage swing at the pre-amplifier output to distinguish logic one (pulses) from logic zeroes (noise floor). This issue was not resolved during hardware development; therefore testing of the IOPPM- path was no longer possible. From this point forward only verification of the dual LED architecture is possible using only the IOPPM+ path.

7.1.5 Equaliser Output (Test Point F)

The equaliser output response at test point F was also tested using the same IOPPM+ configurations and stimuli described in section 7.1.1. The measurement results for the simulated (blue trace) and hardware generated (red trace) pulses are shown in Figure 7-13. The simulated and hardware generated single pulses are similar in duration and amplitude, however, the double pulses are approximately 0.15 V lower than those of the simulation. The pulse and ringing amplitudes are symmetrical about the zero line at ±250 mV.

The amplitude of the signal has reduced from 700 mVpp at the output of the pre-amplifier (test point E) to 500 mVpp at the equaliser output (test point F), indicating an overall voltage attenuation of approximately 3 dB. The reduction is significantly less than that estimated during the design of the equaliser and post-amplifier described in Chapter 5, section 5.3.3 and 5.3.4, where the equaliser attenuation at 4.35 MHz was determined at 23 dB; the error was due measuring the level at a single frequency. The 23 dB value was used to set the initial voltage gain of post-amplifier to 25.38 dB to achieve 1 Vpp at its output (test point G), which is required to satisfy the input requirements of the window comparator. The gain of the post-amplifier was set too high and therefore required reduction to 6 dB to ensure that its output voltage is within the 1 Vpp range required by the window comparator; modification of the post-amplifier gain will be discussed in the next section.

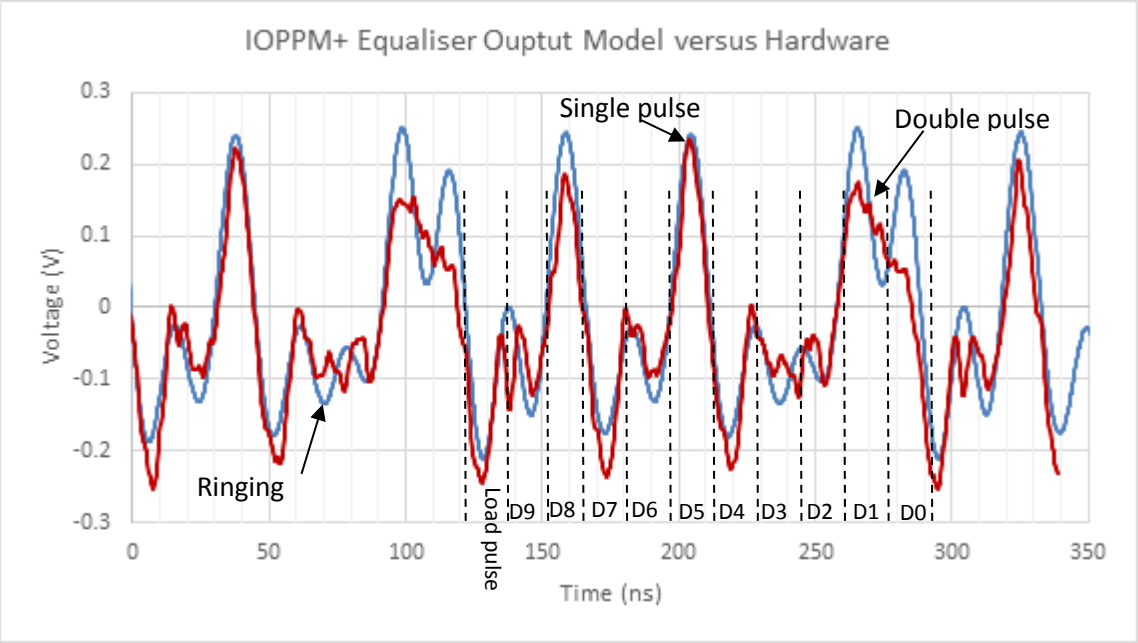


Figure 7-13 IOPPM+ equaliser output

The timing of a single pulse is shown in Figure 7-14. The duration of the simulated (blue trace) and hardware generated (red trace) pulse is measured between the zero crossing points. The simulated pulse duration is 15 ns, representing a -1% error on the theoretical value of 15.15 ns. The hardware generated pulse duration is approximately 13.2 ns, representing an error of -12.9% on theoretical value.

The double pulse timing is shown in Figure 7-15. The duration of the simulated (blue trace) and hardware generated (red trace) pulse is also measured between the zero crossing points. The simulated pulse duration is 30.4 ns, representing a 0.33% error on the theoretical value of 30.30 ns. The hardware generated pulse duration is approximately 26.8 ns, representing an error of -11.6% on theoretical value.

The hardware generated single pulses, although shorter in duration than the theoretical, are centred within their respective slot times, permitting accurate central decision detection. However, the hardware double pulses still exhibit lower voltage levels, at the central decision points, with the leading peak 0.1 V lower than simulate and the trailing peak 0.15 V.

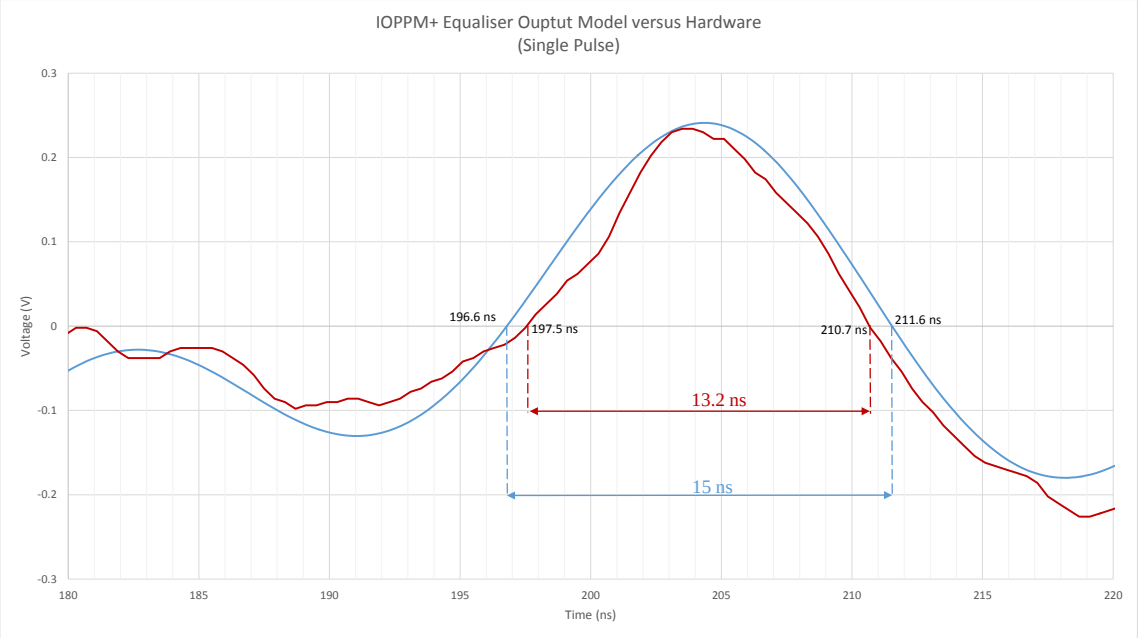


Figure 7-14 IOPPM+ equaliser output (single pulse)

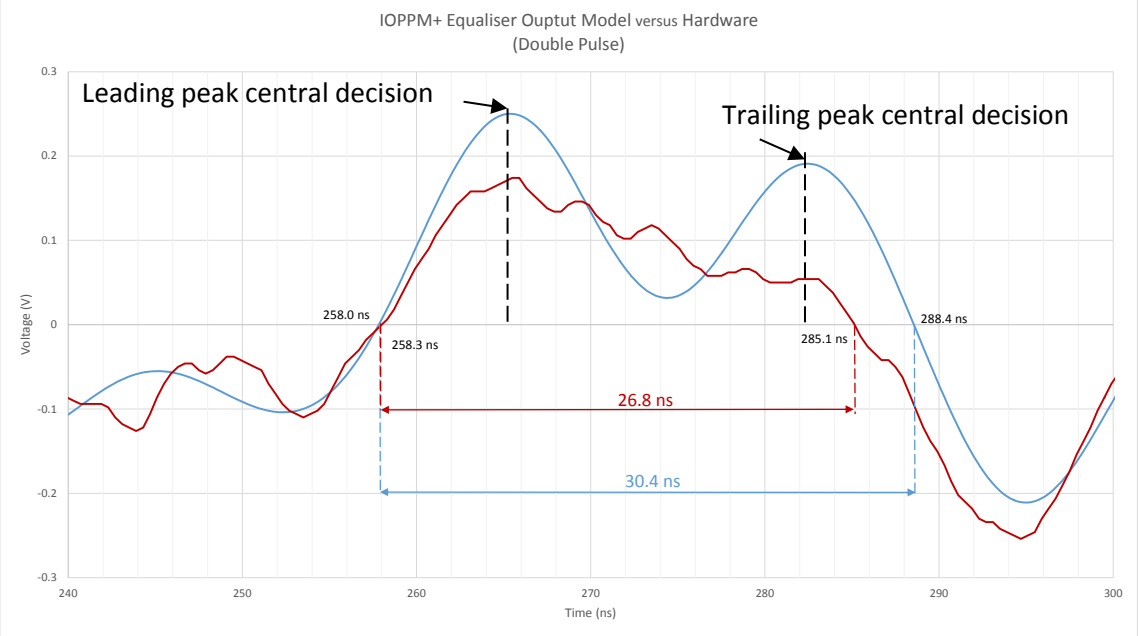


Figure 7-15 IOPPM+ equaliser output (double pulse)

The timing error between the simulated and hardware generate single and double pulses is approximately 13% at this stage in the receiver, and overall the correlation between

simulated and hardware measurements is closely matched. This test verified the operation of the equaliser.

7.1.6 Post-amplifier Output (Test Point G)

As discussed in the previous section, the post-amplifiers voltage gain of 25.38 dB was too high. Given that the input voltage fed to amplifier from the equaliser is at 500 mVpp, a voltage of 9.3 Vpp is generated at the output of the post-amplifier (test point G), which is an order of magnitude larger than the window comparators 1V input range, and is also very close to the maximum 10 Vpp output swing (saturation) of the op-amp used to implement the amplifier. Although a 6 dB voltage gain is sufficient to amplify the 500 mV input to 1 Vpp, it was discovered through hardware experimentation that operating the post-amplifier at such a low gain reduced SNR and increased ringing between the IOPPM pulses. A gain of 24 dB was determined as optimal, as this produced the highest SNR (35 dB) and lowest ringing. The amplifier produced an output voltage swing of 8 Vpp, providing a saturation (clipping) margin of ±1V. Furthermore, voltage attenuation (approximately 18 dB) at the window comparator input is necessary to reduce the swing to meet the 1 Vpp input range.

Figure 7-16 shows the closely correlated, simulated (blue trace) and hardware generated (red trace) post-amplifier output responses at test point G, which were generated using the electrical model and IOPPM+ hardware configuration, and input stimuli described in section 7.1.1. The output swing of the signal is 8 Vpp, as set by the amplifiers 24 dB gain, and the only significant difference between the traces is the simulated ringing between pulses which deviates from the hardware measurements by up to 3 V; the deviation is attributed to impedance mismatching in the model.

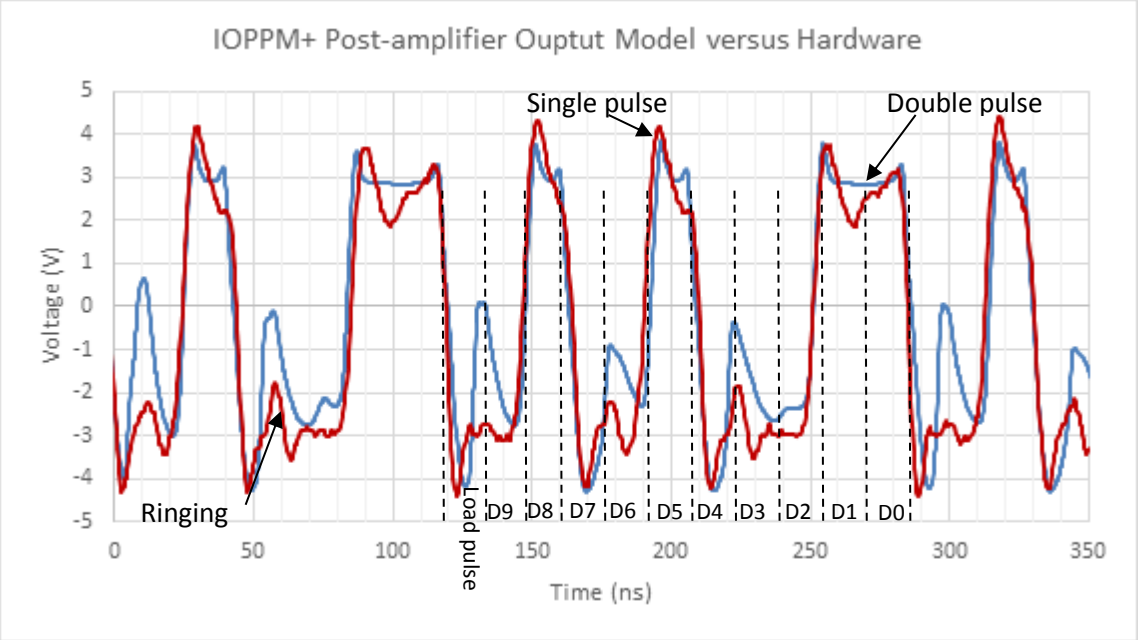


Figure 7-16 IOPPM+ post-amplifier output

The modification of the post-amplifiers voltage gain from 25.38 dB to 24 dB resulted in the change of the R4 feedback resistor from 931 Ω to 800 Ω, as shown in Figure 7-16.

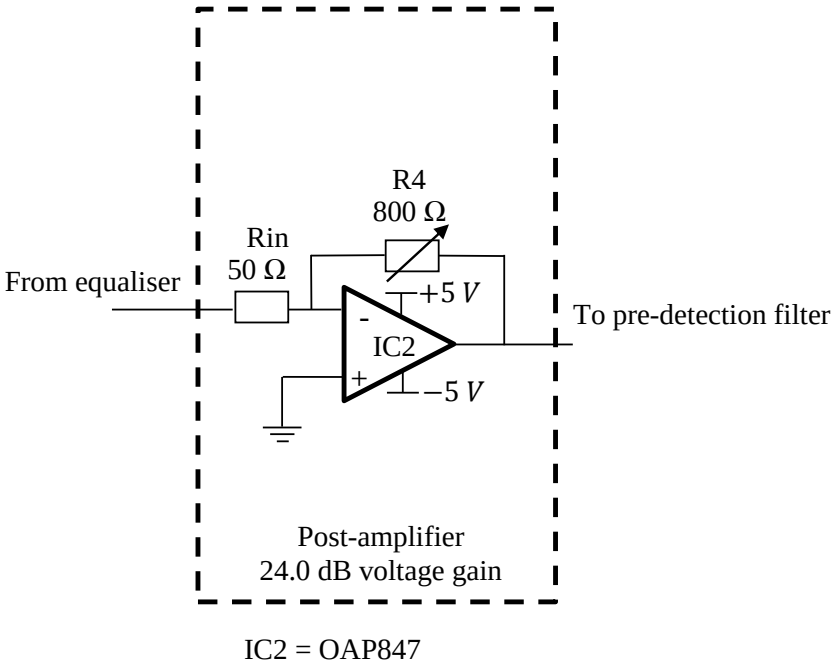


Figure 7-17 Post-amplifier schematic

Note: the approximate 18 dB of voltage attenuation required at the input window comparator is applied at the SMA connector interfaces between the receiver and comparator modules using SMA attenuators; attenuation is also incurred following the pre-detection filter which is subtracted from the 18 dB of attenuation required directly after the amplifier.

The timing of single pulse is shown in Figure 7-18. The simulated (blue trace) pulse exhibits a duration of 16.4 ns, when measured at the zero crossings. This represents an error of 8.3% on the theoretical value of 15.15 ns. The hardware generated pulse (red trace) exhibits a duration of 19.2 ns, representing an error of 26.7% on the theoretical value, and causes approximately 2 ns of overlap with adjacent slot times. The overlap is insufficient to cause significant ISI.

The simulated and hardware pulses show a worst case difference in level of 1 V, however, the centres of the pulses are aligned and at the same level.

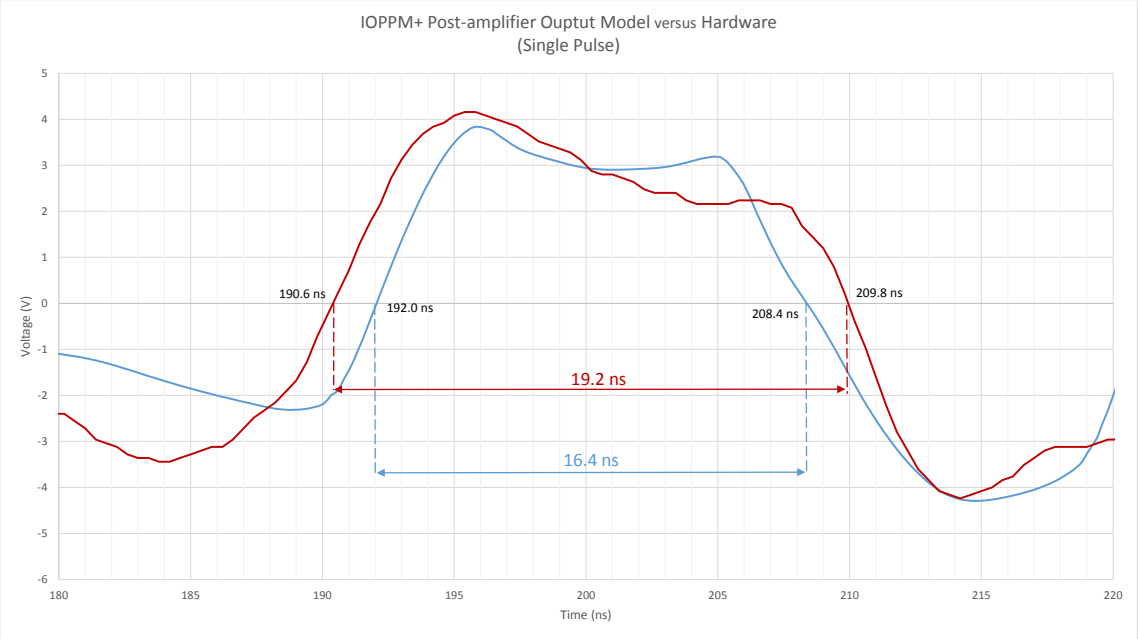


Figure 7-18 IOPPM+ post-amplifier output (single pulse)

Timing of the double pulse is shown in Figure 7-19. The simulated (blue trace) pulse exhibits a duration of 35.6 ns and the hardware generated pulse a duration of 34 ns, representing errors of 12.2% and 17.5% on the theoretical value of 30.30 ns. Hardware pulses effectively overlap adjacent slot times by approximately 2.65 ns, which is insufficient to cause significant ISI.

The errors between the simulated and hardware measured results is 14.5% for single pulses and 4.5% for double pulses.

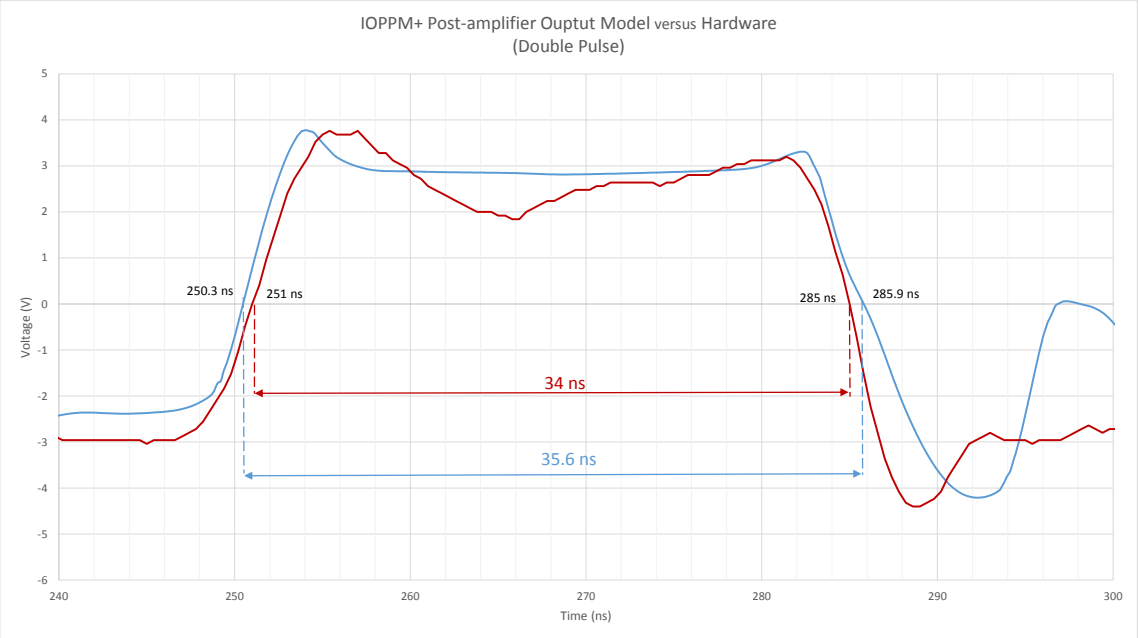


Figure 7-19 IOPPM+ post-amplifier output (double pulse)

This test verified that the post-amplifier provided sufficient voltage gain (24 dB) to drive the pre-detection filter and accommodate the window comparator input voltage range, with the least ringing and highest SNR of 35 dB.

7.1.7 Pre-detection Filter Output (Test Point H)

The pre-detection filter output response at test point H was measured using the electrical model and IOPPM+ hardware configuration and stimuli described in section 7.1.1. The

closely correlated measurement results for the simulated (blue trace) and hardware generated (red trace) pulses are shown in Figure 7-20. The output voltage of the pre-detection filter is 7 Vpp, which is 1 V lower than the output of the post-amplifier, indicating that the pre-detection filter has a voltage attenuation of approximately 1 dB. The simulated waveform shows that the single pulses peak 1V lower than the hardware pulses, and also exhibit a higher level of ringing. The filter effectively reduces the amplitude of the ringing generated in the post-amplifier and smooths the pulse responses, thus enabling pulses and empty slots to be more clearly distinguished during central decision detection.

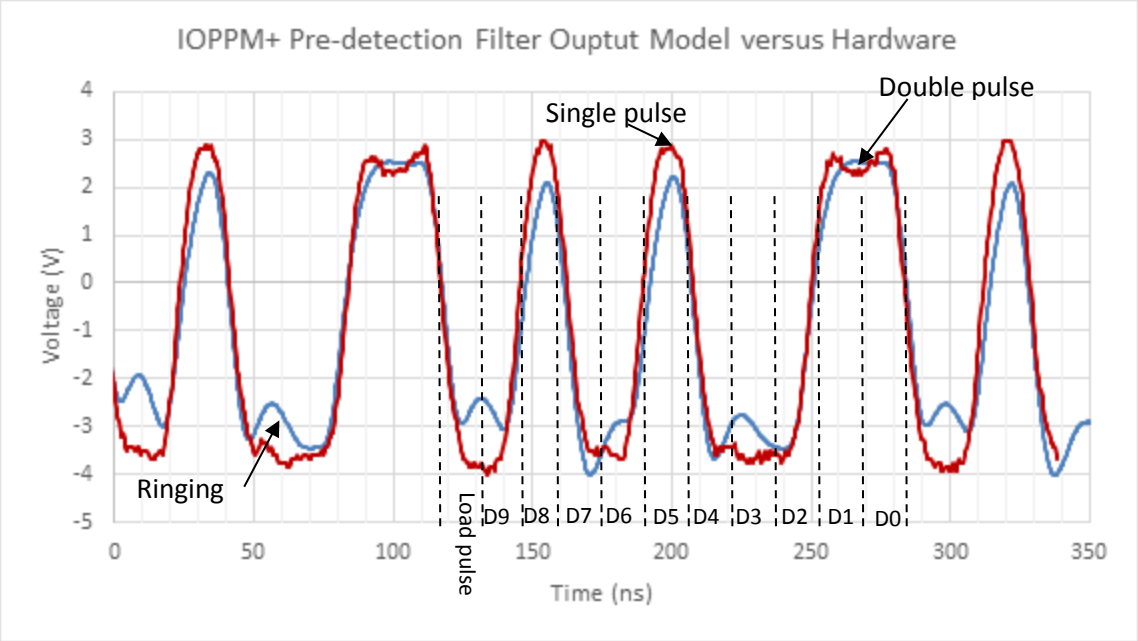


Figure 7-20 IOPPM+ pre-detection filter output

The timing of single pulse is shown in Figure 7-21. The simulated (blue trace) pulse exhibits a duration of 14.2 ns, when measured at the zero crossings and represents an error of -6.3% on the theoretical value of 15.15 ns, and the hardware generated pulse (red trace) exhibits a duration of 17.6 ns, representing an error of 17.6% on the

theoretical value. The simulated pulse is within the theoretical slot time, and the hardware pulse overlaps adjacent slot times by approximately 1.2 ns, and is insufficient to cause significant ISI. The error between simulated and hardware single pulse is 19.3%.

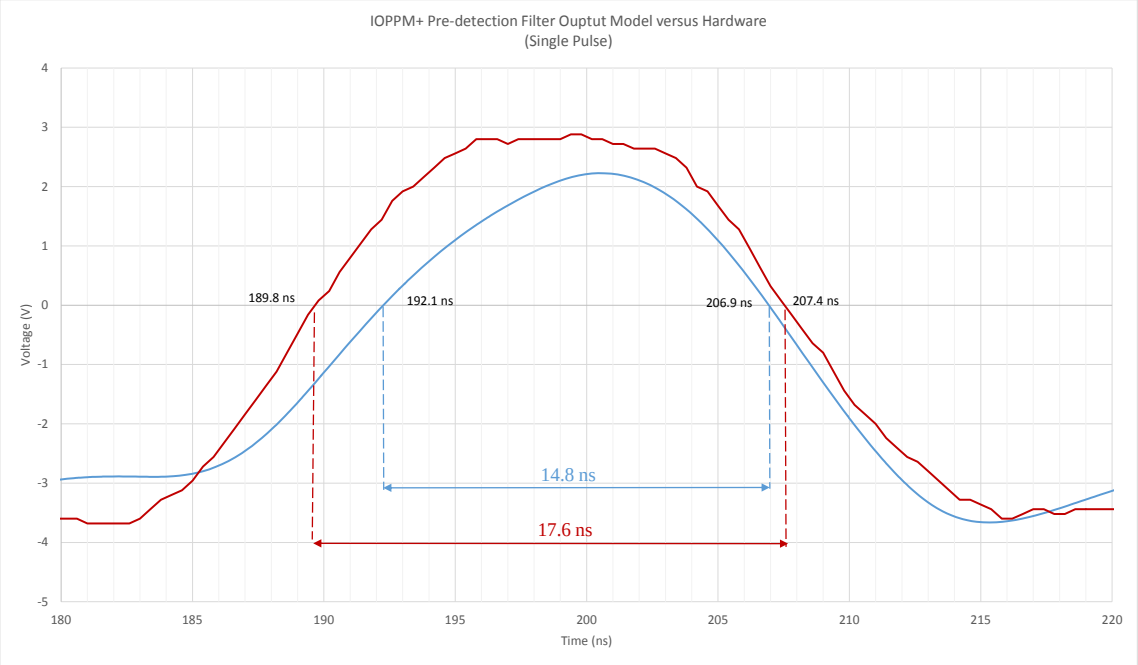


Figure 7-21 IOPPM+ pre-detection filter output (single pulse)

The timing of double pulse is shown in Figure 7-22. The simulated (blue trace) pulse exhibits a duration of 33.1 ns, when measured at the zero crossings and represents an error of 9.2% on the theoretical value of 30.30 ns, and the hardware generated pulse (red trace) exhibits a duration of 33.2 ns, representing an error of 9.6% on the theoretical value. The simulated and hardware pulses overlap adjacent slot times by approximately 1.4 n, which is insufficient to cause significant ISI. The error between simulated and hardware double pulses is 0.3%.

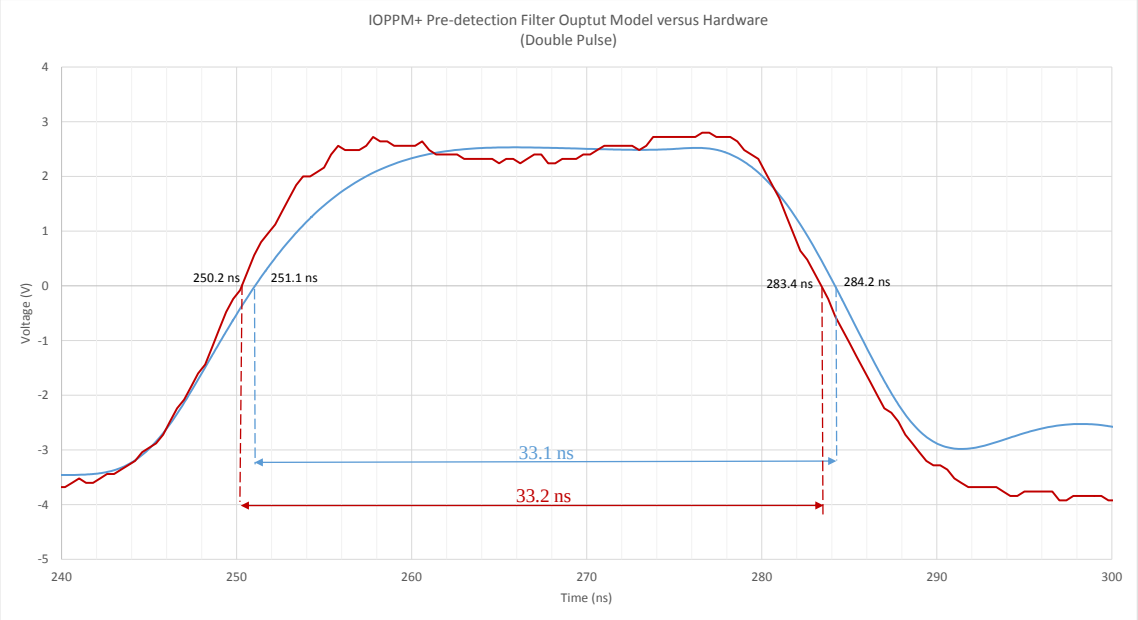


Figure 7-22 IOPPM+ pre-detection filter output (double pulse)

At the output of the pre-detection filter, approximately 17 dB of attenuation was applied to reduce the voltage swing of the waveform from 7 Vpp to 1 Vpp, enabling it to fit inside the window comparators input voltage range. Figure 7-23 shows the attenuated simulated (blue trace) and hardware (red trace) waveforms. The timing of the waveforms is identical to the pre-detection filter output, and the only significant difference in the waveforms is the 0.15 V level reduction of the double pulse trailing edge. The step in the peak of the double pulses trailing edges is non-ideal, as it can cause a null at central decision point if the threshold voltage is set within the stepped region. The threshold voltage, therefore, must be set below the step, which leads to an increase in the duration of the bit period output by the comparator and increases the bit period overlap into adjacent periods. The threshold voltage setting and overlap will be quantified in the next section.

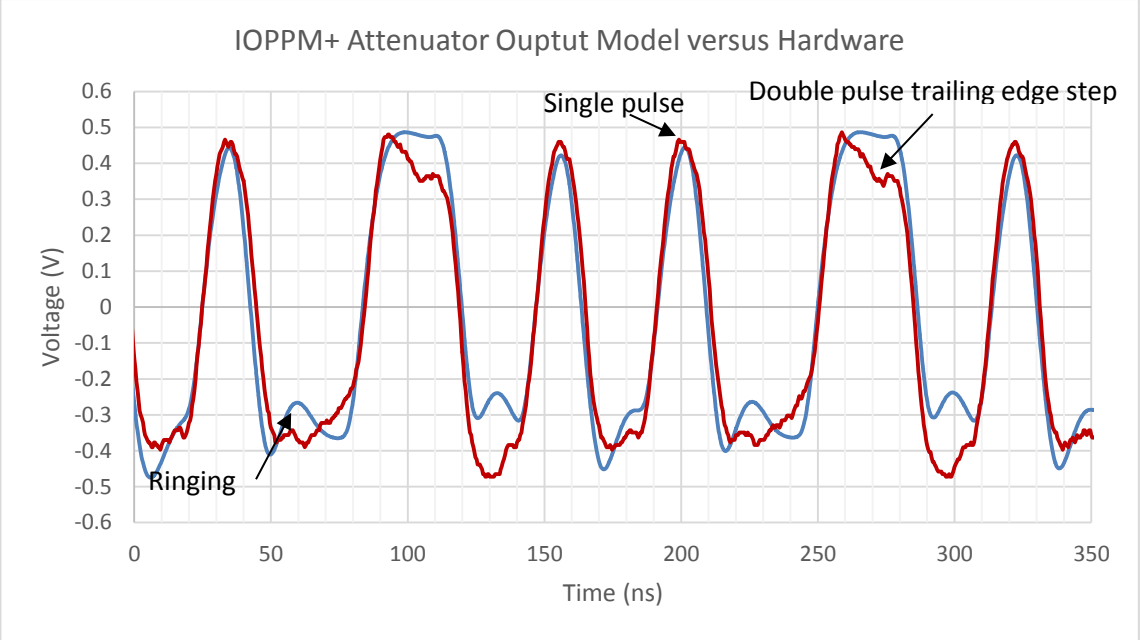


Figure 7-23 IOPPM+ attenuator output

The tests verified that the pre-detection filters 3 dB bandwidth of 46.2 MHz, defined by 70% of the serial clock frequency of 66 MHz, reduced ringing between pulses and smoothed the waveform, thus enabling pulses and empty slots to be more clearly distinguished during central decision detection. The attenuator circuit was also verified as providing the required 1 Vpp input voltage to the window comparator.

7.1.8 Comparator Output (Test points I and J)

The comparator output response at test point I was measured using the electrical model and IOPPM+ hardware configuration and stimuli described in section 7.1.1. Prior to measuring the output response, and using the same configurations and stimuli, the input to comparator was measured to verify that the 0.5 V DC offset was applied to 1Vpp IOPPM+ signal to remove negative excursions, and thus enable it to fit inside the 0V to 1V range accepted by the comparator. Figure 7-24 shows the input circuit to the comparator formed by C1, R1 and R2. C1 AC couples the signal into the potential

divider circuit which provides the 0.5 V DC offset. The IOPPM+ signal was measured at the junction of C1, R1 and R2, in both the model and the hardware, and produced the results shown in Figure 7-25.

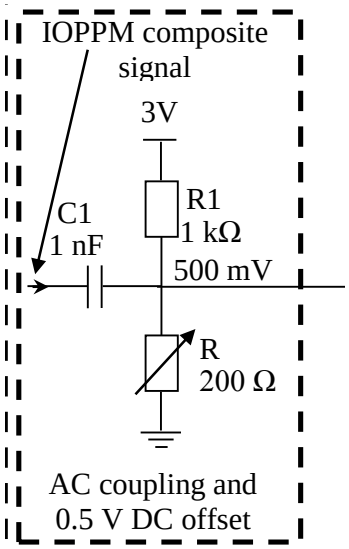


Figure 7-24 Comparator DC offset circuit

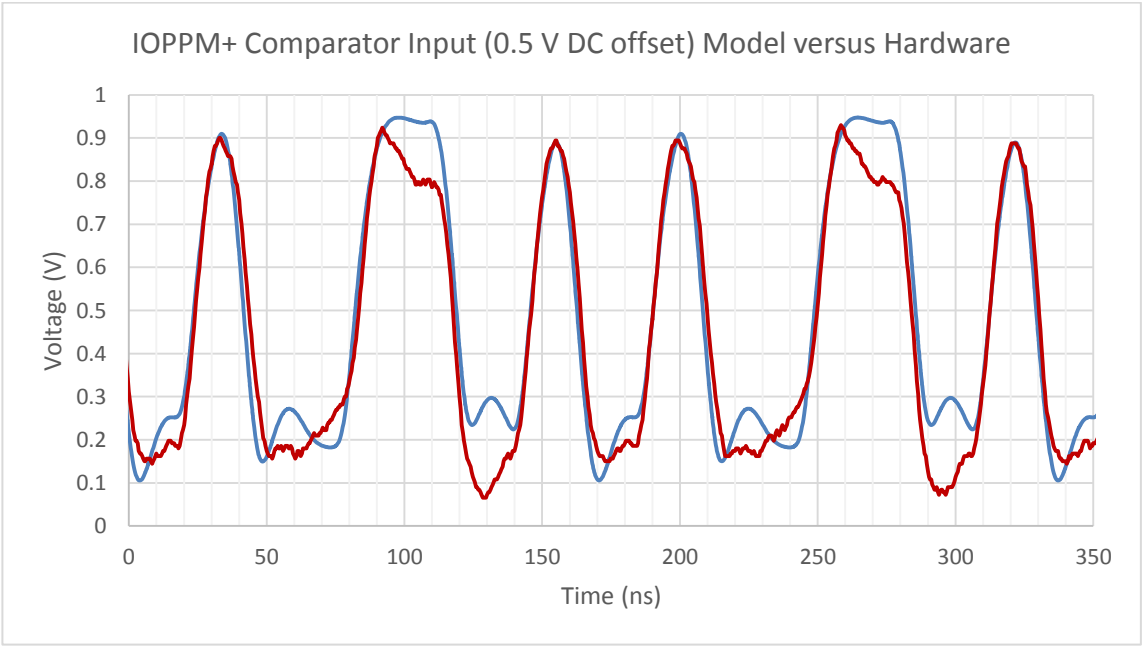


Figure 7-25 IOPPM+ Comparator Input (measured at C1, R1 and C2 junction)

The timing and peak-to-peak voltages of the simulated (blue trace) and hardware (red trace) waveforms are virtually identical to the output of the 17dB attenuator, except that negative voltage excursions are removed and the signal is centred at 0.5 V, deviating within the 0V to 1V window; this measurement verified that the input signal is compatible with the input range of the comparator.

With the signal shown in Figure 7-25 applied to the input of IOPPM+ comparator, the output was measured at test point I (differential PECL to TTL translator output), with the V_{REF+} threshold voltage of the comparator set at 700 mV. This threshold voltage was chosen because it was below the step in the hardware double pulses, providing a margin of 0.1 V between the threshold and the step, and thus avoiding nulls at the central decision; the margin was applied to allow for variations in the signal level. Figure 7-26 shows the 0.1 V margin between the 700 mV threshold voltage (green trace) and the step in the hardware double pulses (red trace).

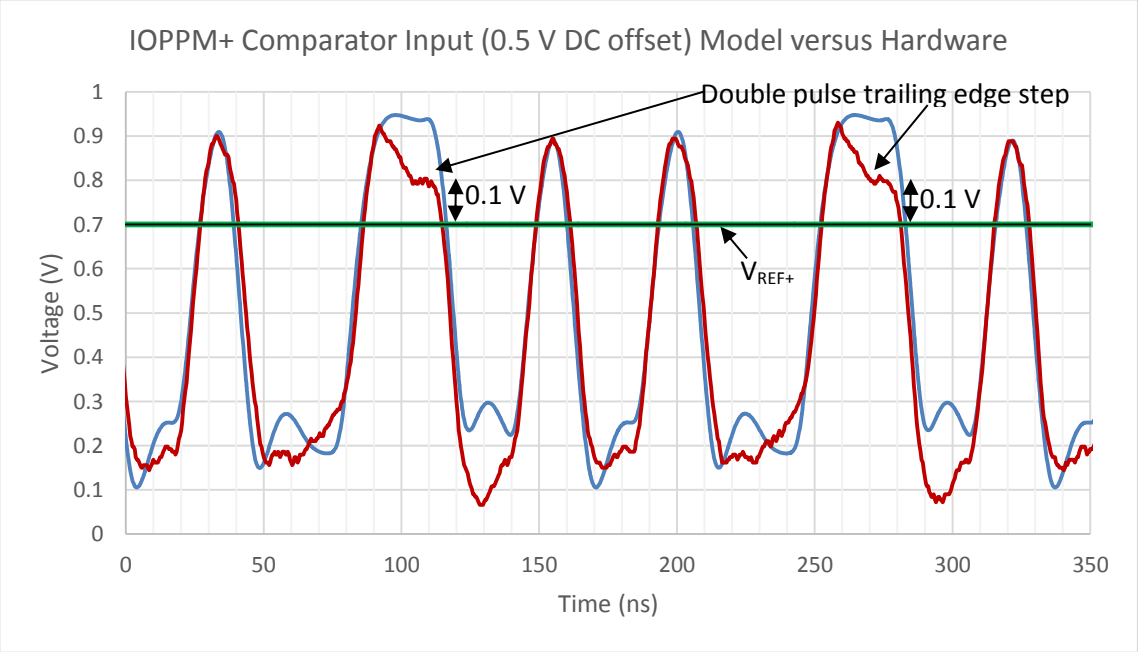


Figure 7-26 IOPPM+ Comparator Input (V_{REF+} = 700 mV)

Using the 700 mV threshold voltage produced the simulated (blue trace) and hardware (red trace) responses shown in Figure 7-27. The most significant difference between the responses is the shape and level of the responses. The simulated response shows an ideal rectangular shape and TTL digital levels (0V to 5V), which is due to an ideal comparator being used in the electrical model to translate the window comparators differential PECL output to TTL. In the hardware response, the levels are lower by 1 V and the shape exhibits over- and undershoots, which were caused by the loading of the translators output. The peak level of the bits fit within the 15.15 ns slot time/bit periods, shown by the vertical dotted lines in the figure, indicating that central detection of the bits is achievable at the IOPPM+ SIPO stage in the IOPPM decoder.

The timing of a single bit (single pulse) is shown in Figure 7-28. The simulated (blue trace) bit exhibits a duration of 12.3 ns, when measured at the zero voltage level and represents an error of -18.8% on the theoretical value of 15.15 ns, and the hardware generated bit (red trace) exhibits a duration of 19.6 ns, representing an error of 29.4% on the theoretical value. The simulated bit is within the theoretical bit period, and the hardware bit overlaps adjacent bit periods by approximately 2.2 ns and is insufficient to cause significant ISI. The error between simulated and hardware double bits 37.2%, which is caused by the simulated single bits having shorter durations than the theoretical value.

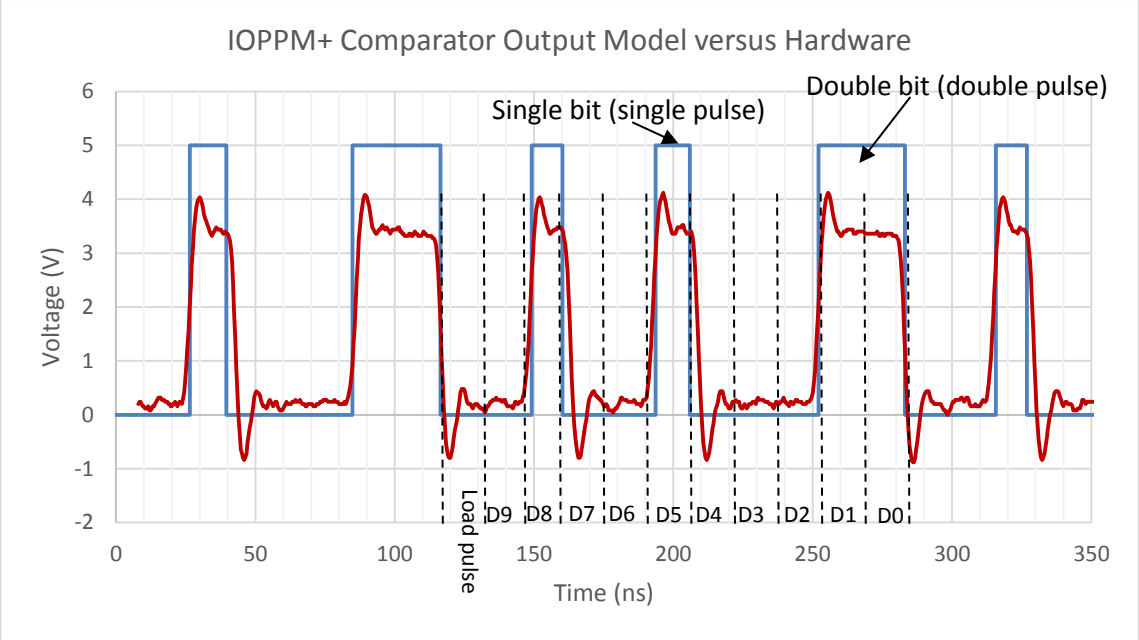


Figure 7-27 IOPPM+ Comparator Output

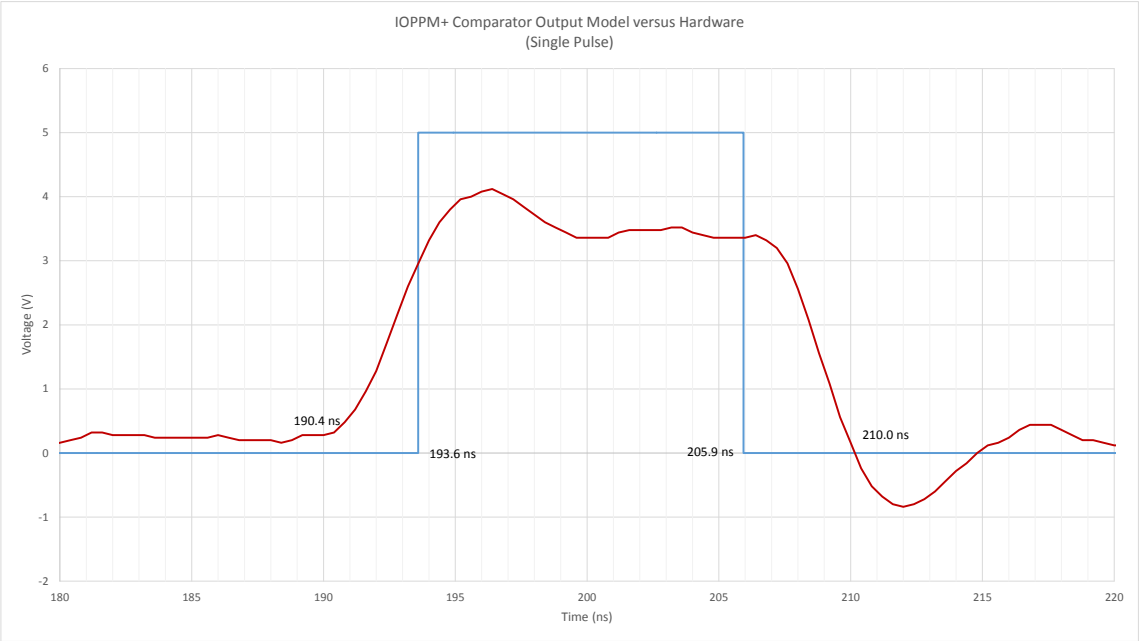


Figure 7-28 IOPPM+ comparator output (single bit)

The timing of double bits (double pulse) is shown in Figure 7-29. The simulated (blue trace) bits exhibits a duration of 32.9 ns, when measured at the zero voltage level and represents an error of 8.6% on the theoretical value of 30.30 ns, and the hardware

generated bits (red trace) exhibits a duration of 35.2 ns, representing an error of 16.2% on the theoretical value. The simulated bits overlap adjacent bit periods by approximately 1.3 ns, and the hardware bits by 2.45 ns. The error between simulated and hardware double pulses is 6.5%.

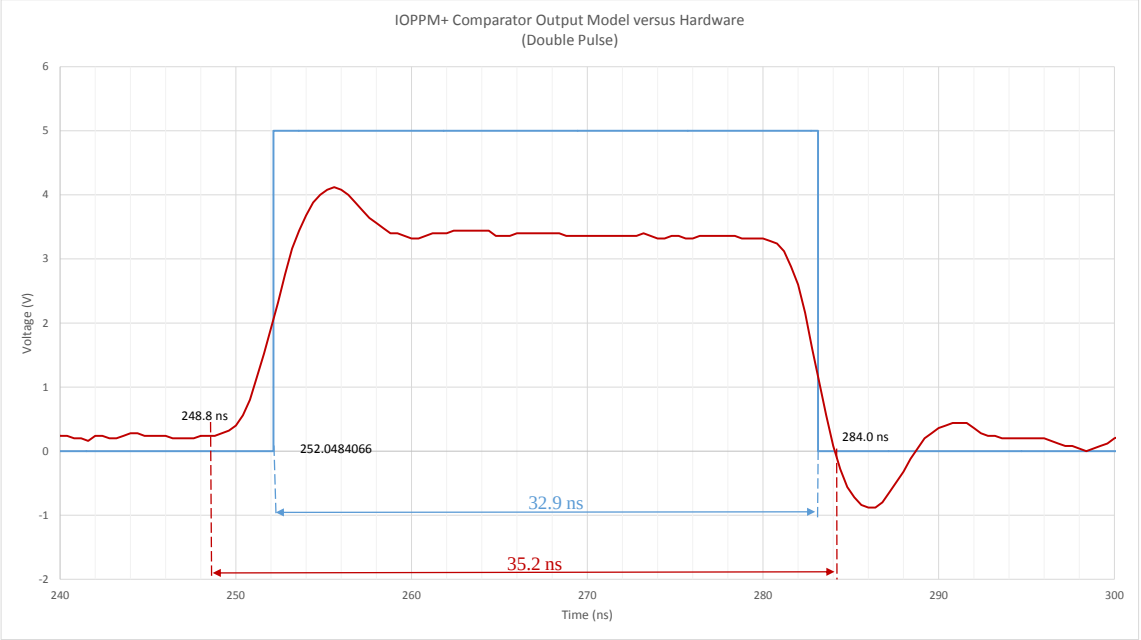


Figure 7-29 IOPPM+ comparator output (double bit)

Overall, good correlation between the electrical model and hardware configurations were observed. The comparator tests verified the parametric end-to-end performance of the VLC systems digital PISO stages and analogue transmitter, receiver and comparator modules.

7.1.9 DVB-T2 Transmission (Live Off-Air)

Live off-air testing of the hardware system was performed using the IOPPM+ hardware configuration described in section 7.1.1, and with the stimulus provided by the MPEG TS generated by the Silicon Lab EVB; the EVB was tuned to DVB-T2 broadcast Channel C41 during testing. The EVBs MPEG TS was IOPPM encoded and transmitted

over the FSO channel and received by the receiver module. The IOPPM+ bit stream was measured at the IOPPM+ input of the transmitter module and at the receiver module output (pre-detection filter output). Figure 7-30 and Figure 7-31 show close correlation between the transmitted bit sequences (blue trace) and the received bit sequences (red trace) at the output of the pre-detection filter; note that propagation delay between transmitter and receiver is removed to enable overlay of the traces. Figure 7-30 shows a bit stream with a high concentration of logic ones being transmitted and Figure 7-31 a low concentration. Consistent timing and waveform shapes are observed in the measurements. The output level of the pre-detection filter exhibits a consistent peak-to-peak variation between single and double pulses of approximately 0.5 V; the traces exhibit stable and repeatable behaviour.

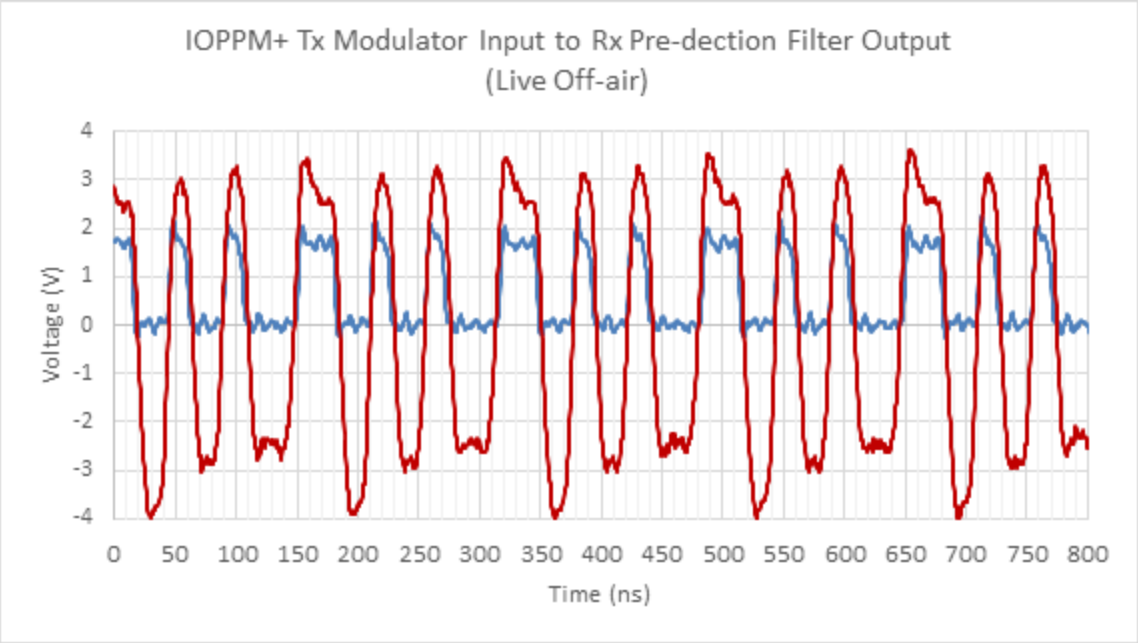


Figure 7-30 IOPPM+ Modulator module input and receiver module output

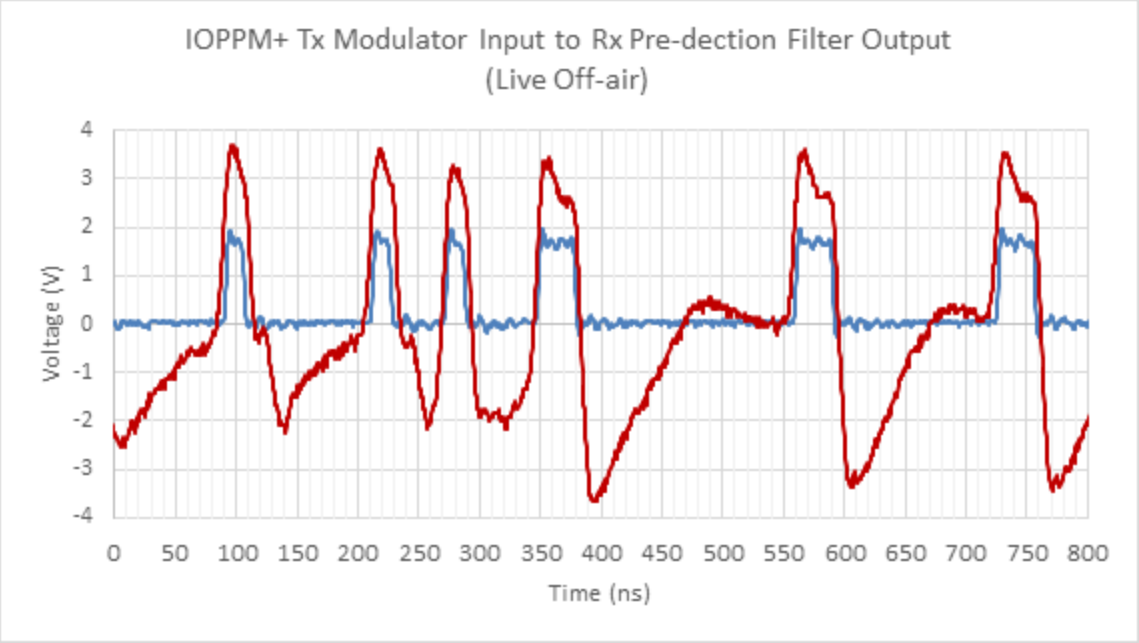


Figure 7-31 IOPPM+ Modulator module input to receiver module output

This testing verified that IOPPM encoded MPEG TS could be transmitted over the FSO channel and successfully recovered at the output of the pre-detection filter.

7.2 IOPPM Encoder and Decoder Verification

Following the verification of the digitally implemented 66 MHz PLL and PISO timing, and the performance of the analogue sub-systems, the IOPPM encoder, decoder and central decision detection were verified. This was achieved using the electrical model and IOPPM+ hardware configuration described in section 7.1.1, and three parallel 10-bit fixed binary test patterns, which were used to stimulate the IOPPM encoder inputs. The test patterns were used to replace the parallel 10-bit MPEG TS generated by the EVB, and exercise all eight combinations of the IOPPM encoders.

Figure 7-32 shows the detailed block diagram of the encoder/transmitter system. The parallel 10-bit MPEG TS bus, which provides input to the IOPPM encoders via the 1-bit buffer, is shown at top-left-hand-side of the figure. The bus is shown divided into four

colour-coded groups, the first three groups consisting of 3-bits each, are labelled: MPEG_TS_D0 to MPEG_TS_D2 (yellow colour-code); MPEG_TS_D3 to MPEG_TS_D5 (green colour-code); and MPEG_TS_D6, MPEG_TS_D7 and MPEG_TS_SYNC (blue colour-code). The fourth group consists of a single bit, MPEG_TS_VALID (purple colour-code). As stated in Chapter 3, the valid bit is at logic one every 31.91 kHz, and therefore is loaded directly (un-coded) into the IOPPM+ PISO. The other three, 3-bit groups are IOPPM coded using three separate 3-bit IOPPM encoders, which accept 3-bit input data and output two separate 3-bit IOPPM codewords (IOPPM+ and IOPPM-), as defined by Table 7-1. The encoder has eight input combinations, represented by the min terms 0 to 7, and since all three IOPPM encoders contain identical logic circuits, it is possible, using just three fixed test patterns, to exercise all eight combinations of the encoder. Before introducing the test patterns, the MPEG TS bus labels are abbreviated to make reading of the encoding tables easier. Table 7-2 shows the mapping of the MPEG TS bus labels to the abbreviated fixed test pattern labels; note the colour-coding of the 3-bit groupings is preserved.

	Input Data			**Output IOPPM+**			**Output IOPPM-**		
Min Term	D_2 MSB	D_1	D_0 LSB	Y_2 MSB	Y_1	Y_0 LSB	Z_2 MSB	Z_1	Z_0 LSB
0	0	0	0	1	0	0	0	0	1
1	0	0	1	0	0	1	0	0	0
2	0	1	0	0	1	0	0	0	0
3	0	1	1	1	0	0	0	0	0
4	1	0	0	0	0	1	1	0	0
5	1	0	1	0	0	0	0	0	1
6	1	1	0	0	0	0	0	1	0
7	1	1	1	0	0	0	1	0	0

Table 7-1 IOPPM encoder (3-bit coding)

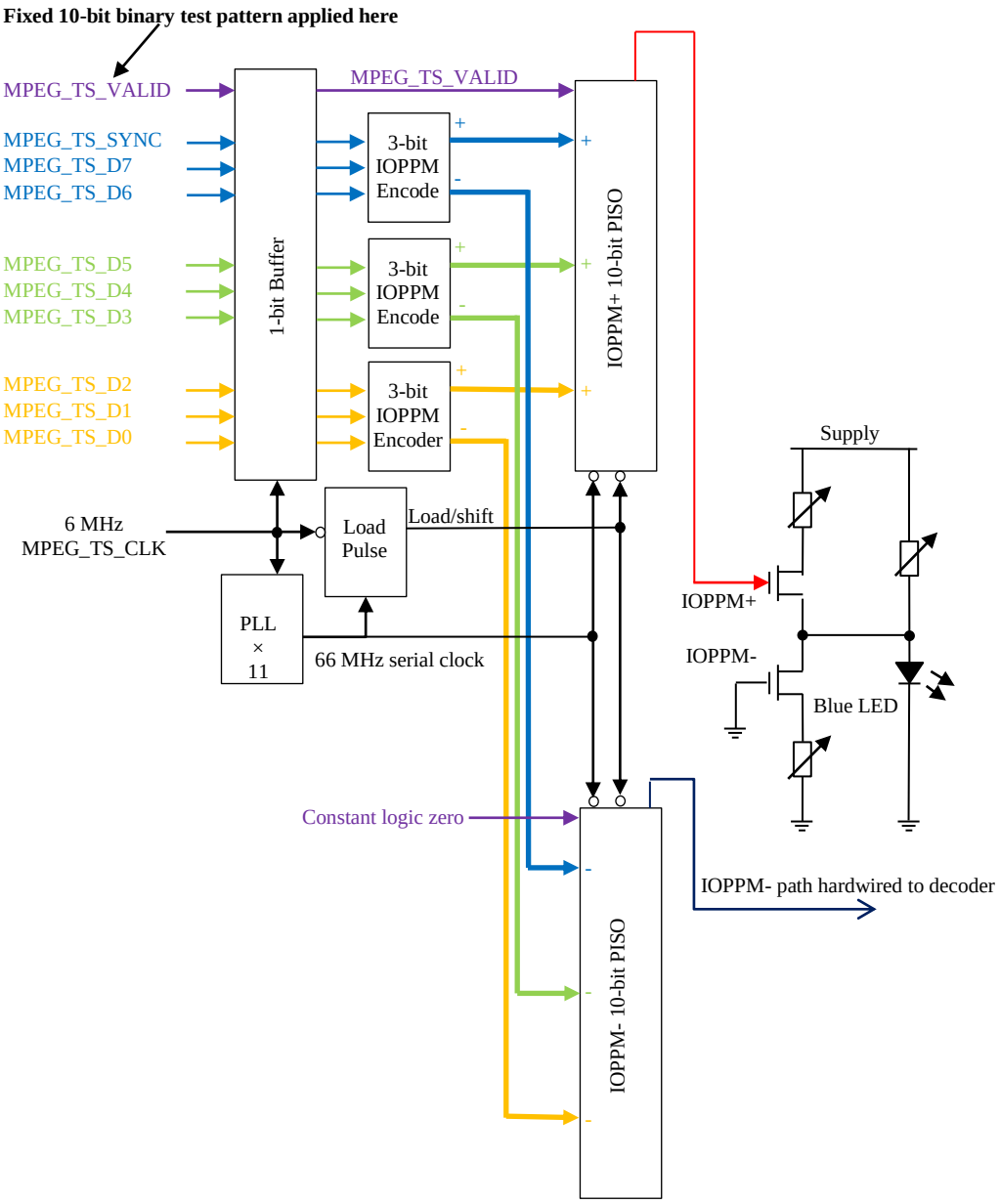


Figure 7-32 IOPPM encoder/transmitter

MPEG TS Bus Label	Fixed Test Pattern Label
MPEG_TS_Valid	V
MPEG_TS_Sync	S
MPEG_TS_D7	D7
MPEG_TS_D6	D6
MPEG_TS_D5	D5
MPEG_TS_D4	D4
MPEG_TS_D3	D3
MPEG_TS_D2	D2
MPEG_TS_D1	D1
MPEG_TS_D0	D0

Table 7-2 Mapping MPEG TS labels to abbreviated fixed test pattern labels

The first test pattern, ‘test pattern 1’, is shown in the left-hand-side column of Table 7-3, and is represented by the fixed parallel input bits D0 through D7, S (Sync) and V (Valid). The LSB and MSB of each 3-bit group are indicated in the table, and enable the groups to be correctly mapped to the IOPPM coding table min terms (Table 7-1). In this case, bits D0 through D2 map to min term 2, D3 through D5 to min term 1, and D6, D7 and S to min term 0. The V (valid) bit, which is set to zero, is un-coded as indicated by the abbreviation UC in the table. The resultant parallel output IOPPM+ and IOPPM- codewords are shown in the right-hand-side column of the table, where the IOPPM+ codewords are represented by Y0 through Y8, and the corresponding IOPPM- codewords by Z0 through Z8. As shown in Figure 7-32, the parallel IOPPM+ and IOPPM- codewords are connected to their respective PISO, along with the un-coded V and C (constant zero bit) bits; note that the constant logic zero C bit is redundant, since all it does is provide 10-bit symmetry with IOPPM+ serialised stream, but carries no data.

Fixed Parallel Input									
D0	D1	D2	D3	D4	D5	D6	D7	S	V
0	1	0	1	0	0	0	0	0	0
LSB		MSB	LSB		MSB	LSB		MSB	UC

IOPPM+ Encoder Parallel Output Loads IOPPM+ PISO									
Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	V
0	1	0	1	0	0	0	0	1	0
LSB		MSB	LSB		MSB	LSB		MSB	UC

IOPPM- Encoder Parallel Output Loads IOPPM- PISO									
Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	C
0	0	0	0	0	0	1	0	0	0
LSB		MSB	LSB		MSB	LSB		MSB	UC

Table 7-3 Test pattern 1 encoding table

Following the assertion of logic low at the load pulse input of the PISOs, the bits are simultaneously loaded into the IOPPM+ and IOPPM- PISOs. After one cycle of the serial clock (66 MHz), logic high is asserted at the load pulse input of the PISOs and the bits are simultaneously clocked serially out of both PISOs; the LSB bits emerge first. Figure 7-33 shows the simulated and hardware generated serial clocking sequence of the IOPPM+ and IOPPM- streams, measured at the serial outputs of the PISOs (IOPPM+ test point A and IOPPM- test point C in the model and IOPPM+ hardware configurations). The simulated IOPPM+ stream is indicated by the red trace, and the hardware generated by the light grey trace. Similarly, the simulated IOPPM- stream is indicated by the blue trace, and the hardware generated by the black trace. Both IOPPM+ and IOPPM- streams show precise correlation between the simulated and measured hardware.

Figure 7-33, also shows dotted vertical lines which represent the 15.15 ns slot times for each bit clocked out of the PISOs, indicating that the timing between the IOPPM+ and IOPPM- streams is correct, since the pulses fit precisely into the slot times. The slots times also contain bit labels (Y0 through V and Z0 through C) which correspond directly with those in Table 7-3, and indicate that the IOPPM coded bit sequences in the

coding table map precisely to the serialised pulses; this verifies that simulated and hardware generated streams for min terms 0, 1 and 2 are correctly encoded.

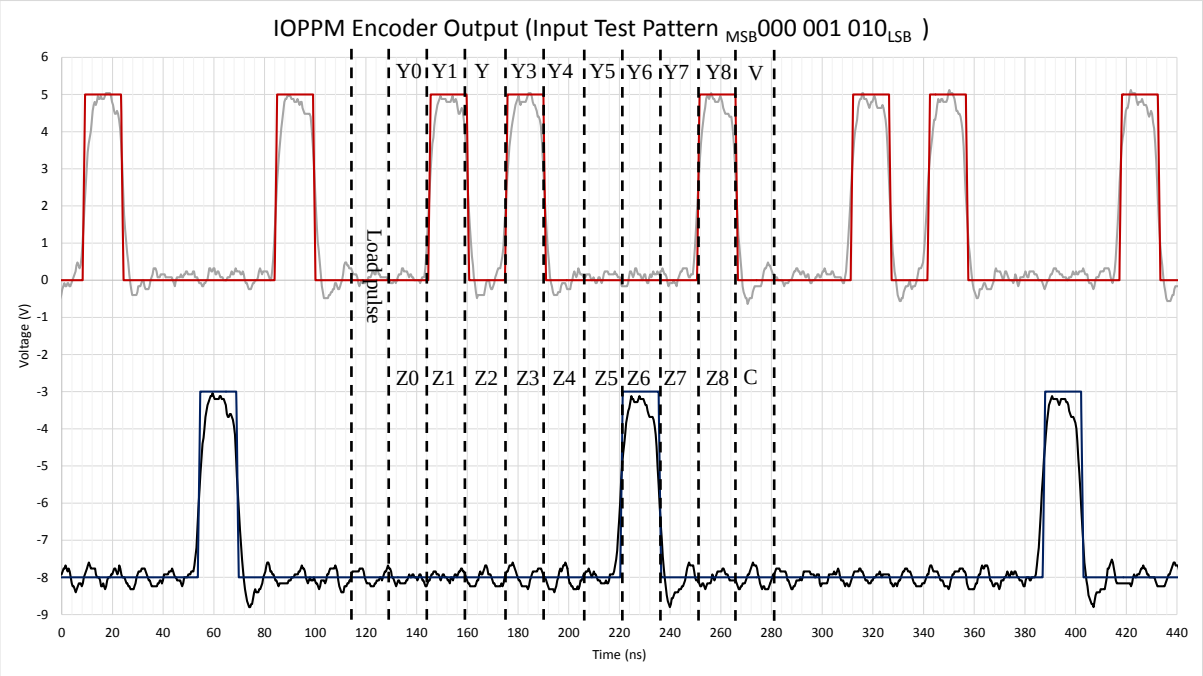


Figure 7-33 Test pattern 1: IOPPM+ and IOPPM- serial output

The verification of the remaining IOPPM encoder min terms was performed using test pattern 2 and test pattern 3. Test pattern 2 is shown in Table 7-4, and in this case, bits D0 through D2 map to min term 5, D3 through D5 to min term 4, and D6, D7 and S to min term 3 of Table 7-1, resulting in the IOPPM+ and IOPPM- codewords shown in the right-hand-side column of Table 7-4. Applying the test pattern to the IOPPM encoders and PISOs, results in the serialised outputs shown in Figure 7-34; note the colour-coding used in the traces is identical to those used for test pattern 1. Again, the serial output of the IOPPM+ and IOPPM- PISO correlates with the coding table for test pattern 2.

Fixed Parallel Input									
D0	D1	D2	D3	D4	D5	D6	D7	S	V
1	0	1	0	0	1	1	1	0	0
LSB		MSB	LSB		MSB	LSB		MSB	UC

IOPPM+ Encoder Parallel Output Loads IOPPM+ PISO									
Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	V
0	0	0	1	0	0	0	0	1	0
LSB		MSB	LSB		MSB	LSB		MSB	UC

IOPPM- Encoder Parallel Output Loads IOPPM- PISO									
Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	C
1	0	0	0	0	1	0	0	0	0
LSB		MSB	LSB		MSB	LSB		MSB	UC

Table 7-4 Test pattern 2 encoding table

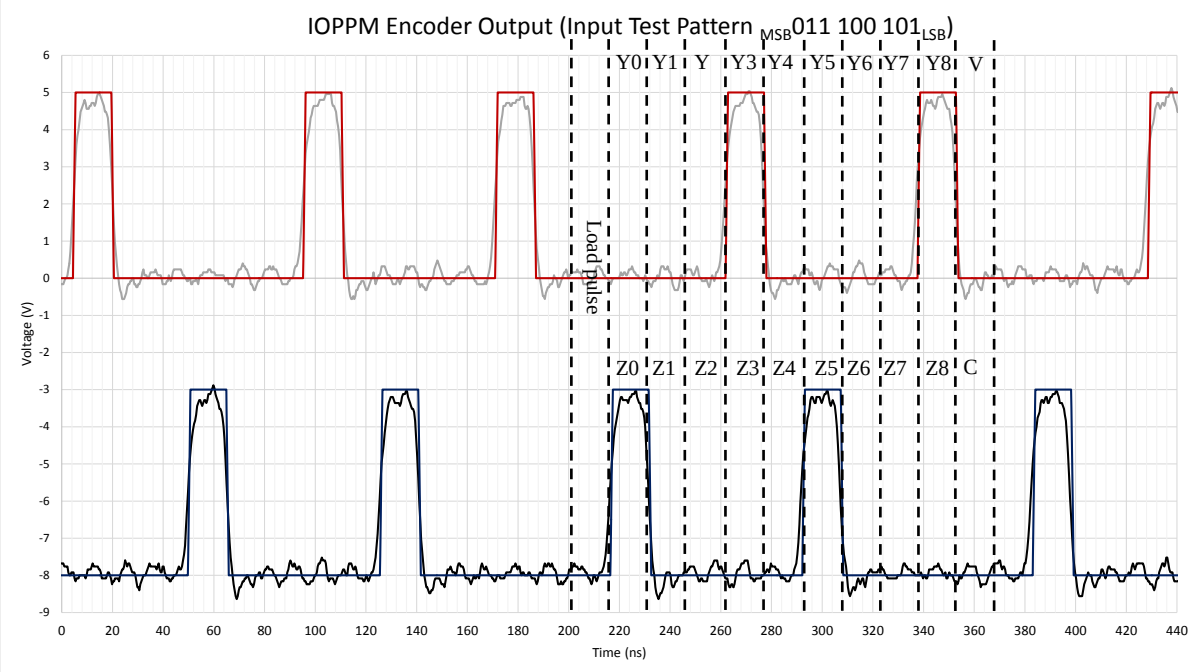


Figure 7-34 Test pattern 2: IOPPM+ and IOPPM- serial output

Finally, test pattern 3, shown in Table 7-5 was used to map bits D0 through D2 to min term 0 (this min term was redundant), D3 through D5 to min term 7, and D6, D7 and S to min term 6 of Table 7-1, resulting in the IOPPM+ and IOPPM- codewords shown in the right-hand-side column of Table 7-5. Applying the test pattern to the IOPPM encoders and PISOs, results in the serialised outputs shown in Figure 7-35; note the colour-coding used in the traces is identical to those used for test pattern 1 and 2. Again, the serial output of the IOPPM+ and IOPPM- PISO correlates with the coding table for

test pattern 3, thus verifying the encoding and serialisation of the IOPPM encoder min terms 6 and 7.

Fixed Parallel Input									
D0	D1	D2	D3	D4	D5	D6	D7	S	V
0	0	0	1	1	1	0	1	1	0
LSB		MSB	LSB		MSB	LSB		MSB	UC

IOPPM+ Encoder Parallel Output Loads IOPPM+ PISO									
Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	V
0	0	1	0	0	0	0	0	0	0
LSB		MSB	LSB		MSB	LSB		MSB	UC

IOPPM- Encoder Parallel Output Loads IOPPM- PISO									
Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	C
1	0	0	0	0	1	0	1	0	0
LSB		MSB	LSB		MSB	LSB		MSB	UC

Table 7-5 Test pattern 3 encoding table

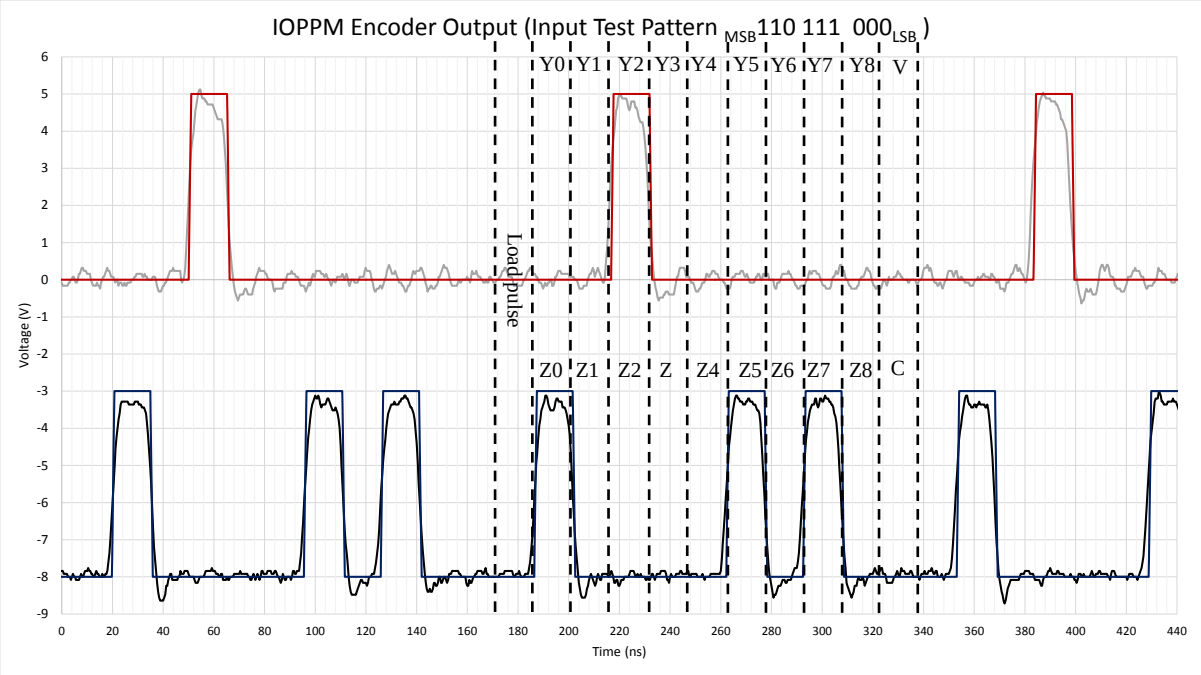


Figure 7-35 Test pattern 3: IOPPM+ and IOPPM- serial output

Following verification of the encoder and PISO serialisation at the receiver, the decoder and central detection was verified at the receiver using the same three test patterns. In this case, the IOPPM+ stream was transmitted over the FSO channel, and the IOPPM- stream was hardwired between the IOPPM encoder and decoder inside the FPGA; note

that the IOPPM- input to the composite LED driver was connected to ground, as shown in Figure 7-32, to ensure the FET was completely turned off, and unable to cause disturbance to the IOPPM+ path during transmission.

During the decoder and central detection verification, the receiver was configured as shown in Figure 7-36.

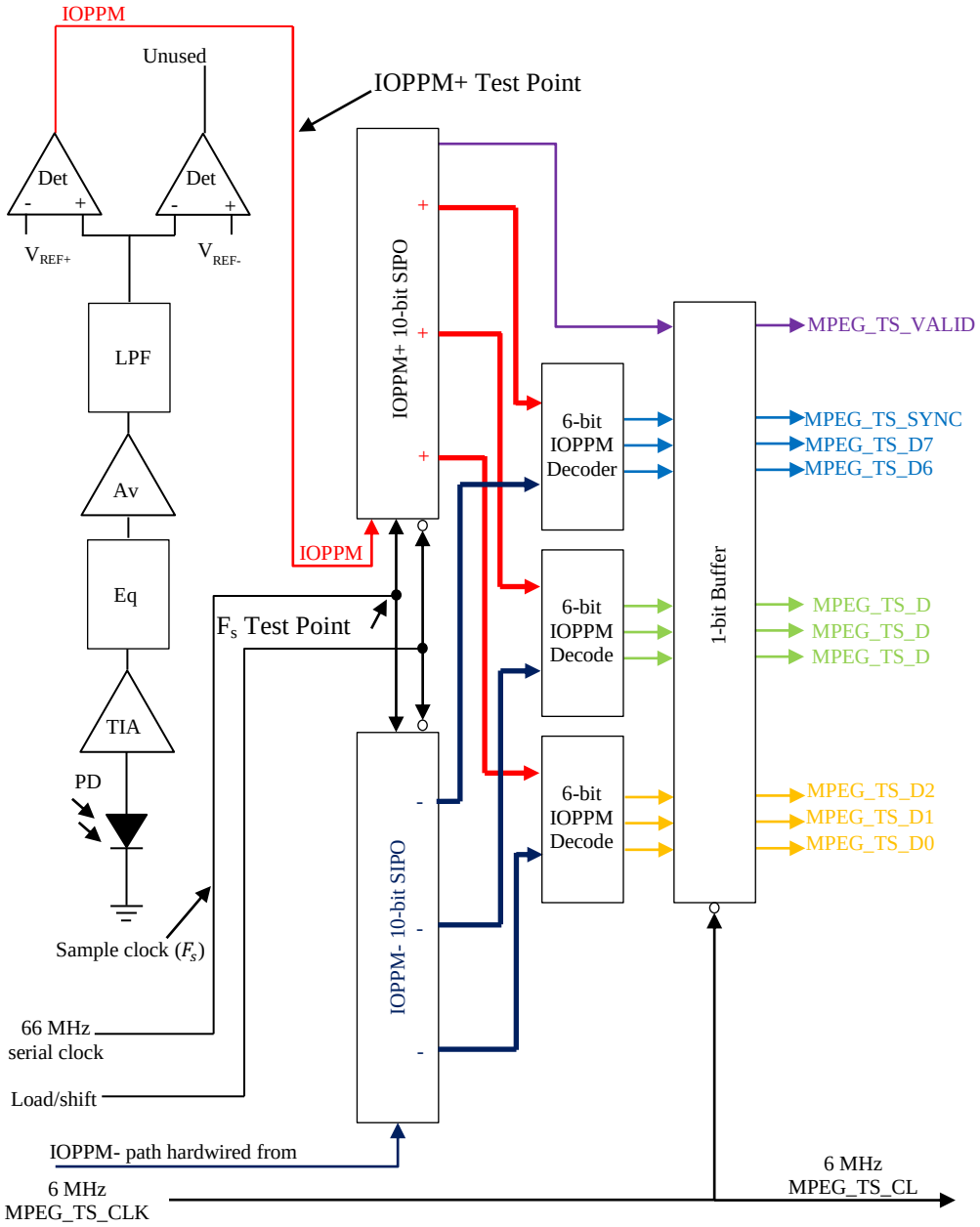


Figure 7-36 IOPPM receiver/decoder

The 66 MHz serial clock, which was shifted by half a clock cycle relative to the transmitter serial clock (effectively become the central decision F_S sample clock), was hardwired, along with the load/shift signal, 6 MHz MPEG TS clock and IOPPM- path to the IOPPM decoder. The IOPPM+ signal was transmitted over the FSO channel and received by the receivers PD and processed by the analogue stages. At the window comparator, the IOPPM+ signal was processed by the non-inverting comparator, which was set with a V_{REF+} of 700 mV.

In order to measure the decision detection point relative to the received IOPPM signal, the IOPPM+ signal was measured at the output of the non-inverting comparator at the 'IOPPM Test Point' (shown in Figure 7-36), and the 66 MHz sample clock at the 'F_S Test Point' (shown in Figure 7-36); note that the FPGA was configured in this test to output the sample clock on an external pin to enable measurement. Figure 7-37 shows the received IOPPM+ signal (blue trace) relative to the sample clock, F_s (red trace). The peaks of the sample clock were found to lead the centre of the IOPPM+ signal by 1.4 ns, so the received signal was clocked into the decoders SIPO slightly early; this was considered a small error and no corrective action was taken.

The decoder was then verified by transmitting test patterns 1, 2 and 3 over the FSO channel and measuring the parallel output of the receiver/decoders 1-bit buffer shown in Figure 7-36. The received bit sequences were compared with original transmitted sequences shown in Table 7-3 (test pattern 1), Table 7-4 (test pattern 2) and Table 7-5 (test pattern 3), and all received sequences matched the transmitted sequences.

The test performed in this section verified the central decision detection and decoder performance of the VLC system.

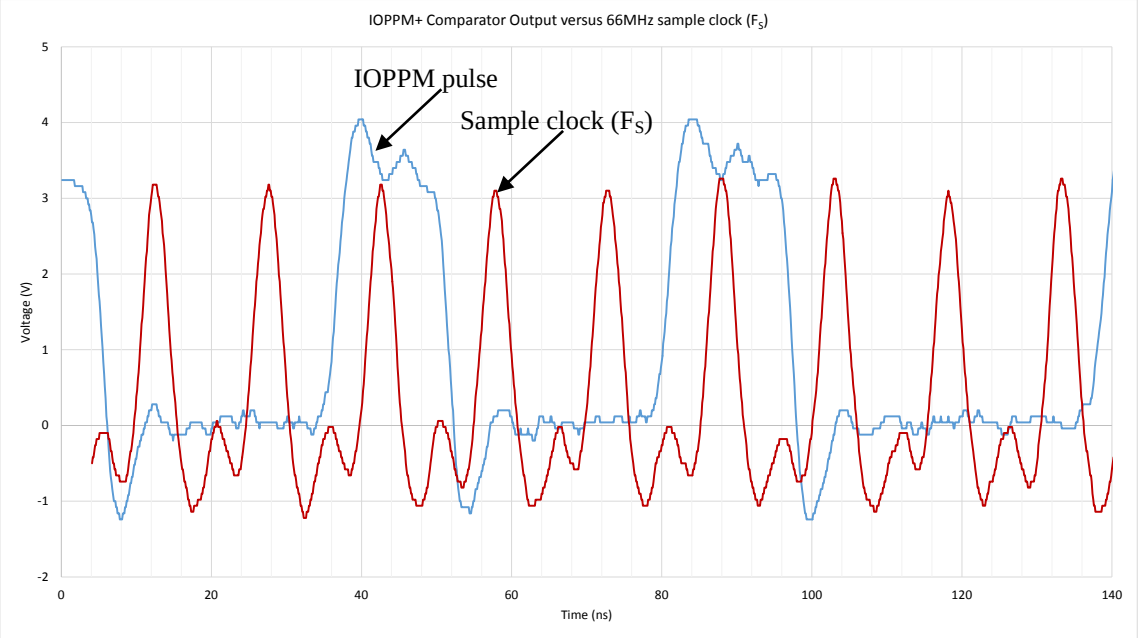


Figure 7-37 Central decision detection

7.3 End-to-End System Verification

The final and definitive test of the VLC system as a video distribution system was to encode a live off-air DVB-T2 broadcast MPEG TS, transmit it over the FSO channel, and then receive and decode the content and reproduce it on an HD monitor. This was achieved using the IOPPM+ hardware configuration shown in Figure 7-38, where the IOPPM+ path was transmitted over the FSO channel and the IOPPM- channel was hardwired to decoder, along with the 6 MHz MPEG TS clock, 66 MHz serial clock and load/shift signal. The off-air DVB-T2 signal was received by the Silicon Labs EVB on Channel C41 (F_C = 634 MHz, Emley Moor Transmitter, West Yorkshire, UK) and contained a combination of MPEG-2 (SDTV) and MPEG-4 (HDTV) content, operating with a of data rate of 40.21 Mbit/s. The RF signal had a QAM 256 constellation, 2/3 code rate, 1/128 guard interval and 32 K FFT. The VLC transmitter, receiver and comparator modules were configured as described in section 7.1.

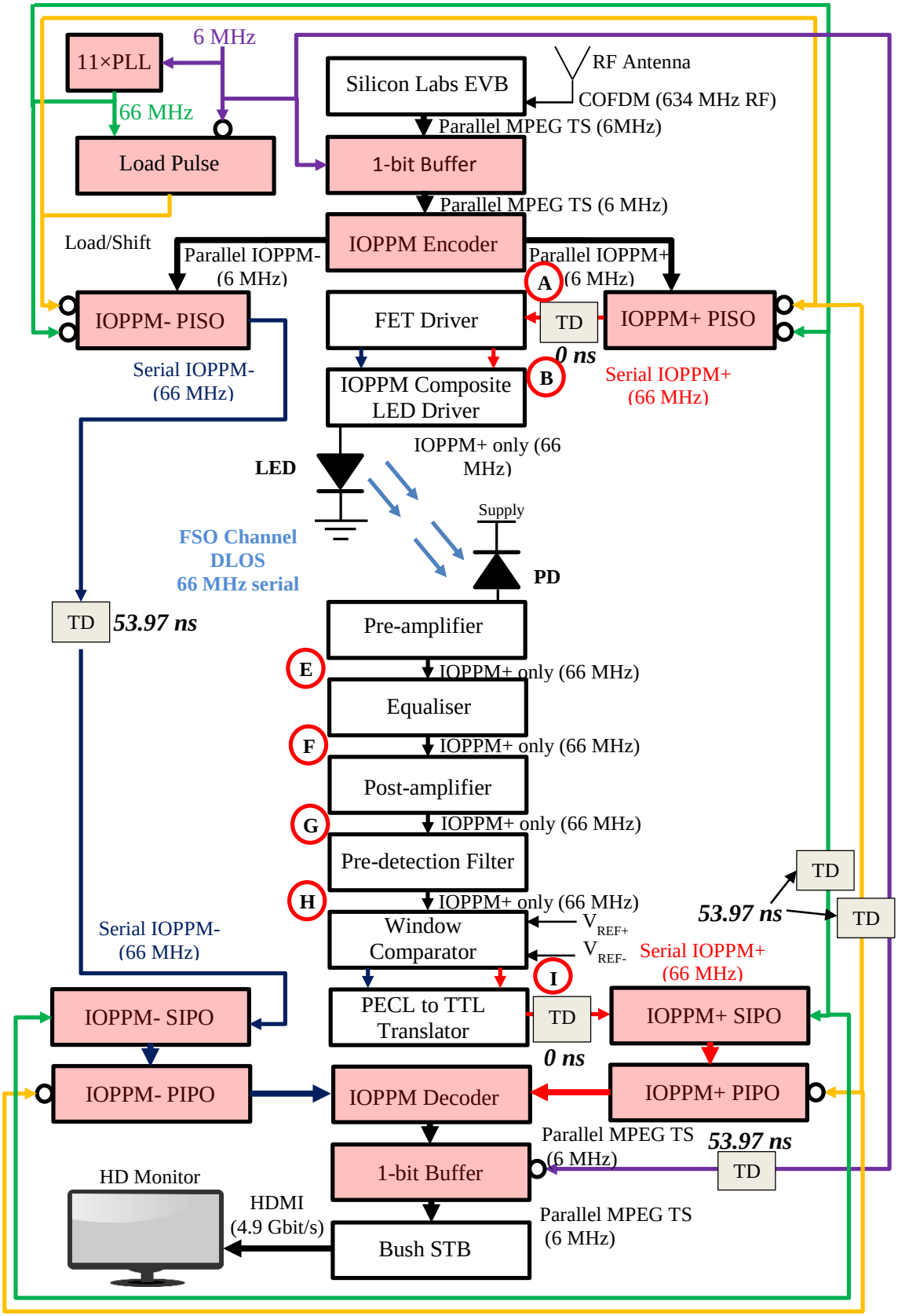


Figure 7-38 VLC IOPPM+ optical transmission configuration

At the receiver, MPEG decoding and HDMI interfacing to the HD monitor was performed by the Bush DH2636 STB.

The DLOS optical rail arrangement described in Chapter 6 (Figure 6-19) was used for the live off-air testing, and the distance between the transmitter modules LED and the receiver modules PD was set at 1.2 m.

7.3.1 Reproduction and Errors

The VLC system successfully reproduced all the elementary streams contained with Channel C41 multiplex. Specifically, the video and audio content of the following elementary streams was reproduced on the HD monitor (including audio output): C86 More4 +1; C101 BBC One HD; C102 BBC Two HD; C103 ITV HD; C104 Channel 4 HD; C105 Channel 5 HD; and C204 CBBC HD. One elementary stream contained SDTV content, namely C86 More4 +1, and the remaining six streams were HDTV.

During reception of live off-air content, the EVB software was used to monitor the number of packet errors in the received RF signal to ensure that these remained at zero during the FSO channel transmission; this was performed to ensure that packet errors due to the RF reception of the channel were not included in the VLC systems packet error count. Similarly, the STB at the receiving end of the VLC system was used to monitor the number of packet errors occurring in the transport stream transmitted over the FSO channel. This was monitored for a period of one hour and the average number of packets received in error during this time was approximately one thousand. Based on the 40.21 Mbits/s data rate and a 188 byte packet size, the bit error rate (BER) was estimated at 1×10^{-5}; this result is a coarse estimate as it does not account for errors in the hardwired IOPPM- path. The BER result was achieved without using error correction coding.

7.3.2 System Latency

The VLC system was able to reproduce content on the HD monitor, on average, within 2.7 s of the EVB data source being issued with a tune command; this time will inevitably increase once clock recovery circuitry is used at the receiver to phase-lock the IOPPM decoders PLL and perform IOPPM frame synchronisation with the transmitters IOPPM encoder.

Note: the average time is based on a sample of 25 measurements.

7.3.3 FSO Channel Signal Blocking and Recovery Time

Blocking of the optical transmission by placing an object between the transmitter and receiver resulted in a loss of content at the HD monitor, on average, after 1.2 s; this implied that 1.2 s of content is buffered in the entire receiver chain, up to and including the HD monitor. Following a blocking event, reproduction is restored, on average, after 1.9 s. The difference between signal acquisition from a tuning command (2.7 s) and recovery from blocking (1.9 s) is 800 ms; this implied that the receiver takes the longest period of time to decode and buffer the received MPEG TS.

Note: the average times are based on a sample of 25 measurements for each condition.

These final system level tests verified the operation of the proof-of-concept VLC video distribution system. Specifically, the test verified that IOPPM transmission using the dual LED architecture described in Chapter 3, section

7.4 Conclusions

In this chapter, the results and analyses of the VLC system electrical model and hardware implementation of the single and dual LED architectures was presented.

It was concluded in this chapter that:

- The parametric digital and analogue results for the electrical model and hardware implementation closely correlate.
- The FPGA timing and duration of the IOPPM pulses is sufficiently accurate to support transmission and central decision detection at the receiver. The single pulse duration was in error by 32% of the theoretical value of 15.15 ns, and the double pulse was in error by 13.5% of the theoretical value of 30.30 ns. These values were insufficient to cause significant ISI, since the pulses were centred within their respective slot times.
- The sinc function behaviour of the IOPPM+ and IOPPM- streams frequency spectrum was confirmed. The first zero crossing (null) in the frequency domain was confirmed at the serial clock frequency of 66 MHz, with harmonically related nulls occurring at 132 MHz and 197 MHz. Spacing of individual frequency components within the spectrum were defined by the parallel MPEG TS parallel clock frequency (6 MHz). It was also concluded that a lower the serial clock frequency results in a lower system bandwidth. Using the 66 MHz serial clock frequency for the VLC system enables bit rates of 30 Mbits/s per IOPPM channel.
- The IOPPM+ composite FET driver circuitry was confirmed to be able to driver the LED with IOPPM encoded data over the FSO channel, however, the IOPPM- FET driver was unable to provide sufficient voltage swing at the output of the receivers pre-amplifier to distinguish logic ones from logic zeroes. Single LED using composite IOPPM drive was abandoned to focus on verification of the dual LED architecture.

- The pre-amplifiers transimpedance gain of 81.6 dBΩ was able to provide a voltage swing of 700 mVpp, which was sufficient to drive the 2nd order RC equaliser and post-amplifier input. In effect, the transmitter module, using a blue LED (470 nm wavelength) operating with a quiescent bias of 13 mA and pulse bias of 26 mA was able to successfully transmit IOPPM encoded data over a FSO with a transmitter and receiver separation of 1.2 m.
- The optical transmission produced Gaussian shaped pulses at the receiver, as predicted in Chapter 2. The shape of the pulses was successfully simulated using the 10th order Butterworth filter and voltage controlled current source of the electrical model. The simulated single pulse duration were demonstrated to be 25.8% longer than the hardware, and the double pulses 15.4% longer.
- The 2nd order RC equaliser, having a roll-off of 15 dB/decade, was sufficient to equalise the roll-off caused by the FSO channel and LED frequency response.
- The post-amplifier voltage gain was revised from 25.38 dB to 24 dB to lower noise and prevent clipping in the output signal, and also to reduce ringing in the pulses. 18 dB of voltage attenuation was applied at the amplifier output to enable the IOPPM+ signal to fit inside the window comparator 0 V to 1 V range.
- The pre-detection filter provided the required 3 dB bandwidth at 70% of the 66 MHz serial clock, and eliminated ringing from the received IOPPM signal.
- The IOPPM+ comparator V_{REF}+ was optimally set at 700 mV.
- The dual LED IOPPM encoder/transmitter and receiver/decoder architecture was aligned, and parametrically and systemically verified.
- Transmission of a 40.2 Mbits/s live off-air DVB-T2 broadcast multiplex containing mixed SDTV and HDTV content was successfully IOPPM encoded, transmitted

over a FSO channel, received at a distance of 1.2 m, the content decoded and then reproduced on an HD monitor.

- The end-to-end system generated, on average, one thousand packet errors every hour, resulting in an estimated BER of 1×10^{-5}.
- The latency from the issuing of a channel tune command on the EVB to reproduction of content on the HD monitor was 2.7 s.

8 Discussion

In this work, a new VLC based system for distributing broadcast video content in consumer premises was presented. The application of the system is aimed at flat-panel TV manufacturers as way to eliminate all connectors from the TV, thereby reducing costs and enabling the production of TVs that are easier to wall-mount in consumer premises. The system also offers manufacturers the ability to produce region-less TVs, fitted with a VLC receiver in place of the tuner and demodulator, which are relocated to a low-cost STB receiver with an integrated VLC transmitter. The STB is installed in the plenum space above the room where the TV is located, and is used to receive content from terrestrial, cable, satellite or IP based broadcasts, and re-encode the content for transmission over a FSO channel using a visible light LED. The LED is mounted on a gimbal, which is attached to ceiling below the plenum space, and provides 360° of horizontal rotation, and vertical tilt control enabling the light emission from the LED to be directed at any wall where the TV is mounted. A PD fitted on the front panel of the TV is used to receive the optical transmission.

In this work, a proof-of-concept VLC digital TV distribution system (Figure 8-1), consisting of an encoder/transmitter and receiver/decoder was demonstrated by simulation and in physical hardware, and good correlation between simulated and hardware measurements were demonstrated and verified. Most notably, the electrical modelling of optical channels Gaussian pulse shaping using a 10^{th} order Butterworth low-pass filter, and modelling of the PD photocurrent using a voltage controlled current source were very successful.

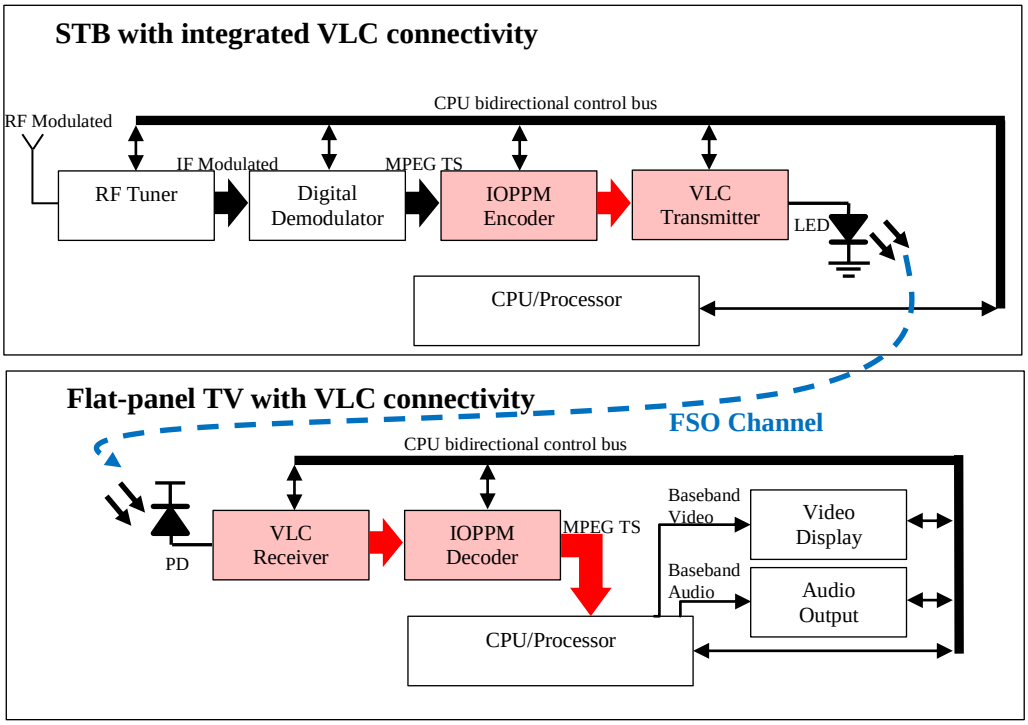


Figure 8-1 Proof-of-concept VLC video distribution system

It was proven that a newly devised coding scheme, called inversion offset PPM (IOPPM), was able to perform real-time encoding of a 6 MHz, parallel MPEG TS using combinational logic circuits, and that two independent data streams generated by the scheme could be serialised using sequential logic circuits clocked at 66 MHz; note minimum theoretical slot time for pulses was 15.15 ns. It was also proven that the two serialised data streams, named IOPPM+ and IOPPM-, were able to intensity modulate two LEDs, thus generating two independent optical transmission channels. A single LED architecture was initially proposed that used a bipolar composite driver levels, generated by the two streams, but the composite LED driver circuit was unable to drive LED correctly to produce the required voltage swing at the optical receiver; the author, however, still believes that this concept is achievable with the correct drive levels and requires further research.

It was proven that a visible light LED, operating at a wavelength of 470 nm (blue emission), and biased using a low forward current in the range of 13 to 26 mA, was capable of transmitting IOPPM encoded data at frequency of 66 MHz over a DLOS FSO channel, where the transmitter and receiver were separated by 1.2 m. It was also demonstrated that the use of visible light enabled simple, intuitive alignment and focussing of the received light at the PD of the receiver in order to achieve optimal signal level, and that due to the use of a low LED forward bias current, manual alignment and focusing by consumers is safe, since the emission power of the LED is well within the regulatory safety limits.

It was proven that a direct-detection receiver using a PD with a responsivity of 0.04 A/W at 470 nm, and a pre-amplifier with a transimpedance gain of 81.6 dBΩ, was sufficient to produce an output voltage swing of 700 mV; based on transmitter and receiver separation of 1.2 m. It was also demonstrated that a 2^{nd} order RC equaliser was sufficient to compensate for the roll-off of the LED and the FSO channel, effectively increasing the bandwidth from 7 MHz to 66 MHz. Furthermore, it was demonstrated that a post-amplifier with a gain of 24 dB was necessary to reduce ringing in the received signal and achieve a higher SNR (~30 dB). It was also proven that a 3^{rd} order Butterworth low-pass pre-detection filter, having a 3dB bandwidth of 46.2 MHz, provided the necessary pulse shaping and reduction in ringing between pulses, to clearly distinguish transmitted pulses to enable threshold detection in the comparator. Use of a 17 dB voltage attenuator and application of a 0.5 V DC offset to the received signal, following pre-detection filtering, was necessary to fit the signal into the 0 V to 1 V input range of the comparator. Using the IOPPM+ comparator in the window comparator, it was proven that a threshold voltage (V_{REF+}) of 700 mV was sufficient to recreate the

IOPPM+ digital stream. Single pulses threshold crossing produced bits with durations of 19.6 ns (29.4% on the 15.15 ns theoretical value), and double pulses produced bits with duration of 35.2 ns (16.2% on the 30.30 ns theoretical value). The overlap of the pulses was not sufficient to cause significant ISI, and the use of central decision detection at the IOPPM decoder, enable logic ones and logic zeroes to be correctly distinguished.

- Using consumer grade STB equipment to source and sink the MPEG TS, verification of the end-to-end performance of the VLC system using live off-air DVB-T2 HDTV content was demonstrated. The system successfully IOPPM encoded and transmitted over the FSO optical channel (1.2 m distance), a live off-air DVB-T2 broadcast multiplex, which had an effective bit rate of 40.21 Mbit/s and contained a combination of MPEG-2 (SDTV) and MPEG-4 (HDTV) program streams. The IOPPM stream was successfully received and decoded, and the content reproduced on an HD monitor at the receiver. Note that, only the IOPPM+ stream was transmitted over the FSO channel, whilst the IOPPM- channel was hardwired between the IOPPM encoder and decoder in the FPGA; this was because only one IOPPM input and output path was available in the FPGA implementation. The end-to-end system generated, on average, one thousand packet errors every hour, resulting in an estimated BER of 1×10^{-5}.

The final, verified system specification for the VLC video distribution system is shown in Table 8-1.

The VLC video distribution system presented in this thesis is the first system of its kind to integrate off-the-shelf consumer grade STB equipment into a complete end-to-end, demonstrable hardware system. The use of IOPPM to encode and decode the optical stream is also novel.

Stage/Device	Specification
MPEG TS source and sink devices	
Broadcast standards	DVB-T and DVB-T2
Clock frequency	6 MHz
MPEG TS mode	Parallel
Bits used	10-bits: valid,sync and D0 through D7
Encoding/Decoding	
Encoding/decoding scheme	IOPPM
Serial clock frequency	66 MHz
Number of channels	2 × IOPPM
Bit rate per channel	33 Mbits/s per channel
Transmitter	
LED wavelength	470 nm wavelength (Blue)
LED bias current	13 mA (quiescent) and 26 mA (peak)
Receiver	
PD responsivity	0.04 A/W (470 nm wavelength)
Pre-amplifier Transimpdance gain	81.6 dBΩ
Equaliser	15dB/decade positive slope (2^{nd} order RC)
Post-amplifier	24 dB
Pre-detection filter	3^{rd} order Butterworth LPF, 46.2 MHz 3dB cut-off
Attenuator	17 dB (set to provide 1 V pp into the window comparator)
Window comparator	0 V to 1 V input range VREF+ = 700 mV VREF- = 300 mV (inferred)
Detection	Central decision
BER	1×10^{-5}
Optical Configuration	Direct line-of-sight. Collimating lens used at transmitter and receiver. Transmitter and receiver separated by 1.2 m.

Table 8-1 VLC system specification

9 Conclusions and Further Work

9.1 Conclusions

Based on the original aims and objectives stated in the introduction of Chapter 1, section 1.3, the accomplishments are stated as follows:

The primary aims of the work were to:

1) **Produce an LED based, FSO VLC unidirectional HDTV distribution system.**

   This was successfully demonstrated with the end-to-end system transmission of live off-air DVB-T2 content.

2) **Produce a FSO VLC transmitter and receiver system that interfaces directly with existing DVB MPEG TS buses used in consumer grade STBs.**

   This was successfully demonstrated by the digital interfacing between the MPEG TS output of the Silicon Labs EVB and input of the FPGAs IOPPM encoder, and similarly between the output of the FPGA IOPPM decoder and input of the Bush DH2636 STB.

3) **Produce a link bit rate of at least 50 Mbit/s to support DVB-T2 broadcasts.**

   This was successfully demonstrated with the dual LED IOPPM architecture which enabled the transmission of two independent IOPPM (+/-) serial streams with effective bit rates of 30 Mbit/s per path over a FSO channel. Each path was used in conjunction with an intensity modulating circuit to drive a blue LED in order to generate an overall 33 Mbit/s FSO link bit rate per channel. The link was also proven to support a live off-air DVB-T2 bit rate of approximately 40.21 Mbit/s, based on the reception of Channel 41 (634 MHz) multiplex from Emley

Moor transmitter in West Yorkshire, UK; note this channel was a DVB-T2 broadcast having a QAM 256 constellation, 2/3 code rate, 1/128 guard interval and 32 K FFT.

The IOPPM composite single could not be evaluated due to a lack of space on the FPGA development board and the fact that the composite drive circuit could not produce sufficient voltage swing at the receiver.

4) **Demonstrate end-to-end transmission of MPEG TS content, and successfully display recovered content on an HD monitor.**

   This was achieved using the same live off-air channel described in point (7) below. The channel was applied to the RF input of the Silicon Labs EVB, which down-converted and demodulated the channel to the required baseband 6 MHz parallel MPEG TS. The TS was then IOPPM encoded and the resultant IOPPM+ and IOPPM- streams serialised at a rate of 66 MHz, enabling the intensity modulation of the blue LEDs emission for transmission over the FSO channel. Located 1.2 m away from the transmitter, the DD receiver recovered the IOPPM streams, performed deserialisation and IOPPM decoding in order to recover the 6 MHz parallel MPEG TS. The TS was then decoded using the Bush DH2636 STB and the content output on the STBs HDMI interface and displayed on an HD monitor.

The specific objectives of the work were to:

1) **Implement the system using low-cost terrestrial STBs**
   a. **Source STB for receiving off-air DVB-T/T2 content. Providing RF to MPEG TS.**

This was successfully demonstrated by the use of the Silicon Labs EVB, which was used to down-convert live off-air DVB-T2 broadcasts to the 6MHz parallel MPEG TS.

b. Sink STB capable of decoding MPEG TS and supporting HDMI baseband output.

This was successfully demonstrated by the use of the Bush DH2636 STBs, which was used to decode the parallel MPEG TS and produce an HDMI output, which enabled reproduction of the decoded content on an HD monitor.

2) Fully analyse MPEG TS, and design a modulation scheme capable of re-encoding the MPEG TS for transmission over a visible light FSO channel.

Analysis of the MPEG TS was demonstrated by the characterisation of the parallel MPEG TS of the Silicon Labs EVB and Bush DH2636 STB. It was determined that the VLC system needed to encode nine bits of the 6 MHz parallel MPEG TS, specifically: eight bits for the data lines, TS_DATA [$7_{MSB}\ldots0_{LSB}$], and one bit for the TS_SYNC line, with the remaining TS_VALID line bit transmitted unencoded. The conclusion was that the minimum bandwidth and serialised clock frequency of the system needed to be 60 MHz. However, this was revised upward to 66 MHz during design of the systems PISO and SIPO used by the encoder and decoder, respectively, because an additional clock cycle was necessary to load and unload the shift-registers.

A new IOPPM scheme, based on the modification of the sign bit used by OPPM was demonstrated. The slot-time of OPPM sign bit was translated to a bipolar level representation, resulting in the generation of two independent, non-conflicting data streams, IOPPM+ and IOPPM-. The two streams were able to

coexist within the same time period. The removal of slot time for the sign bit, enabled the encoders input bit rate to match its output bit rate for 3-bit encoding, but with a 3 dB compromise in receiver sensitivity. The system successfully demonstrates the transmission of IOPPM with a minimum slot time of 15.1515 ns.

3) **Select an appropriate LED type for the system based on optimal characteristics.**

   A blue (470 nm) LED was selected as the optimal device for the system due to wide bandwidth across all forward bias currents, compared to a white, phosphor based LED. At 13 mA, the blue LED produced a bandwidth of 7 MHz, which was 159% wider than the white LED at the same forward bias current. The blue LED was DC biased at 13 mA in the system in order to keep the power consumption low at the transmitter. This bias current provided error-free transmission over a 1.2 m distance.

4) **Select an appropriate type of receiving PD for the system based on optimal characteristics.**

   A PD with a bandwidth of 250 MHz bandwidth was selected. The device achieved this bandwidth with a combination of its small detection surface area of 0.78 mm and also it operation with a 12V reverse voltage to provide a diode capacitance of 3pF. The device also exhibited a fast, 2.5 ns rise- and fall-times, and had a half sensitivity angle of ± 20° that limited multipath effects, and operated with a very small dark current of 5 nA. The responsivity of the device was approximated at 0.04 A/W at the blue LEDs wavelength of 470 nm. This result was found to be of the expected order, but was lower than the 0.14 A/W stated for similar devices operating at 480 nm.

5) **Design and develop circuitry to modulate the transmitting LED based on the modulation scheme.**

   A new FET based IOPPM modulator circuit was designed, but only the IOPPM+ path was proven to work during hardware evaluation. The author believes that the concept is still feasible, but further development of the driver circuit is needed.

6) **Design and develop appropriate pre and post-gain stages and filtering for the receiver.**

   A pre-amplifier stage with an 86 dBΩ transimpedance gain was designed using a commercially available op-amp. A post-amplifier with a voltage gain of 24 dB was also designed using the same op-amp. A pre-detection filter with a cut-off frequency of 46.2 MHz, based on 70 % of the serial clock (66 MHz), was implemented using a 2^{nd} order Butterworth low-pass prototype.

7) **Design and develop passive equalisation circuitry in the receiver to overcome bandwidth limitations of the LED.**

   Using empirical measurements of the cascaded PD and pre-amplifier in the receiver, and polynomial curve fitting techniques, it was determined that a simple RC equaliser circuit was capable of compensating for the roll-off of the LED response. Compensation was applied to the output of the pre-amplifier using a 4 kΩ resistor, fitted in parallel with a 47 pF capacitor. An equalised response exhibiting a 3 dB point at 39.13 MHz, compared to a theoretical 3 dB point at 33 MHz based on 50 % of the serial clock (66 MHz). This represented an 18.6 % error on the theoretical frequency, but did not prevent operation of the system.

8) **Implement MPEG TS encoding and decoding using a FPGA platform.**

The IOPPM encoder and decoder logic was successfully implemented using a commercially available FPGA development board. All logic circuits were generated and simulated using Altera Quartus II environment. Logic circuits were generated with using schematics and primitive blocks, which were then used to generate hierarchical blocks. A 66 MHz PLL was also implemented on the FPGA to create the serial clock for the system. The IOPPM encoder generated 15.15 ns slot times, based on the serial clock period, and were accurate to theoretical value by approximately 0.003%.

9) **Design and develop appropriate comparator circuitry to detect the received re-encoded MPEG TS.**

A window comparator circuit was designed to detect the positive and negative pulses of the IOPPM composite signal. The window comparator was also capable of processing single channel IOPPM using the IOPPM+ path, which was proven to require a V_{REF+} of 700 mV. It was inferred from this value, that a V_{REF-} of 300 mV would be needed for the IOPPM composite signal.

9.2 Further Work

The author suggests further work on the proof-of-concept system in the following areas:

1) Detailed theoretical analysis and optimisation of the IOPPM coding scheme. This includes the generation of a mathematical model for the scheme, and analysis of the schemes performance under wrong slot, erasure and false alarm error conditions. This investigation could lead to another PhD thesis and significant improvements to the scheme.
2) Development of IOPPM+ and IOPPM- path calibration methods, to enable automatic calibration of the receive paths to compensate for asymmetrical time delays. This calibration is the key to eliminating timing errors in the system which leads to non-optimal central decision detection in the receiver and reduced sensitivity; in extreme cases, incorrect timing can lead to IOPPM+ and IOPPM- signals corrupting each other resulting in either complete loss of data or increased error rate.
3) Development of a PLL based clock recovery system to synchronise the receiver with the transmitters 66 MHz serial clock. This work is the key to enabling the receiver to operate independently of the transmitter. In addition, methods are needed in the IOPPM decoder to enable the detection of the beginning and end of IOPPM frames (6 MHz frame rate). One technique that might achieve this is to detect the presence of the un-encoded MPEG TS valid bit transmitted at the beginning of each IOPPM frame. The valid bit is at logic one at a rate of 31.91 kHz and could be detected using additional shift registers, timers and EXOR comparators in the decoder. Another simpler technique might be to transmit a training signal during system initialisation and during channel changes to enable

both IOPPM+ and IOPPM- path timing calibration (described in point (2)) and frame alignment. MPEG lock status from the processor might also be used to signal the decoder that the processor is locked to the TS. A more sophisticated system might be developed that uses remote control commands to check MPEG lock status and trigger reset and calibrations in the IOPPM encoder and decoder; note this functionality would require software access in the data source and sink devices; this not currently possible in the data sink (Bush DH2636 STB); note the use of remote control communications between the transmitter and receiver are mentioned in Chapter 1, section 1.1.5.

4) Development of an AGC system, including a suitable power-detection schemes (peak or average), to control the cascaded gain of the pre and post-amplifier in the system. Determination of optimal take-over-points (TOP) in each amplifier needs investigation.
5) Optimisation of the PISO and SIPO block in the IOPPM encoder and decoder is needed to eliminate the load pulse signal and thereby reduce the system bandwidth from 66 MHz to 60 MHz. A better VHDL based loading method is needed.
6) Development of the IOPPM composite LED driver to increase the voltage swing at the receiver for the IOPPM- stream is necessary.
7) Development of an automated beam alignment and focussing system to collimate the LED emission. This might involve the investigation of servo-motors and feedback systems.
8) Implementation of the analogue processing systems in DSP. This might be considered to reduce hardware costs, improve reliability, reduce temperature drift and enable rapid re-configurability of the system.

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Appendices

Appendix A MATLAB Simulation Code

A.1 MATLAB code for LED intensity simulation

Function: main.m

```
% LED Emission Simulator (line-of-sight)
% Huddersfield University (Copyright 29/07/2013)
% Written by Tim Amsdon (PhD candidate)
% IMPLEMENTATION OF A VISIBLE LIGHT OPTICAL WIRELESS
HDTV DISTRIBUTION SYSTEM FOR CONSUMER PREMISES
% Function: main.m Revision A
% Function description: This function defines the room
space and the
% location of an LED within the space, and calls
appropriate functions to
% determine the number of permissible sample points
within the space, and
% to calculate the LEDs intensity at a specific
coordinate within the
% space.

clear all;
clc;

% Positions are denoted as [i,j,k] where i = width, j
= length, and k =
% height

% Space Definition

space_length = 5;                    % Length of space
[m]
space_width = 5;                     % Width of space
[m]
space_height = 2;                    % Height of Room
[m]

% No. of sample points within the volume space
%sample_points = 20000;
sample_points = 2000000;
```

```
% Call the subvolume
[vectors, act_sample_points] = subvolume_calc(
space_width, space_length, space_height, sample_points
);

% LED source location

% LED cluster location
% !!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

% Defined at the centre of space_length and
space_height and at the maximum
% height of space_height

space_width_centre = space_width / 2;
space_length_centre = space_length / 2;


% LED location at the centre of the room space at
maximum room space height
% ------------------------------
% ------------------------------
% ------------------------------
% ------------------------------
% ---------------L--------------
% ------------------------------
% ------------------------------
% ------------------------------
% ------------------------------

% LED 0 Test LED
LED_0_i = space_width_centre;    % LED 0 width [m]
LED_0_j = space_length_centre;   % LED 0 Length [m]
LED_0_k = space_height;
LED_0_vector = [LED_0_i, LED_0_j, LED_0_k];

% Initialize array and indexing for storing distance
between sample points
% and the LED transmitters
LED_0_rel_vector = zeros (act_sample_points,3); %
Single test LED
LED_0_Ro_vector = zeros (act_sample_points,4);

index = 1;
```

```
 while index < act_sample_points + 1

% Calculate vectors relative to LED and sample point
LED_0_rel_vector(index,:)=([LED_0_vector(1,1:3) -
vectors(index,1:3)]); % Single test LED

index = index + 1;

 end

[LED_0_Ro_vector] = intensity(act_sample_points,
LED_0_rel_vector, vectors);

% 4D plot
scatter3(LED_0_Ro_vector(1:end,1),LED_0_Ro_vector(1:en
d,2),LED_0_Ro_vector(1:end,3),[],LED_0_Ro_vector(1:end
,4),'.');

% Add title and axis labels
title('4D Plot of an LEDs Lambertian Intensity in a 3D
Space');
xlabel('Width (m) i coordinate');
ylabel('Length (m) j coordinate');
zlabel('Height (m) z coordinate');
```

Function: subvolume_calc.m

```
function [ vectors, act_sample_points ] =
subvolume_calc( width, length, height, sample_points )
% LED Emission Simulator (line-of-sight)
% Huddersfield University (Copyright 29/07/2013)
% Written by Tim Amsdon (PhD candidate)
% IMPLEMENTATION OF A VISIBLE LIGHT OPTICAL WIRELESS
HDTV DISTRIBUTION SYSTEM FOR CONSUMER PREMISES
% Function: subvolume_calc.m Revision A
% Function description: This function calculates the
i, j, k coordinates
% 'vectors' and actual sample_points and returns them
to function main.m.
% Calculations are based on width, length, height and
sample points passed
% from function main.m.

% Calculate number of 3D sample points based on
requested sample points
dim_sample = (round(sample_points^(1/3))) + 1;

% Compute actual sample points that will be used
act_sample_points = dim_sample^3;

% Calculate subvolume dimensions
subvolume_w = width / (dim_sample -1);
subvolume_l = length / (dim_sample -1);
subvolume_h = height / (dim_sample -1);

% Initialize i, j and k coordinates
i=0;
j=0;
k=0;

% Initialize loop counters
inc_a = 0;
inc_b = 0;
inc_c = 0;

% Initialize sample point array and indexing
vectors = zeros (act_sample_points,3);
index = 1;

while inc_a < ((dim_sample^2)/dim_sample)

        while inc_b < dim_sample
```

```
            while inc_c < dim_sample


                sample_w =  (i * subvolume_w);
                sample_l =  (j * subvolume_l);
                sample_h =  (k * subvolume_h);

                % Store sample points in an array

vectors(index,:)=([sample_w,sample_l,sample_h]);

            k = k + 1;
            inc_c = inc_c + 1;
            index = index + 1;
            end

        k = 0;
        j = j+1;
        inc_c = 0;
        inc_b = inc_b + 1;
        end

        j = 0;
        inc_b = 0;

    i = i + 1;

    inc_a = inc_a + 1;
end

end
```

Function: intensity.m.m

```
function [ vector_Ro ] = intensity( act_sample_points,
LED_rel_vector, vectors)
% LED Emission Simulator (line-of-sight)
% Huddersfield University (Copyright 29/07/2013)
% Written by Tim Amsdon (PhD candidate)
% IMPLEMENTATION OF A VISIBLE LIGHT OPTICAL WIRELESS
HDTV DISTRIBUTION SYSTEM FOR CONSUMER PREMISES
% Function: intensity.m Revision A
% Function description: Based on the i, j, k
coordinates generated by
% subvolume_calc.m function, this function calculates
the LEDs intensity
% at a specific coordinate within the defined space
and returns these to
% function main.m

vector_Ro = zeros (act_sample_points,4);

index = 1;

        % Loop to calculate the difference vector
between the sample point and the LED
        while index < act_sample_points + 1

          %
LED_rel_vector(index,:)=([LED_vector(1,1:3) -
vectors(index,1:3)]);

                % Horizontal distance from LED to
point of observation
                LED_PD_H_dist =
sqrt((LED_rel_vector(index,1)^2)+(LED_rel_vector(index
,2)^2));

                % Vertical distance from LED point of
observation
                LED_PD_V_dist =
sqrt((LED_PD_H_dist^2)+(LED_rel_vector(index,3)^2));

                % Angle from LED to point of
observation
                angle_rad =
acos(LED_rel_vector(index,3)/LED_PD_V_dist);

                % Radiant intensity inclusive of
inverse square law for
```

```
                % transmission loss
                 Ro = 1/pi * cos(angle_rad);
                %Ro =  1/(pi*( (LED_PD_H_dist^2) +
(LED_PD_V_dist^2) )) * cos(angle_rad);

                % Calculate
                vector_Ro(index,:) =
[vectors(index,1:3),Ro];

                index = index + 1;

        end

end
```

Appendix B IOPPM Encoder and Decoder Circuits

B.1 3-bit IOPPM Encoder Derivation

The IOPPM encoder was designed using combinational logic, sum of products truth table derivation and Karnaugh mapping simplification techniques.

The first step of the encoder design process was to derive a sum of products truth table using the IOPPM coding table shown in Table B.1-1.

3-bit Input Data	IOPPM Encoder Output Data $\frac{IOPPM^+}{IOPPM^-}$
000	100^+
	001^-
001	001^+
	000^-
010	010^+
	000^-
011	100^+
	000^-
100	001^+
	100^-
101	000^+
	001^-
110	000^+
	010^-
111	000^+
	100^-

Table B.1-1Coding table for IOPPM (3-bit coding)

The resulting derived truth table contained 3 inputs and 6 outputs as shown in Table B.1-2.

	Input Data			Output IOPPM+			Output IOPPM-		
Min Term	D_2	D_1	D_0	Y_2	Y_1	Y_0	Z_2	Z_1	Z_0
0	0	0	0	1	0	0	0	0	1
1	0	0	1	0	0	1	0	0	0
2	0	1	0	0	1	0	0	0	0
3	0	1	1	1	0	0	0	0	0
4	1	0	0	0	0	1	1	0	0
5	1	0	1	0	0	0	0	0	1
6	1	1	0	0	0	0	0	1	0
7	1	1	1	0	0	0	1	0	0

Table B.1-2 IOPPM encoder (3 bit coding)

The second step was to generate Boolean expressions for the sum of products min terms, resulting in the following expressions for the IOPPM+ outputs.

$$Y_0(D_2, D_1, D_0) = \sum(\overline{D_2}.\overline{D_1}.D_0 + D_2.\overline{D_1}.\overline{D_0}) \quad \text{Equation B.1-1}$$

$$Y_1(D_2, D_1, D_0) = \sum(\overline{D_2}.D_1.\overline{D_0}) \quad \text{Equation B.1-2}$$

$$Y_2(D_2, D_1, D_0) = \sum(\overline{D_2}.\overline{D_1}.\overline{D_0} + \overline{D_2}.D_1.D_0) \quad \text{Equation B.1-3}$$

And the following expressions for the IOPPM- outputs.

$$Z_0(D_2, D_1, D_0) = \sum(\overline{D_2}.\overline{D_1}.\overline{D_0} + D_2.\overline{D_1}.D_0) \quad \text{Equation B.1-4}$$

$$Z_1(D_2, D_1, D_0) = \sum(D_2.D_1.\overline{D_0}) \quad \text{Equation B.1-5}$$

$$Z_2(D_2, D_1, D_0) = \sum(D_2.\overline{D_1}.\overline{D_0} + D_2.D_1.D_0) \quad \text{Equation B.1-6}$$

The third step was to apply Karnaugh mapping techniques to the min term expressions to determine whether they were in their minimised form. In this case 2×1 variable Karnaugh maps were used to perform simplification.

The Karnaugh map for IOPPM+ encoder Y_0 output is shown in Table B.1-3. This was derived using Equation B.1-1. Two independent terms are highlighted in the map and no groupings are present to allow further simplification. Equation B.1-1 is therefore optimally simplified.

$$Y_0(D_2, D_1, D_0) = \sum (\overline{D_2}.\overline{D_1}.D_0 + D_2.\overline{D_1}.\overline{D_0})$$

$\boldsymbol{Y_0}$	$\boldsymbol{D_1.D_0}$			
	00	**01**	**11**	**10**
0	0	1	0	0
1	1	0	0	0

$\boldsymbol{D_2}$

Table B.1-3 Karnaugh map IOPPM+ encoder Y_0 output

The Karnaugh map for IOPPM+ encoder Y_1 output is shown in Table B.1-4. This was derived using Equation B.1-2. One independent term is highlighted in the map and no groupings are present to allow further simplification. Equation B.1-2 is therefore optimally simplified.

$$Y_1(D_2, D_1, D_0) = \sum (\overline{D_2}.D_1.\overline{D_0})$$

$\boldsymbol{Y_1}$	$\boldsymbol{D_1.D_0}$			
	00	**01**	**11**	**10**
0	0	0	0	1
1	0	0	0	0

$\boldsymbol{D_2}$

Table B.1-4 Karnaugh map IOPPM+ encoder Y_1 output

The Karnaugh map for IOPPM+ encoder Y_2 output is shown in Table B.1-5. This was derived using Equation B.1-3. Two independent terms are highlighted in the map and no groupings are present to allow further simplification. Equation B.1-3 is therefore optimally simplified.

$$Y_2(D_2, D_1, D_0) = \sum(\overline{D_2}.\overline{D_1}.\overline{D_0} + \overline{D_2}.D_1.D_0)$$

Y_2	$D_1.D_0$			
	00	**01**	**11**	**10**
0	1	0	1	0
D_2 **1**	0	0	0	0

Table B.1-5 Karnaugh map IOPPM+ encoder Y_2 output

The Karnaugh map for IOPPM- encoder Z_0 output is shown in Table B.1-6. This was derived using Equation B.1-4. Two independent terms are highlighted in the map and no groupings are present to allow further simplification. Equation B.1-4 is therefore optimally simplified.

$$Z_0(D_2, D_1, D_0) = \sum(\overline{D_2}.\overline{D_1}.\overline{D_0} + D_2.\overline{D_1}.D_0)$$

Z_0	$D_1.D_0$			
	00	**01**	**11**	**10**
0	1	0	0	0
D_2 **1**	0	1	0	0

Table B.1-6 Karnaugh map IOPPM- encoder Z_0 output

The Karnaugh map for IOPPM- encoder Z_1 output is shown in Table B.1-7. This was derived using Equation B.1-5. One independent term is highlighted in the map and no groupings are present to allow further simplification. Equation B.1-5 is therefore optimally simplified.

$$Z_1(D_2, D_1, D_0) = \sum (D_2 . D_1 . \overline{D_0})$$

Z_1	$D_1 . D_0$			
	00	**01**	**11**	**10**
0	0	0	0	0
1	0	0	0	1

(D_2)

Table B.1-7 Karnaugh map IOPPM- encoder Z_1 output

The Karnaugh map for IOPPM- encoder Z_2 output is shown in Table B.1-8. This was derived using Equation B.1-6. Two independent terms are highlighted in the map and no groupings are present to allow further simplification. Equation B.1-6 is therefore optimally simplified.

$$Z_2(D_2, D_1, D_0) = \sum (D_2 . \overline{D_1} . \overline{D_0} + D_2 . D_1 . D_0)$$

Z_0	$D_1 . D_0$			
	00	**01**	**11**	**10**
0	0	0	0	0
1	1	0	1	0

(D_2)

Table B.1-8 Karnaugh map IOPPM- encoder Z_2 output

Although the independent equations, Equation B.1-1 through Equation B.1-6, were optimally simplified, further analysis revealed duplicate terms in the IOPPM+ and IOPPM- expressions. Elimination of the duplicate terms was necessary in order to

reduce the gate count in the synthesised encoder circuit. Table B.1-9 shows the IOPPM+ and IOPPM- expressions with duplicate terms highlighted.

IOPPM+ Expressions	**IOPPM- Expressions**
$Y_0(D_2, D_1, D_0) = \sum(\overline{D_2}.\overline{D_1}.D_0 + D_2.\overline{D_1}.\overline{D_0})$	$Z_0(D_2, D_1, D_0) = \sum(\overline{D_2}.\overline{D_1}.\overline{D_0} + D_2.\overline{D_1}.D_0)$
$Y_1(D_2, D_1, D_0) = \sum(\overline{D_2}.D_1.\overline{D_0})$	$Z_1(D_2, D_1, D_0) = \sum(D_2.D_1.\overline{D_0})$
$Y_2(D_2, D_1, D_0) = \sum(\overline{D_2}.\overline{D_1}.\overline{D_0} + \overline{D_2}.D_1.D_0)$	$Z_2(D_2, D_1, D_0) = \sum(D_2.\overline{D_1}.\overline{D_0} + D_2.D_1.D_0)$

Table B.1-9 IOPPM+ and IOPPM- expressions with duplicate terms highlight

B.2 3-bit Integrated IOPPM+ and IOPPM- Encoder Synthesis

The Boolean expressions derived in Table B.1-9 were used to synthesis the 3-bit integrated IOPPM+ and IOPPM- encoder combinational logic circuit.

In order to reduce the gate count of the circuit, only 3 NOT gates were used to implement the negated terms for D_0, D_1, and D_2. Also, the duplicate terms $D_2.\overline{D_1}.\overline{D_0}$ and $\overline{D_2}.\overline{D_1}.\overline{D_0}$ were implemented once, and cross-wiring between the IOPPM+ and IOPPM- used to reduce gate count. Figure B.2-1 shows the final 3-bit Integrated IOPPM+ and IOPPM- encoder with the duplicate cross-wiring highlighted.

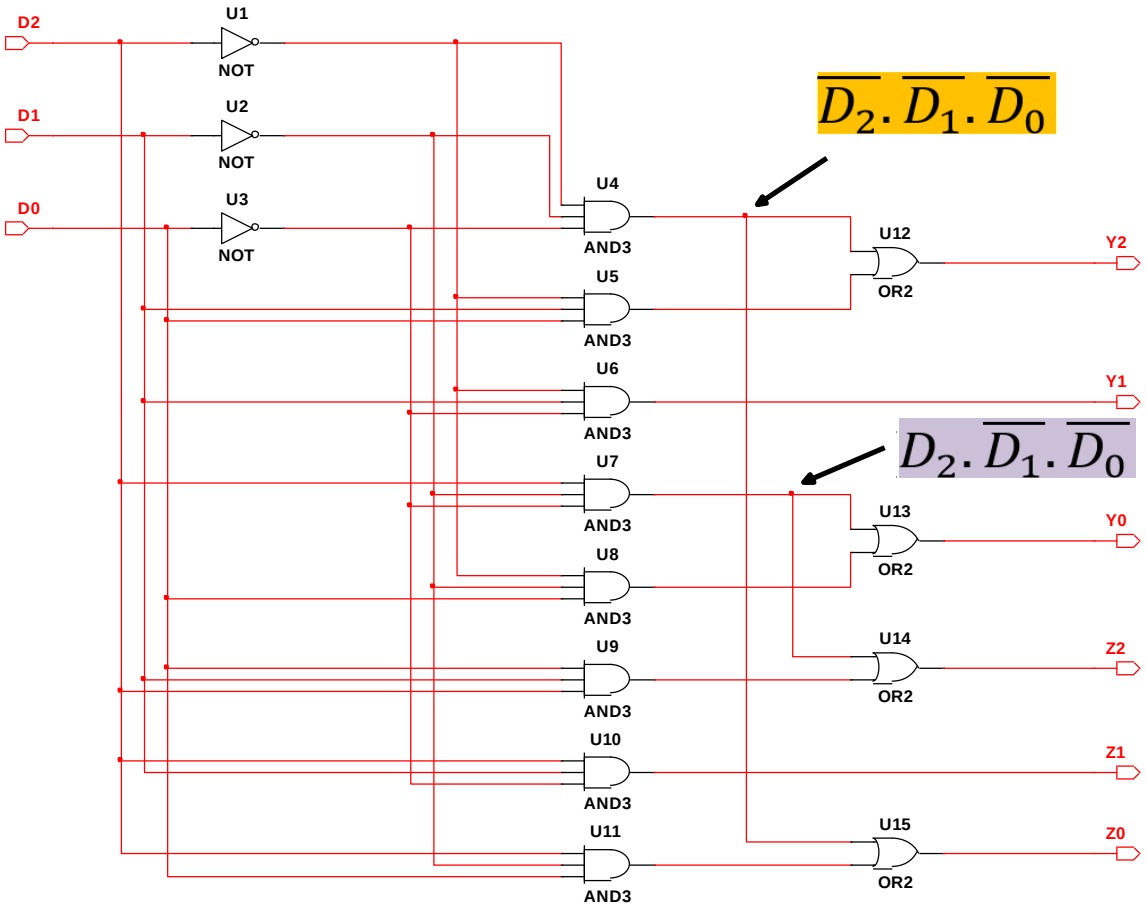

Figure B.2-1 3-bit IOPPM encoder combinational logic circuit

B.3 3-bit IOPPM Encoder Test Circuit and Test Data

The test circuit used to verify that both IOPPM+ and IOPPM- encoders operated correctly is shown in Figure B.3-2. The circuit was constructed and tested using NI Multisim 14.0.

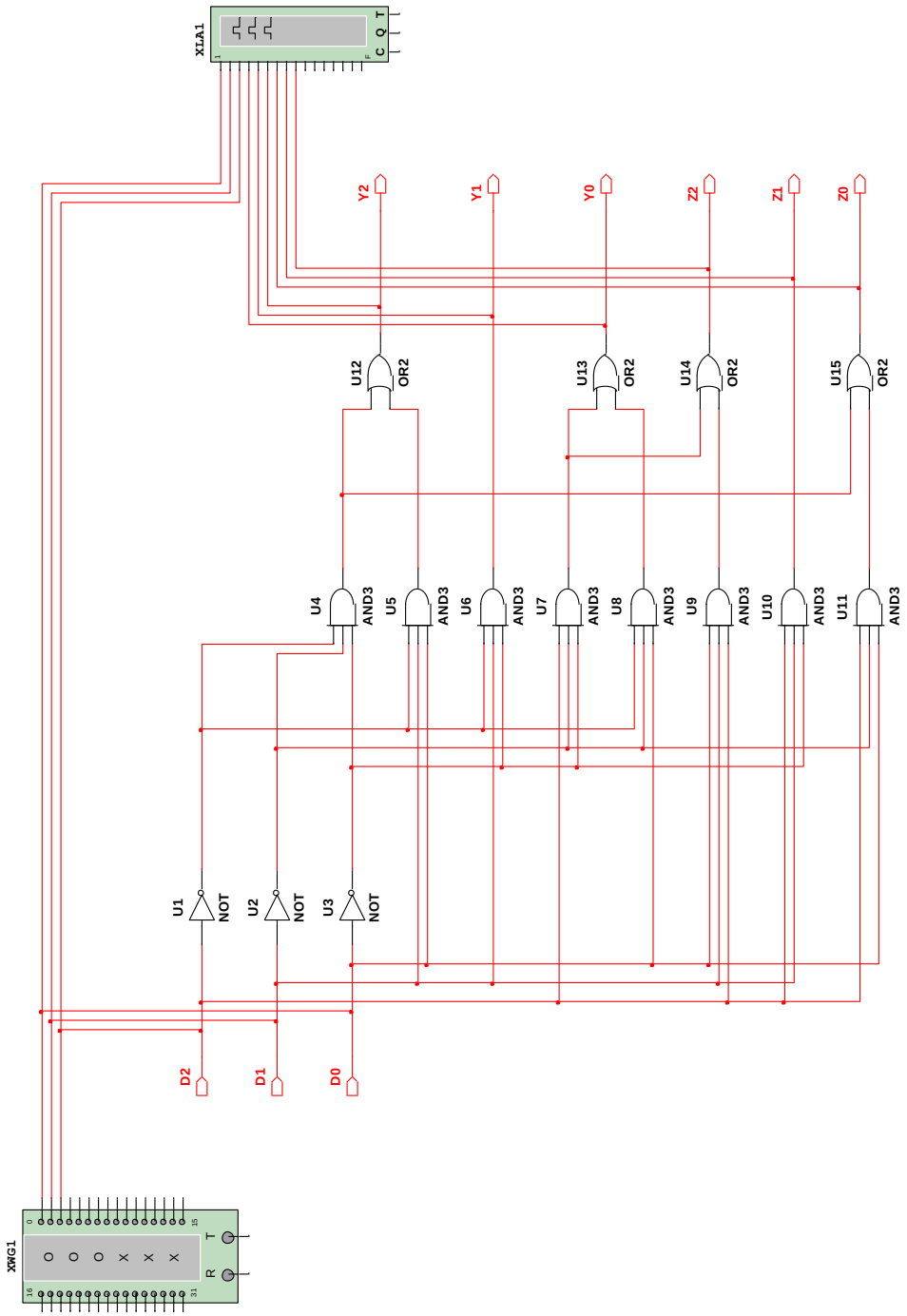

Figure B.3-2 3-bit IOPPM encoder test circuit

The input stimulus to the encoder was provided by a Word Generator (XWG1) and the output of the encoder was monitored by a Logic Analyser (XLA1). Figure B.3-3 shows the Word Generator test vectors applied to the circuit, which consisted of a cycled count from 0 to 7 to simulate the input min terms. A clock frequency of 6 MHz was used to simulate the MPEG TS parallel clock frequency used on the STB platforms.

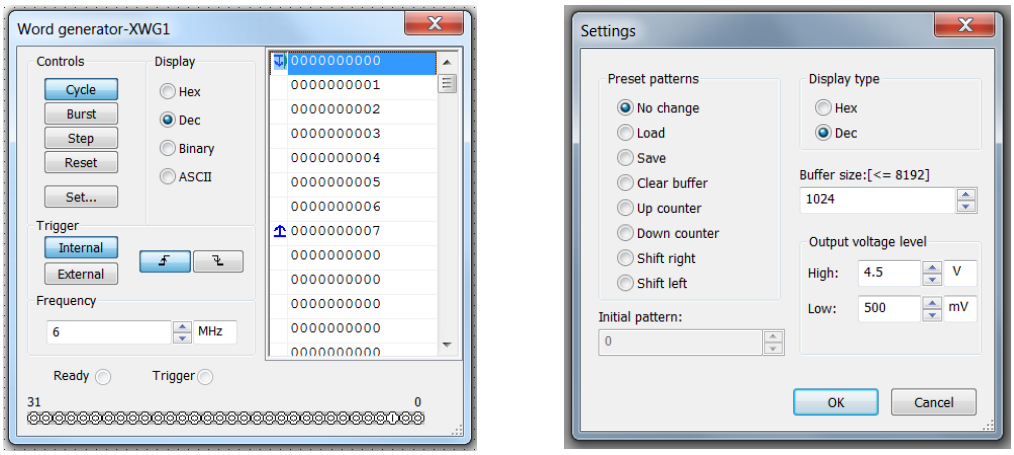

Figure B.3-3 NI Multisim Word Generator IOPPM encoder test settings

Figure B.3-4 shows the Logic Analyser configured to trigger on the rising-edge of an internally generated 6 MHz reference clock.

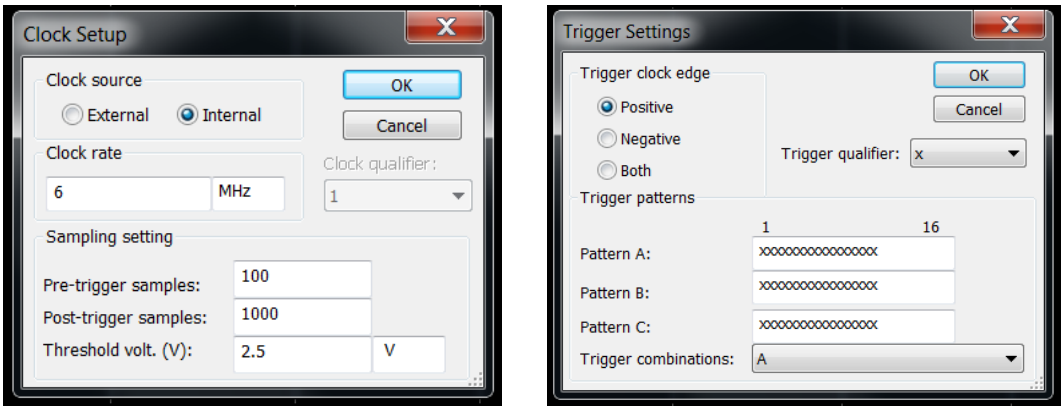

Figure B.3-4 NI Multisim Logic Analyser IOPPM encoder test settings

The simulation results for the 3-bit IOPPM encoder are shown in Figure B.3-5. The input and output ports of the decoder are labelled on the left-hand-side of the timing traces.

Annotation for the min terms is shown at the top of the trace on the D_0 waveform. The min term applies to the inputs D_0, D_1, and D_2.

Comparing the min term values D_0, D_1, and D_2 and outputs traces D_0, D_1, and D_2 with the truth table for the 3-bit IOPPM encoder, shown in Table B.1-2, agreement between the design and simulated results is demonstrated.

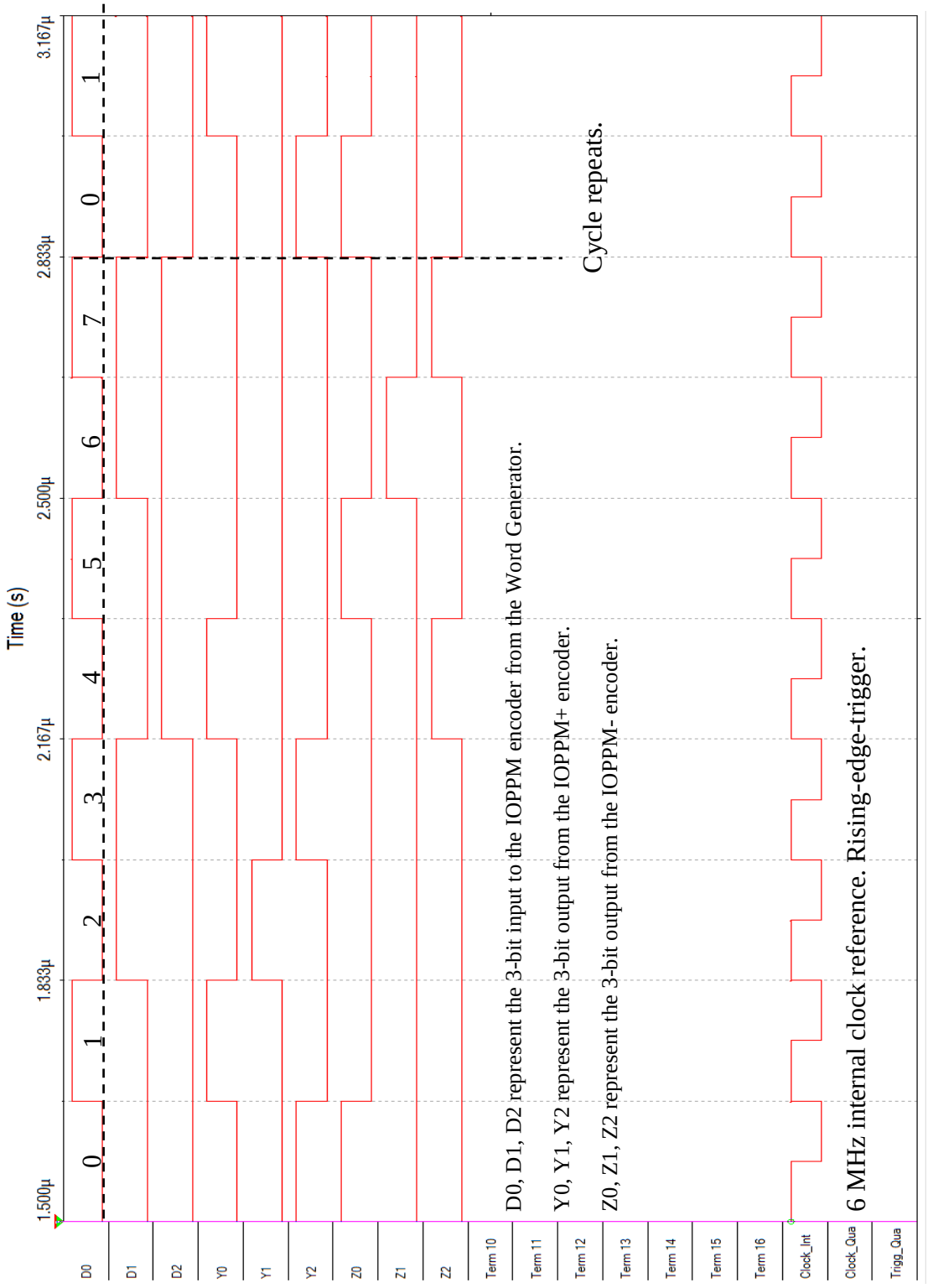

Figure B.3-5 IOPPM encoder test simulation timing traces

B.4 MPEG TS to IOPPM Encoding System

Figure B.4-6 shows the IOPPM encoder required to encode 9-bits of the MPEG TS. Three, 3-bit IOPPM encoder blocks are needed to generate the 2 × 9-bit IOPPM output streams.

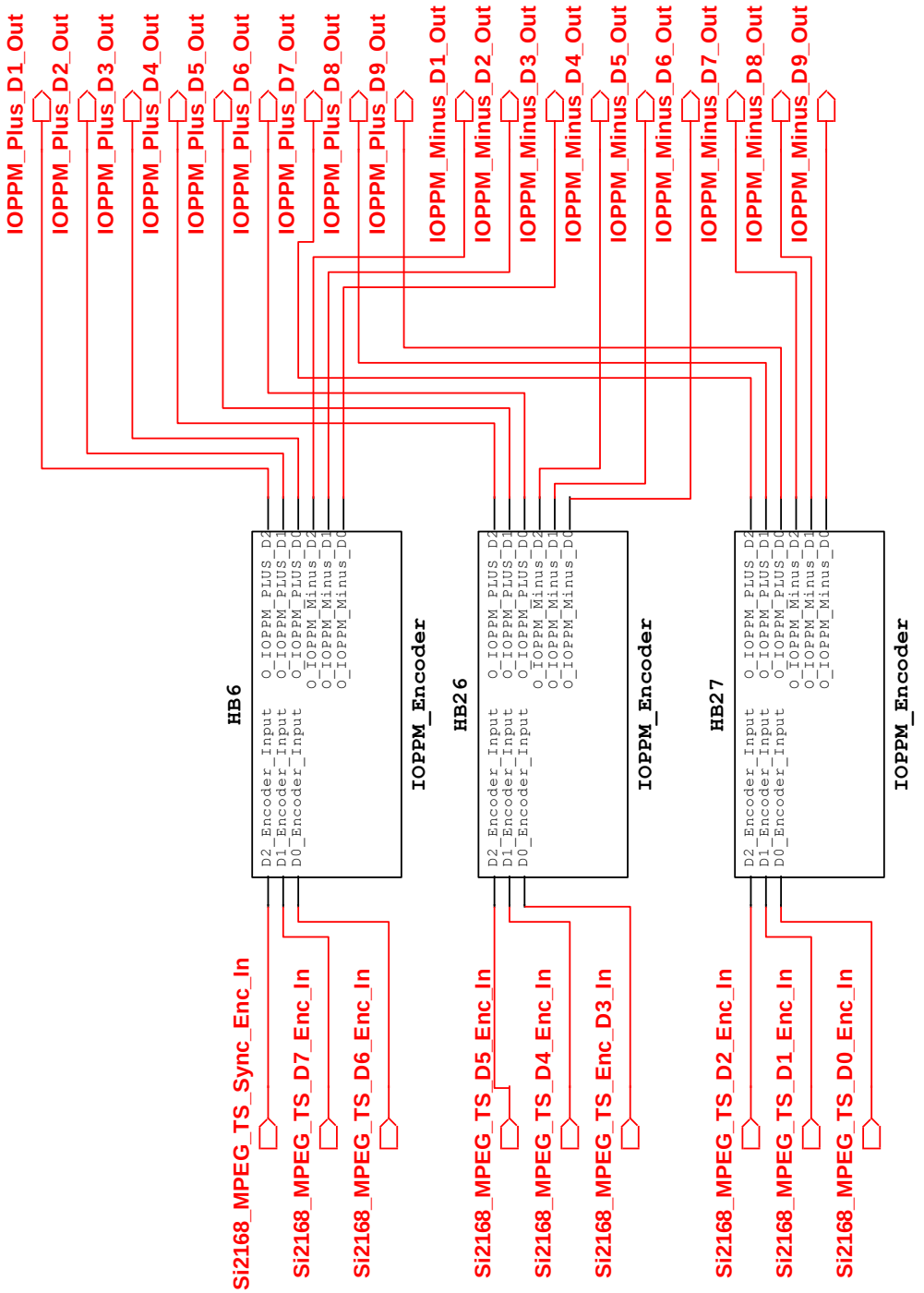

Figure B.4-6 9-bits of MPEG TS mapped to 3 × 3-bit IOPPM encoders

B.5 3-bit IOPPM Decoder Derivation

The IOPPM decoder was also designed using the combinational logic, sum of products truth table derivation and Karnaugh mapping simplification techniques.

The first step of the decoder design process was to derive a sum of products truth table based on the 3-bit encoder truth table of Table B.1-2. This was achieved by reversing the table, so that input bits in encoder truth table became output bits in the decoder truth table, similarly, output bits in encoder became input bits in the decoder. Table B.5-10 shows the resulting truth table for the decoder, which contains 8 valid combinations, comprised of 6 inputs bits and 3 outputs bits.

	Input IOPPM+			**Input IOPPM-**			**Output Data**		
Min Term	Y_2	Y_1	Y_0	Z_2	Z_1	Z_0	D_2	D_1	D_0
33	1	0	0	0	0	1	0	0	0
8	0	0	1	0	0	0	0	0	1
16	0	1	0	0	0	0	0	1	0
32	1	0	0	0	0	0	0	1	1
12	0	0	1	1	0	0	1	0	0
1	0	0	0	0	0	1	1	0	1
2	0	0	0	0	1	0	1	1	0
4	0	0	0	1	0	0	1	1	1

Table B.5-10 Valid IOPPM decoder inputs and outputs (3 bit decoding)

These 8 valid inputs are a subset of a larger set of input combinations, which also contains invalid inputs for the decoder. The total number of input combinations to the decoder is 2^6, or 64 combinations; 8 valid inputs and 56 invalid inputs. Table B.5-11 shows the complete truth table for the decoder containing all 64 combinations. Valid

decoder inputs and outputs are highlighted in green. Invalid inputs are set to give outputs with all zeroes.

	Input IOPPM+			Input IOPPM-			Output Data		
Min Term	Y_2	Y_1	Y_0	Z_2	Z_1	Z_0	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	1	0	1
2	0	0	0	0	1	0	1	1	0
3	0	0	0	0	1	1	0	0	0
4	0	0	0	1	0	0	1	1	1
5	0	0	0	1	0	1	0	0	0
6	0	0	0	1	1	0	0	0	0
7	0	0	0	1	1	1	0	0	0
8	0	0	1	0	0	0	0	0	1
9	0	0	1	0	0	1	0	0	0
10	0	0	1	0	1	0	0	0	0
11	0	0	1	0	1	1	0	0	0
12	0	0	1	1	0	0	1	0	0
13	0	0	1	1	0	1	0	0	0
14	0	0	1	1	1	0	0	0	0
15	0	0	1	1	1	1	0	0	0
16	0	1	0	0	0	0	0	1	0
17	0	1	0	0	0	1	0	0	0
18	0	1	0	0	1	0	0	0	0
19	0	1	0	0	1	1	0	0	0
20	0	1	0	1	0	0	0	0	0
21	0	1	0	1	0	1	0	0	0
22	0	1	0	1	1	0	0	0	0
23	0	1	0	1	1	1	0	0	0
24	0	1	1	0	0	0	0	0	0
25	0	1	1	0	0	1	0	0	0
26	0	1	1	0	1	0	0	0	0
27	0	1	1	0	1	1	0	0	0
28	0	1	1	1	0	0	0	0	0
29	0	1	1	1	0	1	0	0	0
30	0	1	1	1	1	0	0	0	0
31	0	1	1	1	1	1	0	0	0
32	1	0	0	0	0	0	0	1	1
33	1	0	0	0	0	1	0	0	0
34	1	0	0	0	1	0	0	0	0
35	1	0	0	0	1	1	0	0	0
36	1	0	0	1	0	0	0	0	0
37	1	0	0	1	0	1	0	0	0
38	1	0	0	1	1	0	0	0	0
39	1	0	0	1	1	1	0	0	0
40	1	0	1	0	0	0	0	0	0
41	1	0	1	0	0	1	0	0	0
42	1	0	1	0	1	0	0	0	0
43	1	0	1	0	1	1	0	0	0
44	1	0	1	1	0	0	0	0	0
45	1	0	1	1	0	1	0	0	0
46	1	0	1	1	1	0	0	0	0
47	1	0	1	1	1	1	0	0	0
48	1	1	0	0	0	0	0	0	0
49	1	1	0	0	0	1	0	0	0
50	1	1	0	0	1	0	0	0	0
51	1	1	0	0	1	1	0	0	0
52	1	1	0	1	0	0	0	0	0
53	1	1	0	1	0	1	0	0	0
54	1	1	0	1	1	0	0	0	0
55	1	1	0	1	1	1	0	0	0
56	1	1	1	0	0	0	0	0	0
57	1	1	1	0	0	1	0	0	0
58	1	1	1	0	1	0	0	0	0
59	1	1	1	0	1	1	0	0	0
60	1	1	1	1	0	0	0	0	0
61	1	1	1	1	0	1	0	0	0
62	1	1	1	1	1	0	0	0	0
63	1	1	1	1	1	1	0	0	0

Table B.5-11 All IOPPM decoder input and output combinations (3 bit decoding)

The second step was to generate Boolean expressions for the sum of products min terms shown in Table B.5-10. The resulting expressions for the IOPPM decoder outputs were obtained.

$$D_0(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.Z_0 + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.Z_2.\overline{Z_1}.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.Y_0.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} + \\ Y_2.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} \end{pmatrix} \qquad \text{Equation B.5-7}$$

$$D_1(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.Z_1.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.Z_2.\overline{Z_1}.\overline{Z_0} + \\ \overline{Y_2}.Y_1.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} + \\ Y_2.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} \end{pmatrix} \qquad \text{Equation B.5-8}$$

$$D_2(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.Z_0 + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.Z_1.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.Z_2.\overline{Z_1}.\overline{Z_0} + \\ Y_2.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.Z_0 \end{pmatrix} \qquad \text{Equation B.5-9}$$

The third step was to apply Karnaugh mapping techniques to the min term expressions to determine whether they were in their minimised form. In this case 3×3 variable Karnaugh maps were used to perform simplification. Note that the Karnaugh maps in this case have a boundary line, shown in red, indicating that groupings across the boundary are not permitted. This is due to the fact that crossing the boundary results in increments greater than 1 bit i.e. non-gray coded.

The Karnaugh map for IOPPM decoder D_0 output is shown in Table B.5-12. This was derived using Equation B.5-7. Four independent terms are highlighted in the map, with no groupings present to allow further simplification, Equation B.5-7 was deemed optimal.

$$D_0(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.Z_0 + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.Z_2.\overline{Z_1}.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.Y_0.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} + \\ Y_2.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} \end{pmatrix}$$

D_0	$Z_2.Z_1.Z_0$							
$Y_2.Y_1.Y_0$	**000**	**001**	**011**	**010**	**100**	**101**	**111**	**110**
000	0	1	0	0	1	0	0	0
001	1	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	0	0	0	0	0	0	0	0
100	1	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	0	0

Table B.5-12 Karnaugh map IOPPM decoder D_0 output

The Karnaugh map for IOPPM decoder D_1 output is shown in Table B.5-13. This was derived using Equation B.5-8. Four independent terms are highlighted in the map, with no groupings present to allow further simplification, Equation B.5-8 was deemed optimal.

$$D_1(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.Z_1.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.Z_2.\overline{Z_1}.\overline{Z_0} + \\ \overline{Y_2}.Y_1.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} + \\ Y_2.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} \end{pmatrix}$$

D_1	$Z_2.Z_1.Z_0$							
$Y_2.Y_1.Y_0$	**000**	**001**	**011**	**010**	**100**	**101**	**111**	**110**
000	0	0	0	1	1	0	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	1	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	0	0

Table B.5-13 Karnaugh map IOPPM decoder D_1 output

The Karnaugh map for IOPPM decoder D_2 output is shown in Table B.5-14. This was derived using Equation B.5-9. Four independent terms are highlighted in the map, with one grouping present, allowing simplification. The simplified expression for $D_2$is shown in Equation B.5-10.

$$D_2(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.Z_0 + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.Z_1.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.Z_2.\overline{Z_1}.\overline{Z_0} + \\ Y_2.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.Z_0 \end{pmatrix}$$

D_2	$Z_2.Z_1.Z_0$							
$Y_2.Y_1.Y_0$	**000**	**001**	**011**	**010**	**100**	**101**	**111**	**110**
000	0	1	0	1	1	0	0	0
001	0	0	0	0	1	0	0	0
011	0	0	0	0	0	0	0	0
010	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	0	0

Table B.5-14 Karnaugh map IOPPM decoder D_2 output

$$D_2(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.Z_0 + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.Z_1.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.Z_2.\overline{Z_1}.\overline{Z_0} \end{pmatrix}$$ Equation B.5-10

The expressions for the IOPPM decoder, specifically, Equation B.5-7, and Equation B.5-8, were checked for duplicate terms, and three were found, as shown in Table B.5-15.

IOPPM Decoder Expressions

$D_0(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.Z_2.\overline{Z_1}.Z_0 + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.Z_2.\overline{Z_1}.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.Y_0.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} + \\ Y_2.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} \end{pmatrix}$
$D_1(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.Z_1.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.Z_2.\overline{Z_1}.\overline{Z_0} + \\ \overline{Y_2}.Y_1.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} + \\ Y_2.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.\overline{Z_0} \end{pmatrix}$
$D_2(Y_2, Y_1, Y_0, Z_2, Z_1, Z_0) = \sum \begin{pmatrix} \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.\overline{Z_1}.Z_0 + \\ \overline{Y_2}.\overline{Y_1}.\overline{Y_0}.\overline{Z_2}.Z_1.\overline{Z_0} + \\ \overline{Y_2}.\overline{Y_1}.Z_2.\overline{Z_1}.\overline{Z_0} \end{pmatrix}$

Table B.5-15 IOPPM decoder expressions with duplicate terms highlighted

B.6 3-bit IOPPM Decoder Synthesis

The duplicate terms shown in Table B.5-15 were eliminated in the synthesised circuit, shown in Figure B.6-7, by using cross-wiring to enable the reuse of the terms. Only 6 NOT gates were needed to implement the negated terms for Y_0, Y_1, Y_2, Z_0, Z_1, and Z_2.

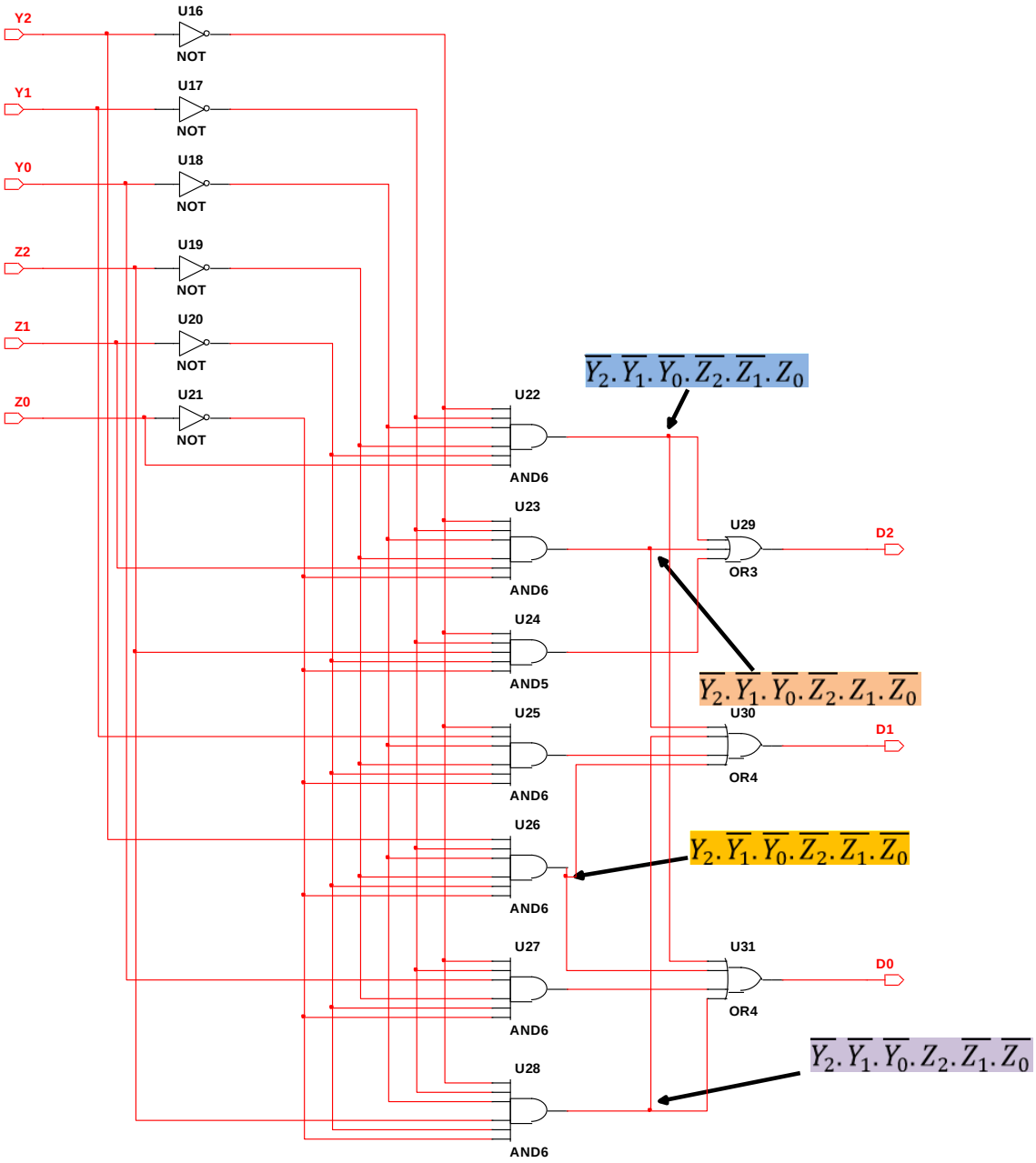

Figure B.6-7 IOPPM decoder logic circuit

B.7 3-bit IOPPM Decoder Test Circuit and Test Data

The test circuit used to verify the correct operation of the IOPPM decoder circuit is shown in Figure B.7-9. The Word Generator (XWG1) instrument was connected to inputs Y_0, Y_1, Y_2, Z_0, Z_1, and Z_2 of the decoder, and the Logic Analyser (XLA1) was connected to the same inputs, as well as D_0, D_1, and D_2 outputs of the decoder. This arrangement enabled the simultaneous monitoring of the input and output states of the decoder.

The min terms for the valid input and output of the IOPPM decoder, shown in Table B.5-10, were used to generate test vectors. These vectors were applied to the input of the IOPPM decoder circuit to verify correct operation.

Figure B.7-8 shows the test vector settings for the Word Generator. The valid min terms 33, 8, 16, 32, 12, 1, 2 and 4 were cycled to stimulate the input of the circuit. Again, a clock frequency of 6 MHz was used to simulate the MPEG TS parallel clock frequency used on the STB platforms.

Note that all the other settings for the Word Generator and Logic Analyser were identical to the settings used in the IOPPM encoder testing.

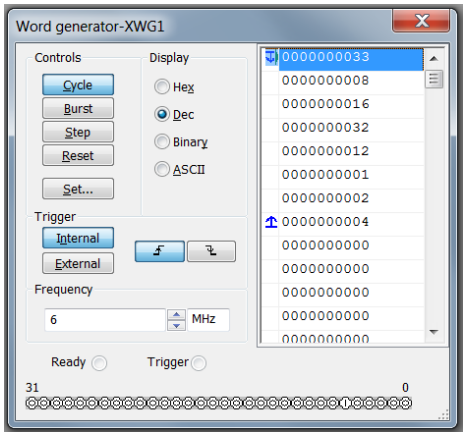

Figure B.7-8 NI Multisim Word Generator IOPPM decoder test settings

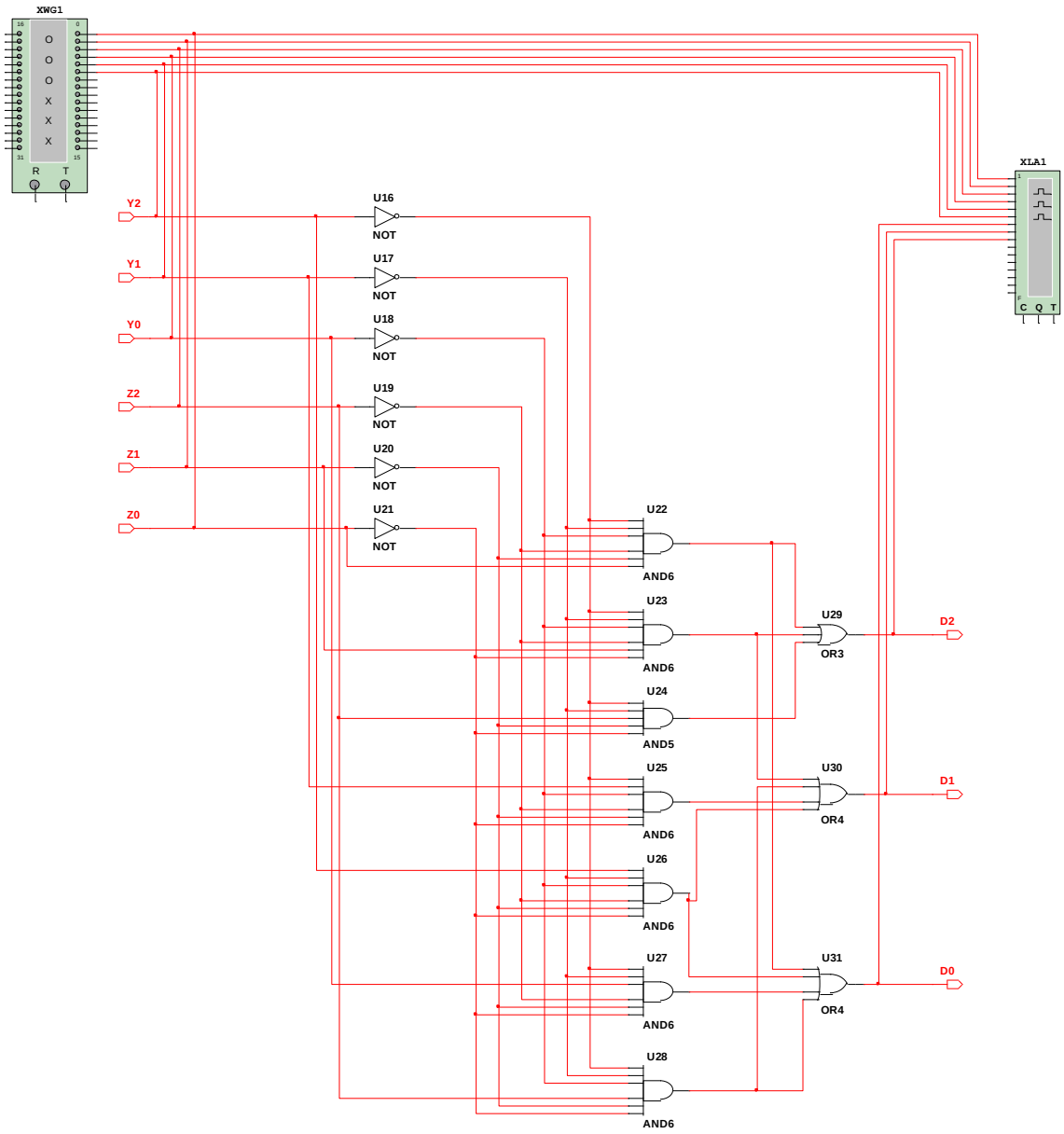

Figure B.7-9 IOPPM decoder test circuit

The simulation results for the IOPPM decoder are shown in Figure B.7-10. The input and output ports of the decoder are labelled on the left-hand-side of the timing traces.

Annotation for the min terms is shown at the top of the trace on the Z_0 waveform. The min term applies to the inputs Y_0, Y_1, Y_2, Z_0, Z_1, and Z_2

Comparing the min term values for Y_0, Y_1, Y_2, Z_0, Z_1, and Z_2 and outputs traces D_0, D_1, and $D_2$with the truth table for the IOPPM decoder, shown in Table B.5-10, agreement between the design and simulated results is demonstrated.

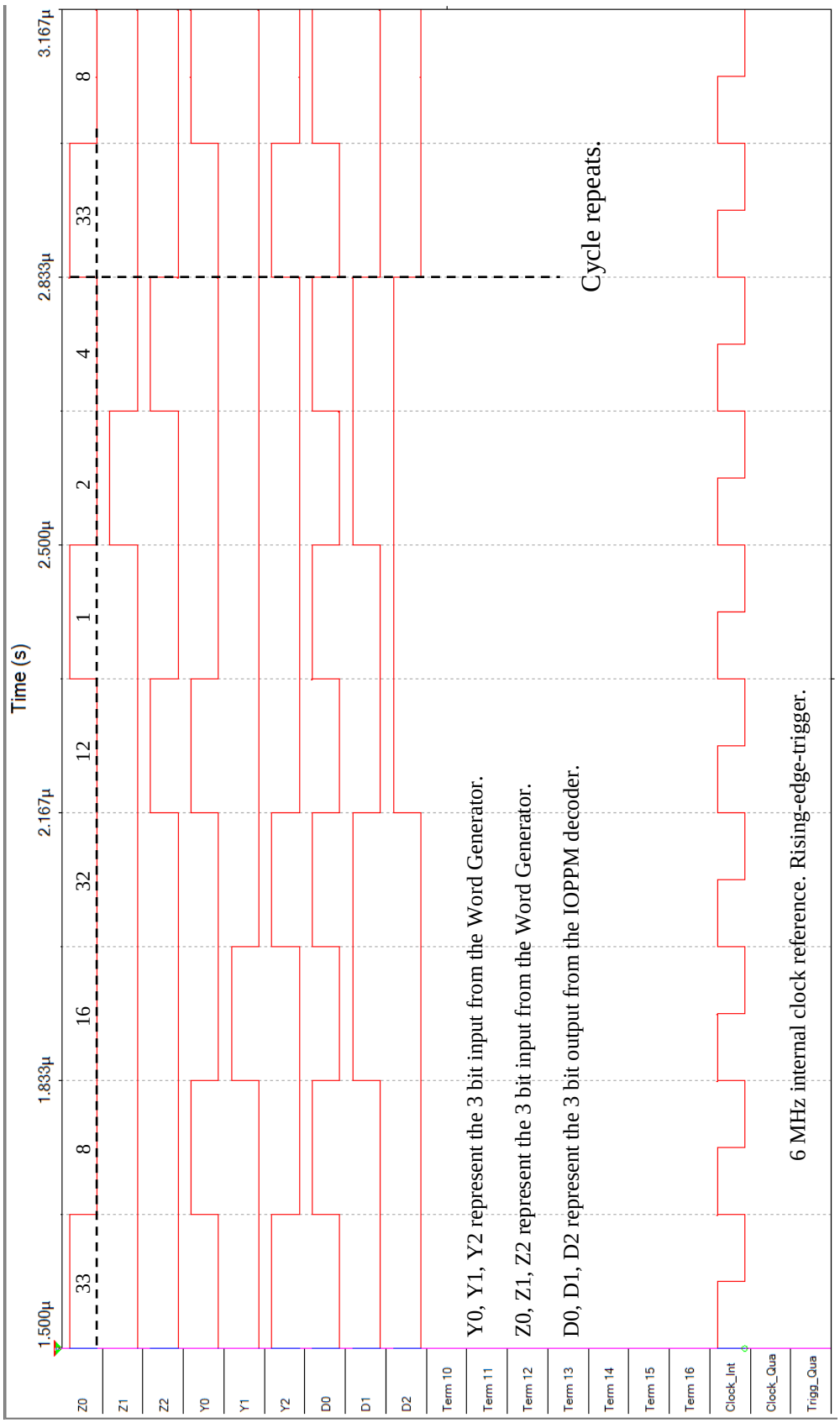

Figure B.7-10 IOPPM decoder test simulation timing traces (valid inputs)

In addition to the testing of the valid min terms, the invalid min terms were also used to stimulate the decoder to confirm that only logic zeros were output for these input stimuli. The Word Generator was set to cycle through all the invalid min terms, shown in Table B.5-11, with valid min terms 33, 8, 16, 32, 12, 1, 2 and 4 excluded. Figure B.7-11 shows the results of this simulation and it was demonstrated that outputs D0, D1 and D2 were zero, as expected. Note that the clocks/div setting on this trace was set to 13, enabling all the invalid conditions to be displayed.

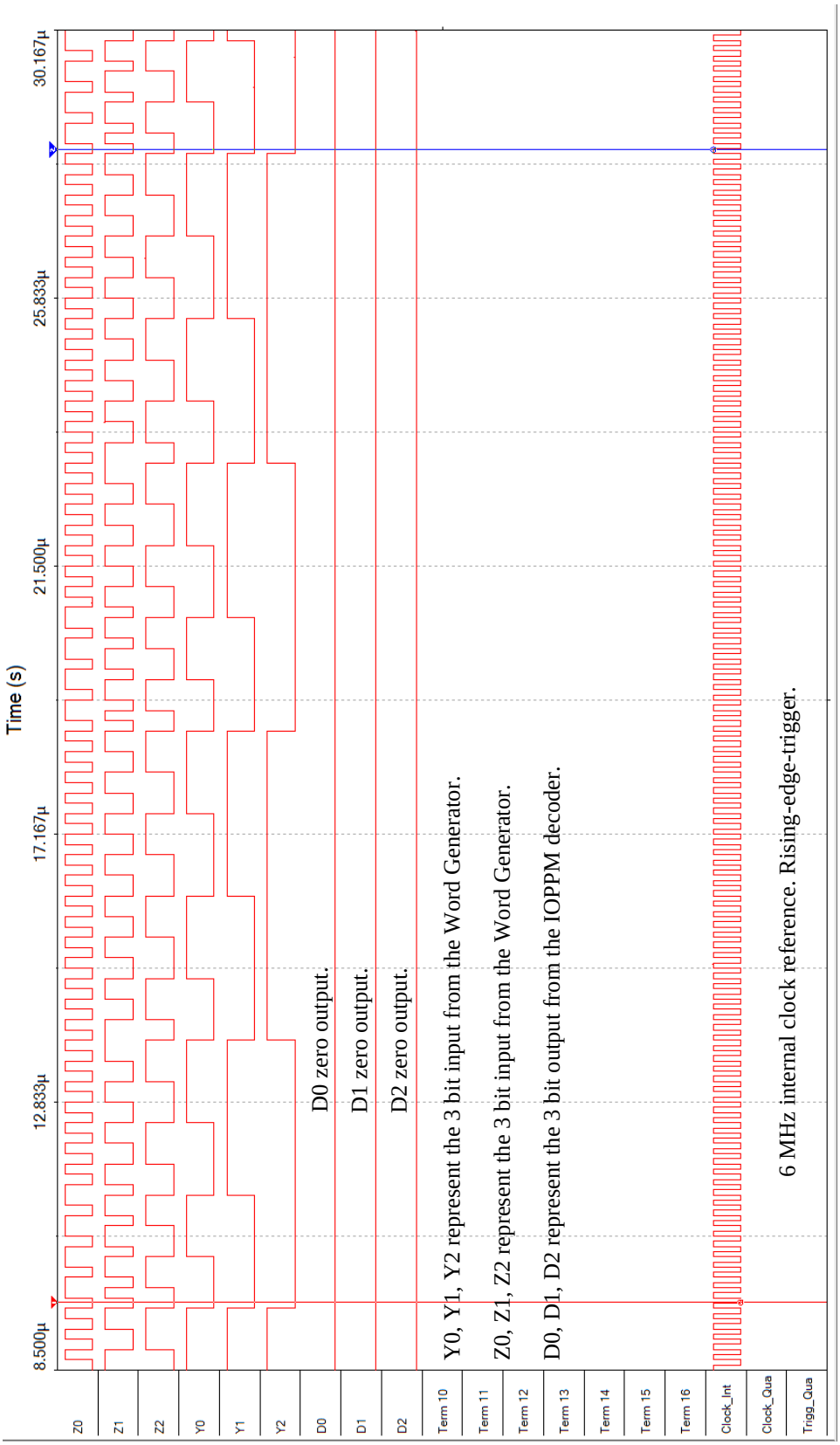

Figure B.7-11 IOPPM decoder test simulation timing traces (invalid inputs)

B.8 MPEG TS to IOPPM Decoding System

Figure B.4-6 shows the IOPPM decoder required to decode 2× 9-bit IOPPM streams to 9-bits of MPEG TS. Three, 6-bit to 3-bit IOPPM decoder blocks are needed to generate 9-bits of MPEG TS.

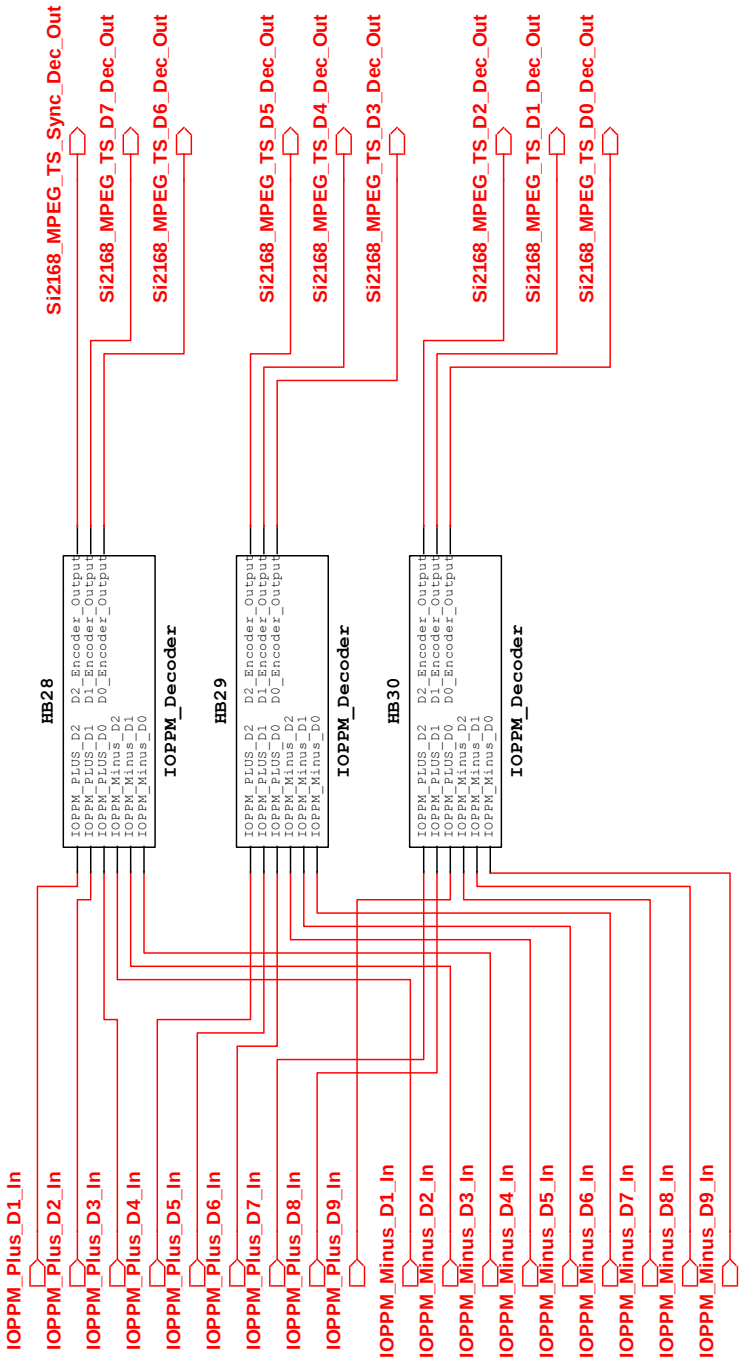

Figure B.8-12 3 × 6-bit to 3-bit IOPPM decoders to generate 9-bits of MPEG TS

B.9 IOPPM Encoder and Decoder End-to-End Testing

Using the IOPPM encoder and decoder circuits synthesised in previous sections, it was possible to perform end-to-end testing. This involved connecting the output of the 3-bit encoder to the input of the 6-bit decoder and stimulating the encoder input with the 8 valid test vectors shown in Table B.9-16.

	IOPPM Encoder Input Data			**IOPPM Decoder Output Data**		
Min Term	D_2	D_1	D_0	D_2	D_1	D_0
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	0	0	1	0
3	0	1	1	0	1	1
4	1	0	0	1	0	0
5	1	0	1	1	0	1
6	1	1	0	1	1	0
7	1	1	1	1	1	1

Table B.9-16 IOPPM encoder input and decoder output valid test vectors

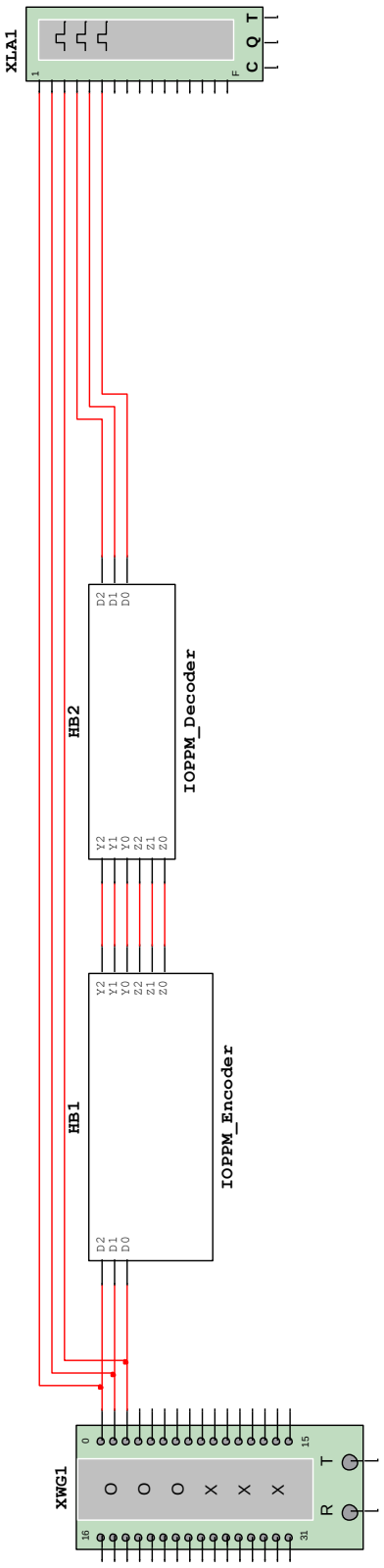

Figure B.9-13 IOPPM encoder and decoder end-to-end test circuit

Appendix C Silicon Labs Inc NDA and Reprint Permission Documents

C.1 Silicon Labs Inc Non-Disclosure Agreement (N-14-)

CONFIDENTIALITY AGREEMENT	NDA Number: N-14-
	Effective Date: 1/15/2014

Silicon Laboratories Inc., a Delaware corporation ("Silicon Labs"), and **Tim Amsdon**, having an address listed below, and **Dr. Martin Sibley**, having an address listed below; each a "party" or collectively, the "parties", agree as follows:

1. Silicon Labs desires to confidentially provide Tim Amsdon, as a full-time student, access to a Silicon Labs TV tuner evaluation board (EVB) for specific use in a graduate project that is an optical free-space transmitter/receiver link ("Purpose"). Tim Amsdon's faculty advisor and supervisor, Dr. Martin Sibley, will be loaned the EVB which is to be used only to generate a live off-air DVB-T/T2 MPEG parallel transport stream that will be fed to an optical encoder of the research project. Tim Amsdon and Dr. Martin Sibley will ensure they alone have access to documentation, hardware and software associated with the EVB provided by Silicon Labs. The terms of this Agreement constitute Confidential Information. Tim Amsdon may use Silicon Labs tuner and demodulator part numbers and the Silicon Labs trademark in materials for conferences and in a graduate thesis. Use of the EVB in public demonstrations at conference and the University of Huddersfield is permitted, but the EVB will be in a sealed enclosure and no information regarding Silicon Labs products and the EVB may be disclosed beyond the scope of publicly available information. The EVB will kept in a secured and locked room and will otherwise not be left unattended by Tim Amsdon.

2. This Agreement terminates on 5/30/2015 (or, if earlier, upon written notice of termination), provided that, as to each item of Confidential Information, the parties' rights and obligations under this Agreement shall continue for a period of three (3) years from the date of initial disclosure, except that no right to use any of the other party's Confidential Information shall survive termination of this Agreement.

3. "Confidential Information" shall mean all information which is provided by either party to the other party in written, electronic, or other tangible form and which is marked with a conspicuous written legend as being proprietary or confidential or, if provided orally or visually, is identified as confidential at the time of disclosure and confirmed as confidential in writing to the receiving party within thirty (30) days thereafter. Any information disclosed orally or visually and later confirmed in writing, consistent with the foregoing sentence, shall be treated as confidential, in accordance with this Agreement, from the date of first disclosure. Confidential Information of Silicon Labs specifically includes business and technical information relating to tuner and demodulator products or projects of Silicon Labs, related technology, data sheets, block diagrams, specifications, application notes, test results, process change notices, schematics, layouts, software, roadmaps, pricing information, presentation materials, and the EVB physical specimens and samples.

4. Tim Amsdon and Dr. Martin Sibley shall protect Confidential Information received from Silicon Labs by using the same degree of care as it uses to protect its own Confidential Information of like nature, but no less than a reasonable degree of care, to prevent the unauthorized disclosure to any third party. Tim Amsdon and Dr. Martin Sibley each agree to promptly notify the other party in writing of any misuse or misappropriation of received Confidential Information that may come to its attention.

5. Tim Amsdon and Dr. Martin Sibley each agree to use the Silicon Labs Confidential Information only for the Purpose, and each agrees not to use such Confidential Information for any other reason.

6. Information shall not be deemed to be Confidential Information if: (a) the information is or becomes generally available to the public, except as the result of unauthorized disclosure by the receiving party; or (b) the disclosing party agrees in writing that it can be disclosed by the receiving party on a non-confidential basis; or (c) the information is known to the receiving party, on an unrestricted basis before its receipt; or (d), the receiving party, without use of or reference to Confidential Information, independently develops the information; or (e) the receiving party lawfully receives it from a third party, that is not under a duty of confidentiality to the disclosing party.

7. Each of Tim Amsdon and Dr. Martin Sibley shall be entitled to disclose the Silicon Labs Confidential Information to the extent required by law or legal process, provided that the receiving party gives prompt written notice to the disclosing party so that it may oppose such process and follows any orders that the disclosing party obtains from a court or administrative agency concerning the protection surrounding such disclosure.

8. Upon the expiration or any termination of this Agreement and upon written request of Silicon Labs, each of Tim Amsdon and Dr. Martin Sibley shall return all of the Silicon Labs Confidential Information, including the EVB, along with all copies and/or derivatives made.

9. Each party shall have the right to refuse to receive any information under this Agreement and nothing herein shall obligate either party to disclose any particular information to the other party.

10. Nothing in this Agreement shall be construed to grant to either party any right or license under any intellectual property right of the other party, including patent, copyright, mask work right, or trademark. Confidential Information is provided "as is." **NO REPRESENTATIONS OR WARRANTIES ARE MADE OR IMPLIED REGARDING THE ACCURACY, MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR A PARTICULAR PURPOSE OF CONFIDENTIAL INFORMATION.** A disclosing party shall have no liability or responsibility for any expense, losses, damages, or action incurred or undertaken by the other as a result of the receipt of Confidential Information.

11. This Agreement does not represent or imply any agreement or commitment to enter into any further business relationship, or to expend funds or other resources in the development of products or services. No obligation or commitment relating to the Purpose shall arise between the parties except as may be set forth in a written agreement duly executed by authorized representatives of each party. Subject to the obligations of this Agreement, neither party is

Page 1 of 2

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Address: 400 W. Cesar Chavez Austin, TX 78701, USA	**Address:** School of Computing & Engineering (Research Office: CE2/14) University of Huddersfield Queensgate, Huddersfield HD1 3DH, United Kingdom
Signature:	**Signature:**
Printed Name: James Stansberry	
Title: Vice President, General Manager, Broadcast	**Capacity:** Graduate Student
Date:	**Date:** 01/22/2014.

Dr. Martin Sibley
Address: School of Computing & Engineering (Research Office: CE2/14) University of Huddersfield Queensgate, Huddersfield HD1 3DH, United Kingdom
Signature:
Capacity: Faculty Advisor

C.2 Silicon Labs Inc Reprint Permission

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August 28, 2019

Mr. Tim Amsdon BEng(Hons), CEng, FIET, SMIEEE, FHEA
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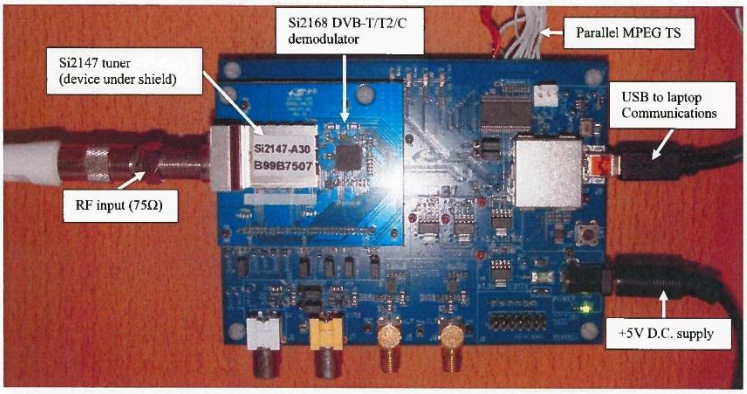
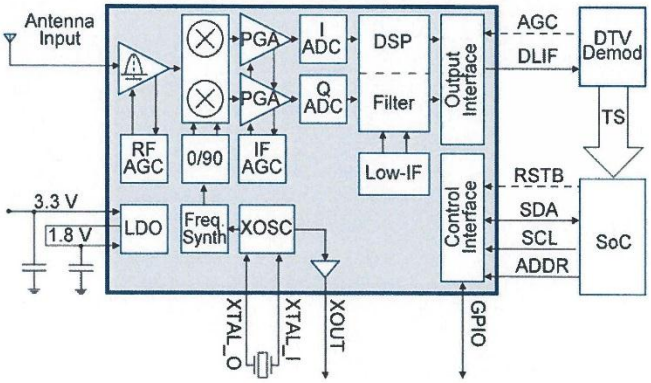
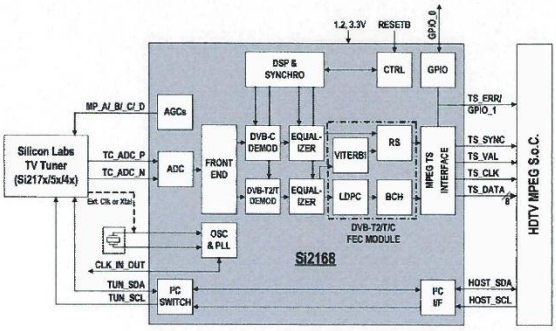


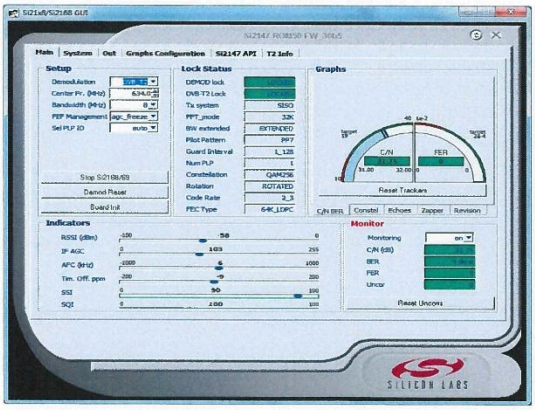
Silicon Labs EVB



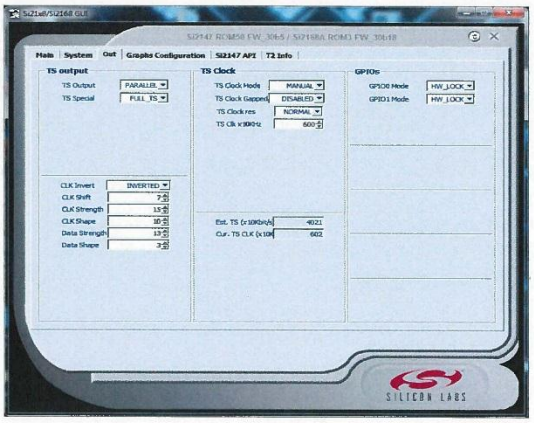
Silicon Labs Si2147 DVB low-IF tuner block diagram (Silicon Labs Inc.)



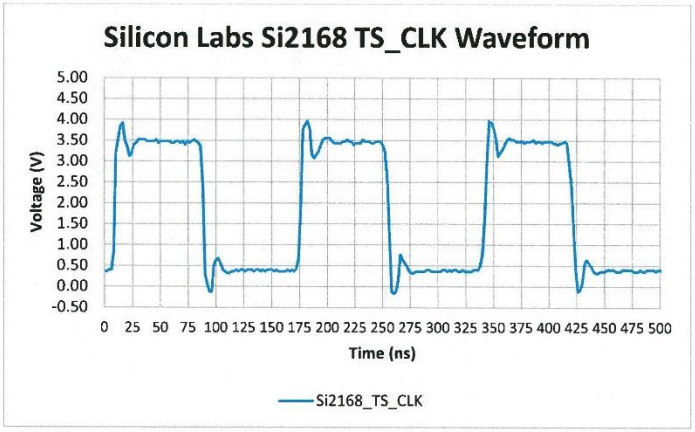
Silicon Labs Si2168 DVB-T/T2/C digital demodulator block diagram (Silicon Labs Inc.)



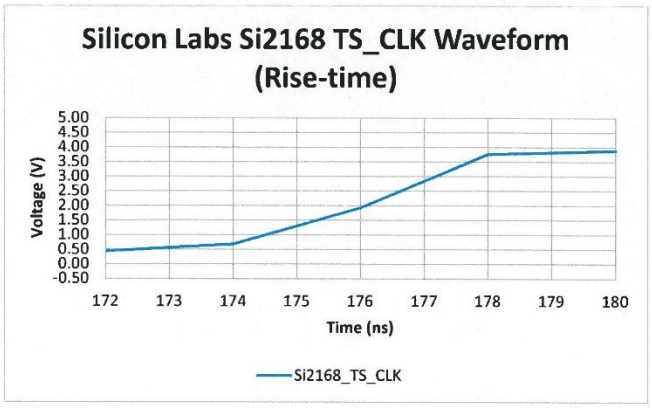
Silicon Labs Si2147/Si2168 software settings (main tab) (Silicon Labs Inc.)



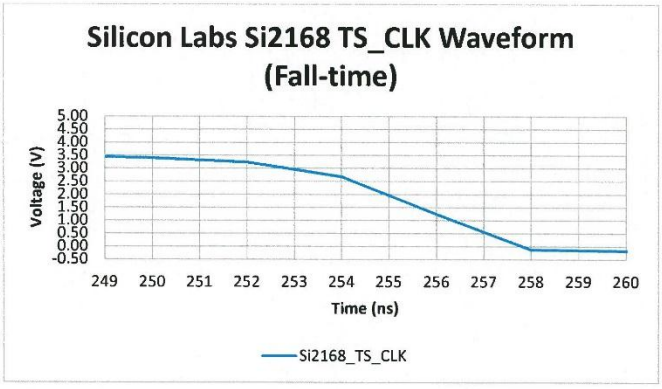
Silicon Labs Si2147/Si2168 software settings (out tab) (Silicon Labs Inc.)



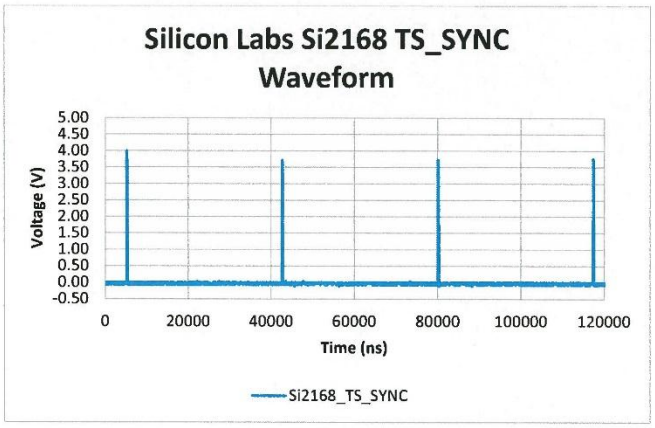
Si2168 MPEG TS CLK (6.008 MHz, 50% duty cycle)



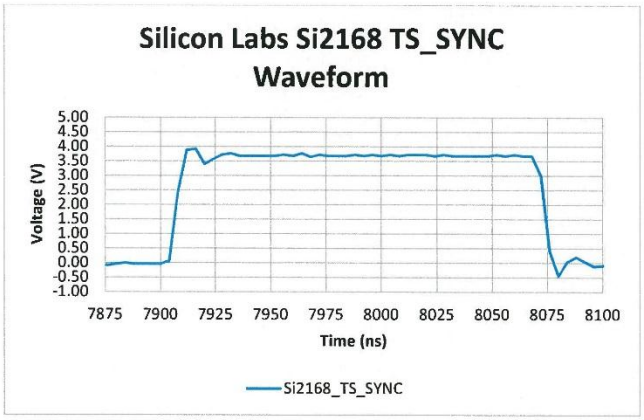
Si2168 MPEG TS CLK (Rise-time)



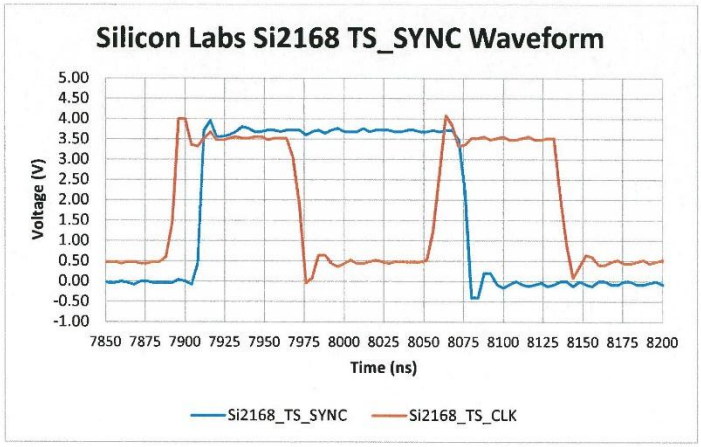
Si2168 MPEG TS CLK (Fall-time)



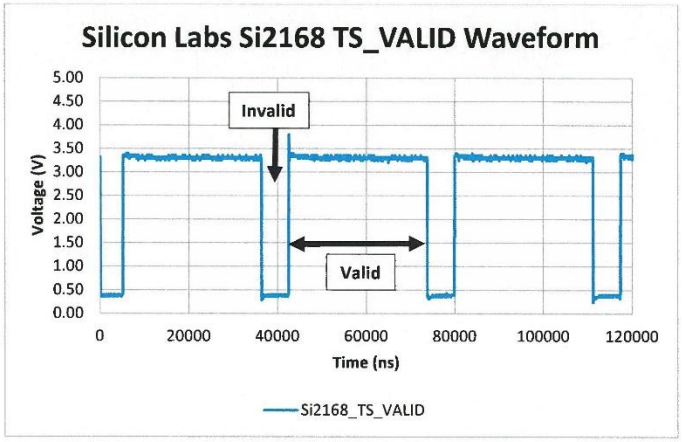
Si2168 MPEG TS SYNC



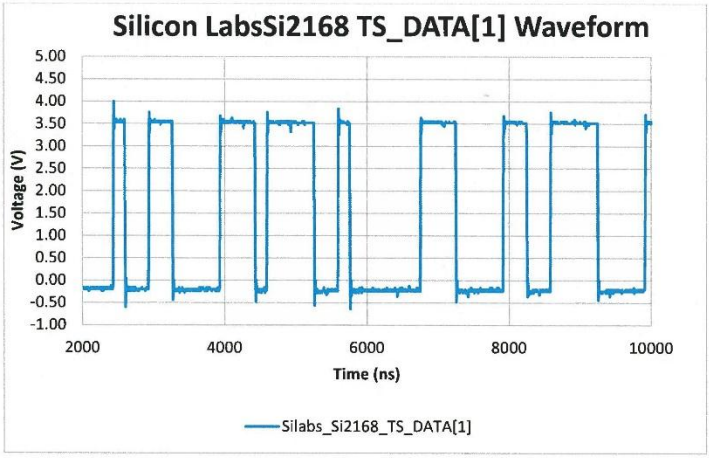
Si2168 MPEG TS SYNC (single pulse)



Si2168 MPEG TS SYNC (single pulse relative to clock)



Si2168 MPEG TS VALID



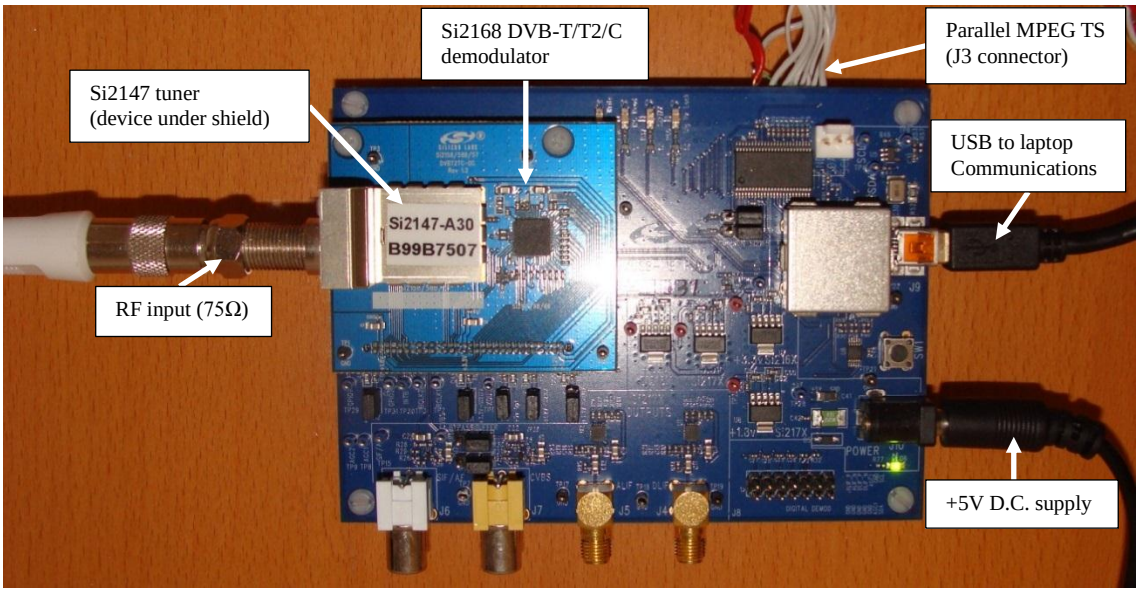
Si2168 MPEG TS DATA (Data line D1)

Appendix D Silicon Labs EVB

D.1 Overview

The EVB consists of a Si2147 digital only, low-IF silicon tuner capable of receiving ATSC, DVB-T/T2/C/C2, ISDB-T/C, and DTMB standards, and a Si2168 integrated digital demodulator, capable of supporting DVB-T/T2/C demodulation. The EVB is fully configurable using Silicon Labs proprietary application software.

The layout of the EVB, along with labelling of the key features, is shown on the next page. The EVB is constructed using a daughter board fitted with the Si2147 and Si2168 devices, and interfaces with a motherboard via a pin header. The motherboard, which is powered from a 5V DC source, provides step-down regulation to 1.8 V and 3.3 V supply voltages which are used to power the Si2147 and Si2168. I^2C bus communication to the devices is provided by USB connection to a computer. In addition, the motherboard provides connector interfaces, enabling the connection of test instruments for circuit evaluation purposes. The Si2147, located under an RF shield, enables connection to an RF antenna or test instruments via a 75Ω F-type connector. Parallel MPEG TS is provided via the J3 (labelled in on the diagram on the next page) connector at the bottom of the motherboard.



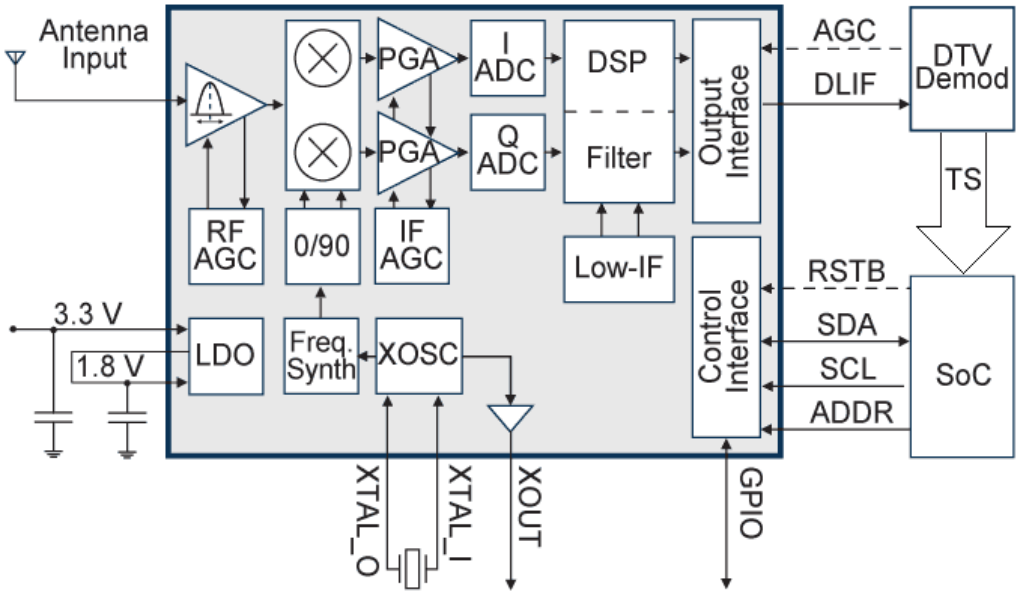
Silicon Labs EVB (author generated image)

Si2147 Tuner Operation

The block diagram of the Si2147 is shown on the next page. The device uses a 3.3 V rail to supply power to internal analogue circuitry, and a 1.8 V rail to power internal core digital circuitry. Device configuration is provided by I^2C communication via SCL (clock) and SDA (data) lines; commands are generated by the Silicon Labs application software and sent via USB to the EVB.

The device is capable of receiving digitally modulated channels within the frequency range 42 MHz to 870 MHz, and provides down-conversion of a selected channel to a programmable IF (default F_c = 5 MHz) which is accepted by a digital demodulator. In order to perform this operation, the tuner is tuned to the centre frequency of the desired TV channel using I^2C tuning commands. Once the tuner is tuned, the received RF spectrum, presented at the tuners RF input, via an antenna, is filtered using band-pass

tracking filter which is centred at the same frequency as the tuned desired channel; note that the centring of the tracking filter is set by the I^2C tuning commands. The filter rejects a large number of the undesired channels in the received spectrum, effectively isolating the desired channel. Amplification of the desired channel is then provided by an automatic gain controlled, low-noise amplifier (LNA). The filtered and amplified channel is then presented to an IQ mixer which down-converts the channel to baseband; note the local oscillators frequencies used in the mixer are also set by the I^2C tuning command. The IQ mixer uses the homodyne mixing process, which produces two separate signals; I (in-phase) and Q (quadrature), which are then amplified by two separate AGC programmable gain amplifiers (PGA). The I and Q signals are then passed to separate ADCs where the signals are digitised and processed using DSP techniques. Finally the signal is converted back into an analogue signal, up-converted to a low-IF signal (F_c = 5 MHz), and output on the digital low-IF (DLIF) output of the tuner. The IF is then presented to the Si2168 digital demodulator.



Silicon Labs Si2147 DVB low-IF tuner block diagram (Silicon Labs Inc.)

(V_{DD_H}=3.3 V, V_{DD_L}=1.8 V, V_{DD_D}=1.8 V, T_A=25 °C)

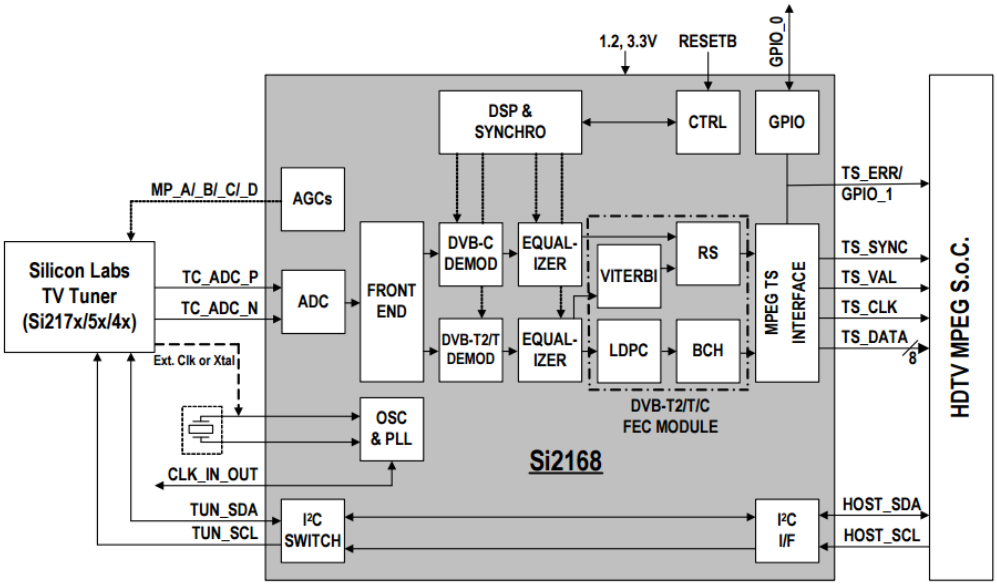
Parameter	Test Condition	Typ	Unit
Supply voltage		1.8 and 3.3, or only 3.3	V
Total Power Consumption	XOUT Disabled	484	mW
RF Input Frequency Range		42 to 870	MHz
NF, terrestrial*	VHF-L	4.0	dB
	VHF-H	3.7	dB
	UHF	3.8	dB
Return Loss*	Terrestrial mode	3	dB
	Cable mode	9	dB
Wideband IIP3*	VHF-H, N±18, ±36	+5	dBm
Inband IIP3*	VHF-H, N±1, ±2	–6	dBm
LO Phase Noise at 860 MHz	1 kHz | 10 kHz | 100 kHz | 1 MHz	–100 | –100 | –105 | –132	dBc/Hz
LO Integrated Phase Noise at 860 MHz	DSB: 125 Hz to 4 MHz	0.25 (-47)	°rms (dBc)
DLIF Output Center Frequency	channel BW=6 MHz | 7 MHz | 8 MHz	4 to 7 | 4.5 to 6.5 | 5 to 6	MHz
DLIF Differential Output Voltage	Programmable	0.5 to 2.0	Vppd
***Note:** Measured at the F-connector input of the Si2147 EVB and includes all connector, PCB, and front-end circuit losses.			

Silicon Labs Si2147 public domain data short

The complete Si2147 Worldwide Digital TV Tuner data short is available at Digikey website (Silabs, 2012).

Si2168 Demodulator Operation

The Si2168 is an integrated digital demodulator capable of supporting DVB-T, DVB-T2, and DVB-C demodulation. A block diagram of the device is shown on the next page. The demodulator also uses the 3.3 V rail for analogue circuitry and a 1.8 V rail for the core digital circuitry. Programming of the device is also achieved through I^2C communication; note that the demodulator is connected via the SCL (clock) and SDA (data) lines of the tuner, in a master-slave configuration.



Silicon Labs Si2168 DVB-T/T2/C digital demodulator block diagram (Silicon Labs Inc.)

The demodulator accepts the 5 MHz DLIF output from Si2147 tuner, and then digitise the IF using an ADC. Prior to demodulation, the device requires configuration for DVB-T, DVB-T2 or DVB-C reception using I^2C commands. This is necessary because different demodulation and channel equalisation is needed for terrestrial COFDM and cable QAM broadcasts. Once the demodulation standard is configured, symbol de-mapping and forward-error correction (FEC) is performed. The FEC detects, and where possible, correct errors in the received data stream. If a DVB-T broadcast is received, convolutional inner decoding (Viterbi decoding) is applied, followed by and Reed-Solomon (RS) outer decoding for error detection and correction. In the case of DVB-T2 reception, LDPC (Low Density Parity Check) inner decoding and Bose-Chaudhuri-Hocquenghem outer decoding (BCH) are applied. And finally, in the case of DVB-C reception, only RS outer decoding is necessary. Finally, the decoded MPEG TS is output in one of two configurations, parallel TS or serial TS.

Refer to Appendix F.1 for the SI2168 IC pinout.

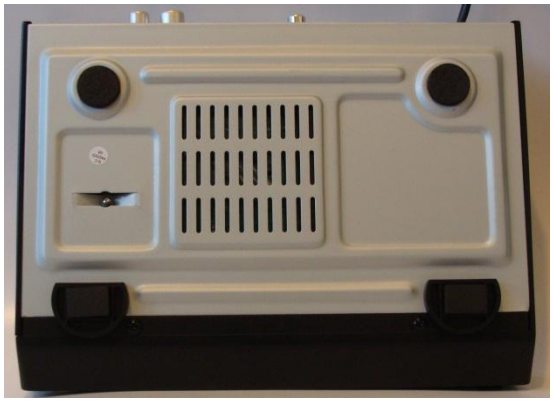
Appendix E Bush DH2636 DVB-T/T2 STB

E.1 Overview

Front panel

Rear panel

Top cover

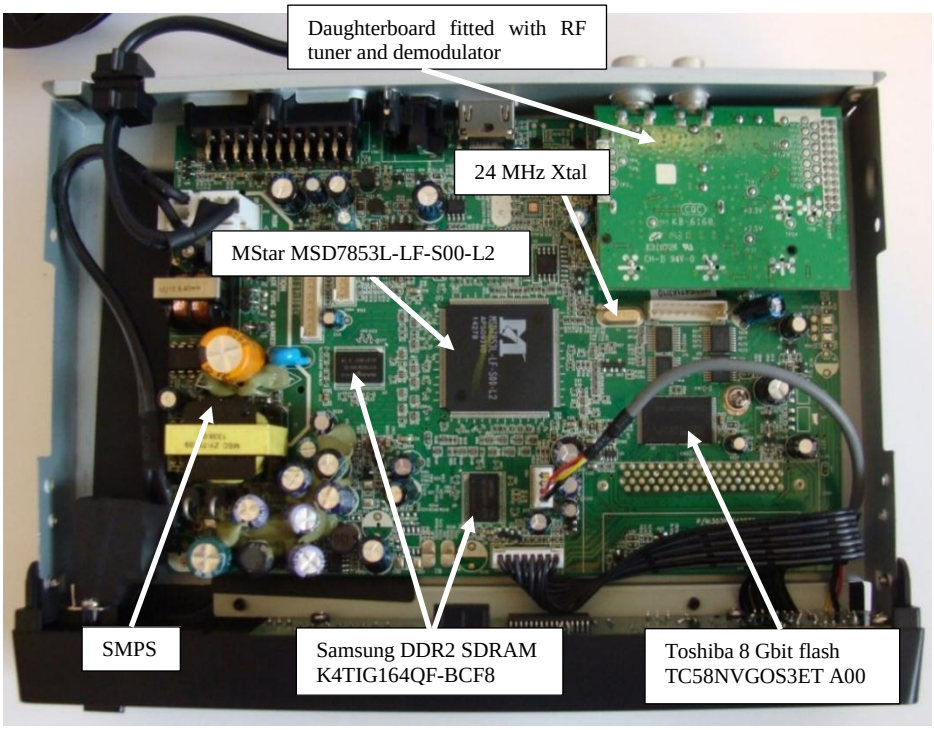


Chassis base

Bush DH2636 STB (external view)

The front panel consists of a mains power on/off switch, a 4-digit, 7-segment display, channel up and down select buttons, and a USB 2.0 interface enabling DVR content storage and media file access. The rear panel consists of a 240 V RMS cable input, a 75 Ω IEC female RF input connector, a 75 Ω IEC male RF output connector (loop-through amplifier output), a coaxial digital audio input, a SCART connector for analogue video

and audio signals, and an HDMI 1.4 interface. The unit also comes with an IR remote control. The internal appearance of the STB, with top cover removed, is shown below.



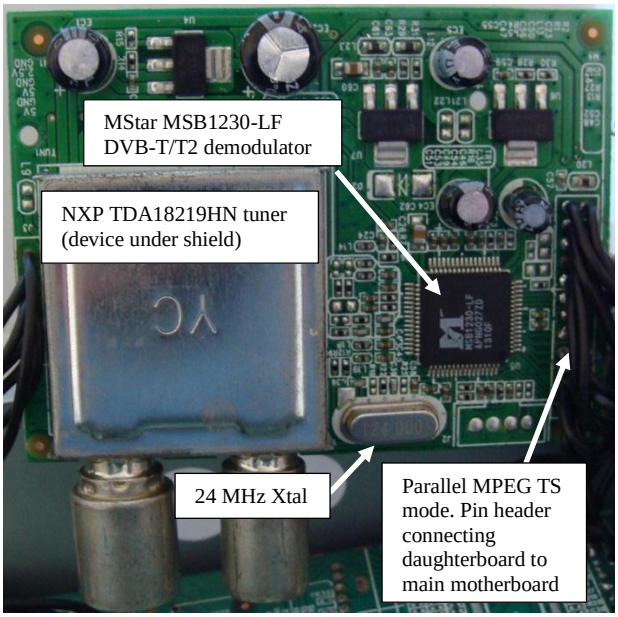
Bush DH2636 STB (internal view)

The main semiconductor devices and other features of the motherboard are labelled. A switch-mode power supply (SMPS) circuit is used to convert the 240 V RMS mains supply to various supply rails needed by the subsystems of the STB. The core semiconductor device on the motherboard is the MStar MSD7853L-LF-S00-L2 processor, shown in below (IC close-up)

MStar MSD7853L-LF-S00-L2 processor

The device provides the STBs key processing functions and also controls all the subsystem of the STB architecture. The processor uses a 24 MHz reference crystal, synchronous dynamic random-access memory (SDRAM) for data storage, and flash memory to store the platform firmware.

One of the primary functions of the processor is to provide MPEG-2 (SDTV) and MPEG-4 AVC/H.264 (HDTV) MPEG decoding of an 8-bit parallel MPEG TS, in this case sourced from the output of the demodulator IC fitted on the bottom of the daughterboard. The bottom of the daughterboard where an MStar MSB1230 DVB-T/T2 demodulator is fitted is shown below. Note that the demodulator is configured for parallel MPEG TS.

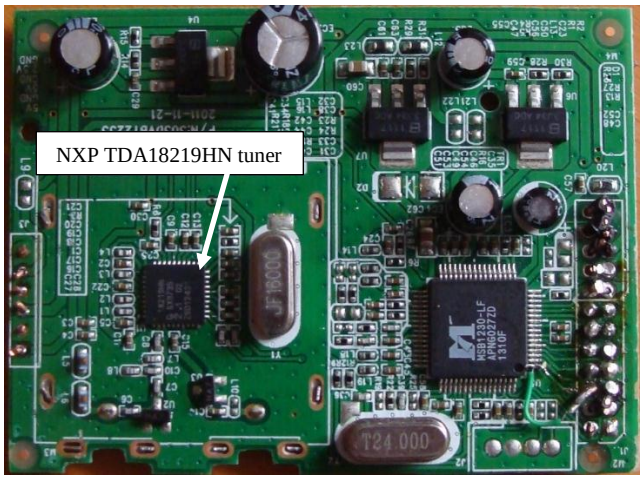


Daughterboard

A close-up of the MSB1230 IC is shown below. Refer to Appendix F.2 for the MSB1230 IC pinout.

MStar MSB1230 DVB-T/T2 demodulator IC

Also on the bottom of the daughterboard is an RF shield with the integrated IEC connectors, under which is fitted the NXP TDA18219HN silicon tuner, capable of terrestrial and cable digital TV reception (NXP, 2012). The RF shield removed is shown below, revealing the TDA18219HN IC.



Daughterboard (shield removed)

The function of the TDA18219HN silicon tuner and MSB1230 DVB-T/T2 demodulator is identical, respectively, to the Silicon Lab EVBs Si2147 and Si2168 devices.

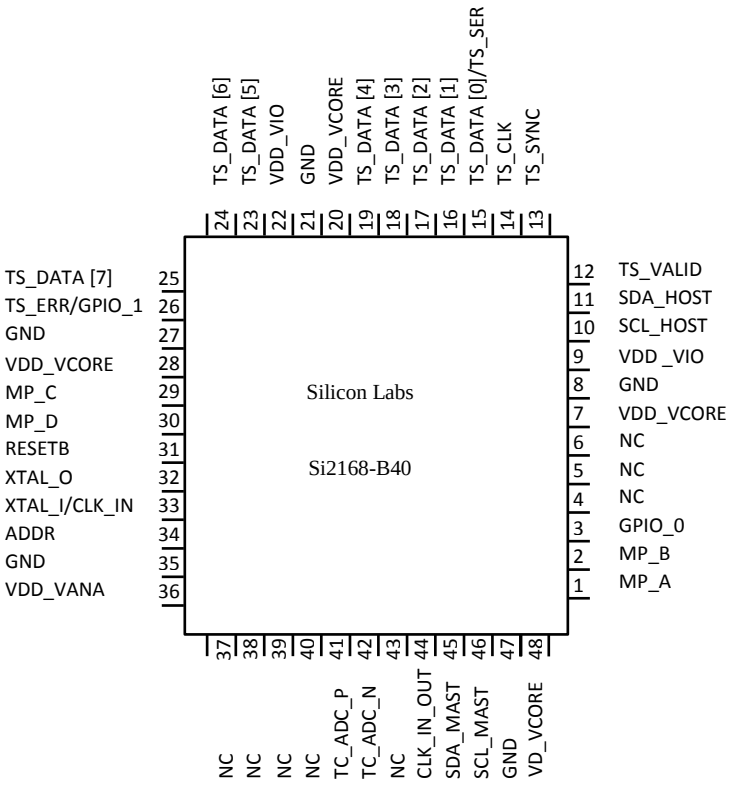
E.2 Product Specification

Item	Specification	
Service	Freeview	Standard Definition and High Definition
RF Front-end	Frequency Range	175 MHz to 860 MHz
	Input Impedance	75 Ω (unbalanced)
	Dynamic Range	-65 dBm to -25 dBm
RF Demodulation	Modes	QPSK, 16 QAM, 64 QAM, 256 QAM
	FEC	LDPC + BCH Code Rate: 1/2, 3/5, 2/3, 3/4, 4/5, 5/6
Decoding	Video	MPEG-2 Transport MP@ML.HL MPEG-4 AVC/H.264 HP@L4
	Audio	MPEG-2 Audio Layer I&II
Display	Aspect ratio	4:3 (letterbox, pan and scan) 16:9
	Analogue	PAL/NTSC
	Resolution	1080p, 1080i, 720p, 720x576 (PAL), 720x480 (NTSC), 576p, 576i, 480p, 480i
Compliances	DVB-T	EN300744
	DVB-T2	EN302755
	Stereo Audio (left and right)	
Interfaces	RF Input	IEC Female (primary RF input from antenna)
	RF Output	IEC Male (RF loop-through)
	USB	USB 2.0
	SCART Output	Audio/Video (legacy analogue)
	HDMI	Interface for transferring uncompressed HDTV audio/video data. HDMI 1.4
Power	Mains Voltage	100 V RMS – 240 V RMS
	Mains Frequency	50 Hz or 60 Hz
	Consumption On mode power Standby power	 Max. 8 W 1 W
Physical	Dimensions (Height x Width x Depth)	4.5 cm x 22 cm x 16 cm
	Mass	1 kg

Bush DH2636 DVB-T/T2 STB public domain product specification

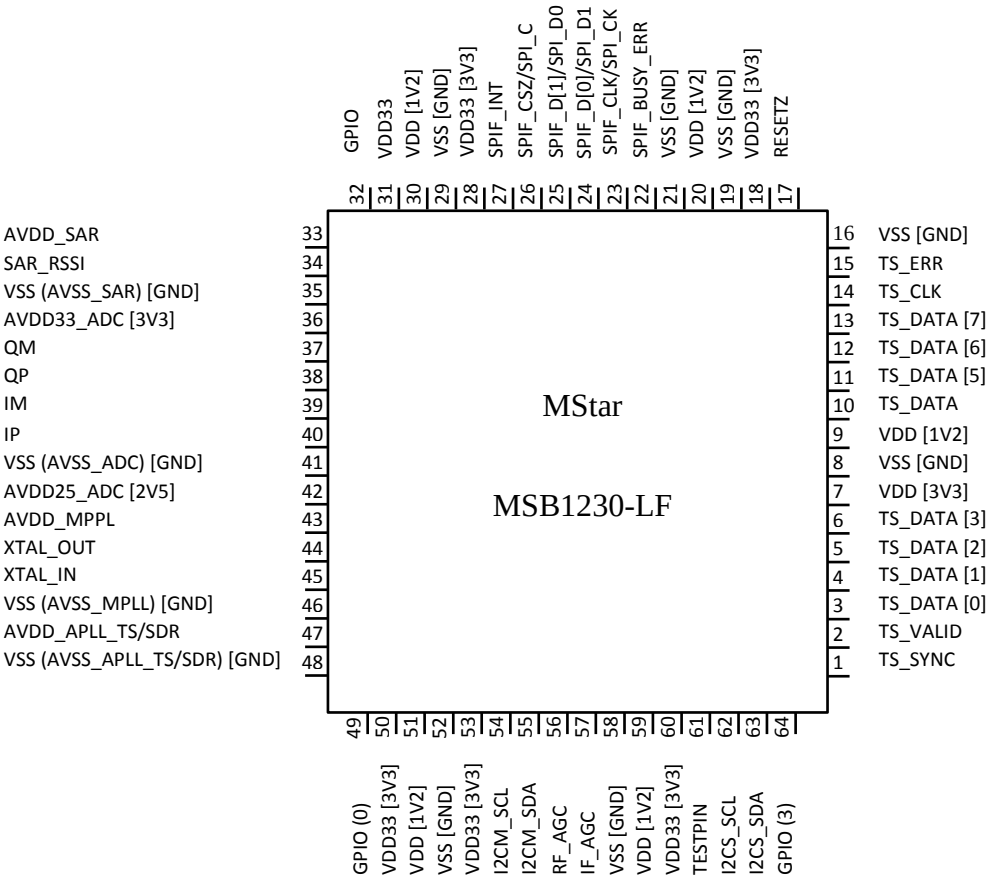
Appendix F MPEG TS Source and Sink ICs

F.1 Silicon Labs Si2168-B40 DVB-T2/T/C digital TV demodulator IC pinout



	Silicon Labs Si2168-B40
MPEG TS Function	IC Pin Number
TS_CLK	14
TS_SYNC	13
TS_VALID	12
TS_ERR	26
TS_DATA[0]/TS SER	15
TS_DATA[1]	16
TS_DATA[2]	17
TS_DATA[3]	18
TS_DATA[4]	19
TS_DATA[5]	23
TS_DATA[6]	24
TS_DATA[7]	25

F.2 MStar MSB1230-LF DVB-T2/T digital TV demodulator IC pinout



	MStar MSB1230-LF
MPEG TS Function	IC Pin Number
TS_CLK	14
TS_SYNC	1
TS_VALID	2
TS_ERR	15
TS_DATA[0]	3
TS_DATA[1]	4
TS_DATA[2]	5
TS_DATA[3]	6
TS_DATA[4]	10
TS_DATA[5]	11
TS_DATA[6]	12
TS_DATA[7]	13

Appendix G MPEG TS Characterisation Test Setup

G.1 Silicon Labs Si2168 Test Setup

Measurements of the individual eleven pins of the Si2168 MPEG TS were performed using a Tektronix TBS1000 Series, TBS1202B-EDU (200MHz/2GS/s) oscilloscope, and a probe with a 10 MΩ impedance, and capacitance ≤12 pF. The MPEG TS was accessed via J3 connector on the bottom of the motherboard, as shown in Appendix D.1.

The Si2147 and Si2168 reception parameters were configured using the controls on the '*Main*' tab of the Silicon Labs application software graphical user interface (GUI), as shown in Figure G.1-14.

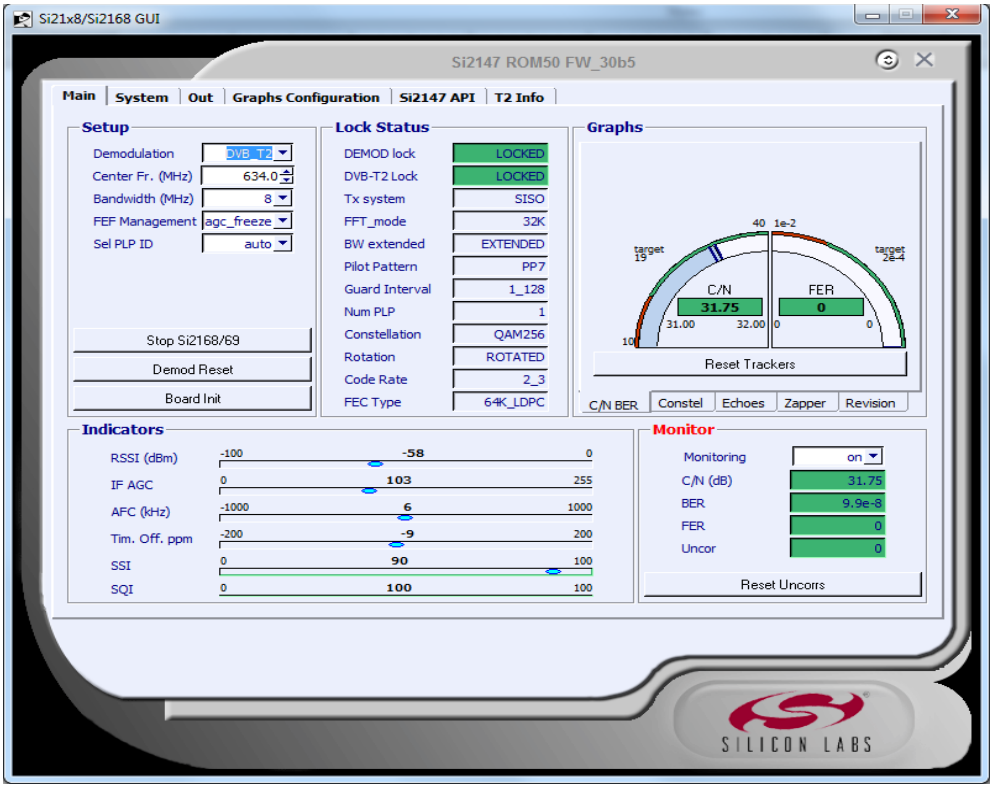


Figure G.1-14 Silicon Labs Si2147/Si2168 software '*Main*' tab settings (Silicon Labs Inc.)

The Si2147 tuners RF input was connected to a roof-top Yagi array antenna, and the tuner, tuned using the GUIs '*Setup*' window controls to a live off-air terrestrial DVB-T2 broadcast transmitted by Emley Moor transmitter in West Yorkshire, UK. Channel C41, with an RF centre frequency of 634 MHz and bandwidth of 8 MHz, was chosen because it contained both SDTV and HDTV multiplexed programme streams, specifically: C86 More4 +1; C101 BBC One HD (England no regional news); C102 BBC Two HD (England); C103 ITV HD (ITV Granada); C104 Channel 4 HD North ads; C105 Channel 5 HD; and C204 CBBC HD (Butterworth, 2004).

Once the Si2147 and Si2168 were tuned and locked to Channel C41 (634 MHz), the GUI reported information about the received channel on the GUIs '*Lock Status*' window. Specifically, the channel was reported with a QAM 256 constellation, 2/3 code rate, 1/128 guard interval and 32 K FFT.

The GUIs '*Monitoring*' window reported the carrier-to-noise ratio (CNR) of the channel at approximately 31.75 dB. This window also reported that the demodulated MPEG TS had an estimated bit-rate of 40.21 Mbit/s, with a BER of approximately 9.9×10^{-8}, well below the QEF limit of 2.4×10^{-4}. Note that throughout the characterisation of the MPEG TS, the FER and uncorrected TS packets were monitored, and no uncorrected errors were observed during the measurement periods.

The MPEG TS output interface of the Si2168 was configured using the '*Out*' tab of the GUI, as shown in Figure G.1-15. Parallel MPEG TS output with a non-inverted clock (inverted shown in figure) was set using the '*TS Output*' window, and a 6 MHz MPEG TS clock frequency was set using the '*TS Clock*' window.

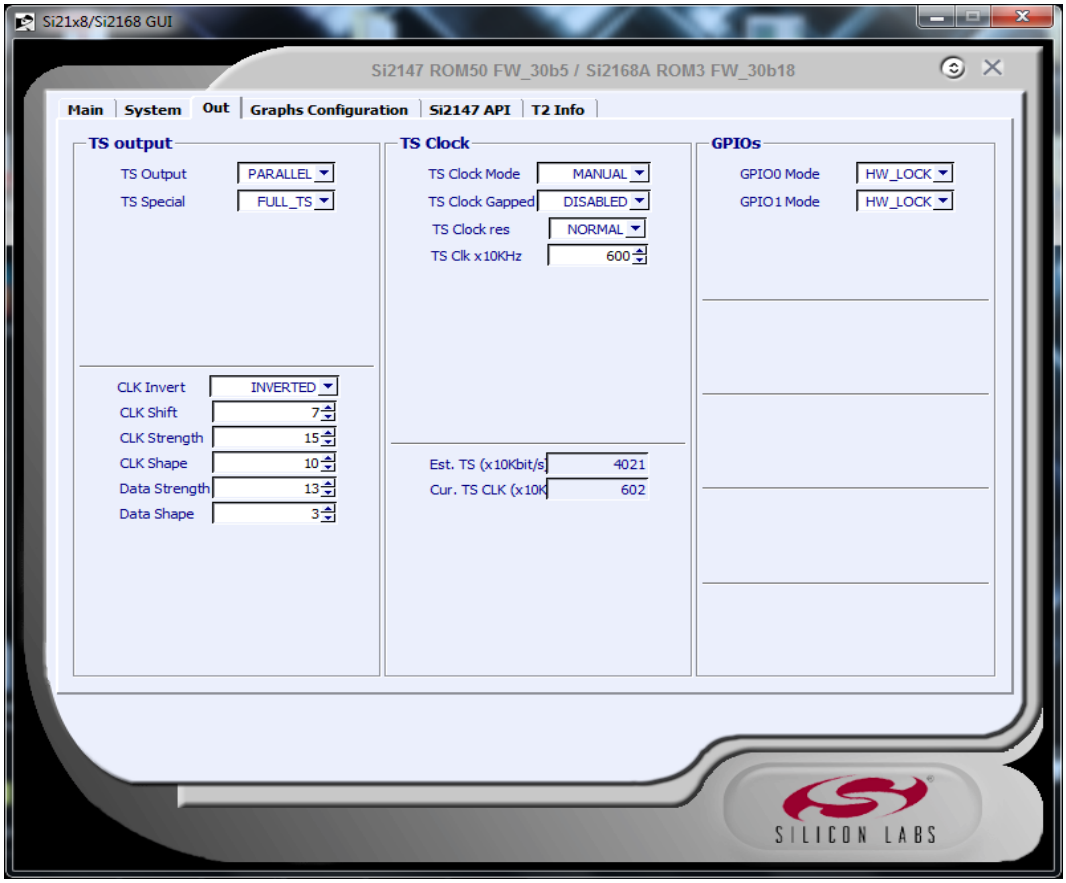


Figure G.1-15 Silicon Labs Si2147/Si2168 software '*Out*' tab settings (Silicon Labs Inc.)

G.2 MStar MSB1230 Test Setup

The characterisation of the MPEG TS MSB1230 followed a similar approach to that of the Si2168. Eleven pins of the MPEG TS were individually measured using the same Tektronix TBS1202B-EDU oscilloscope and probe (Z = 10 MΩ, c <= 12 pF) used during the Si2168 characterisation. The MPEG TS was accessed at the pin header which connected the daughterboard to the main motherboard of the STB. Using the DH2636 STB IR remote control and built-in menus, and with a roof-top Yagi array antenna connected to the RF input of the STB, a channel scan was performed. Amongst a number of other terrestrial broadcast channels, Channel C41 (634 MHz) was found and stored in the STB channel look-up table, and then using the remote control, the BBC One HD elementary stream of the multiplex was selected. The MPEG TS of Channel

C41 was output on the parallel MPEG TS pins of the MSB1230. All settings of the tuner and demodulator were under the control of the STB firmware, and were not accessible by the author. Note that during measurement periods described in the following sections, no uncorrected errors were observed.

Appendix H Bypass Board Configuration

H.1 MSB1230 and MB J3 connector transport streams pin assignments

Bypass Board Switch Function	Bypass Board Switch Number	MSB1230 Pin Number	MB J3 Pin Number
N.C.	1	15	12
TS_CLK	2	14	13
TS_DATA[7]	3	13	2
TS_DATA[6]	4	12	3
TS_DATA[5]	5	11	4
TS_DATA[4]	6	10	5
TS_DATA[3]	7	6	6
TS_DATA[2]	8	5	7
TS_SYNC	9	1	11
TS_VALID	10	2	10
TS_DATA[0]	11	3	9
TS_DATA[1]	12	4	8

N.C. = No connect

MSB1230 and MB J3 connector transport streams pin assignments

H.2 Bypass Board MPEG TS Switching Schematic

Bypass board MPEG TS switching schematic

Appendix I LED Characterisation Setup

I.1 Frequency Response and Bandwidth Test Setup

Characterisation of the LEDs was performed using the setup shown in Figure I.1-16.

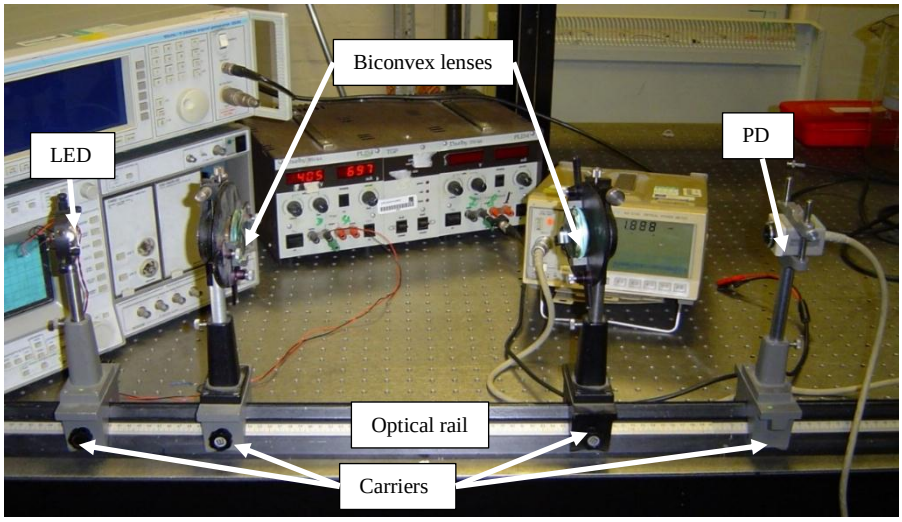


Figure I.1-16 LED characterisation setup

(author generated image)

An optical rail was used to mount and precisely position vertically and horizontally adjustable carriers, upon which the LED under test, two biconvex lenses, and a reference PD were attached. The biconvex lenses were arrange to collimate the light emission from the LED and focus it onto the PDs detecting area, as shown in Figure I.1-17. Optimal focussing of the incident light on the PD was achieved using a separation of 95 cm between LED and PD, and equidistant separations of 19 cm between the respective biconvex lens closest to the LED and PD.

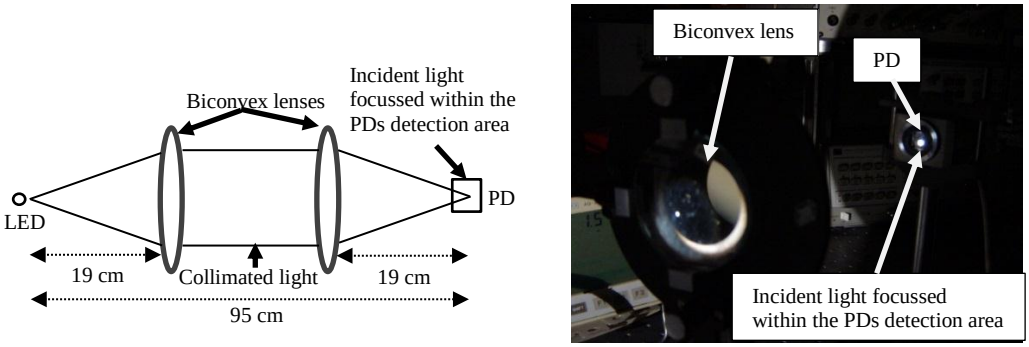


Figure I.1-17 Collimating lenses arrangement (author generated image)

A test circuit was devised to enable the simultaneous connection of a variable DC constant current source and sinusoidal voltage source to the anode of the LED. Figure I.1-18 shows the schematic and physical arrangement of the test circuit. The test circuit consisted of a 1.2 Ω current limiting resistor, and a 1 nF capacitor to enable coupling of the sinusoidal voltage source into the anode of the LED.

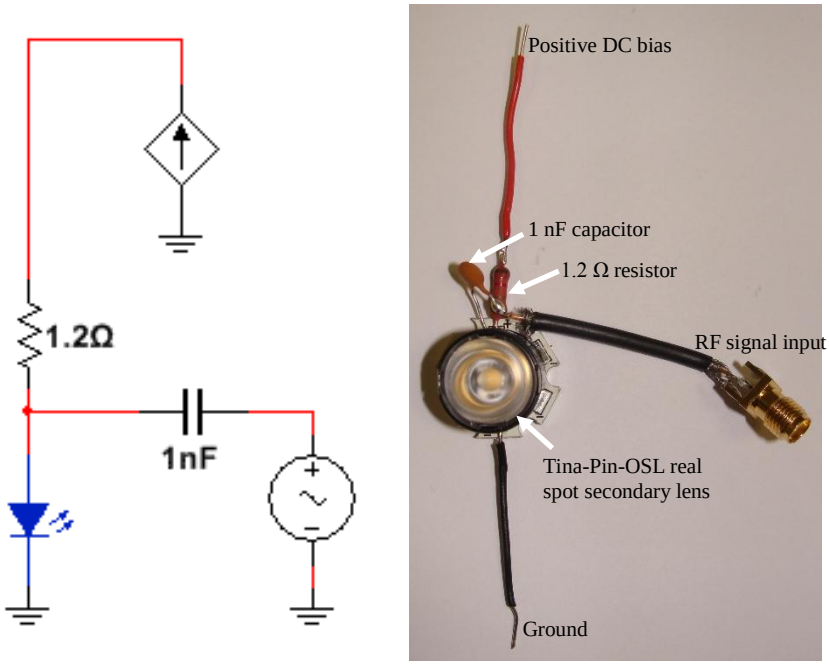


Figure I.1-18 LED test circuit configuration (author generated image)

Note that a secondary Tina-Pin-OSL real spot lens, also manufactured by Osram, was mounted over the LED. This lens provides a full-width, half-maximum (FWHM) angle

of ± 4°, effectively reducing the irradiance angle and concentrating the LED emission into a narrow beam.

A Thurlby Thandar Instruments (TTi) PL154 (0 to 15.5 V, 0 to 4 A) DC power supply was used to provide the diode with a constant DC forward bias current. A Marconi 2030 10 kHz to 1.35 GHz RF signal generator was used to modulate the emission of the LED by providing a frequency sweep from 10 kHz to 200 MHz at a signal amplitude of 1 V p-p. The emission was detected by a Thorlabs PDA10A-EC Si amplified PD with 200 to 1100 nm wavelength detection range; the data sheet of this device is available at www.thorlabs.com (Thorlabs, 2018).

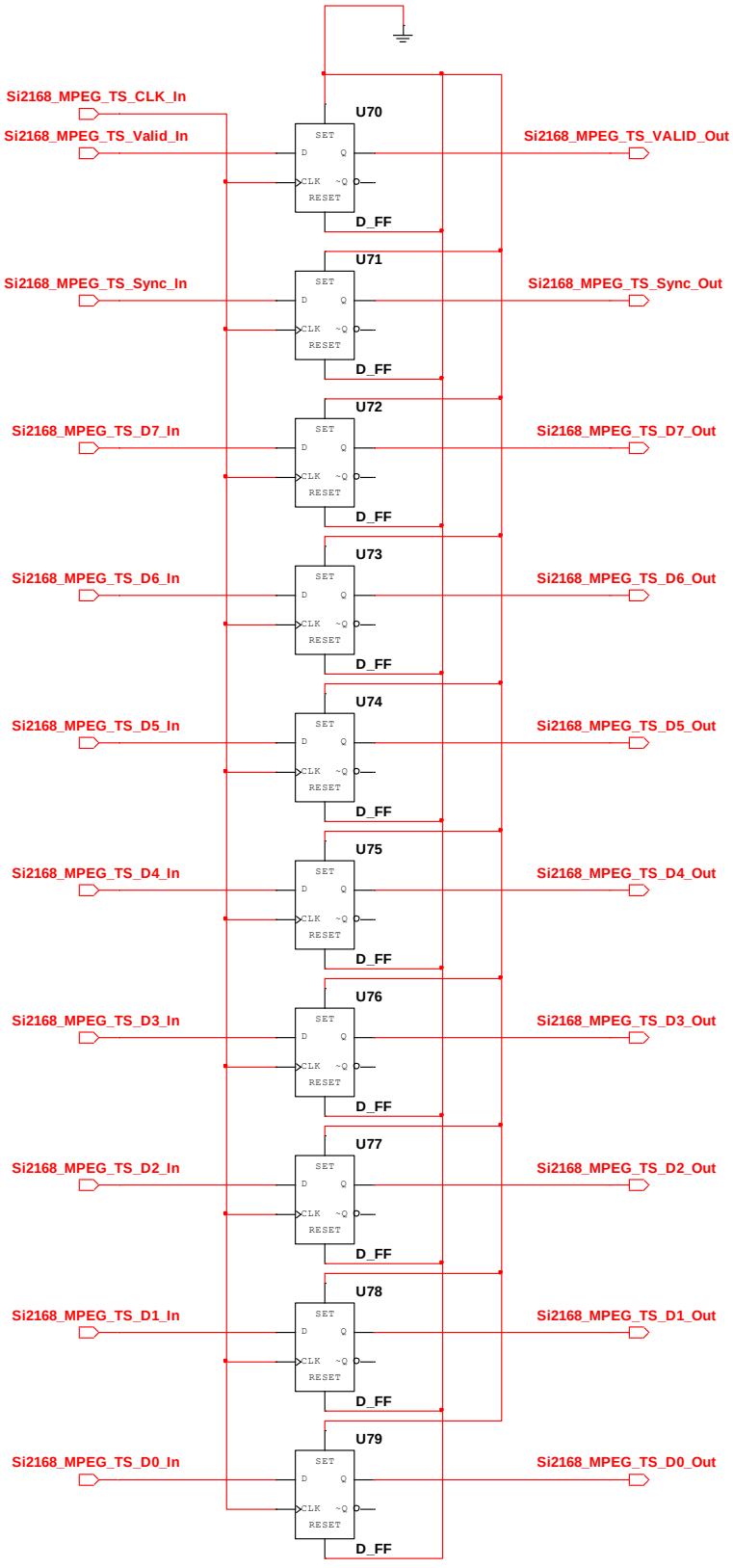
I.1 Received Power Test Setup

The received power at the reference PD was also measured using the same characterisation setup and carriage separations shown in Figure I.1-16. However, the Thorlabs PDA10A-EC Si amplified PD was replaced with an Ando AQ-2718 power sensor having a wavelength detection range of 400 to 1150 nm. The sensor was operated using an Ando AQ-2105 optical power meter fitted with an AQ2109 OPM unit. Measurements were performed with the OPM unit operating in continuous wave (CW) mode, giving a measurement dynamic range of -70 to +10 dBm at a wavelength of 850 nm.

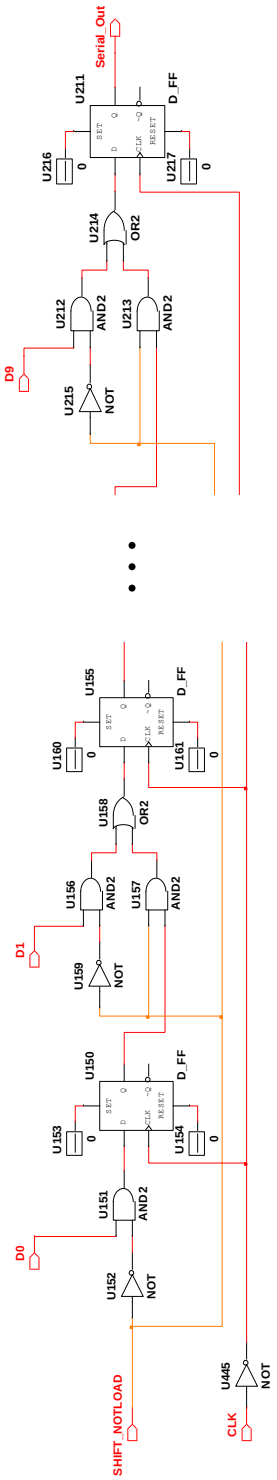
During the measurements, the RF signal generator was set and fixed at the peak of the frequency responses at 2.3 MHz (white LED) and 3.18 MHz (blue LED) with a signal amplitude of 1 V p-p.

Appendix J Multisim Circuits

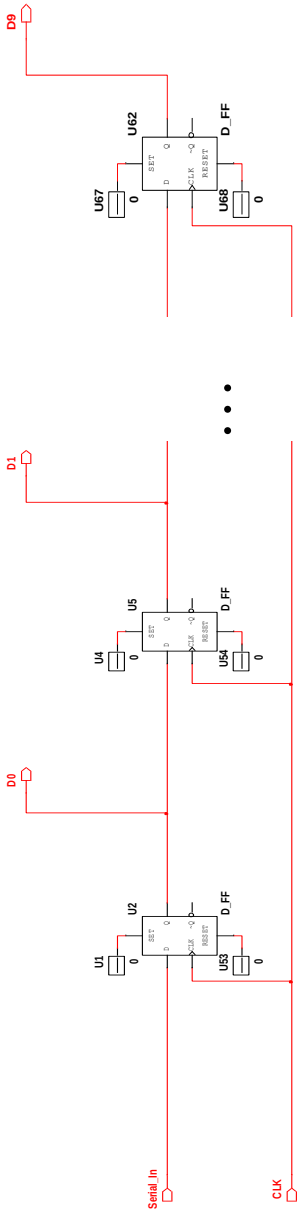
J.1 10-bit MPEG TS Buffer Register Circuit



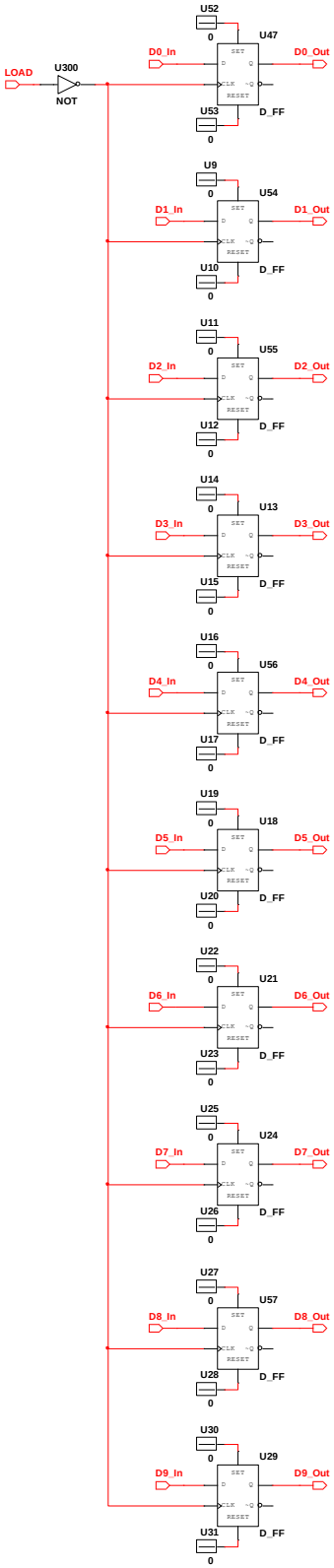
J.2 10-bit PISO Circuit



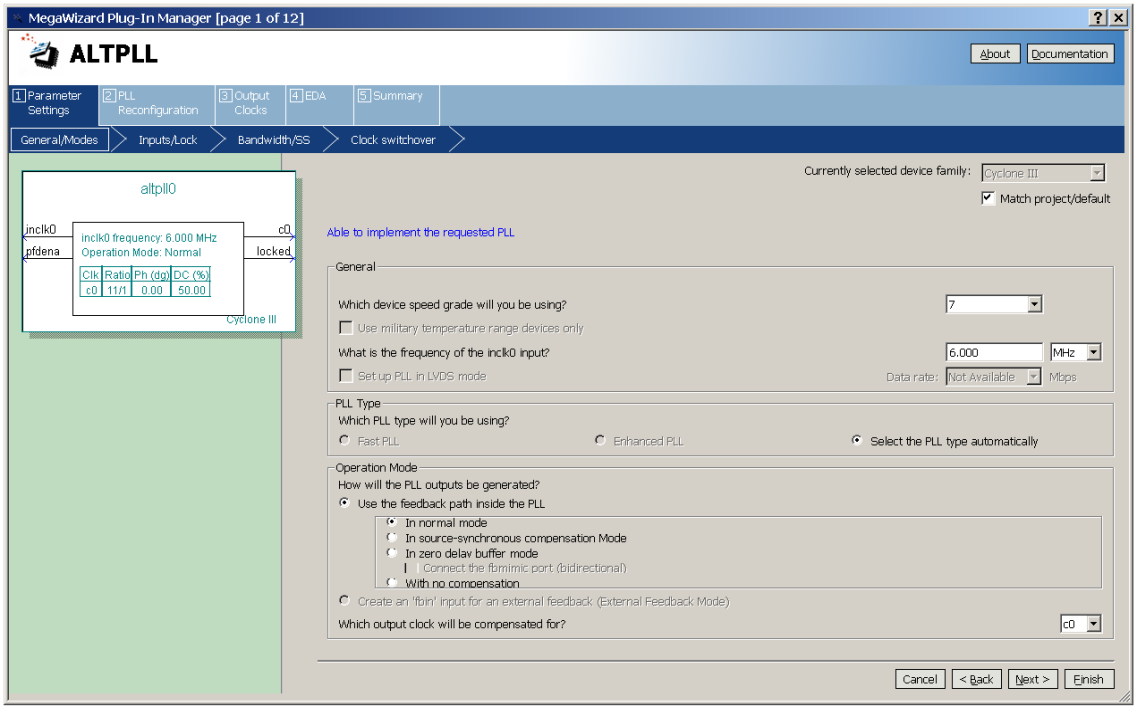
J.3 10-bit SIPO Circuit – Serial shift

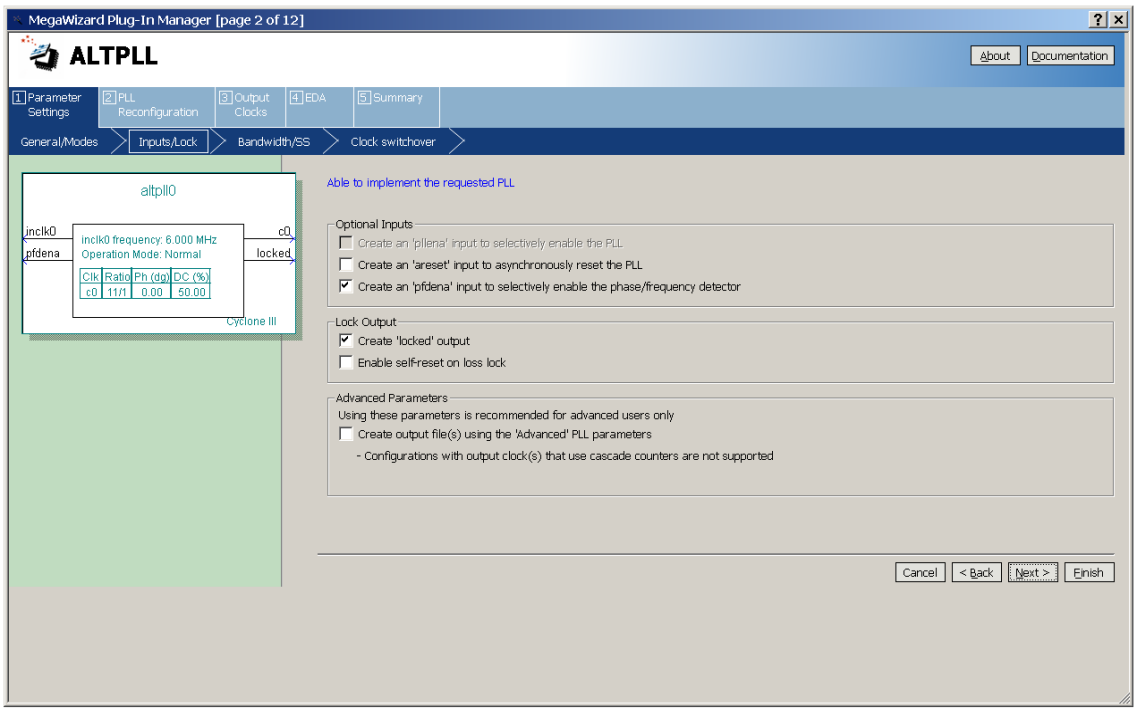


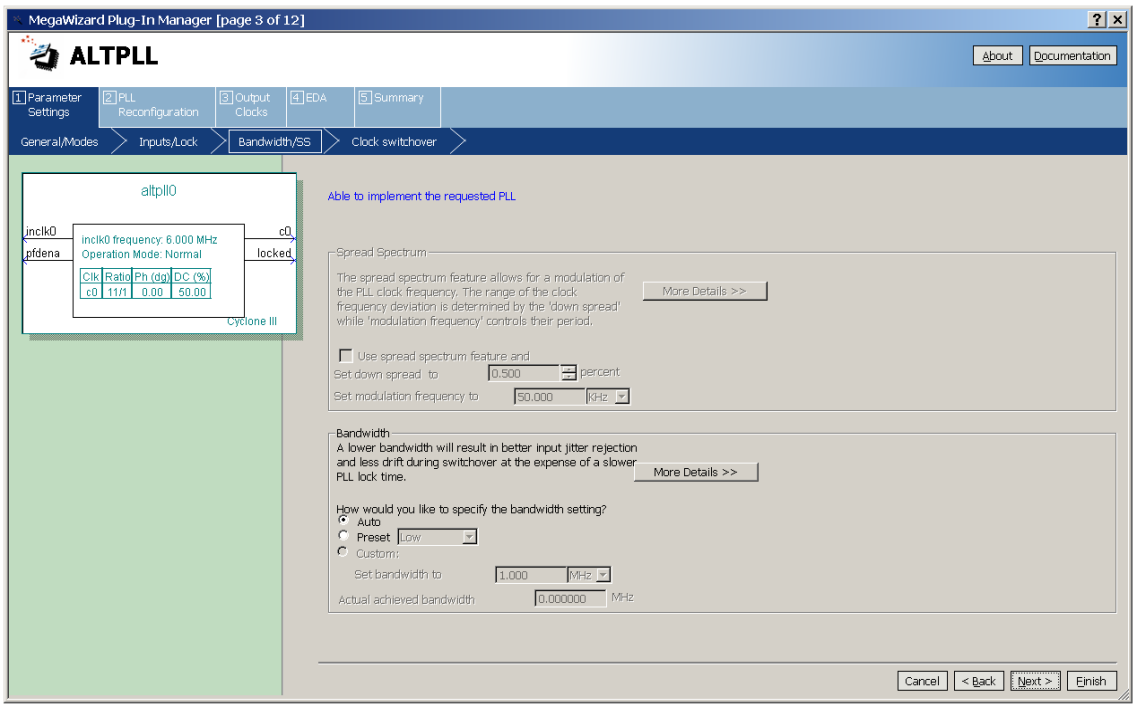
J.4 10-bit SIPO Circuit – Parallel load



Appendix K Altera Quartus II 66 MHz PLL Design



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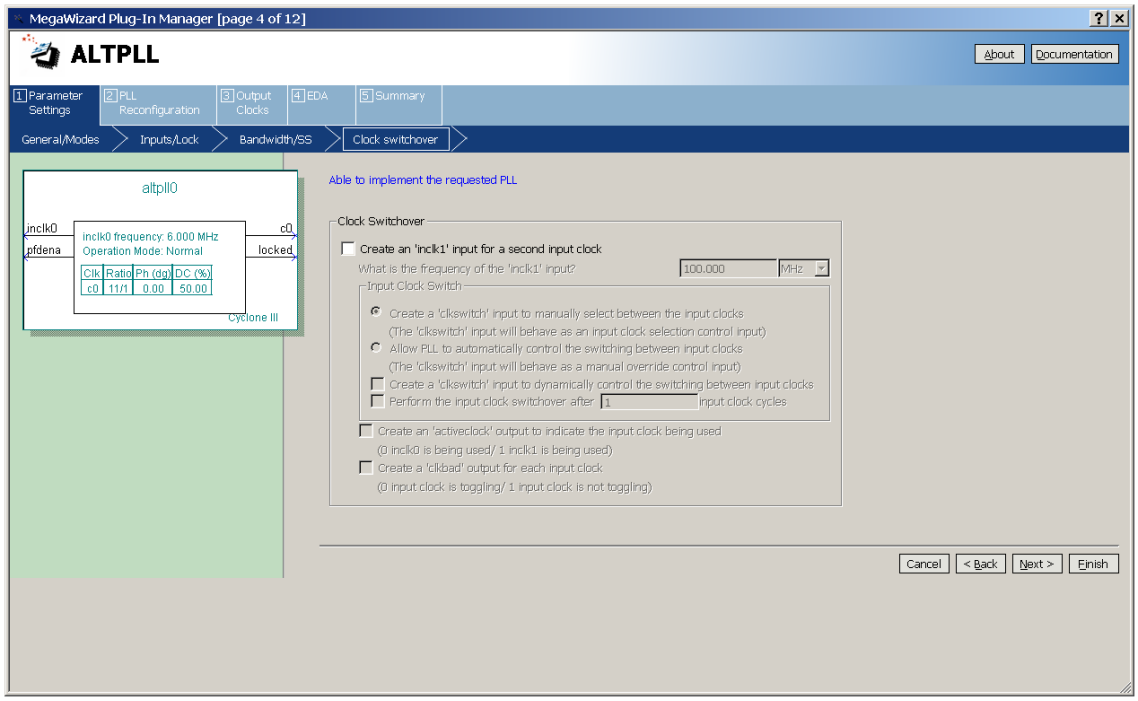
ALTPLL
About
Documentation
1 Parameter Settings
2 PLL Reconfiguration
3 Output Clocks
4 EDA
5 Summary
General/Modes
Inputs/Lock
Bandwidth/SS
Clock switchover
altpll0
inclk0
pfdena
c0
locked
inclk0 frequency: 6.000 MHz
Operation Mode: Normal
Clk Ratio Ph (dg) DC (%)
c0 11/1 0.00 50.00
Cyclone III
Able to implement the requested PLL
Spread Spectrum
The spread spectrum feature allows for a modulation of the PLL clock frequency. The range of the clock frequency deviation is determined by the 'down spread' while 'modulation frequency' controls their period.
More Details >>
Use spread spectrum feature and
Set down spread to 0.500 percent
Set modulation frequency to 50.000 KHz
Bandwidth
A lower bandwidth will result in better input jitter rejection and less drift during switchover at the expense of a slower PLL lock time.
More Details >>
How would you like to specify the bandwidth setting?
Auto
Preset Low
Custom:
Set bandwidth to 1.000 MHz
Actual achieved bandwidth 0.000000 MHz
Cancel
< Back
Next >
Finish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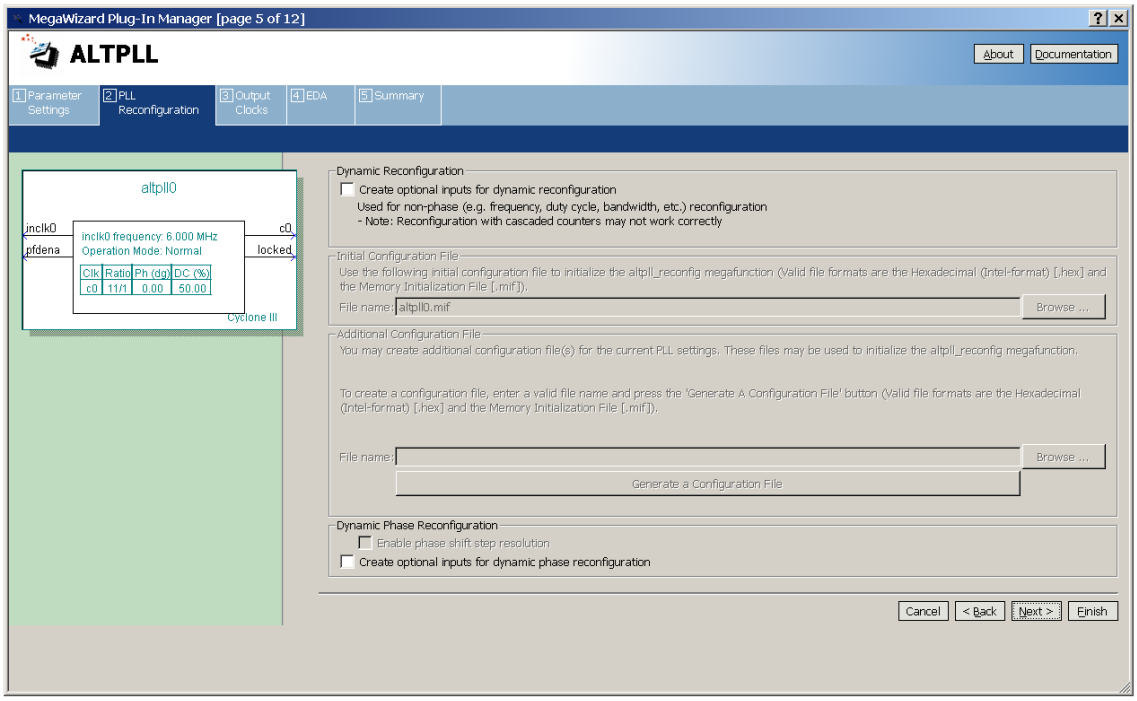
1 Parameter Settings
2 PLL Reconfiguration
3 Output Clocks
4 EDA
5 Summary
General/Modes
Inputs/Lock
Bandwidth/SS
Clock switchover
altpll0
inclk0
pfdena
c0
locked
inclk0 frequency: 6.000 MHz
Operation Mode: Normal
Clk Ratio Ph (dg) DC (%)
c0 11/1 0.00 50.00
Cyclone III
Able to implement the requested PLL
Clock Switchover
Create an 'inclk1' input for a second input clock
What is the frequency of the 'inclk1' input? 100.000 MHz
Input Clock Switch
Create a 'clkswitch' input to manually select between the input clocks
(The 'clkswitch' input will behave as an input clock selection control input)
Allow PLL to automatically control the switching between input clocks
(The 'clkswitch' input will behave as a manual override control input)
Create a 'clkswitch' input to dynamically control the switching between input clocks
Perform the input clock switchover after 1 input clock cycles
Create an 'activeclock' output to indicate the input clock being used
(0 inclk0 is being used/ 1 inclk1 is being used)
Create a 'clkbad' output for each input clock
(0 input clock is toggling/ 1 input clock is not toggling)
Cancel
< Back
Next >
Finish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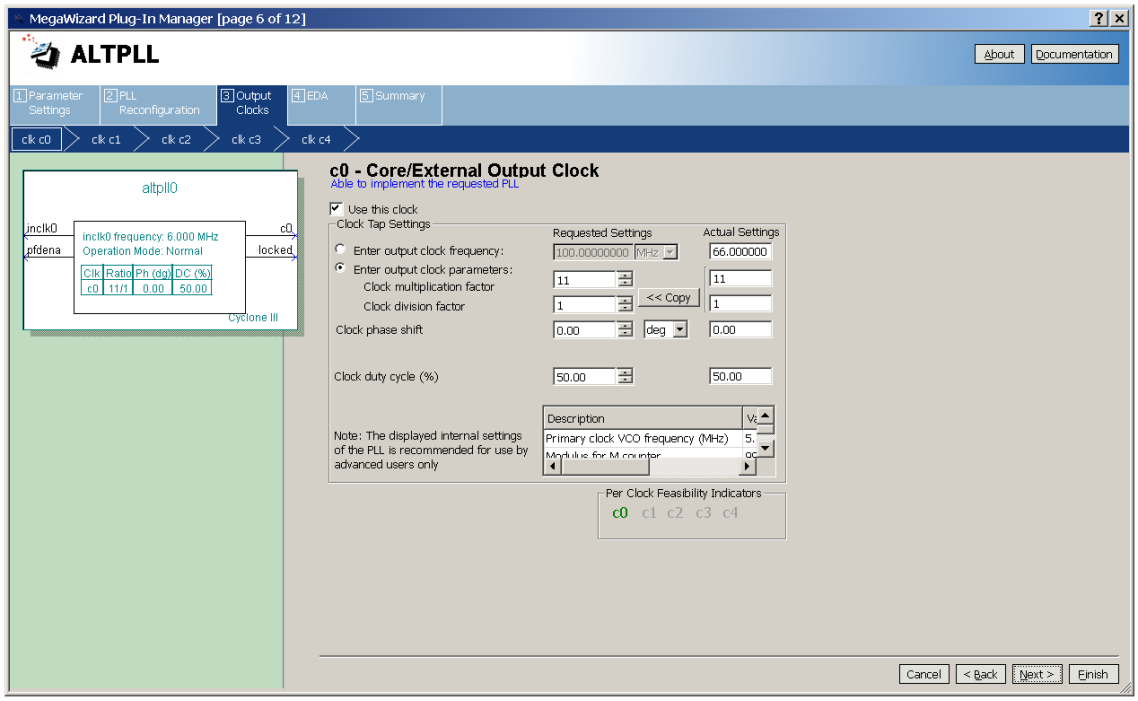
3 Output Clocks
4 EDA
5 Summary
altpll0
inclk0
pfdena
inclk0 frequency: 6.000 MHz
Operation Mode: Normal
Clk Ratio Ph (dg) DC (%)
c0 11/1 0.00 50.00
c0
locked
Cyclone III
Dynamic Reconfiguration
Create optional inputs for dynamic reconfiguration
Used for non-phase (e.g. frequency, duty cycle, bandwidth, etc.) reconfiguration
- Note: Reconfiguration with cascaded counters may not work correctly
Initial Configuration File
Use the following initial configuration file to initialize the altpll_reconfig megafunction (Valid file formats are the Hexadecimal (Intel-format) [.hex] and the Memory Initialization File [.mif]).
File name: altpll0.mif
Browse ...
Additional Configuration File
You may create additional configuration file(s) for the current PLL settings. These files may be used to initialize the altpll_reconfig megafunction.
To create a configuration file, enter a valid file name and press the 'Generate A Configuration File' button (Valid file formats are the Hexadecimal (Intel-format) [.hex] and the Memory Initialization File [.mif]).
File name:
Browse ...
Generate a Configuration File
Dynamic Phase Reconfiguration
Enable phase shift step resolution
Create optional inputs for dynamic phase reconfiguration
Cancel
< Back
Next >
Finish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About
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1 Parameter Settings
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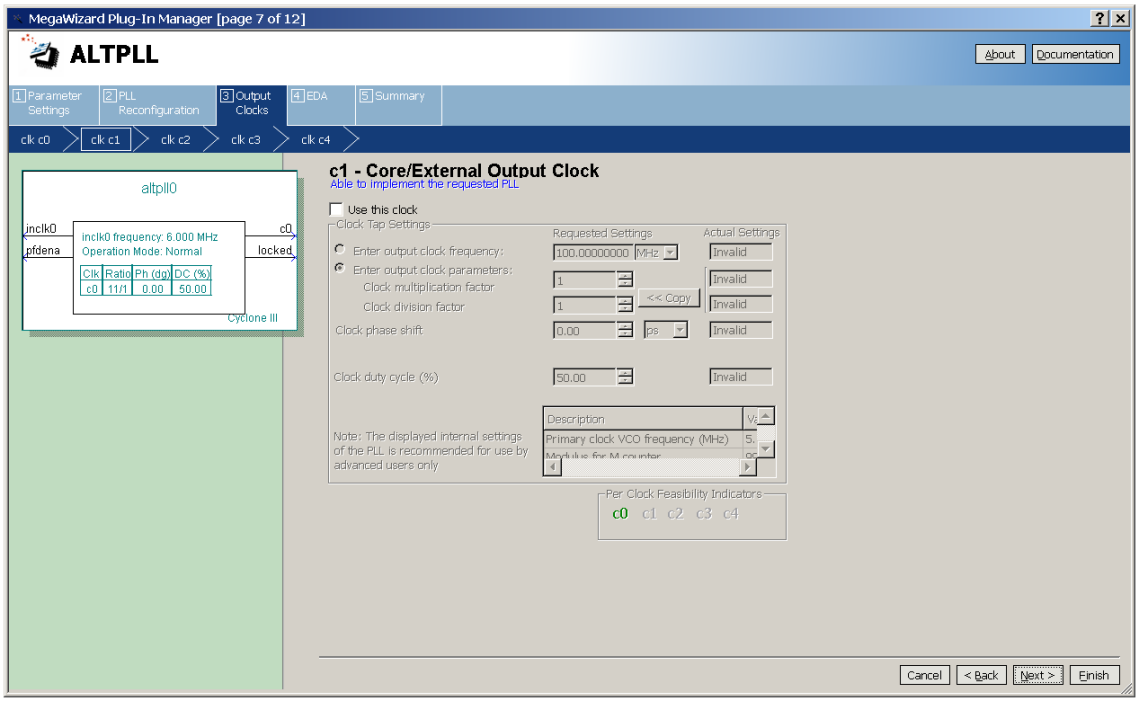
3 Output Clocks
4 EDA
5 Summary
clk c0
clk c1
clk c2
clk c3
clk c4
altpll0
inclk0
pfdena
inclk0 frequency: 6.000 MHz
Operation Mode: Normal
Clk Ratio Ph (dg) DC (%)
c0 11/1 0.00 50.00
c0
locked
Cyclone III
c0 - Core/External Output Clock
Able to implement the requested PLL
Use this clock
Clock Tap Settings
Requested Settings
Actual Settings
Enter output clock frequency:
100.00000000 MHz
66.000000
Enter output clock parameters:
Clock multiplication factor
11
11
Clock division factor
1
<< Copy
1
Clock phase shift
0.00
deg
0.00
Clock duty cycle (%)
50.00
50.00
Description
Primary clock VCO frequency (MHz)
Note: The displayed internal settings of the PLL is recommended for use by advanced users only
Per Clock Feasibility Indicators
c0 c1 c2 c3 c4
Cancel
< Back
Next >
Finish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1 Parameter Settings
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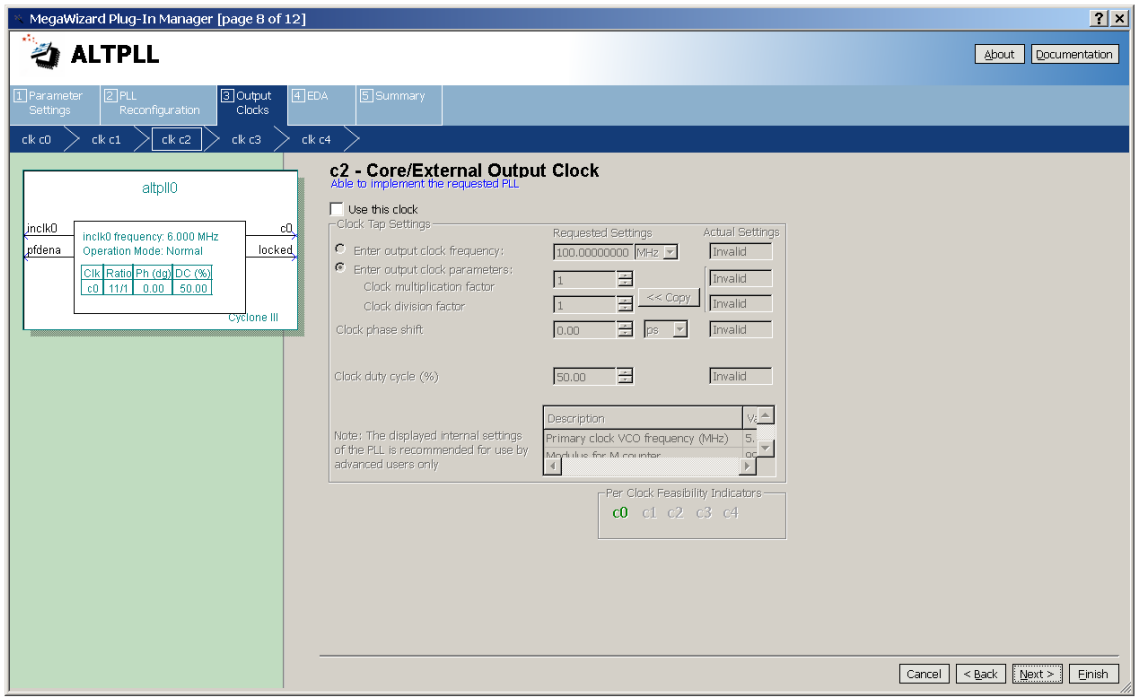
3 Output Clocks
4 EDA
5 Summary
clk c0
clk c1
clk c2
clk c3
clk c4
altpll0
inclk0
pfdena
c0
locked
inclk0 frequency: 6.000 MHz
Operation Mode: Normal
Clk
Ratio
Ph (dg)
DC (%)
c0
11/1
0.00
50.00
Cyclone III
c1 - Core/External Output Clock
Able to implement the requested PLL
Use this clock
Clock Tap Settings
Requested Settings
Actual Settings
Enter output clock frequency:
100.00000000
MHz
Invalid
Enter output clock parameters:
Clock multiplication factor
1
Clock division factor
<< Copy
Clock phase shift
ps
Clock duty cycle (%)
Description
Primary clock VCO frequency (MHz)
Note: The displayed internal settings of the PLL is recommended for use by advanced users only
Per Clock Feasibility Indicators
c0 c1 c2 c3 c4
Cancel
< Back
Next >
Finish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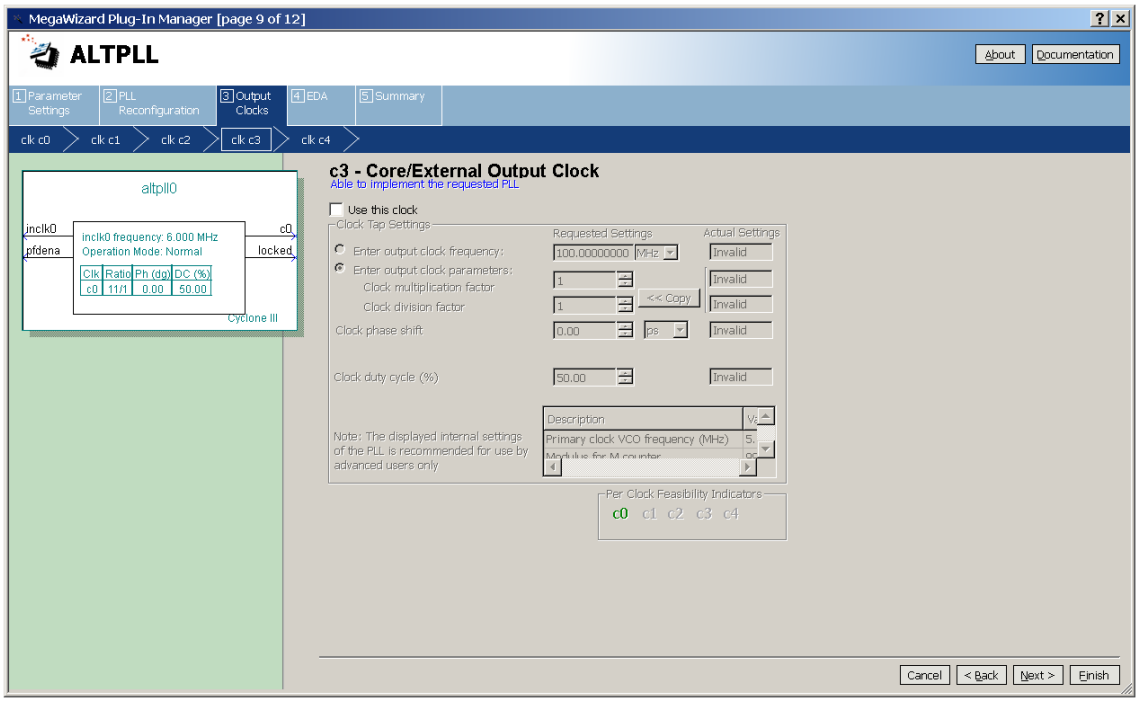
5 Summary
clk c0
clk c1
clk c2
clk c3
clk c4
altpll0
inclk0
pfdena
c0
locked
inclk0 frequency: 6.000 MHz
Operation Mode: Normal
Clk
Ratio
Ph (dg)
DC (%)
c0
11/1
0.00
50.00
Cyclone III
c2 - Core/External Output Clock
Able to implement the requested PLL
Use this clock
Clock Tap Settings
Requested Settings
Actual Settings
Enter output clock frequency:
100.00000000
MHz
Invalid
Enter output clock parameters:
Clock multiplication factor
1
Clock division factor
<< Copy
Clock phase shift
ps
Clock duty cycle (%)
Description
Primary clock VCO frequency (MHz)
Note: The displayed internal settings of the PLL is recommended for use by advanced users only
Per Clock Feasibility Indicators
c0 c1 c2 c3 c4
Cancel
< Back
Next >
Finish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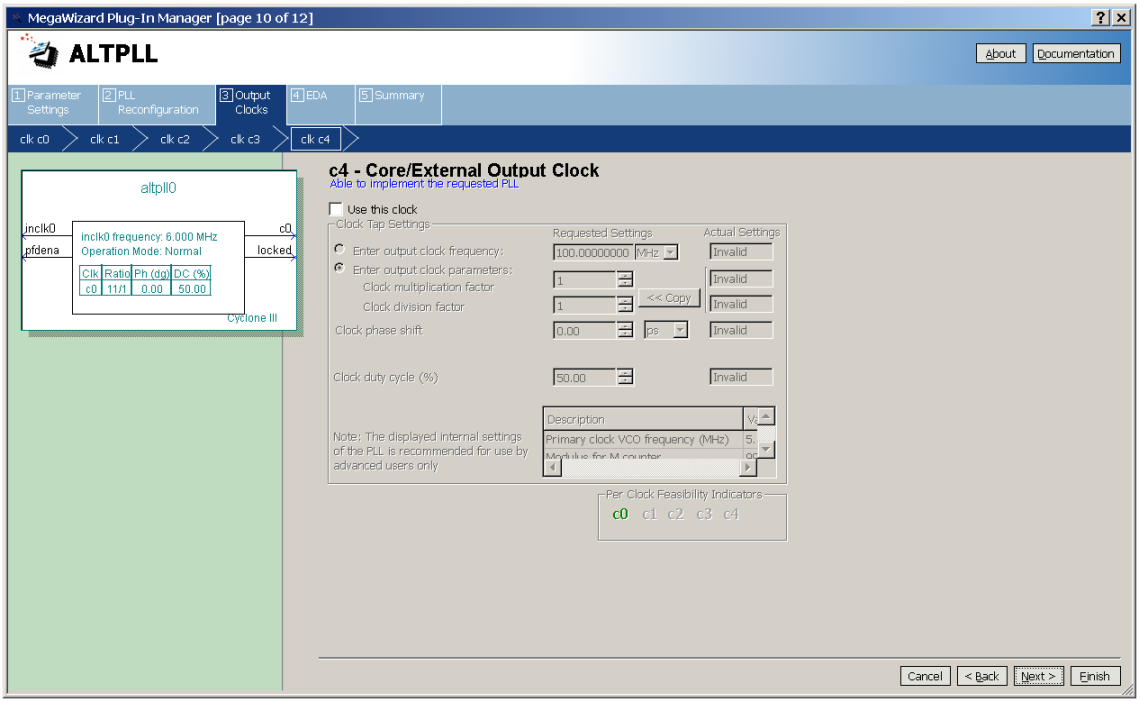
3 Output Clocks
4 EDA
5 Summary
clk c0
clk c1
clk c2
clk c3
clk c4
altpll0
inclk0
pfdena
c0
locked
inclk0 frequency: 6.000 MHz
Operation Mode: Normal
Clk
Ratio
Ph (dg)
DC (%)
c0
11/1
0.00
50.00
Cyclone III
c3 - Core/External Output Clock
Able to implement the requested PLL
Use this clock
Clock Tap Settings
Requested Settings
Actual Settings
Enter output clock frequency:
100.00000000
MHz
Invalid
Enter output clock parameters:
Clock multiplication factor
1
Clock division factor
<< Copy
Clock phase shift
0.00
ps
Clock duty cycle (%)
50.00
Description
Primary clock VCO frequency (MHz)
Note: The displayed internal settings of the PLL is recommended for use by advanced users only
Per Clock Feasibility Indicators
c0 c1 c2 c3 c4
Cancel
< Back
Next >
Finish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1 Parameter Settings
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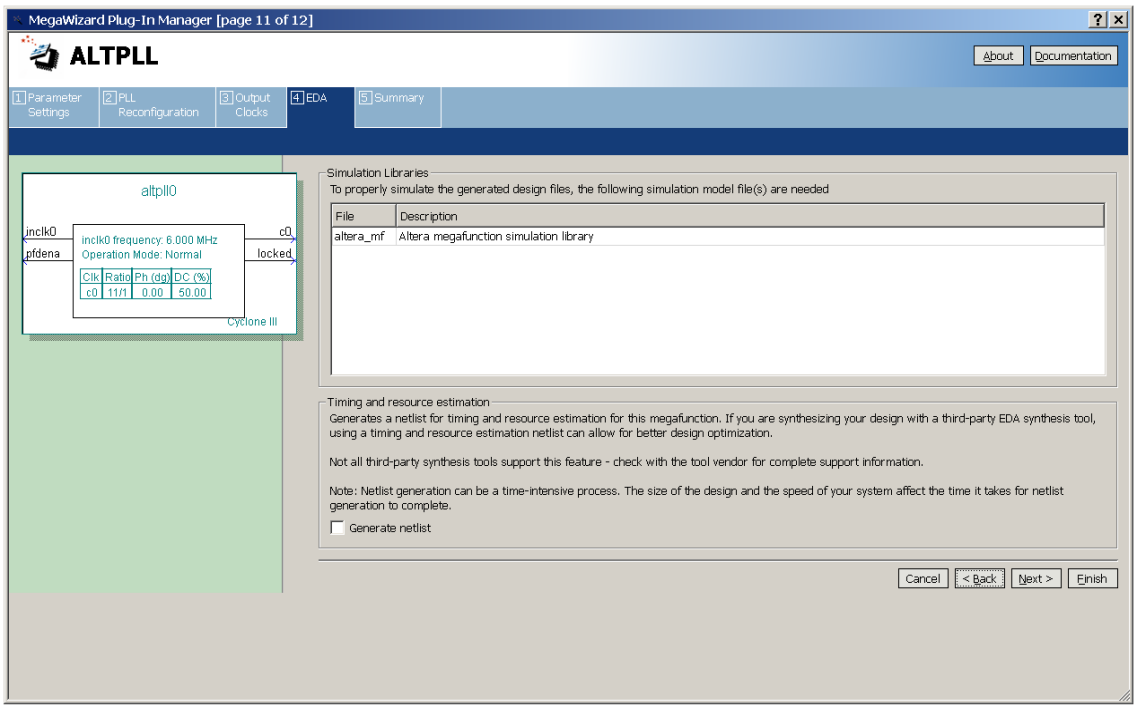
3 Output Clocks
4 EDA
5 Summary
clk c0
clk c1
clk c2
clk c3
clk c4
altpll0
inclk0
pfdena
c0
locked
inclk0 frequency: 6.000 MHz
Operation Mode: Normal
Clk
Ratio
Ph (dg)
DC (%)
c0
11/1
0.00
50.00
Cyclone III
c4 - Core/External Output Clock
Able to implement the requested PLL
Use this clock
Clock Tap Settings
Requested Settings
Actual Settings
Enter output clock frequency:
100.00000000
MHz
Invalid
Enter output clock parameters:
Clock multiplication factor
1
Clock division factor
<< Copy
Clock phase shift
0.00
ps
Clock duty cycle (%)
50.00
Description
Primary clock VCO frequency (MHz)
Note: The displayed internal settings of the PLL is recommended for use by advanced users only
Per Clock Feasibility Indicators
c0 c1 c2 c3 c4
Cancel
< Back
Next >
Finish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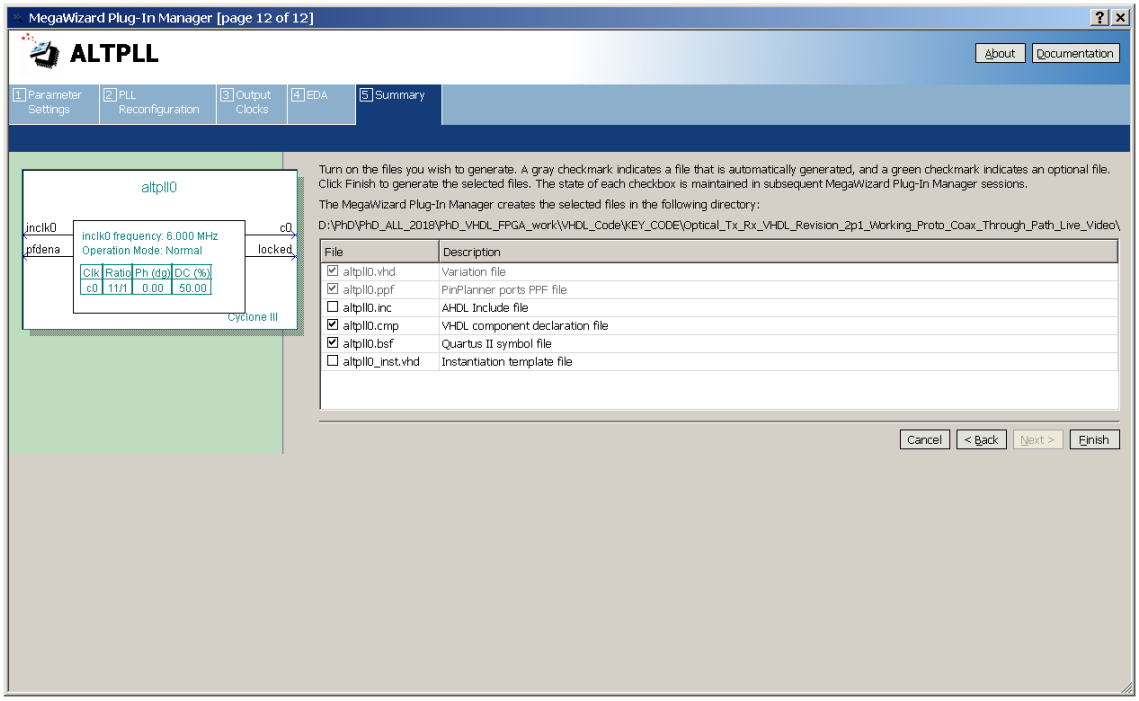
2 PLL Reconfiguration
3 Output Clocks
4 EDA
5 Summary
altpll0
inclk0
pfdena
c0
locked
inclk0 frequency: 6.000 MHz
Operation Mode: Normal
Clk | Ratio | Ph (dg) | DC (%)
c0 | 11/1 | 0.00 | 50.00
Cyclone III
Simulation Libraries
To properly simulate the generated design files, the following simulation model file(s) are needed
File | Description
altera_mf | Altera megafunction simulation library
Timing and resource estimation
Generates a netlist for timing and resource estimation for this megafunction. If you are synthesizing your design with a third-party EDA synthesis tool, using a timing and resource estimation netlist can allow for better design optimization.
Not all third-party synthesis tools support this feature - check with the tool vendor for complete support information.
Note: Netlist generation can be a time-intensive process. The size of the design and the speed of your system affect the time it takes for netlist generation to complete.
Generate netlist
Cancel
< Back
Next >
Finish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About
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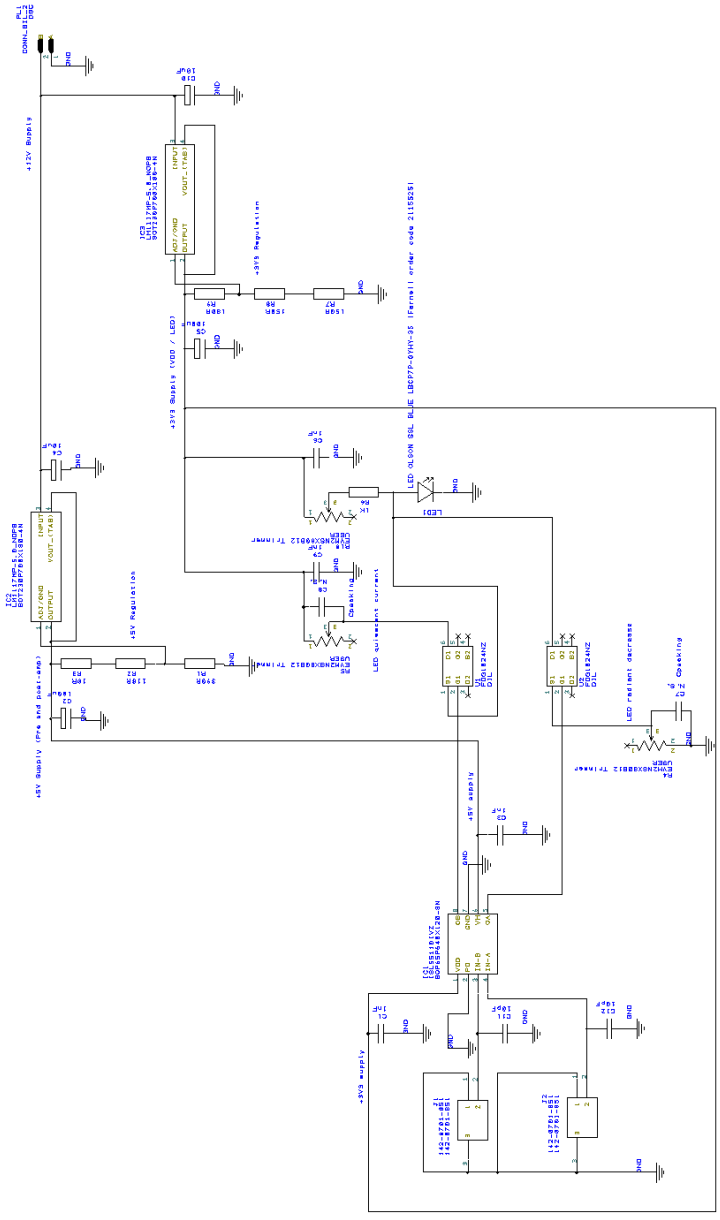
1 Parameter Settings
2 PLL Reconfiguration
3 Output Clocks
4 EDA
5 Summary
altpll0
inclk0
pfdena
c0
locked
inclk0 frequency: 6.000 MHz
Operation Mode: Normal
Clk | Ratio | Ph (dg) | DC (%)
c0 | 11/1 | 0.00 | 50.00
Cyclone III
Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.
The MegaWizard Plug-In Manager creates the selected files in the following directory:
D:\PhD\PhD_ALL_2018\PhD_VHDL_FPGA_work\VHDL_Code\KEY_CODE\Optical_Tx_Rx_VHDL_Revision_2p1_Working_Proto_Coax_Through_Path_Live_Video\
File | Description
altpll0.vhd | Variation file
altpll0.ppf | PinPlanner ports PPF file
altpll0.inc | AHDL Include file
altpll0.cmp | VHDL component declaration file
altpll0.bsf | Quartus II symbol file
altpll0_inst.vhd | Instantiation template file
Cancel
< Back
Next >
Finish

Appendix L System Schematics, BOMs and Layouts

L.1 LED intensity modulator (Tx) circuit

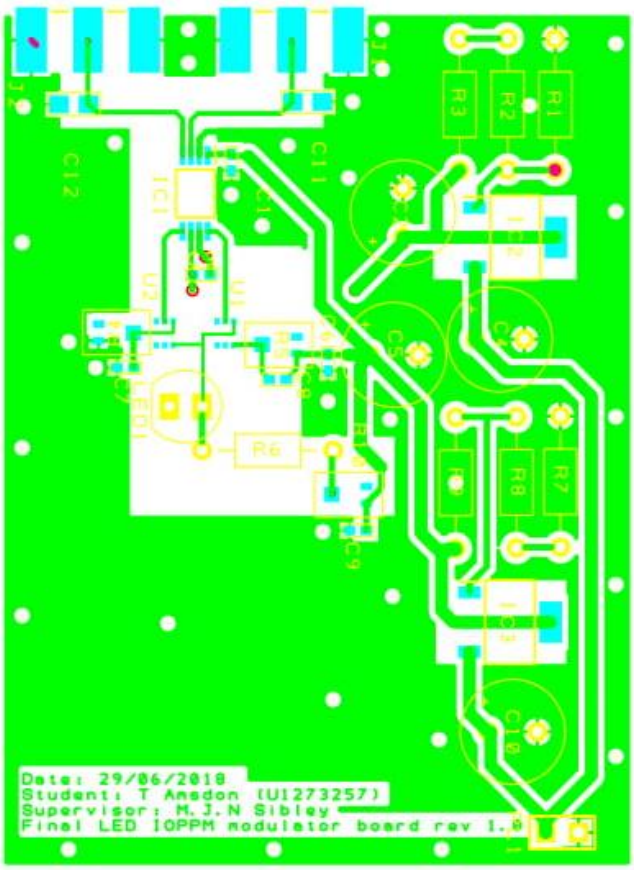
Schematic for the LED intensity modulator circuit. This circuit used the Osram Oslon LB CP7P-GYHY-35 SSL blue (470 nm) LED, the Intersil ISL55110/11 dual high speed MOSFET driver, and, the Fairchild Semiconductor FDG1024NZ dual N-channel PowerTrench® MOSFET.



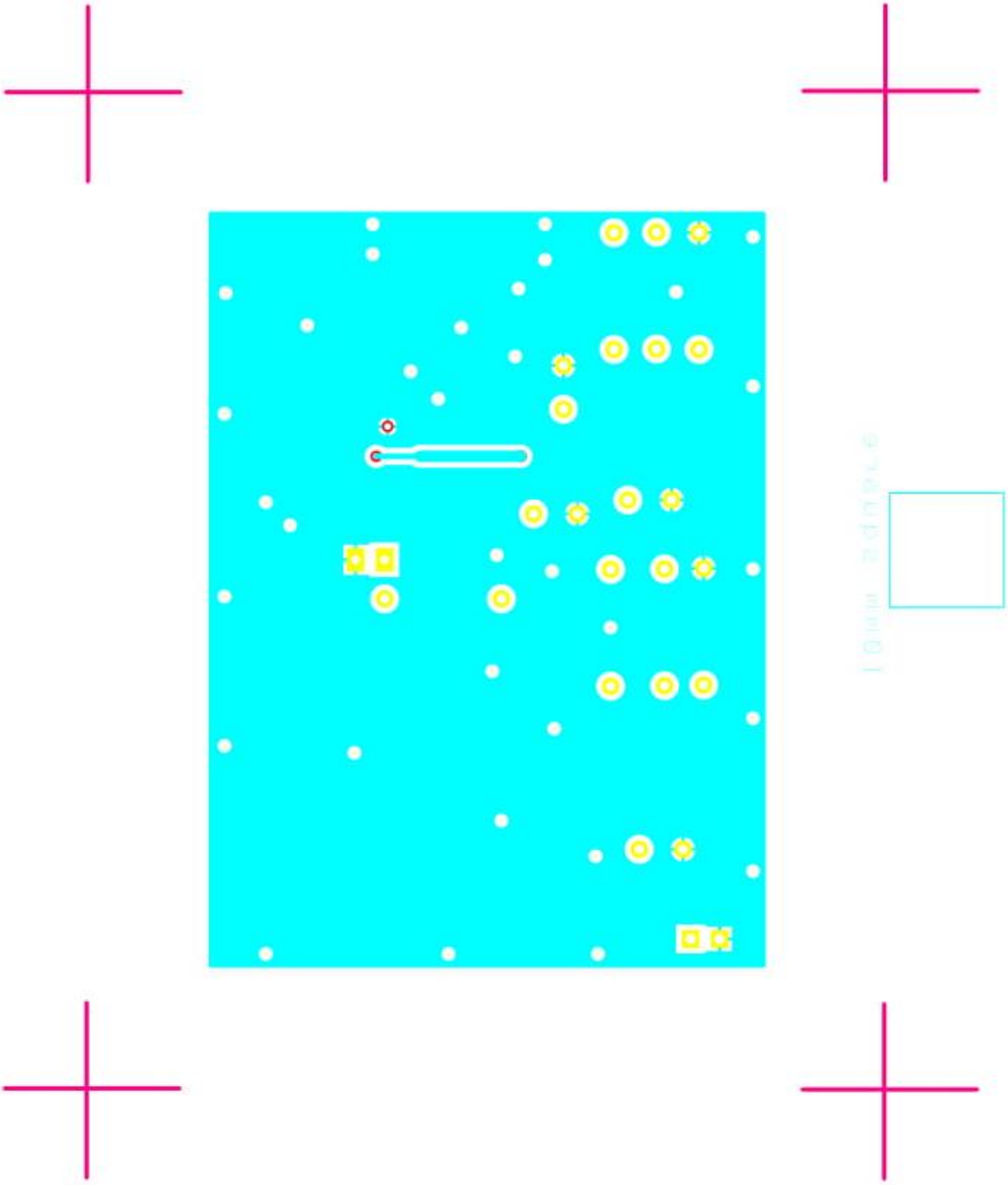
LED intensity modulator circuit. Bill of materials.

Reference Name	Qty	Component	Value	Package	Manufacturer	Manufacturer Part No.	Description
C1, C3, C6, C9	4	Capacitor	1nF	402			Capacitor, Ceramic
C2, C5	2	Capacitor Polarised	100uF	DSCV			Capacitor, Electrolytic
C4, C10	2	Capacitor Polarised	10uF	DSCV			Capacitor, Electrolytic
C7, C8	2	Capacitor	N.S.	402			Capacitor, Ceramic
C11, C12	2	Capacitor	10pF	402			Capacitor, Ceramic
IC1	1	ISL55110IVZ	N/A	SOP65P640X120-8N	Intersil	ISL55110IVZ	Intersil ISL55110IVZ, Dual MOSFET Power Driver, 3.5A, 5 12 V, Inverting, 8-Pin TSSOP
IC2, IC3	2	LM1117MP-5.0_NOPB	N/A	SOT230P700X180-4N	Texas Instruments	LM1117MP-5.0/NOPB	LM1117MP-5.0/NOPB, Low Dropout Voltage Regulator, 1.5A, 5 V 1%, 4-Pin SOT-223
J1, J2	2	SMA Connector	N/A	142-0701-851	Cinch Connectivity Solutions Johnson	142-0701-851	SMA 50 Ohm End Launch Jack Receptacle - Tab Contact
LED1	1	LED	N/A	N/A	OSRAM	LBCP7P-GYHY-35	High Brightness LED, OSLON SSL Series, Blue, 470 nm, 80 °, 28 lm, 1 A
PL1	1	CONN_SIL_2	N/A	DSC			2 way Pin Header
R1	1	Resistor	390R	DSC			Resistor
R2	1	Resistor	118R	DSC			Resistor
R3	1	Resistor	10R	DSC			Resistor
R4, R5, R10	3	Trimmer Potentiometer	100R	USER_DEFINED	Panasonic	EVM2NSX80B12	Trimmer Potentiometer, 100 Ohm, 1 Turns, Surface Mount Device, 150 mW, ± 25%
R6	1	Resistor	1K	DSC			Resistor
R7, R8	2	Resistor	150R	DSC			Resistor
R9	1	Resistor	180R	DSC			Resistor
U1, U2	2	FDG1024NZ	N/A	SC70-6	Fairchild Semiconductor	FDG1024NZ	Dual N-Channel, Power Trench MOSFET, 20 V, 1.2 A, 175 mOhm

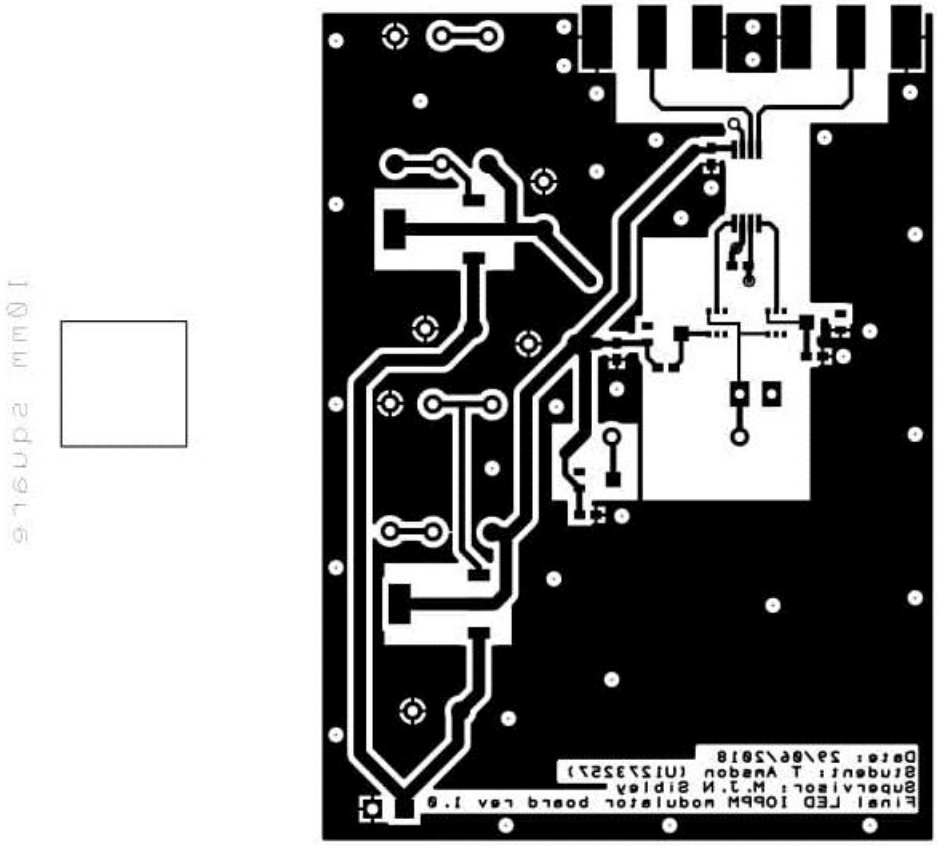
LED intensity modulator circuit. Top copper layout (not-to-scale).



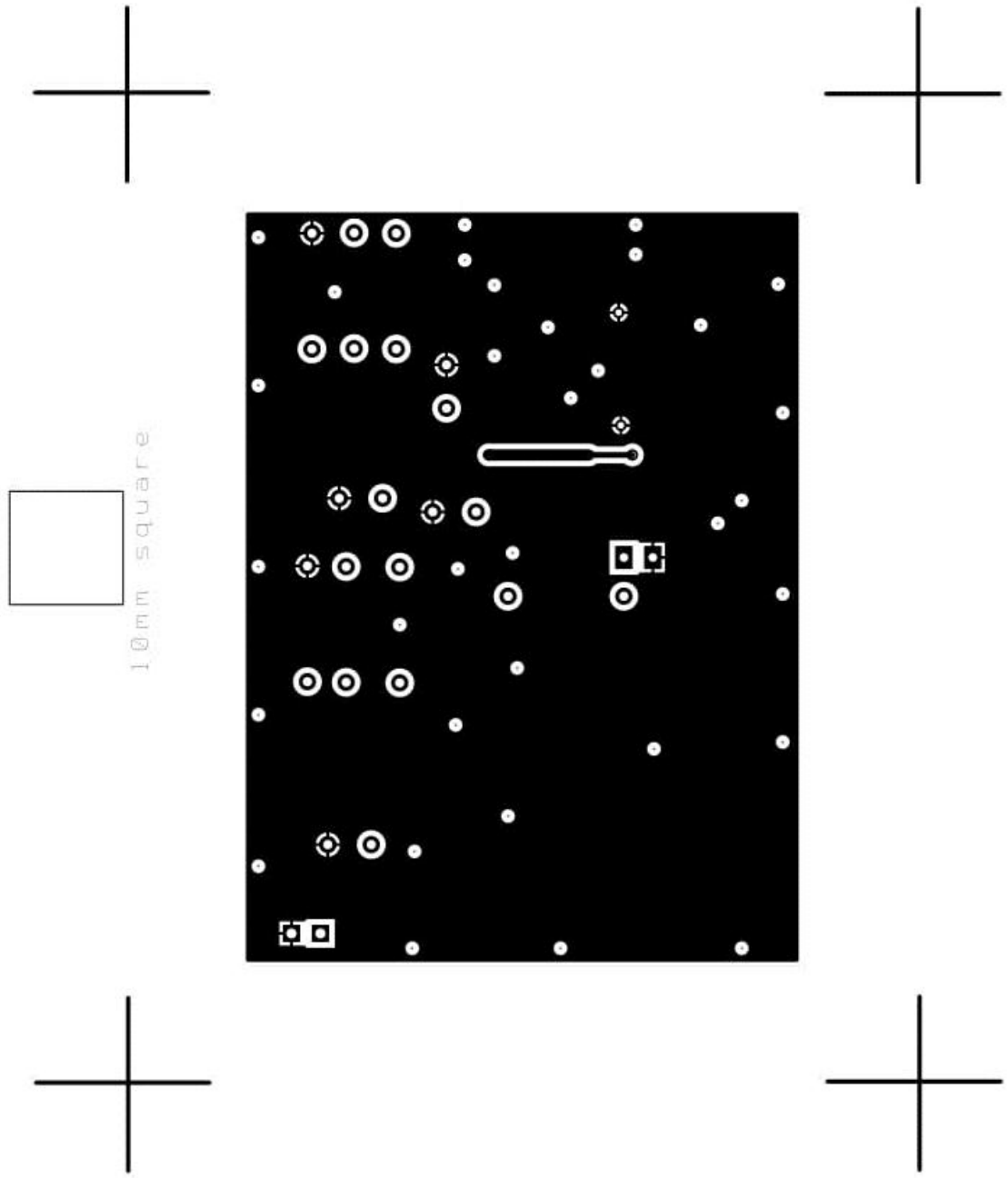
LED intensity modulator circuit. Bottom copper layout (not-to-scale).



LED intensity modulator circuit. Top copper layout (not-to-scale) mirrored.

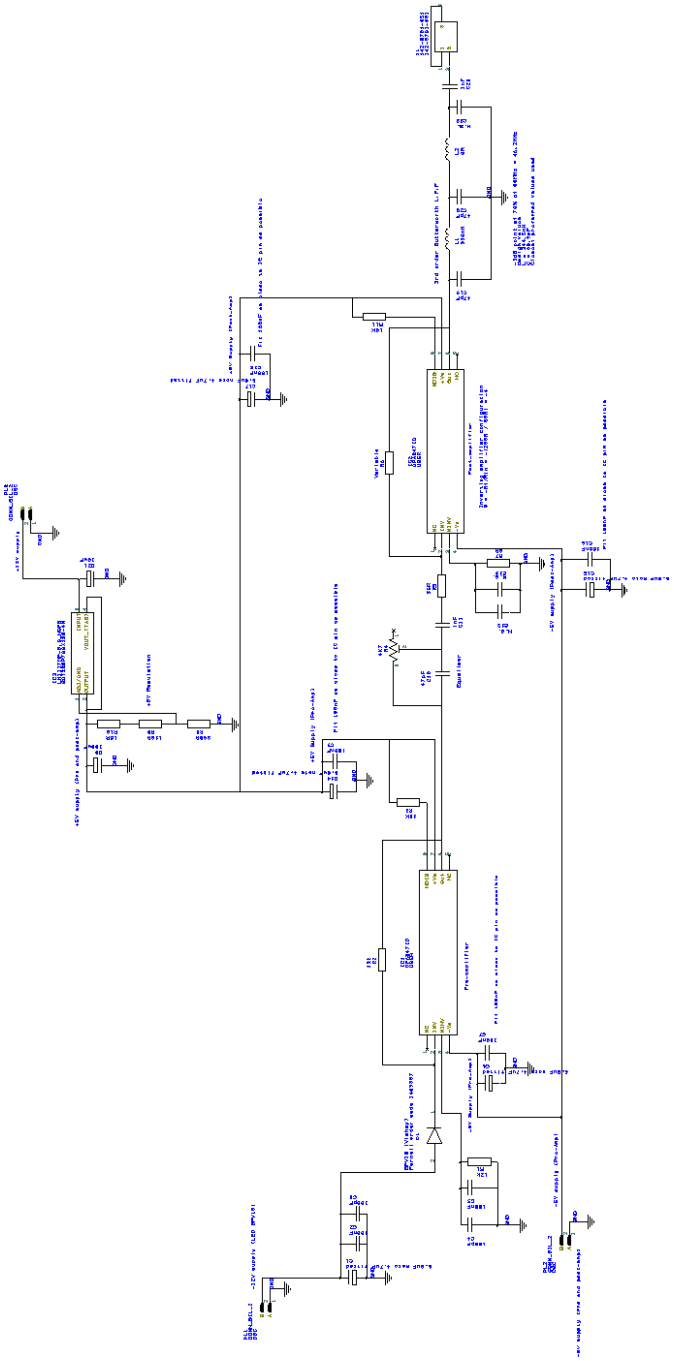


LED intensity modulator circuit. Bottom copper layout (not-to-scale) mirrored.



L.2 Pre and post-amplification circuit (Rx)

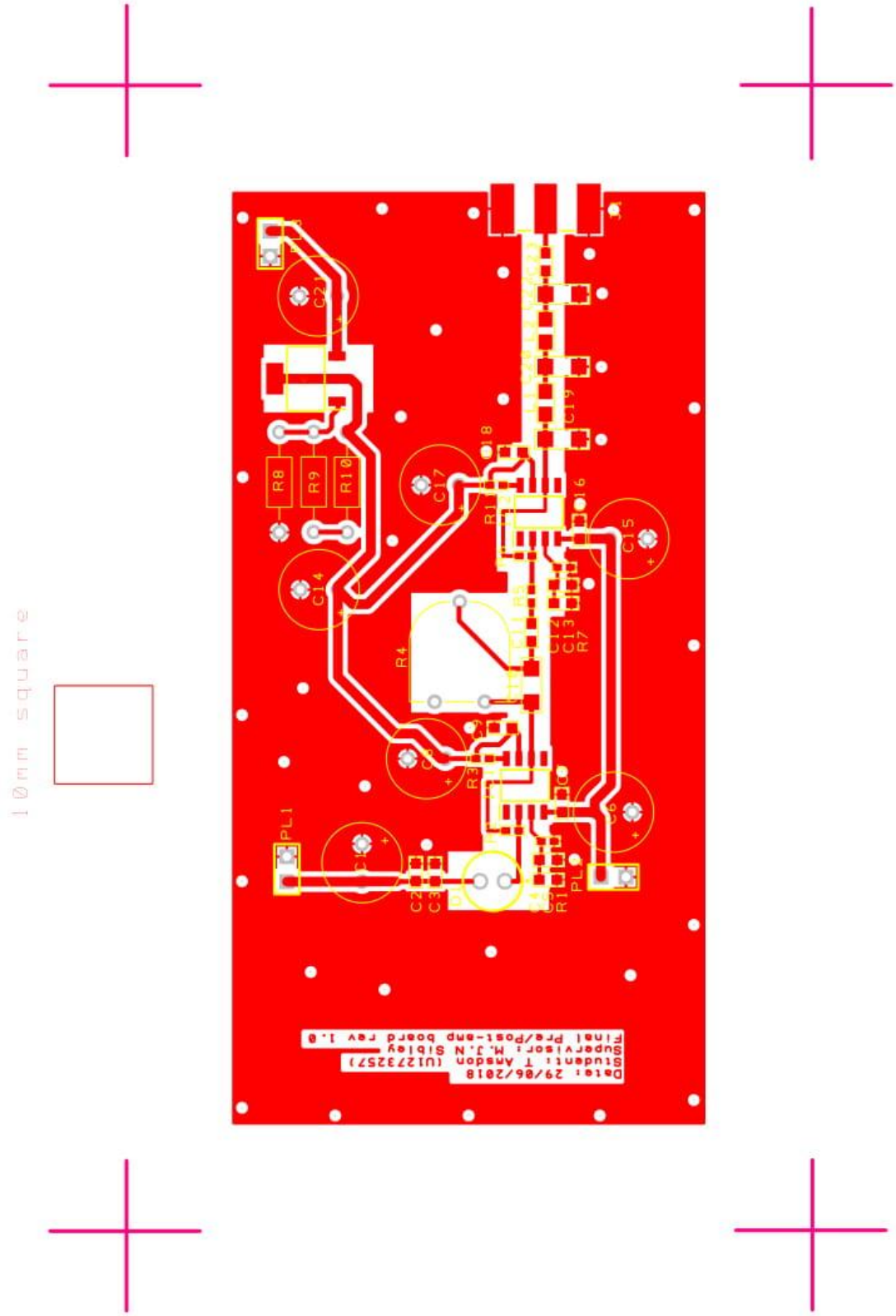
Schematic for the pre and post-amplification circuits of the system. Includes PD, pre-amplifier, passive equalisation, post-amplifier and Butterworth 3rd order LPF stages. This circuit used the Vishay Semiconductors BPV10 Silicon PIN PD, and the Texas Instruments OPA847 wideband ultra-low noise, voltage-feedback operational amplifier.



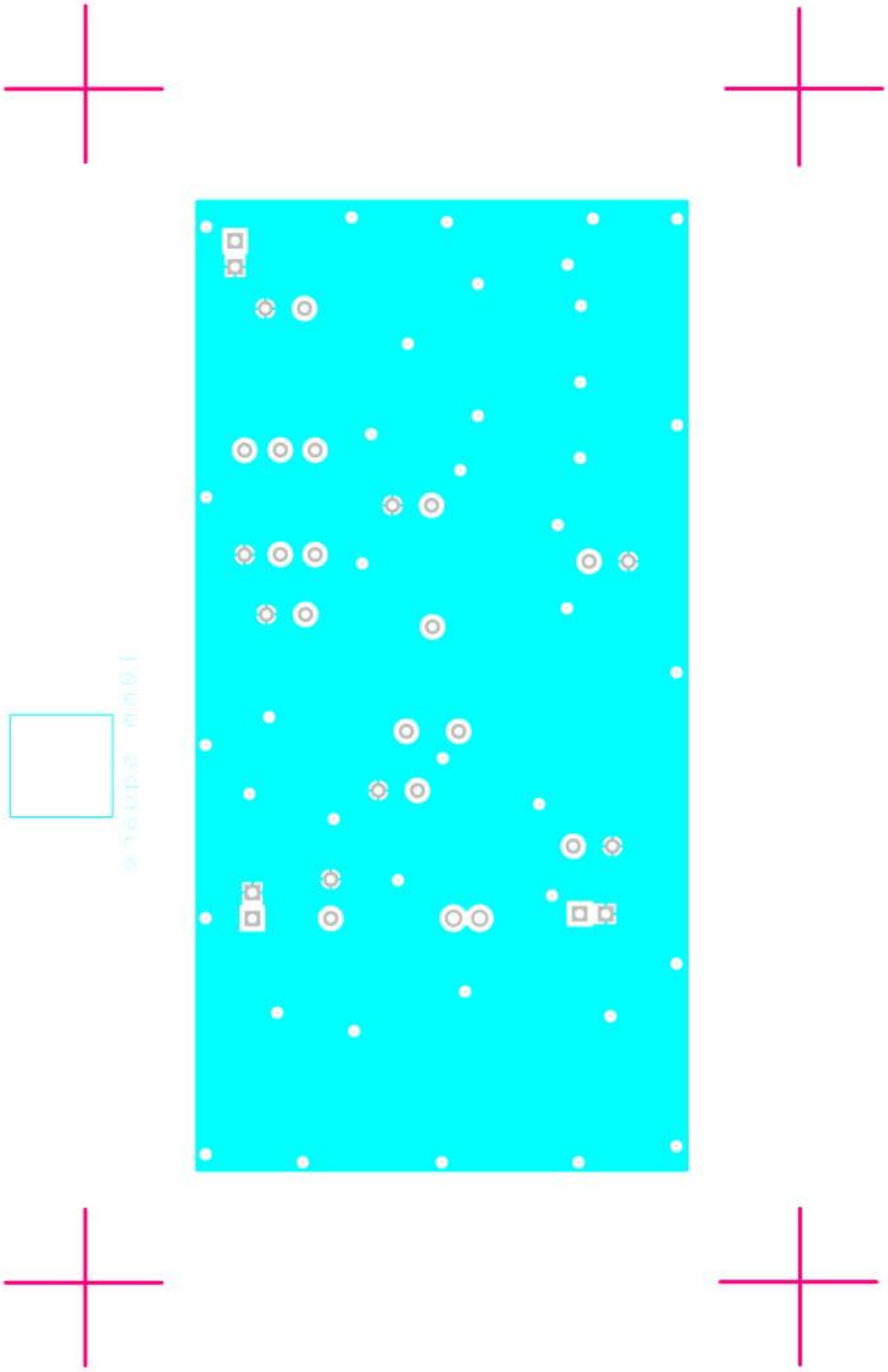
Pre and post-amplification circuits. Bill of materials.

Reference Name	Qty	Component	Value	Package	Manufacturer	Manufacturer Part No.	Description
C1, C6, C14, C15, C17	5	Capacitor Polarised	6.8uF note 4.7uF fitted	DSCV			Capacitor, Electrolytic
C2, C5, C7, C9, C16, C18	6	Capacitor	100nF	603			Capacitor, Ceramic
C3, C4	2	Capacitor	100pF	603			Capacitor, Ceramic
C8	1	Capacitor Polarised	100uF	DSCV			Capacitor, Electrolytic
C10, C19, C20	3	Capacitor	47pF	1206			Capacitor, Ceramic
C11, C23	2	Capacitor	1nF	603			Capacitor, Ceramic
C12, C13	2	Capacitor	N.S.	603			Capacitor
C21	1	Capacitor Polarised	10uF	DSCV			Capacitor, Electrolytic
C22	1	Capacitor	N.S.	1206			Capacitor
D1	1	Photodiode	N/A	N/A	OPTEK TECHNOLOGY	OP999	PIN Silicon photodiode
IC1, IC2	2	Op-Amp	N/A	SO-8	Texas Instruments	OPA847ID	Wideband, Ultra-Low Noise, Voltage-Feedback Op-Amp with Shutdown
IC3	1	LM1117MP-5.0_NOPB	N/A	SOT230P700X180-4N	Texas Instruments	LM1117MP-5.0/NOPB	LM1117MP-5.0/NOPB, Low Dropout Voltage Regulator, 1.5A, 5 V 1%, 4-Pin SOT-223
J1	1	142-0701-851		142-0701-851	Cinch Connectivity Solutions Johnson	142-0701-851	SMA 50 Ohm End Launch Jack Receptacle - Tab Contact
L1	1	Inductor	330nH	SM			Inductor
L2	1	Inductor	0R	SM			Inductor. 0R link fitted in place of inductor. Needed for through line.
PL1, PL3, PL2	3	CONN_SIL_2	N/A	DSC			2 way Pin Header
R1, R2	2	Resistor	12k	SM			Resistor
R3, R11	2	Resistor	10K	DSC			Resistor
R4	1	Preset	4K7	DSC			Preset Potentiometer
R5	1	Resistor	56R	SM			Resistor
R6	1	Resistor	Variable	DSC			Resistor Potentiometer
R7	1	Resistor	0R	SM			Resistor
R8	1	Resistor	390R	DSC			Resistor
R9	1	Resistor	118R	DSC			Resistor
R10	1	Resistor	10R	DSC			Resistor

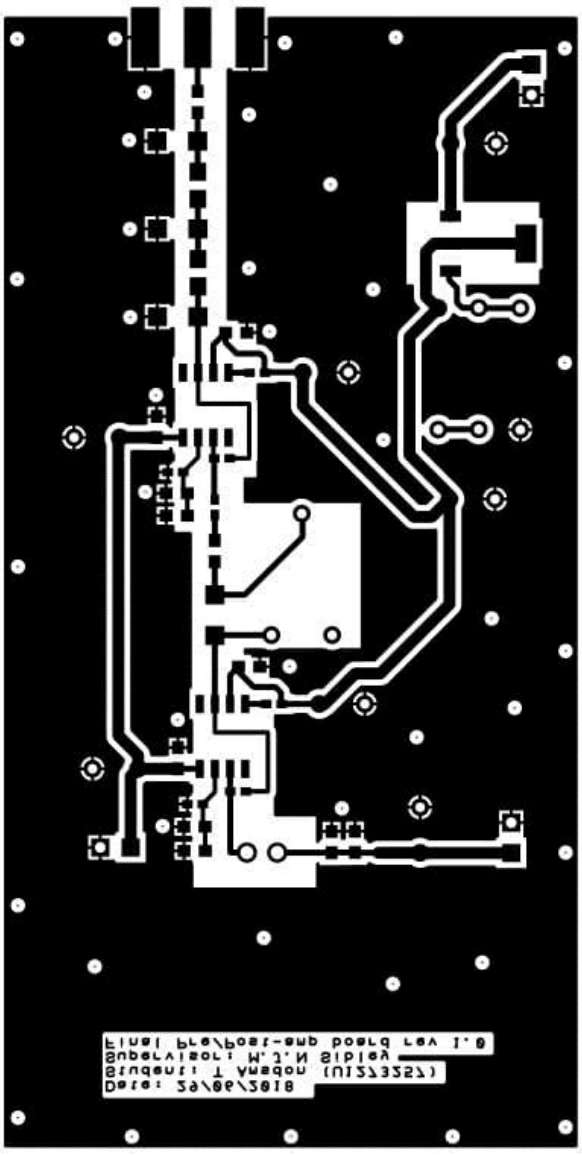
Pre and post-amplification circuits. Top copper layout (not-to-scale).



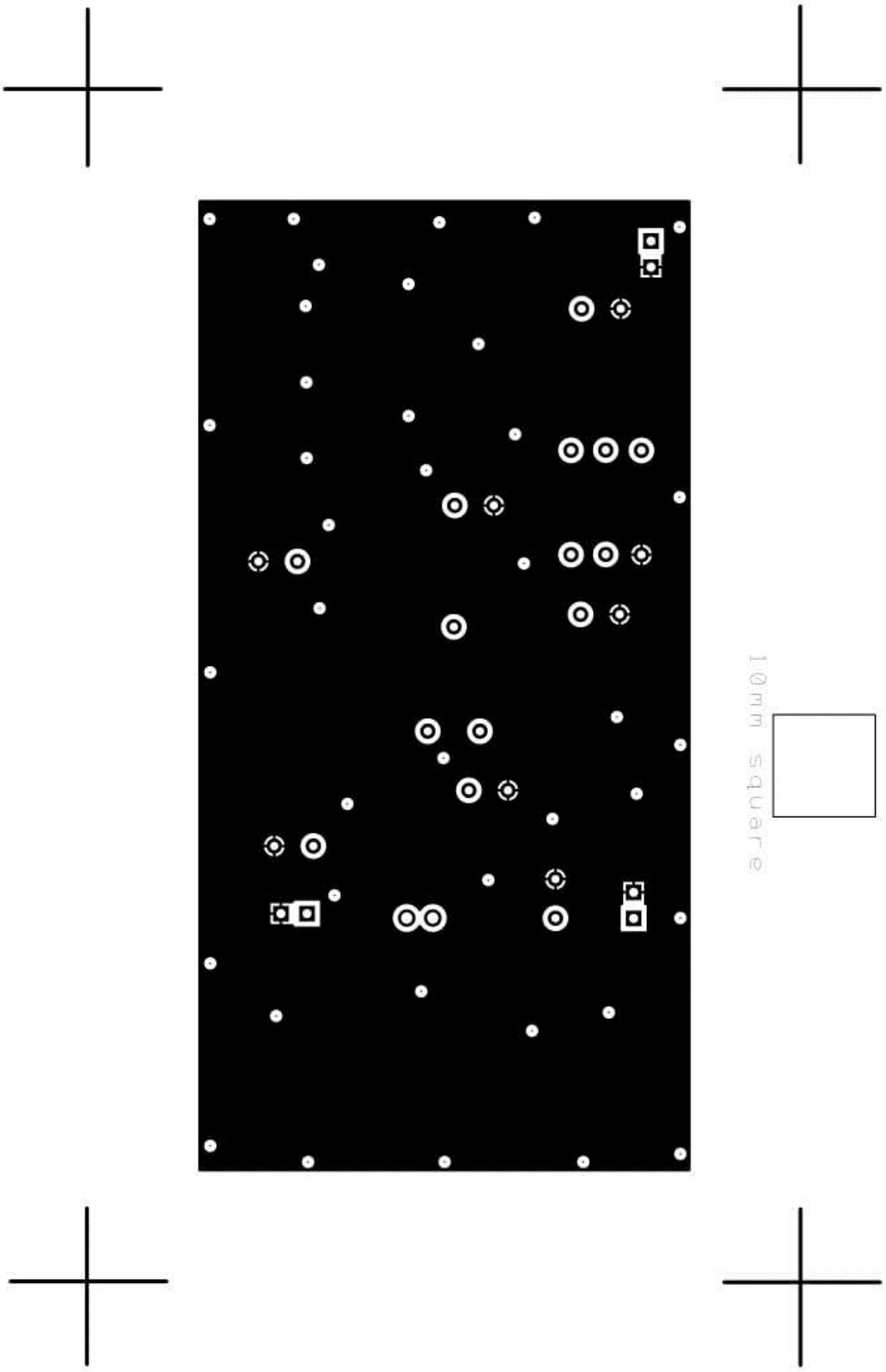
Pre and post-amplification circuits. Bottom copper layout (not-to-scale).



Pre and post-amplification circuits. Top copper layout (not-to-scale) mirrored.

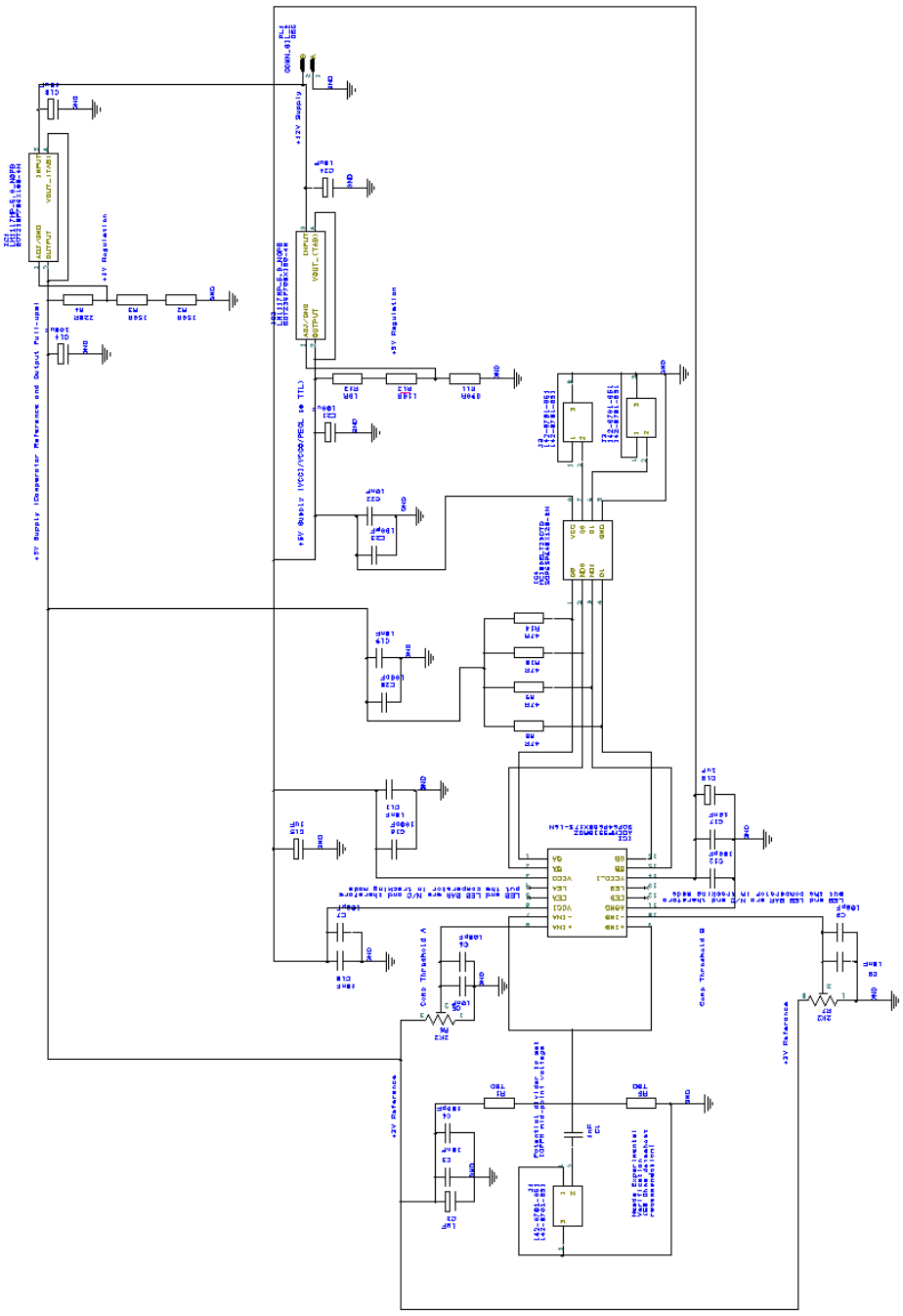


Pre and post-amplification circuits. Bottom copper layout (not-to-scale) mirrored.



L.3 Window Comparator circuit (Rx)

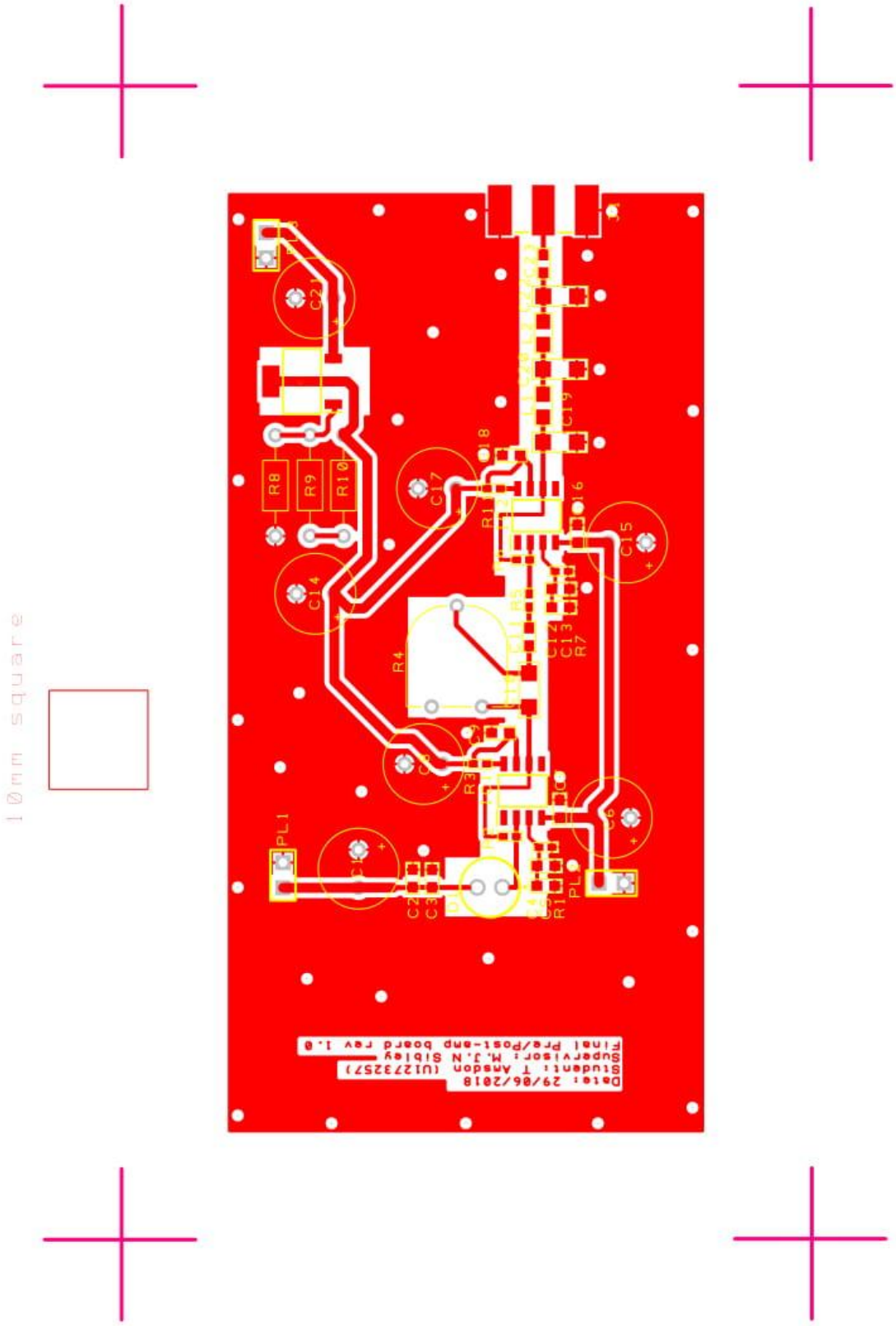
Schematic for the comparator circuit. This circuit used the Analog Devices ADCMP551 single-supply, high speed PECL/LVPECL comparator, and the ON Semiconductor MC100ELT23 5 V dual differential PECL to TTL translator.



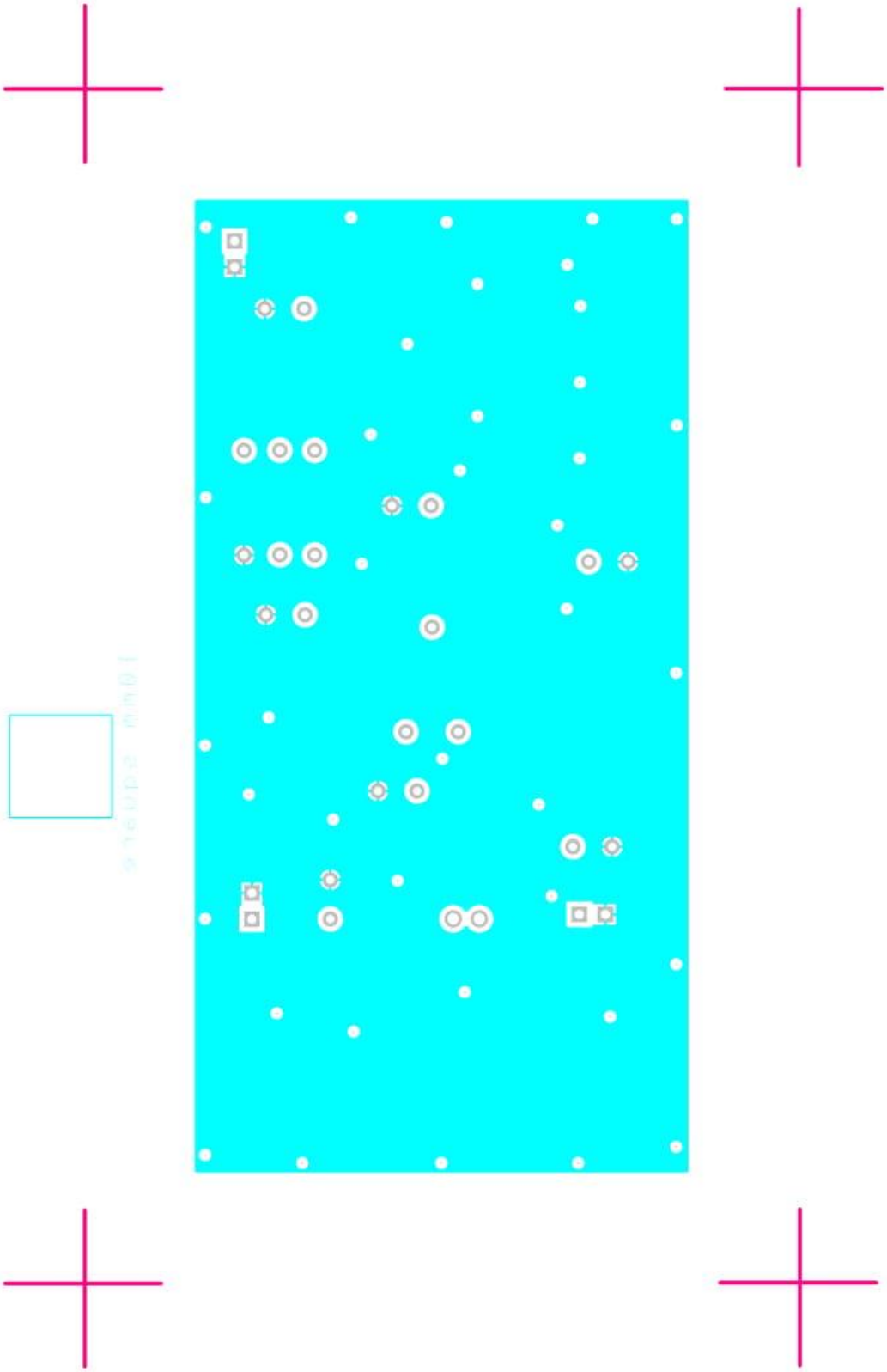
Comparator circuit. Bill of materials.

Reference Name	Qty	Component	Value	Package		Manufacturer	Manufacturer Part No.	Description
C1	1	Capacitor	1nF		603			Capacitor
C2, C15, C18	3	Capacitor Polarised	1uF	DSCV				Capacitor, Electrolytic
C3, C5, C8, C10, C11, C17, C19, C22	8	Capacitor	10nF		603			Capacitor, Ceramic
C4, C6, C7, C9, C12, C16, C20, C23	8	Capacitor	100pF		603			Capacitor, Ceramic
C13, C24	2	Capacitor Polarised	10uF	DSCV				Capacitor, Electrolytic
C14, C21	2	Capacitor Polarised	100uF	DSCV				Capacitor, Electrolytic
IC1, IC3	2	LM1117MP-5.0_NOPB		SOT230P700X180-4N		Texas Instruments	LM1117MP-5.0/NOPB	LM1117MP-5.0/NOPB, Low Dropout Voltage Regulator, 1.5A, 5 V 1%, 4-Pin SOT-223
IC2	1	ADCMP551BRQZ		SOP64P600X175-16N		Analog Devices	ADCMP551BRQZ	ADCMP551BRQZ, Comparator Complementary 3.3 V 16-Pin QSOP
IC4	1	MC100ELT23DTG		TSSOP-8, DT SUFFIX, CASE 948R		ON Semiconductor	MC100ELT23DTG	5 V Dual Differential PECL to TTL Translator
J1, J2, J3	3	142-0701-851		142-0701-851		Cinch Connectivity Solutions Johnson	142-0701-851	SMA 50 Ohm End Launch Jack Receptacle - Tab Contact
PL1	1	CONN_SIL_2		DSC				2 way Pin Header
R1, R5	2	Resistor	560R		402			Resistor
R2, R3	2	Resistor	150R	DSC				Resistor
R4	1	Resistor	220R	DSC				Resistor
R6, R7	2	Preset	2K2	DSC				Preset Potentiometer
R8, R9, R10, R14	4	Resistor	47R	DSC				Resistor
R11	1	Resistor	390R	DSC				Resistor
R12	1	Resistor	118R	DSC				Resistor
R13	1	Resistor	10R	DSC				Resistor

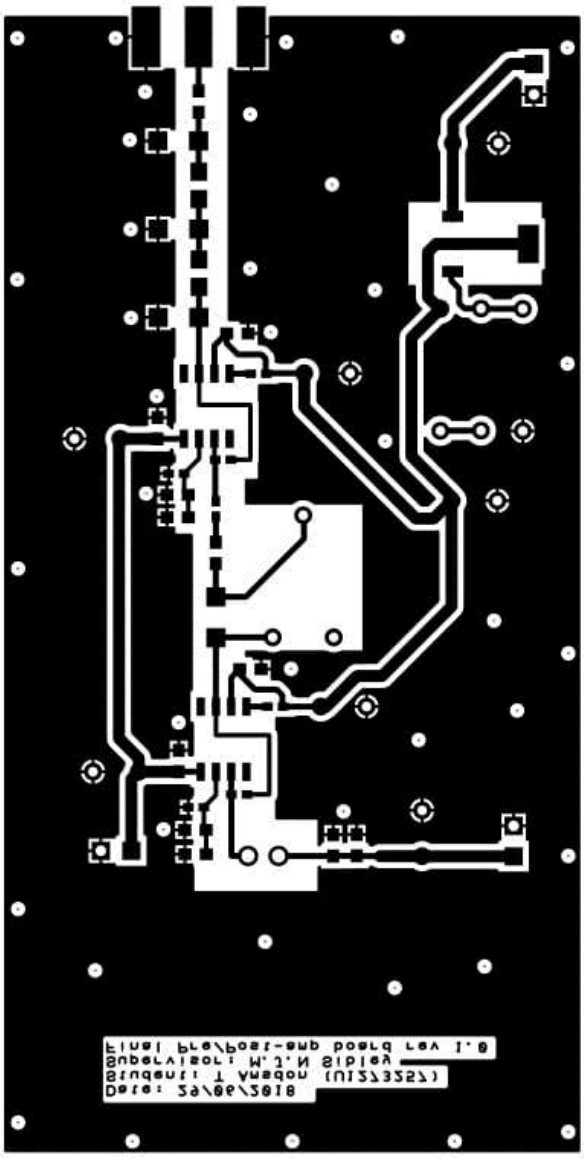
Comparator circuit. Top copper layout (not-to-scale).



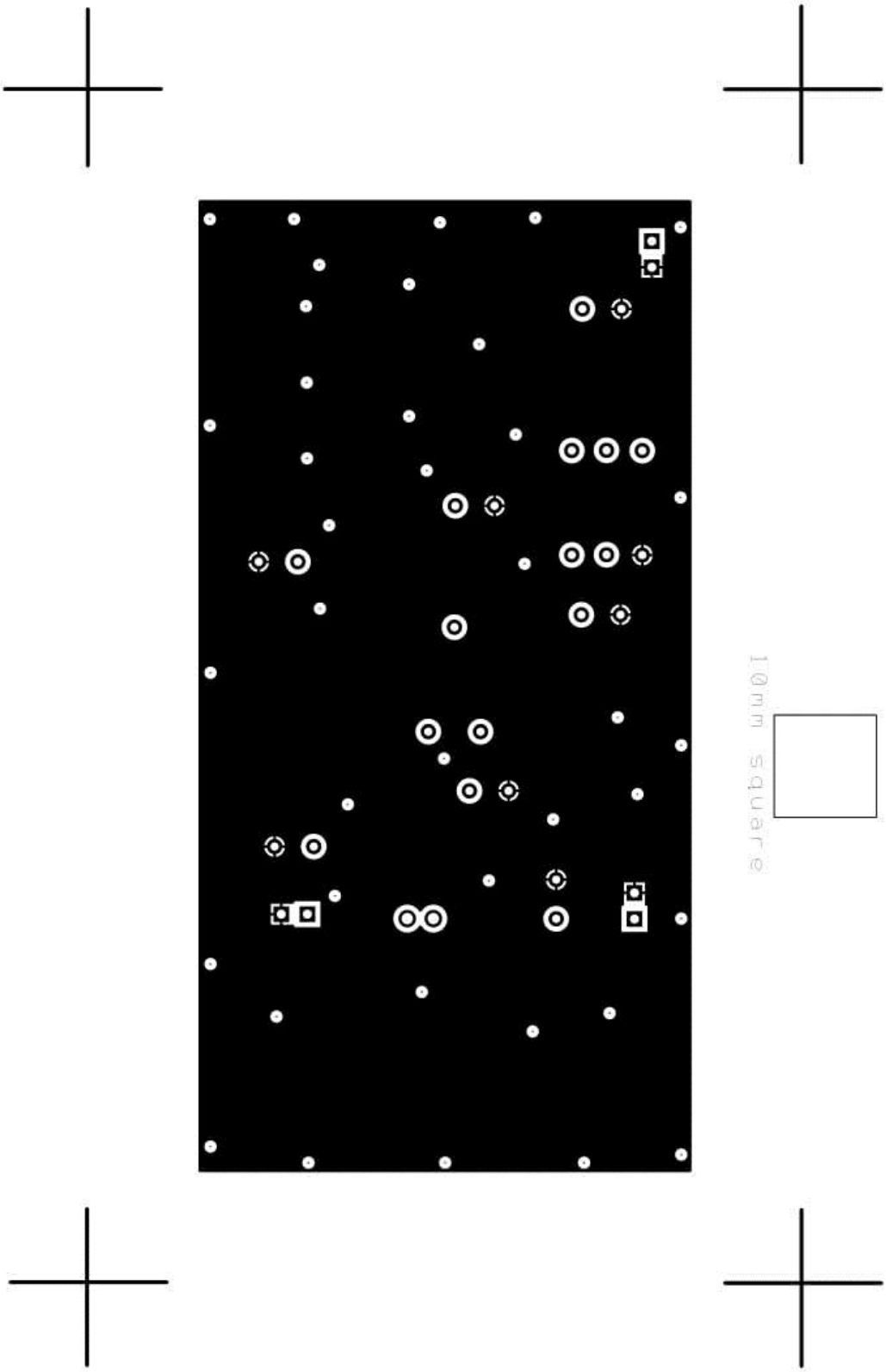
Comparator circuit. Bottom copper layout (not-to-scale).



Comparator circuit. Top copper layout (not-to-scale) mirrored.

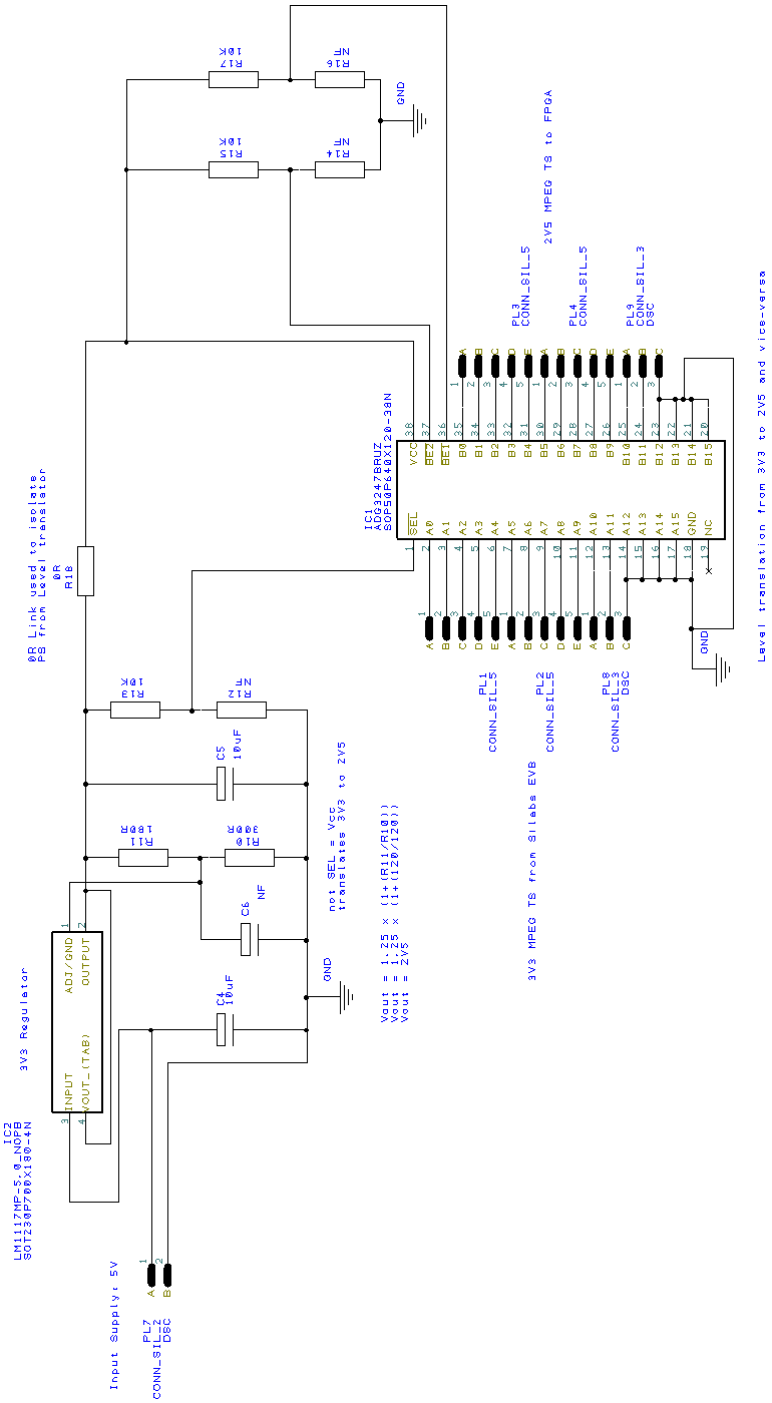


Comparator circuit. Bottom copper layout (not-to-scale) mirrored.



L.4 Si2168-B40 to FPGA TTL level translator

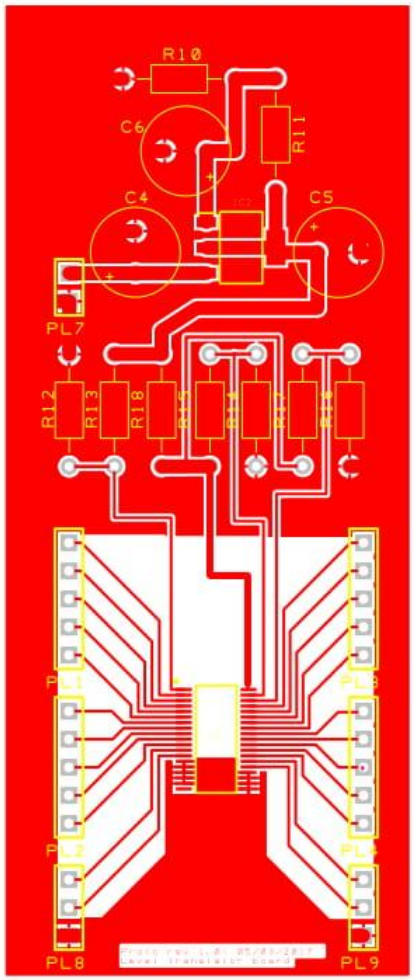
Schematic for the Si2168-B40 to FPGA TTL level translator. This circuit used the Analog Devices ADG3247 2.5 V/3.3 V, 16-bit, 2-port level translating, bus switch to perform TTL level shifting between platforms.



Si2168-B40 to FPGA TTL level translator. Bill of materials.

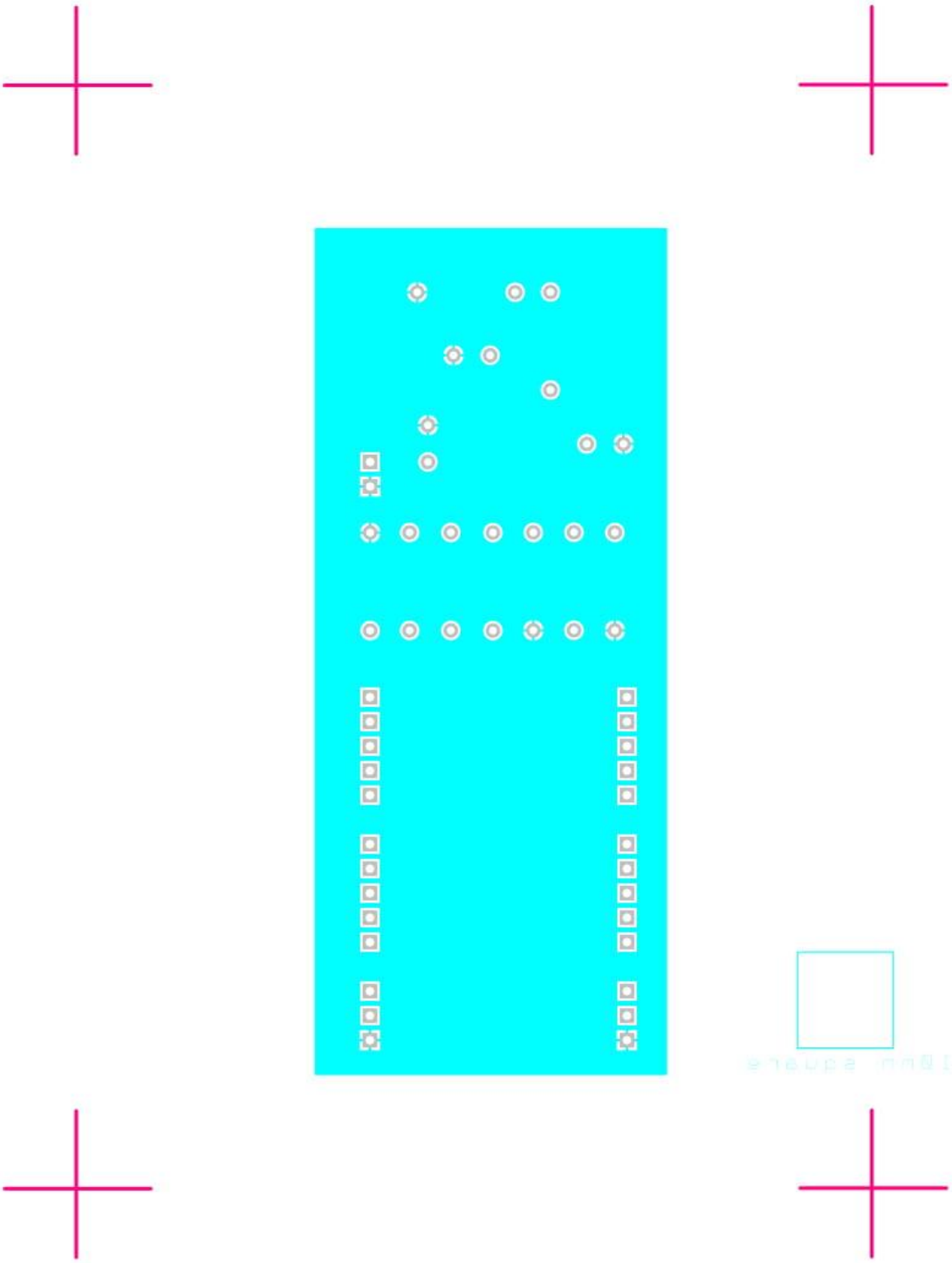
Reference Name	Qty	Component	Value	Package	Manufacturer	Manufacturer Part No.	Description
C4, C5	2	Capacitor Polerised	10uF	DSCV			Capacitor, Electrolytic
C6	1	Capacitor Polerised	N.S.	DSCV			Capacitor, Electrolytic
IC1	1	ADG3247BRUZ		SOP50P640X120-38N	Analog Devices	ADG3247BRUZ	ADG3247BRUZ, Bus Switch 8 x 1:1, 2.3 to 3.6V 38-Pin TSSOP
IC2	1	LM1117MP-5.0_NOPB		SOT230P700X180-4N	Texas Instruments	LM1117MP-5.0/NOPB	LM1117MP-5.0/NOPB, Low Dropout Voltage Regulator, 1.5A, 5 V 1%, 4-Pin SOT-223
PL1, PL2, PL3, PL4	4	CONN_SIL_5		DSC			5 way Pin Header
PL7	1	CONN_SIL_2		DSC			2 way Pin Header
PL8, PL9	2	CONN_SIL_3		DSC			3 way Pin Header
R10, R11	2	Resistor	120R	DSC			Resistor
R12, R14, R16	3	Resistor	N.S.	DSC			Resistor
R13, R15, R17	3	Resistor	10K	DSC			Resistor
R18	1	Resistor	0R	DSC			Resistor

Si2168-B40 to FPGA TTL level translator. Top copper layout (not-to-scale).

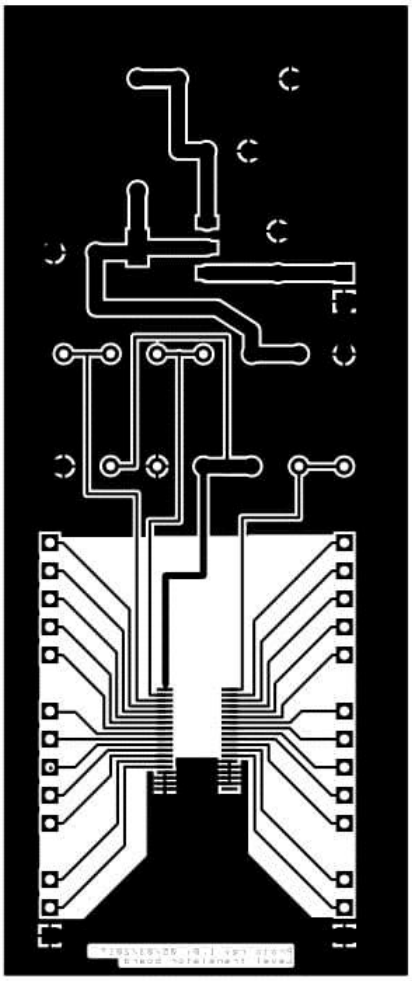


10mm square

Si2168-B40 to FPGA TTL level translator. Bottom copper layout (not-to-scale).



Si2168-B40 to FPGA TTL level translator. Top copper layout (not-to-scale) mirrored.



Si2168-B40 to FPGA TTL level translator. Bottom copper layout (not-to-scale) mirrored.