IMPLEMENTATION OF

OFFSET PULSE POSITION MODULATION

FAAIZ HADI MAHMOOD

A thesis submitted to The University of Huddersfield

in partial fulfilment of the requirements for

the degree of Doctor of Philosophy

The University of Huddersfield

February 2017

Copyright Statement

Acknowledgment

All thanks and praises are due to Almighty God for granting me the wisdom, health and strength to undertake this research task and enabling me to its completion.

The work presented in this thesis would not have been possible without my close association with many people. I take this opportunity to extend my sincere gratitude and appreciation to all those who made this Ph.D. thesis possible.

First and foremost, I would like to extend my sincere gratitude to my research supervisor Dr. Martin Sibley for introducing me to this exciting field of science and for him dedicated help, advice, inspiration, encouragement and continuous support, throughout my Ph.D.

Special thanks are also given to Dr. Peter Mather, whose enthusiasm and technical guidance have been greatly appreciated, his encouragement and help made me feel confident with during my PhD course. Through his depth of knowledge and enthusiasm, he such as a spot light inspiration and enlightened my way in this project whenever I needed to help me whether in theoretical or practical investigation during this project.

I would like to express my special appreciation and thanks to present and past members of the School Research & Administration Office staff: Cathie Raw, Gwen Wood, Chris Sentence, Nicola Williams, Belinda Perfitt, and Liz Rees.

Nobody has been more important to me in the pursuit of this project than my parents. Words cannot express how grateful I am to my Mum, Dad, whose love and guidance are with me in whatever I pursue. They are the ultimate role models.

A special thanks to my younger sisters Dr. Ban, and Dr. Aseel, have all extended their support in a very special way, and I gained a lot from them, through their personal and scholarly interactions, their suggestions at various points of my research.

A special thanks to my brothers and sisters. Words cannot express how grateful I am to them. Your prayer for me was what sustained me thus far.

Most importantly, I Wish to thank my loving and supportive wife, Sarah, and my two wonderful children, Yusur, and Abdulhadi, Who provide unending inspiration.

Dr. Mothana Amaar Hassan was kind enough to undertake the editing work and I acknowledge the meticulous work he has done. Mothana, had finely sketched out the map of the study area, and I thank and appreciate his efforts.

I am grateful to Dr. Basman Monther Al-Nedawe for sharing his knowledge that influenced the

work.

Abstract

Optical fibre systems have played a key role in making possible the extraordinary growth in world-wide communications that has occurred in the last 25 years, and are vital in enabling the proliferating use of the Internet. Its high bandwidth capabilities, low attenuation characteristics, low cost, and immunity from the many disturbances that can afflict electrical wires and wireless communication links make it ideal for gigabit transmission and a major building block in the telecommunication infrastructure.

The main concern of this thesis is a full and detailed investigation and implementation of the Offset Pulse Position Modulation (Offset PPM) communication system. Novel work is carried out for applying Offset PPM over an optical communication channel theoretically and experimentally to examine the system performance.

An Offset PPM encoder and decoder were implemented to code Pulse Code Modulation (PCM) format into Offset PPM format and to decode back the Offset PPM to PCM. The first paradigm of implementation was implemented using electronic components.

A further investigation took place on the Offset PPM associated output. Computer programming and simulation using the VHSIC Hardware Description Language (VHDL) of this PPM code was considered and comparison with previous theoretical results presented. The received Offset PPM signal returned back to its original input PCM form without errors.

Successful VHDL and Field Programmable Gate Array (FPGA) implementation using Altera Quartus II of Offset PPM encoder and decoder as a single system has been presented in the study. An FPGA embedded Bit Error Rate (BER) test device has also been implemented for sensitivity measurements purposes and all the designs have been tested successfully with back-to-back testing. Results show that Offset PPM is an advantageous PPM code for optic communication. Furthermore, the system has achieved a very high data rate of 50 Mb/s without an optical communication set.

An optical communication system (transmitter/receiver) over POF was developed and the Offset PPM scheme was investigated through this optical channel. Results show that the Offset PPM sequence transferred through the optic system without being altered. In addition, this implementation is optimised PPM coding; the system is working perfectly with up to 10 Mb/s with 10^{-12} BER based on the limitations of the optical communication set.

All the results and analyses indicate that Offset PPM is an ideal alternative to be considered for highly dispersive optical channels, and performance evaluation for higher bandwidths also favourably compares to existing coding schemes.

List of Contents

Abstract ..... **III**

List of Contents ..... **V**

List of Figures ..... **IX**

List of Tables ..... **XIII**

List of Abbreviations ..... **XIV**

1 Introduction **1**

1.1 Optical Communication Background 1

1.2 Features of Fibre Optic Communication Systems 4

1.2.1 Advantages 4

1.2.2 Disadvantages 6

1.3 Aims and Objectives 8

1.4 Contributions 9

1.5 Organization of the Thesis 10

2 Literature Review **12**

2.1 Introduction 12

2.2 Coding Schemes in Optical Fibre Communication System 12

2.3 Timing Extraction and Synchronisation 25

2.3.1 Phase Locked Loops (PLL) 27

2.4 Digital Communication Errors and Error Correction 29

2.4.1 Maximum Likelihood Sequence Detection (MLSD) 30

2.5 Non-Return-To-Zero and Return-To-Zero Formats 32

2.6 (FPGA) and Microcontroller Comparison 33

2.7 VHSIC Hardware Description Language (VHDL) 35

2.8 Summary 36

3 Optoelectronics of Optical Fibre Communication System **37**

3.1 Introduction 37

3.2 Optical Transmitter 37

3.2.1 Optical Source 38

3.2.2 Laser Diodes 39

3.2.3 Light Emitting Diodes 39
3.3 Optical Receiver 40
3.3.1 Common Types of Photodetector 41
3.4 Photo Amplifier 41
3.5 Optical Fibre 42
3.5.1 Types of Optical Fibre 43
3.5.2 Plastic Optic Fibre 45
3.5.3 Glass Optic Fibre 46
3.6 Summary 47

4 Offset PPM Theory 48
4.1 Introduction 48
4.2 Coding Scheme 50
4.3 Errors affect Offset PPM 50
4.3.1 Wrong slot errors 51
4.3.2 Erasure errors 51
4.3.3 False Alarm Errors 52
4.4 Summary 52

5 Offset PPM Encoder and Decoder Design, Implementation and Testing 53
5.1 Introduction 53
5.2 Parallel Offset PPM Encoder Design and Implementation 53
5.2.1 Offset PPM Encoder Design 53
5.2.2 Offset PPM Encoder Hardware Implementation 57
5.2.3 Encoder Hardware Implementation 57
5.2.4 Offset PPM Encoder FPGA Implementation 58
5.3 Parallel Offset PPM Decoder Design and Implementation 59
5.3.1 Offset PPM Decoder Design 59
5.3.2 Offset PPM Decoder Hardware Implementation 64
5.3.3 Offset PPM Decoder Hardware Implementation 65
5.3.4 Decoder FPGA Implementation 65
5.4 Summary 66

6 VHDL Source Code, Simulation, and Implementation of Offset PPM 67
6.1 Introduction 67

6.2 VHDL and FPGA 67
6.2.1 VHDL 67
6.2.2 Field Programmable Gate Arrays (FPGA) 70
6.3 Cyclone III Development Board 70
6.3.1 SMA Breakout Cables 71
6.4 System Schematic 73
6.5 Offset PPM system Components 74
6.5.1 Phase-locked Loop (PLL) Clock 74
6.5.2 Pseudo Random Binary Sequence (PRBS) 76
6.5.3 Parallel Offset PPM Encoder 77
6.5.4 Parallel Offset PPM decoder 78
6.5.5 Parallel Input Serial Output (PISO) 79
6.5.6 Serial Input Parallel Output (SIPO) 80
6.6 Parallel Offset PPM coding System Implementation 80
6.7 Serial Offset PPM Coding System Implementation 82
6.8 Summary 91

7 Optical Offset PPM Communication System 92
7.1 Introduction 92
7.2 Serial Set Offset PPM coding system with Optical Components and External PRBS 94
7.3 Experiment Hardware and Software Resources 94
7.3.1 FPGA & VHDL 94
7.3.2 Optical Fibre Communication System Components 94
7.3.2.1 Optical Transmitter 94
7.3.2.2 Optical Receiver 97
7.3.2.3 Plastic Optical Fibre (POF) 99
7.3.3 Voltage Comparator 100
7.3.4 PRBS Generator 103
7.4 Implementation of Offset PPM System 104
7.4.1 Simulation Results 107
7.4.2 Real Time Results 109
7.5 Digital Transmission Measurements and Analysis 112
7.6 Summary 116

8 Conclusions and future work 117
8.1 Conclusions 117
8.2 Future Work 118
9 Appendixes 120
9.1 VHDL codes 120
9.2 Optical transmitter/receiver data sheet 128
9.3 POF data sheet 140
9.4 Comparator data sheet 150
10 References 164

List of Figures

Figure 1-1 Schematic diagram of general communication system 2

Figure 1-2 Schematic diagram of a fibre-optic system 3

Figure 1-3 Typical digital fibre-optic link 4

Figure 2-1 Pulse Position Modulation (Liu, 2002) 15

Figure 2-2 Conversion of PCM to Multiple PPM double pulses per frame 16

Figure 2-3 Conversions of PCM data into DPPM (Middle trace) and DiPPM 18

Figure 2-4 Conversion of PCM data (top trace) into dicode (Middle trace) 19

Figure 2-5 Conversion of OOK data (top trace) into DuoPPM (bottom trace) 20

Figure 2-6 PAM (A), PFM (B), PPM (C) and PDM (D) 21

Figure 2-7 Pulse Code Modulation 22

Figure 2-8 Simplified block diagram of a digital receiver 28

Figure 2-9 Generation of different types of error considering Gaussian type pulse shape 31

Figure 2-10 Shown how (a) erasures and (b) false alarms affect the decoding of offset PPM 32

Figure 2-11 (a) NRZ and (b) RZ bit patterns corresponding to the bit sequence 10101101 33

Figure 3-1 Possible applications of optical amplifiers 42

Figure 3-2 Optical fibre cable structure 43

Figure 3-3 Multimode fibre light propagation 44

Figure 3-4 Single mode fibre light propagation 44

Figure 3-5 Multimode and singlemode fibres layout 45

Figure 4-1 Offset PPM coder and transmitter system (M. J. Sibley, 2011) 49

Figure 4-2 Schematic of an optical receiver system (M. J. Sibley, 2011) 49

Figure 5-1 Karnaugh map application for pin (D) 55

Figure 5-2 Karnaugh map application for pin (E) 55

Figure 5-3 Karnaugh map application for pin (F) 56
Figure 5-4 Karnaugh map application for pin (G) 56
Figure 5-5 Offset PPM encoder Schematic 57
Figure 5-6 Offset PPM encoder implementation using a Limrose board 58
Figure 5-7 FPGA hardware implementation for the Offset PPM encoder 59
Figure 5-8 Karnaugh map for pin A 61
Figure 5-9 Karnaugh map for pin B 62
Figure 5-10 Karnaugh map for pin C 63
Figure 5-11 Offset PPM decoder schematic 64
Figure 5-12 Offset PPM decoder implementation using a Limrose board 65
Figure 5-13 FPGA implementation for the Offset PPM decoder 66
Figure 6-1 VHDL Implementation flow chart 68
Figure 6-2 Offset PPM VHDL code sequence 69
Figure 6-3 Cyclone III FPGA 71
Figure 6-4 MC Connectors (Altera, 2015) 72
Figure 6-5 SMA Breakout Cable 73
Figure 6-6 Block Diagram of Parallel Offset PPM coding 73
Figure 6-7 Block Diagram of First version of serial Offset PPM coding schematic 74
Figure 6-8 Block Diagram of Serial Offset PPM 74
Figure 6-9 Offset PPM PLL design for clocking requirements 75
Figure 6-10 PLL clock generation simulation result 75
Figure 6-11 Main section of the PRBS generator VHDL code 76
Figure 6-12 PRBS data generation in VHDL 76
Figure 6-13 Main section Parallel Offset PPM Encoder VHDL source code 77
Figure 6-14 Offset PPM encoder VHDL simulation results 78

Figure 6-15 Parallel Offset PPM decoder VHDL code 78
Figure 6-16 Offset PPM decoder VHDL simulation results 79
Figure 6-17 PISO top block view 79
Figure 6-18 SIPO top block view 80
Figure 6-19 Parallel Offset PPM 81
Figure 6-20 Real time waveform parallel Offset PPM 82
Figure 6-21 Serial Offset PPM system layout 83
Figure 6-22 Offset PPM system without optical fibre links 83
Figure 6-23 First version serial Offset PPM 85
Figure 6-24 Serial Offset PPM schematic diagram 86
Figure 6-25 Serial Offset PPM simulation 88
Figure 6-26 Real time waveform serial Offset PPM 90
Figure 6-27 PRBS output (top trace), Offset PPM decoder (bottom trace) 91
Figure 7-1 Frame work of the full Offset communication system 92
Figure 7-2 Frame work of the full Offset communication system with external PRBS 93
Figure 7-3 Test bench setup 93
Figure 7-4 Optical transmitter layouts (Appendix 9.2) 96
Figure 7-5 Optical Transmitter Circuit 96
Figure 7-6 Optical transmitter part 96
Figure 7-7 Optical receiver layouts 98
Figure 7-8 Power supply Circuit for Optical Receive (Appendix 9.2) 99
Figure 7-9 Optical receiver part 99
Figure 7-10 HFBR-R optical fibre (Appendix 9.3) 100
Figure 7-11 Voltage comparator circuit (Appendix 9.4) 102
Figure 7-12 MAX941 Pin configuration 102

Figure 7-13 Voltage comparator part 102
Figure 7-14 Voltage comparator Input/Output 103
Figure 7-15 Hewlett-Packard HP 3780A PRBS generator 104
Figure 7-16 Optical Offset PPM system design using Altera Quartus II v. 9.1 software 106
Figure 7-17 Offset PPM system simulation results 108
Figure 7-18 External PRBS output waveform and Offset PPM decoder output 110
Figure 7-19 PRBS waveform output and Offset PPM Decoder output 111
Figure 7-20 Minimum BER recorded 113
Figure 7-21 Digital transmission measurements and analysis based on FPGA 114
Figure 7-22 Real time waveform output error and clock counters 115

List of Tables

Table 2.1 DiPPM Symbol Alphabet 19

Table 2.2 Generation of different types of coding from equivalent 3 bits of data 25

Table 3.1 Typical specifications of plastic optical fibre used in communication applications 46

Table 4.1 Generating the offset pulse, the sign bit in offset PPM is shown in italics 49

Table 5.1 Truth table of Offset PPM encoder 54

Table 5.2 Truth table for the Offset PPM Decoder 60

List of Abbreviations

ADC	Analogue to Digital Converter
ADM	Adaptive-Delta Modulation
ADPLL	All Digital Phase Looked Loop
BER	Bit Error Rate
CCD	Charge Coupled Detectors
CCPPM	Colour Coded PPM
CDR	Clock and Data Recovery
CPLD	Complex Programmable Logic Device
CVSDM	Continuously Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
DCM	Digital Clock Managers
DiPPM	Dicode Pulse Position Modulation
DPLL	Digital Phase Looked Loop
DPPM	Digital Pulse Position Modulation
DuoPPM	Duobinary Pulse Position Modulation
EM	Electromagnetic
FPGA	Field Programmable Gate Array
GaAsP	Gallium Arsenide Phosphide
GaP	Gallium Phosphide
GHz	Giga Hertz
I/O	Input/output
IEEE	Institute of Electrical and Electronics Engineers
IFI	Inter-frame Interference

ISI	Inter-Symbol Interference
Km	Kilometre
LD	Laser Diode
LED	Light Emitting Diode
LSI	Large-Scale Integrate
MHz	Mega Hertz
MLSD	Maximum Likelihood Sequence Detection
mm	Millimetre
MPPM	Multiple Pulse Position Modulation
MSB	Most Significant Bit
MSI	Medium-Scale Integrated
nm	Nanometre
NRZ	Non Return-to-Zero
Offset PPM	Offset Pulse Position Modulation
OOK	On-Off Keying
OPPM	Overlapping Pulse Position Modulation
PAM	Pulse Amplitude Modulation
PC	Personal Computer
PCM	Pulse Code Modulation
PDM	Pulse Density Modulation
PFM	Pulse Frequency Modulation
PISO	Parallel Input Serial Output
PLD	Programmable Logic Device
PLL	Phase Looked Loop
PMMA	Polymethyl Methacrylate and Fluorinated Acrylic

POF	Plastic Optical Fibre
PPM	Pulse Position Modulation
PRBS	Pseudo Random Binary Sequence
PWM	Pulse Width Modulation
QPAM	Quadrature Pulse Amplitude Modulation
RAM	Random Access Memory
RZ	Return-to-Zero
SIPO	Serial Input Parallel Output
SNR	Signal to Noise Ratio
SPLL	Software Phase Looked Loop
SPPM	Shortened Pulse Position Modulation
SSI	Small-Scale Integrated
STA	Signal Tap Analyser
TIR	Total Internal Reflection
TTL	Transistor-Transistor Logic
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuits
VLSI	Very Large-Scale Integrated
WDM	Wavelength-Division Multiplexing
ΣΔM	Sigma-delta

1 Introduction

1.1 Optical Communication Background

Communication is defined as a process by which information is imparted or exchanged; a communication system facilitates the transmission of this information from a sender to a receiver. The elements of a communication system the hardware, carrier medium, etc. are generally determined by characteristics of the application in which it is to be used. For example, the information may need to be communicated over short distances (several kilometres) or between continents (in the order of thousands of kilometres).

Electromagnetic (EM) radiation, specifically with frequencies in the range from radio waves (megahertz), through microwave (in the order of gigahertz) to near infrared and visible light (several hundred terahertz) are often used as the carrier medium for communication. Communication systems employing the visible and near infra-red parts of the EM spectrum as carrier waves are referred to as ‘light-wave’, or ‘optical’ communication systems. The use of optical transmission was first made possible following the demonstration of laser light by Theodore Mainman in 1962. The following year, as reported by (Ghassemlooy & Popoola, 2010), a laser beam was first used to carry a television transmission. A further significant advance in optical communication systems occurred seven years later when high speed signal modulation was made possible by the production of a small scale semiconductor laser.

In the 1970’s, the focus of optical transmission research was the development of fibre-optic communication systems. After its invention in the early part of that decade, interest in use of the fibre optic cable as a means of transmitting information rapidly grew on account of its very low signal loss. The high bandwidth and rapid transmission rate enabled by fibre-optic cable rapidly caused it to become widespread, and it has been employed globally in communication systems since the early 1980’s, changing the nature of telecommunications beyond recognition. Such has been its

impact that it could be considered to have been one of the principal driving forces behind the information revolution (G. P. Agrawal, 2002).

The internet, digital television, computer networks and digital media amongst many other applications rely on the transfer of massive quantities of data. To date, only optical fibre offers sufficient bandwidth to transmit this data; without it, it is unlikely that such developments would have expanded to the extent that they have today. This situation is likely to remain for the foreseeable future; there is considerable demand for wireless technology, which offers many of the same benefits, but to be exploited fully, this is largely required to be connected to and compatible with fibre-optic communication systems (Dai, Wang, & Yang, 2012).

All communication systems comprise three components – a transmitter, a transmission medium and a receiver. Figure (1.1) shows a schematic diagram of such a system. The source is the entity that from which the information to be sent originates. The information must be converted into a form in which it can be carrier through the communication system; this conversion is performed by the transmitter, in a process known as modulation. The transmitter then passes the modulated information to the transmission medium, through which the information travels until it reaches the receiver, where it is converted back (demodulated) to a form that can be understood by the entity to whom the information is being relayed.

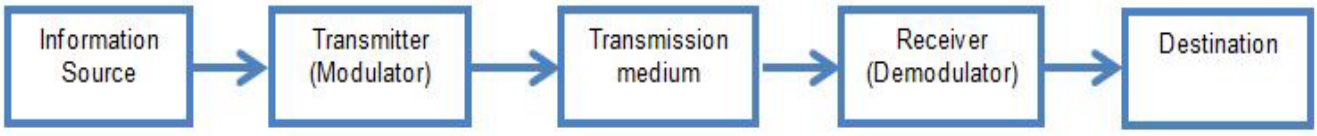


Figure 1-1 Schematic diagram of general communication system

All fibre-optic communication systems comprise the same three fundamental components. In these systems, the transmitter is a light source, such as a Laser or a Light Emitting Diode (LED) and the optical fibre acts as the carrier, guiding the light signals from source to destination. The modulation in fibre-optic systems is performed by converting an electrical signal to light. One means of doing

this, ‘digital’ or ‘direct’ modulation, is analogous to the production of a Morse code signal, only optical rather than audible pulses are created. The pattern with which the electrical signal is switched on and off is reproduced in the light signals (DeCusatis & DeCusatis, 2010). Figure (1.2) shows a schematic of a fibre-optic system, in which the information from the source is passed to the transmitter. The modulation of the optical carrier is provided by this transmitter driving the optical source.

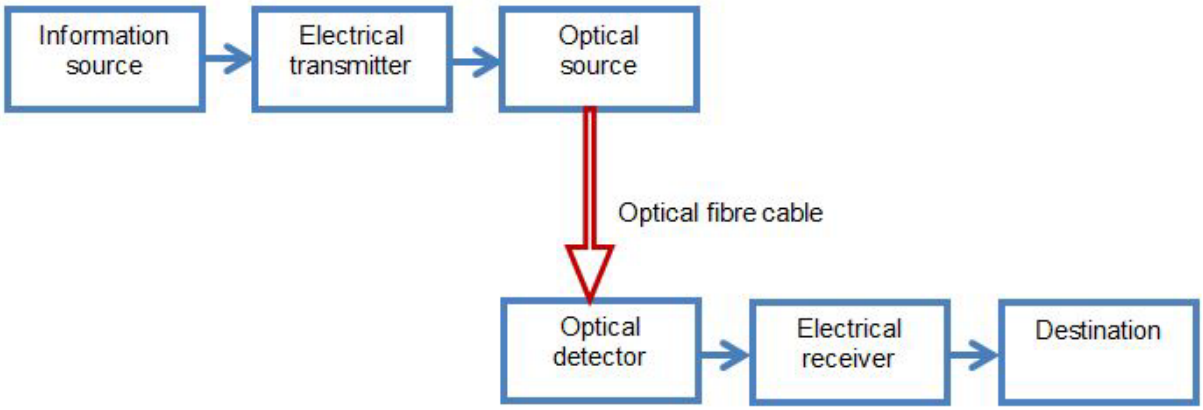


Figure 1-2 Schematic diagram of a fibre-optic system

In figure (1.3), the more detailed components of a typical digital fibre-optic link are illustrated schematically. In this situation, the digital optical signal that enters the fibre-optic cable is created by the direct modulation of the semiconductor laser intensity with the encoded digital signal that has been input from the information source. At the receiving end, the signal is detected by a photodiode detector, which converts the optical signals into electrical signals, after which any signal processing that may be required is applied (for example, amplification or noise reduction) before the signal is decoded to pass the original information in the form of a digital signal to the receiver (Westbrook & Moodie, 1996).

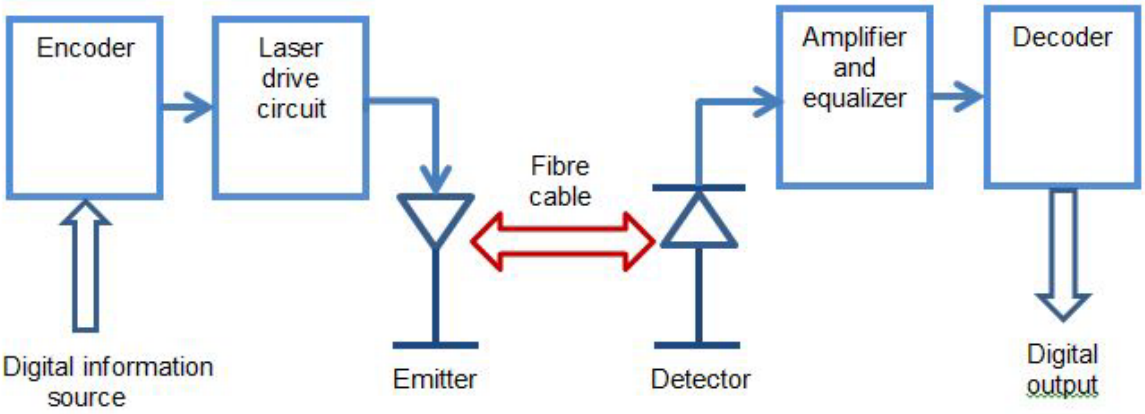


Figure 1-3 Typical digital fibre-optic link

1.2 Features of Fibre Optic Communication Systems

1.2.1 Advantages

The principal alternative to optical fibre in communication systems is metal-based electrical cabling. There are many ways in which optical fibres are advantageous to electrical systems (Keiser, 2003), including the following:

- **Transmission Over Long Distances: Lower Signal Degradation and Loss**

  Fibre-optic communication systems are associated with significantly lower signal loss than copper-based systems. The nature of signal transmission within fibre-optic cables minimizes signal attenuation and maintains the integrity of the signals; fibre-optic cable can carry signals over fifty times as far as copper cables before processing is required for performance to be enhanced.

- **Future-Proofing for Bandwidth Expansion**

  As the required bandwidth necessitated by increased internet use and increasingly data-intensive applications expands, the need to increase the data capacity of systems will continue to grow. Within any given system, fibre-optic cables are by several orders of magnitude the most efficient means of transmitting signals. As financial and logistical

constraints often necessitate the use of existing infrastructure when expanding systems (for example, installing cables in pre-existing cable runs), the high performance and small dimensions of fibre-optic cables make them the most effective and efficient means of future-proofing.

- **Availability of Resources**

  Electrical cabling systems depend on large quantities of copper and aluminium, resources of which are finite. The principal raw material for fibre-optic cable is sand which is not only available in far greater abundance, but is also much cheaper than those metals. (Furthermore, the cost of metal cabling is likely to rise in the future as resources, adding to the benefits in the previous point.)

- **Unaffected by Electromagnetic Interference**

  Fibre-optic cables are ideal for use where EM interference might affect the performance of copper-based cables. They are electrical insulators and, as such, are not affected by the impact of fields from other electrical cables, radio-frequency interference or more severe problems such as lightning strikes.

- **Electrical Safety**

  Using light, rather than electrical signals, fibre-optic communication is safer in that there are considerably lower electrical safety hazards.

- **Greater Data Security**

  Fibre-optic cables provide higher security than traditional metal cabling as the absence of magnetic fields prevents the external detection of the signals. This clearly makes fibre-optic communication systems the preferential option when data protection is vital; while data can be intercepted, it requires the cable to be spliced, which is almost impossible to do undetected. Fibre-optic cable is the most secure means of transmitted data at present.

- **Longevity**

  The fibre-optic cable hardware has greater longevity than copper-based cables as glass is not subject to corrosion or oxidation. Copper is more liable to be degraded by acids, moisture and toxic gases and other such conditions found in more challenging environments. Therefore, fibre-optic cable can be expected to last much longer than copper cable.

- **Temperature Independence**

  The performance of metallic conductors is affected by changes in temperature (for example, the bandwidth is reduced by reductions in temperature). Fibre-optic cable is not impacted by temperature.

1.2.2 Disadvantages

- **Limited Applications**

  Unlike metal-based communication systems, fibre-optic systems cannot be easily used with mobile communication facilities. Their use is restricted to fixed installations, thereby limited their application.

- **Low-Power Sources Limit Transmission Distance**

  In general, an advantage of fibre-optic communication systems is their ability to carry signals for long distances with relatively little degradation. However, most commonly used light sources for fibre-optic communication systems are very low-power devices, which limits this advantage for those systems requiring high rates of data transmission. While devices operating at higher power levels are available, their cost is such that using a number of repeater amplifiers is a cheaper means of transmitting the signal over long distances.

- **Limited Modulation**

  There is less flexibility in the modulation of the light source compare to the modulation of metal-based transmission. However, this is, to some extent, mitigated by the ability to

modulate the subcarrier signals using more advanced techniques before the signals are applied to the optical fibre systems.

- **Greater Fragility**

  Unlike optical fibres, metal-based cables are a tried and tested technology, having been used for many decades. Although protected by the casing, the glass in optical fibres is fragile. Microscopic cracking may occur over time; vibration testing has been performed but cannot fully replicate the conditions faced over time and include the impact of the effects of aging and the physical conditions to which the cables are exposed.

- **Higher Initial Cost**

  The cost of optical fibre itself is low, considering the bandwidth it is capable of carrying. However, the associated cost of interfacing with networks and other equipment necessitates a higher initial than metal-based communication systems.

- **More Expensive Maintenance**

  The reliance on total internal reflection of fibre-optic cable necessitates the use of more specialist, expensive equipment and skilled labour for maintaining the infrastructure and repairing any damage that arises.

- **Susceptibility to Nuclear Radiation**

  Ionizing radiation is known to darken glass; in optical fibres, this increases signal attenuation. As long as the dose to which the fibre is exposed is not too high, the attenuation decreases over time (in the order of decades). The speed and extent of attenuation loss are greater the harder the glass; harder glass also takes longer to recover.

1.3 Aims and Objectives

The aim of this project is to design and subsequently implement in hardware the Offset Pulse Position Modulation (Offset PPM) technique, applied over a fibre-optic link. There are four intermediate objectives of the research; these are described below.

- **To implement the Offset PPM encoder/decoder and practically verify some of the theoretical models**

No practical Offset PPM encoder/decoder has been constructed to date. Many PPM formats that have previously been proposed have advanced no further than the theoretical stage, if the Offset PPM is to become a reality, hardware Offset PPM encoder/decoder must be implemented to prove that the Offset PPM system can occur in real time. Therefore, this objective is to construct the Offset PPM encoder/decoder using low-cost components; this in itself takes it a step beyond most other PPM schemes.

- **To confirm theoretical predictions with measurements**

It is necessary to compare the output of the Offset PPM encoder/decoder with the predicted output. The results of this comparison with theory will verify both that the encoder generates correct Offset PPM sequences and that the decoder correctly decodes those sequences into Pulse Code Modulation (PCM).

- **To Design and implement a complete Offset PPM communication system using an FPGA**

As the Offset PPM encoder/decoder hardware use discrete component architecture and high frequencies, and in order to reduce the impact of internal and external interference, as well as distortions and delays, the Offset PPM encoder/decoder will be synthesized onto a Field Programmable Gate Array (FGPA).

- **To confirm theoretical predictions with measurements (fibre optics).**

The principal focus of this thesis is the investigation of the performance of the Offset PPM through optics. Therefore, an optical communication system was constructed; this system was used to determine the performance of the Offset PPM waveforms through Plastic Optical Fibre (POF). A clock sequence required in order for the PPM decoder to be able to decode the Offset PPM sequence into PCM format.

1.4 Contributions

The main areas of original contribution are:

- ❖ The development of hardware implementation using electronic chips of the Offset PPM encoder and decoder, this shows that the Offset PPM scheme can be achieved for real time operation. Outcomes agree with theory.
- ❖ Established a computer programming using and ALTERA® Quartus II software to define the Offset PPM coding over optical channel is implemented and the outcome is simulated.
- ❖ Developed a VHSIC hardware description language (VHDL) source code for the Offset PPM system. A schematic and a full block description of the system are given.
- ❖ ALTERA® FPGA development board has been used to implement the VHDL designs for FPGA. It uses Cyclone® III series FPGA EP3C120F780. The complete design includes: FPGA clock control block, Phase-locked Loop (PLL) for clock generation and division, Pseudo Random Binary Sequence (PRBS) PCM data generation, Offset PPM encoder and decoder, and finally a Bit Error Rate Test (BERT) system which regenerates the original sent PRBS data sequence and uses logic gates to check if any errors have occurred by comparing the original sequence with the regenerated data sequence.

- An optical communication system (transmitter/receiver) design of the Offset PPM has been completed to operate over a highly dispersive POF link to use it with the Offset coding system.
- Established a practical implementation of the designed system by using ALTERA® Quartus II software, and Cyclone III Field Programmable Gate Array (FPGA) based DSP development board. The implementation of the optical system transceiver is done as well.
- Experimental tests have been performed in order to examine Offset PPM system performance in a real-time transmission link. Also to calculate the BER using HP 3780A Bit Error Rate Tester (BERT).
- Tested digital transmission measurement including BER was applied to Offset PPM optical communication system based on VHDL source code and Cyclone III Field Programmable Gate Array (FPGA). Software was used to simulate the system. The system has shown that it has the ability to detect and correct erasure and error symbols when they not overcome its limitations.

1.5 Organization of the Thesis

The remaining chapters are briefly introduced in this section and each of the chapters is organized as follows:

Chapter 2 discusses the coding schemes in optical fibre communication system, their basics, advantages and disadvantages. Thereafter, a simple application of FPGA and VHDL was introduced.

Chapter 3 tabulates the optical transmitter, optical receiver, optical amplifier, and the optical fibre. It reports different OFDM design kernels.

Chapter 4 introduces the Offset PPM as a new technique of PPM. Afterwards, the digital errors that affect the Offset PPM are described.

Chapter 5 reports the electronic design stage and implementation process of both the Offset PPM encoder and Offset PPM decoder.

Chapter 6 introduces the Cyclone III development board and SMA Breakout Cable with the lists of features of the board and specific information. The VHDL circuits design for the Offset PPM encoder and decoder system. After that, the two main full implementations of Offset PPM system were defined.

Chapter 7 explores the POF that is used as an optical channel, and describes the optical transmitter, optical receiver, and a voltage comparator. The practical design and implementation of the system were discussed.

Chapter 8 summarizes the conclusions of this study with some recommendations for future studies.

2 Literature Review

2.1 Introduction

This chapter reviews the current understanding of the fundamental results of coding and modulation that were used in optical communication. The PPM schemes have been discussed with more details in order to give a full vision of using these techniques. Moreover, the purpose of this chapter is to present the comparison between FPGA and Microcontroller. In the end of this chapter, the fundamental of VHDL software and its relationship with FPGA has been defined.

2.2 Coding Schemes in Optical Fibre Communication System

There are a wide range of coding schemes used in optical fibre communication systems; some of them and their associated advantaged and disadvantages are discussed below.

- **On-Off Keying (OOK)**

On-off keying, the most basic form of modulation, is cheap to implement and requires little power. The optical power is modulated according to the (binary) data input signal, and is not dependent on the presence of a carrier wave. Aside from its use in optical fibre communication systems, it is commonly utilised in remote control systems and in RF carrier waves (Babar et al., 2017).

- **Digital Pulse Position Modulation (DPPM)**

DPPM (Calvert, Sibley, & Unwin, 1988; R. Cryan, Unwin, Garrett, Sibley, & Calvert, 1990; I Garrett, 1983; Ian Garrett, 1983; Gol’dsteyn, 1980; Massarella & Sibley, 1992; M. J. Sibley, 1993) is a technique that offers superior sensitivity than OOK, albeit at the expense of higher bandwidth and line rate. In common with OOK, it is an inexpensive and uncomplicated scheme, the main motivation for its development being to increase transmission efficiency by better exploiting the available bandwidth available in optical fibre communication systems. The increase in data transfer

rate can be significant – for example, when using 64 slots and encoding 6 bits of data, the maximum rate is over ten times that achieved with OOK.

M bits of data are coded into a single pulse; this pulse occupies a time slot, of which there are 2^M in a block. In order to reduce the impact of channel dispersion – which may cause Inter-frame Interference and Inter-Symbol Interference (IFI and ISI respectively) a guard interval of one or more empty time slots may be inserted at the end of a frame. While the increased data transfer rate is desirable, the increased bandwidth used by DPPM places extra demand on the processing electronics, restricting its use in some applications.

- **Shortened Pulse Position Modulation (SPPM)**

SPPM, described by (R. A. Cryan, 2010) is a coding *M* bits of OOK data into $n = 1 + 2^{M-1}$ bits. The scheme was first suggested for use in the context of subsea wireless optical communication systems.

- **Overlapping Pulse Position Modulation (OPPM)**

A modification of DPPM, Overlapping Pulse Position Modulation (OPPM) is a scheme in which overlap between adjacent pulse positions is permitted Modulation (Calderbank & Georghiades, 1993; H. Shalaby, 1993; H. M. Shalaby, 1999). This concept enables a higher transmission rate than DPPM despite using a lower bandwidth, provides signals that are easily decoded and also has a relatively low cycle. However, these positive attributes are at the expense of a loss of orthogonally and, given that the frame length must vary according to the degree of overlap that occurs, the synchronization procedures are more restricted.

- **Pulse Position Modulation**

(Liu, 2002) presented pulse position modulation (PPM) as in figure (2.1), describing it as a method of encoding information in a signal through variation of pulse position. While the unmodulated

signal comprises a train of pulses whose amplitude, duration and frequency are all constant, their positions are changed during modulation to reflect the information that is being encoded. In PPM, the position of the pulse is modulated relative to its unmodulated relative to its unmodulated position. Digital pulse modulation results in an efficient system characterized by high security, robustness, integration, reliability and overall performance; the less Ko by noise, described by Ko (2001).

There is a trade-off between final line rate and the enhanced consumption of bandwidth that PPM achieves through the representation of m bits of data by a single pulse in PMM. PPM must transport the same quantity data as PCM in an identical time frame. In order to do this, for a PCM bit interval with a bit time of T_b, the time frame is mT_b, there are 2^m PPM time slots. Therefore, to meet the requirement of the same data traffic flow, the PPM rate must be $2^m / m$ faster than the PCM (H. M. Shalaby, 1999; M. J. Sibley, 1993, 2003, 2004; M. J. Sibley & Massarella, 1993; Zwillinger, 1988).

The tolerance to the effect of noise from signal distortions and communication channels increases with the use of digital communication systems. Such systems are also very reliable as they are able to use powerful coding schemes to control errors and encryption algorithms to increase security. Analogue communication systems are less efficient than digital ones; PPM sacrifices bandwidth for a higher signal to noise ratio. It is vital that communication is performed using effective systems in order to retain the correct meanings of the messages being transferred. To lose these meanings between source and transmitter and receiver is to create serious problems, as all messages are different. For a communication system to be effective, the information source, its transmitter, the carried signals and the receiver must all be engaged; considered as a whole, these elements and the associated processes may be discrete, continuous or mixed.

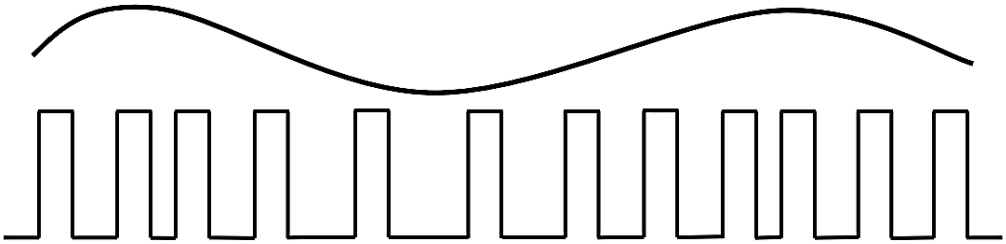


Figure 2-1 Pulse Position Modulation (Liu, 2002)

- **Multiple Pulse Position Modulation (MPPM)**

First proposed as a viable means of increasing the efficiency of bandwidth usage in optical PPM (Sugiyama & Nosu, 1989), Multiple Pulse Position Modulation (MPPM) has also been investigated for dispersive optical channels (Nikolaidis & Sibley, 2007, 2010; M. Sibley, 2004). As demonstrated by Sugiyama and Nosu, MMPM optical pulses are, as shown in figure (2.2), transmitted in one single block in multiple pulses. Using this method, the same transmission efficiency is achieved but using approximately half the transmission bandwidth in optical PPM – that is, the band-utilization efficiency is approximately doubled. Sibley demonstrated the MPPM to be one of the most bandwidth-efficient PPM coding schemes in his analysis of MMPM operating over graded-index plastic optical fibre, producing a sensitivity equivalent to that of digital PPM but without the same bandwidth expansion. The MPPM scheme utilizes multiple pulses in a frame, their positions determined by the original PCM word.

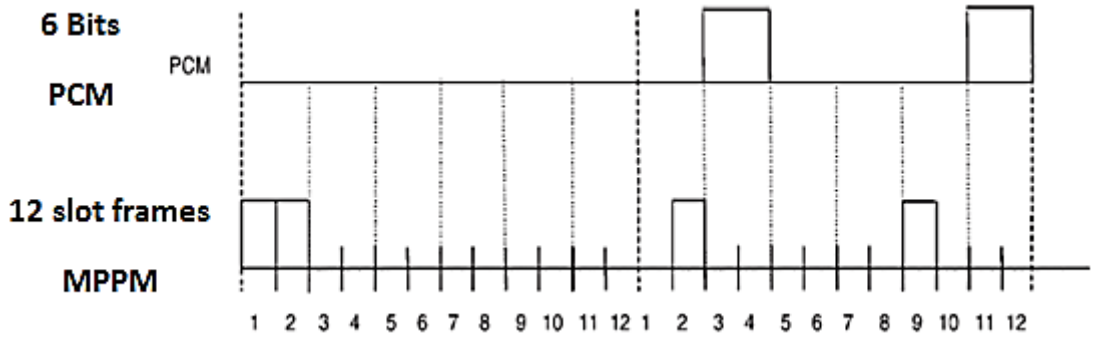


Figure 2-2 Conversion of PCM (top trace) to Multiple PPM double pulses per frame (Bottom trace)

In figure (2.2), (12/2) MPPM in which a 12-slot frames using two data pulses to code 6 bits of PCM is shown. In this example, linear mapping translates PCM 000000 to 1, 2 (that is, pulses in slots 1 and 2), whereas the PCM word 010001 translates to 2, 9. The line rate for this (12/2) code is twice the line rate of the PCM. Higher order codes will result in greater reductions, as shown by (Sugiyama & Nosu, 1989). For example, (15/4) cam code 10 bits of PCM; this results in a line rate 1.5 times that of the PCM line rate.

In addition, the error performance was analysed, the Maximum Likelihood Sequence Detection (MLSD) scheme as introduced, simplifying error performance prediction using bounds. The power of multiple PPM was found to be more efficient than digital PPM, as was its bandwidth utilization. MPPM showed a higher predicted sensitivity (0.58 bits per photon compared to 0.5 bits per photon respectively when operating at an error rate of 1 in 10^9). As with previous coding schemes, MPPM was found to be susceptible to erasure, false alarm and wrong-slot errors. The causes of this may be attributable to optical pulse detection at the receiver, to dispersion of the photons trough the transmission channel or to both. The application of appropriate MLSD can increase the sensitivity of MPPM.

- **Digital Pulse Position Modulation (DPPM)**

The digital PPM technique uses $log_2 M$ data bits mapped onto one of M possible symbols in each frame, such that N bits PCM is encoded by one pulse in one of M time slots (where, $M = 2^N$). Within each time slot, the single pulse has a constant power and is repeated every T seconds. It is then followed by $M-1$ empty slots. Each frame's length is equal to the length of the PCM time frame. The DPPM coding scheme is based on the position of each pulse within the symbol; Figure (2.3) shows the encoded pulse position related to the decimal value of each data bit. Inter-frame interference (IFI) may be eliminated by the insertion of a number of guard intervals to a PPM frame. This will also improve the performance of the system (R. Cryan et al., 1990; M. J. Sibley & Massarella, 1993). If $T_b = 1/B$ represents the PCM bit time, B the original data rate and N the number of PCM bits, the digital PPM slot duration is given by:

$$T_s = \frac{N.T_b}{2^N} \qquad (2.1)$$

Decoding of the received pulses and recovery of the PCM information is performed in the presence of both slot and symbol synchronization. The time at which the PPM pulses reach the crossing point is determined by a threshold signal detector; the arrival time may be influence by signal interference, as described by (M. J. Sibley & Massarella, 1993).

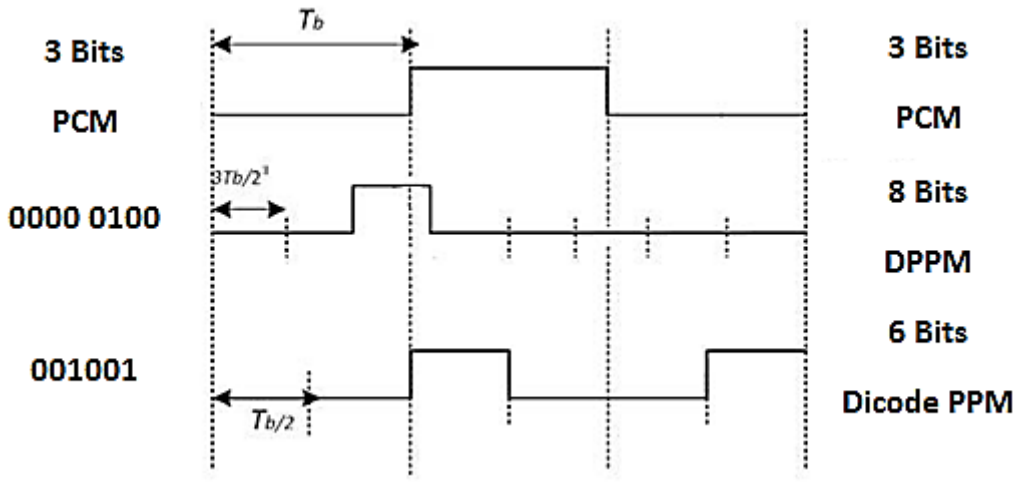


Figure 2-3 Conversions of PCM data (top trace) into DPPM (Middle trace) and DiPPM (Bottom Trace)

- **Dicode Pulse Position Modulation**

Dicode Pulse Position Modulation (DiPPM) is an appealing coding scheme in that both coding and implementation are straightforward. In the absence of a change in the PCM signal, a zero pulse is present, a logic one to logic zero data transition is coded by negative (-V) and a logic zero to logic one is coded by positive (+V) in the dicode technique. Four slots are used to code a single bit of PCM. However, two further signals are converted into two pulse positions in data frames – these are the SET and RESET signals as shown in figure (2.4). Should there be no data transition present, there is no pulse. A transition from zero to one result in a SET(S) pulse, while a transition from to one to zero results in a RESET(R) pulse (Al-Nedawe, 2014). When the PCM data is constant, no signal is transmitted (M. J. Sibley, 2003). As a single slot in PCM can be coded into a single S or R slot in DiPPM, the power requirement is lessened. As with other schemes, guard intervals can be inserted to the time slot to lessen the impact of ISI. DiPPM, T_s is expressed as follows:

$$T_s = \frac{T_b}{2 + gu} \tag{2.2}$$

Whereis the guard intervals. *gu*nd is the original data rate a*B* denotes the PCM bit time, $T_b = 1/B$

Just two slots are used to transmit one bit of PCM in a zero-guard DiPPM. In this situation, the line rate becomes twice that of the original PCM; both the resultant speed and required bandwidth are lower than those of digital PPM (Sibley, 2003b).

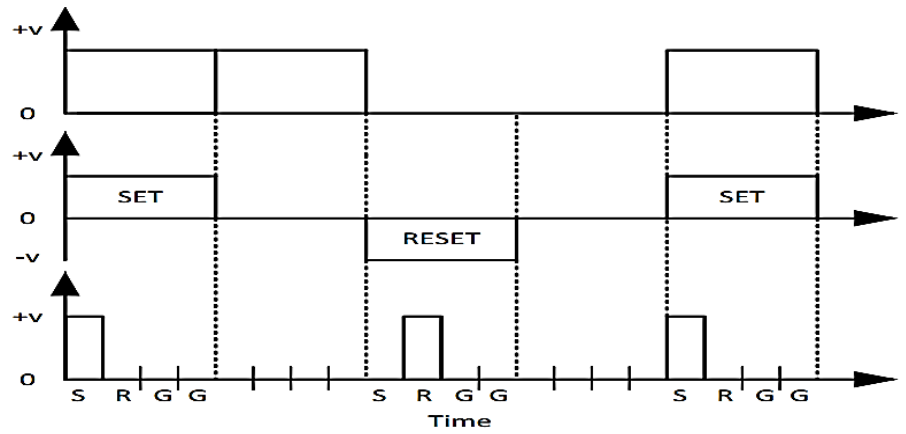


Figure 2-4 Conversion of PCM data (top trace) into dicode (Middle trace)

Table (2.1) shows the four symbols in the DiPPM alphabet (S, R, and 2N for 00 and 11 transitions). A transmitted S pulse can be followed only by R or N, both having a probability of 1/2. The maximum DiPPM run could be R, nN and S if the coding of the original PCM line is such that the run of like symbols is limited to n.

Table 2.1 DiPPM Symbol Alphabet

PCM	Probability	DiPPM	Symbol
00	1/4	No pulse	N
01	1/4	SET	S
10	1/4	RESET	R
11	1/4	No pulse	N

According to this condition, the probability of the next pulse (R symbol) is unity – its presence is guaranteed at the end of a series of N symbols that is n symbols long. If the pulse originally transmitted is an R pulse, a similar situation can arise (R. Cryan & Unwin, 1993).

- **Duobinary Pulse Position Modulation**

The Duobinary Pulse Position Modulation (DuoPPM) signalling technique offers a significant reduction in bandwidth expansion in comparison to digital PPM, as the line rate is twice that of the original NRZ OOK data, as shown in figure (2.5) (Mostafa, Sibley, & Mather, 2014). In the scheme, a constant stream of data of logic 1 produces a pulse in slot 1 of the DuoPPM slot 1, which a constant stream of data of logic 0 produces on in slot 0. When the data is in transition from logic 1 to logic 0 and vice versa, no pulse is transmitted in the frame, as shown in figure (2.5). The nature of this scheme reduces the ISI, negating the need for guard slots; a new MLSD and correction technique ensure a particular error type can be wholly eliminated (Mostafa, 2015).

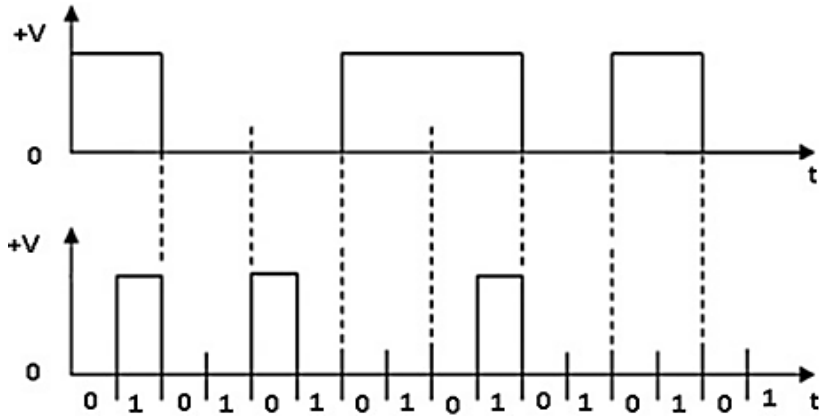


Figure 2-5 Conversion of OOK data (top trace) into DuoPPM (bottom trace)

- **Pulse Amplitude Modulation (PAM)**

The sophistication of the fundamental pulse amplitude modulation (PAM) scheme, shown in the figure (2.6), in which the information is transmitted in the pulse amplitude – can be increased by utilizing more amplitude levels. For example, in Quadrature Pulse Amplitude Modulation (QPAM, or QAM), four amplitude levels can be used for each of four groups – each group contains two signal bits (00, 01, 10 and 11). Pulse-amplitude modulation is the basis of direct-sequence spread spectrum (DSS) (Mazzini, Traverso, & Nowell, 2017).

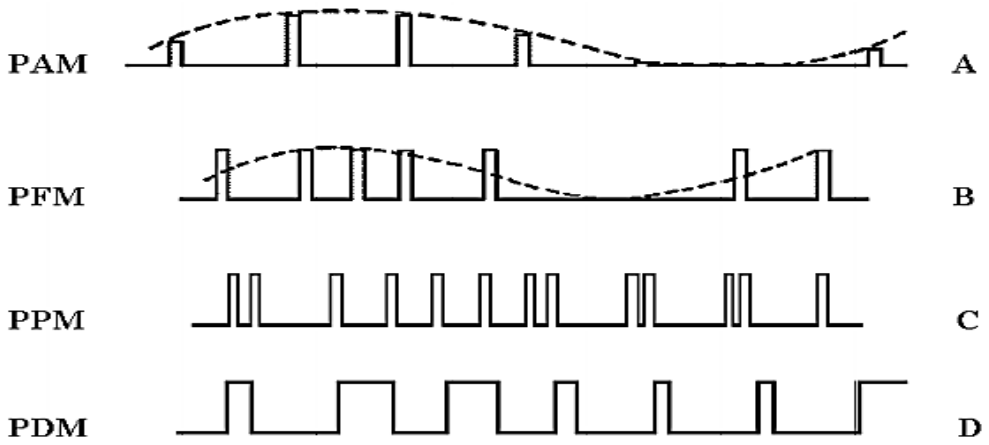


Figure 2-6 PAM (A), PFM (B), PPM (C) and PDM (D)

- **Pulse Density Modulation (PDM) or Pulse Width Modulation (PWM)**

A means of converting analogue signals into digital signals, pulse density modulation (PDM) is a technique in which the relative pulse density is proportional to the magnitude of the input, analogue signal. Pulse-width modulation, PWM, is a special case of PDM that is often used in motor control as shown in figure (2.6) (Li, Fang, Chen, Wang, & Tang, 2017).

- **Pulse Frequency Modulation (PFM)**

Pulse frequency modulation (PFM) utilizes the modulating wave to frequency modulate a pulse-generating circuit by varying the repetition rate of fixed-duration pulses. (In this respect, it differs from PWM and PDM, in which the frequency remains constant but the width of square pulses is varied.) As an example, with a pulse rate of 800 pulses per second (p/s) for a signal voltage of 0 V, the pulse rate may step up to 900 p/s for maximum positive signal voltage and step down to 7000 p/s for maximum negative signal voltage. The PFM generation circuitry required for this method of modulation is complicated, requiring a stable, frequency modulated oscillator to drive a pulse generator. As a result, PFM is not extensively used as shown in figure (2.6).

- **Pulse Code Modulation (PCM)**

Illustrated in the figure (2.7), pulse code modulation (PCM) is a scheme used in the transmission of analogue data in binary form that is not dependent on the analogue waveform's complexity. Therefore, it is suitable for the transfer of all types of analogue data, including music, video, voice and telemetric data.

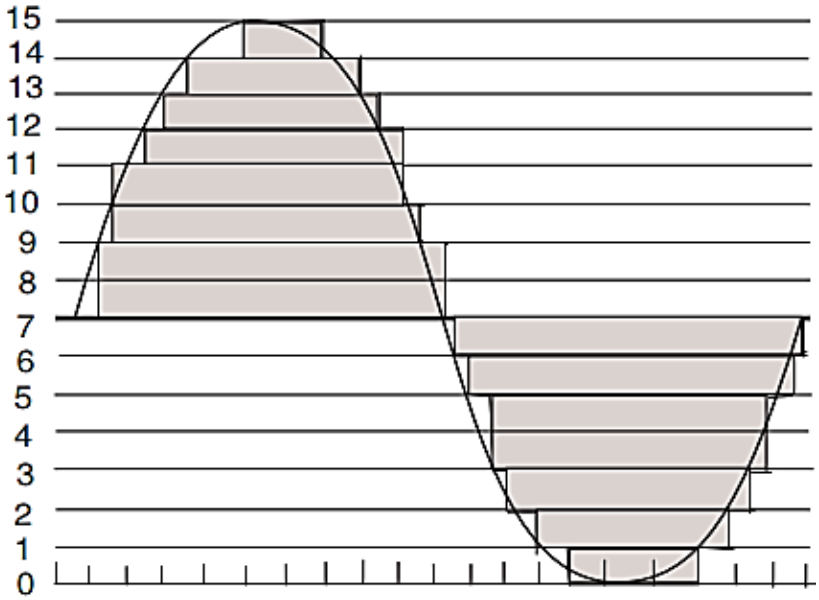


Figure 2-7 Pulse Code Modulation

At the transmitter, the amplitude of the analogue waveform is sampled at a regular frequency that is several times greater than the maximum frequency of the waveform (that is, the Nyquist rate) to form the PCM. The amplitude at each sampling point is quantized (that is, it is rounded to the nearest binary level) and represented by a binary word of at least two binary bits. To decode the PCM, a pulse code at the receiver converts these binary numbers into pulses with the same quantum levels as the levels in the modulator; the pulses are processed further to restore the analogue waveform. Adaptive Differential Pulse Code Modulation (ADPCM) is a technique for the conversion of analogue information or sound into binary information. ADPCM is defined by the International Telecommunication Union (ITU). Frequent samples of audio signals are taken and the values of the sampled audio modulation are expressed in binary terms, resulting in a lower bit rate,

enabling both digital and voice data to be sent simultaneously. Unlike PCM, on which ADPCM is a variation, only the difference between adjacent samples is transmitted. There are several applications of ADPCM, including the storage of information (such as image, text and code) on data storage media, sending audio on long-distance fibre-optic lines, digital cordless telephony and in radio/wireless local loops (Uddin, Ansari, & Naaz, 2016).

- **Sigma-delta modulation (ΣΔM)**

Sigma-Delta modulation (ΣΔM) is a technique utilized in encoding high resolution signals into lower resolution signals through pulse-density modulation and has become increasingly popular in electronic components recently. Examples of Sigma-Delta modulation applications are frequency synthesizers, motor controls, analogue-to-digital and digital-to-analogue convertors and switched mode power suppliers. Delta-Sigma modulation, first demonstrated in the early 1960's, can produce very high resolution when used in Analogue to Digital Converter (ADC) or Digital to Analogue Converter (DAC) circuits. However, although data conversion was one of its earliest and commonest uses being in data conversion, it has only been with more recent silicon-based technological developments that it has come into more widespread use as these have facilitated implementation on low-cost processes on digital integrated circuits (Zerek, Elfituri, & Emhimid, 2017).

- **Continuously Variable Slope Delta Modulation (CVSDM), also called Adaptive-Delta Modulation (ADM)**

First proposed by (Greefkes & Riemens, 1970), Continuously Variable Slope Delta Modulation (CVSD, or CVSDM) is a method of voice coding and is a delta modulation with variable step size. That is, it is a special case of adaptive delta modulation. The technique encodes at 1 bit per sample – that is, audio sampled at 16 kHz is encoded at 16 bit/s. During the encoding process, the step size is continuously adapted. This has two benefits – increasing the step of quantization when the signal

changes rapidly avoids slope overload, while decreasing the step of quantization reduces granular noise when the signal is constant. A reference sample and step size is maintained by the encoder, to which each input sample is compared and the reference sample adjusted if the input sample varies in size from the reference. If the input sample is smaller than the reference sample, the encoder emits a 0 bit and subtracts the step size from the reference sample. Conversely, if the input sample is larger, the encoder emits a 1 bit, adding the step size to the reference sample. Furthermore, the previous N bits of the output are retained by the encoder in order to determine adjustments to the step size (typically 3 or 4 bits are retained). If the retains bits are all 0s or all 1s, the step size is doubled; otherwise, the step size is halved. For each input sample processed, the step size is adjusted. At the decoder, the adjustment process is reversed. That is, the step size is added or subtracted from the reference sample according to the bit stream. The reconstructed waveform comprises the sequence of adjusted reference samples; the step size is doubled or halved according to the same logic as was used in the encoder.

- **Colour Coded PPM (CCPPM)**

Davidson and Bayoumi first proposed colour coded PPM (CCPPM) in a number of publications (F. Davidson, 1985; F. Davidson & Bayoumi, 1987). Higher energy efficiency (in nats per average number of received photons per pulse) was found than in an ordinary PPM system using CCPPM, which utilizes an overlapping centre frequency for each individual PPM data slot. A further development of the technique combining laser diodes operated in different wavelengths with a pulse position modulated (PPM) format was considered by (R. M. Gagliardi & Kim, 1988). That is, they combined several laser diode sources into a single beam for digital PPM transmission, using a set of three individual system architectures. In one system, the PPM pulse comprised a number of optical frequencies, combined prior to the digital PPM modulator into a single PPM data pulse. In architecture, each optical wavelength was combined after PPM modulation. In their study, the

influences of the number of wavelengths involved, the PPM coding level, the optical Signal to Nosie Ratio (SNR) and losses associated with the beam optics on the performance on the data rate were compared. Table (2.2) show the Generation of different types of coding from equivalent 3 bits of data

Table 2.2 Generation of different types of coding from equivalent 3 bits of data

OKK	Digital PPM	Differential PPM	Digital PIM	DH-PIM	Offset PPM	SPPM	MPPM
000	0000 0001	0000 0001	1	100	0000	0 0001	1 1000
001	0000 0010	0000 001	10	1000	0001	0 0010	1 0100
010	0000 0100	0000 01	100	1000 0	0010	0 0100	1 0010
011	0000 1000	0000 1	1000	1000 00	0100	0 1000	1 0001
100	0001 0000	0001	1 0000	1100 00	1000	1 0001	0 1100
101	0010 0000	001	10 0000	1100 0	1001	1 0010	0 1010
110	0100 0000	01	100 0000	1100	1010	1 0100	0 1001
111	1000 0000	1	1000 0000	110	1100	1 1000	0 1100

2.3 Timing Extraction and Synchronisation

Timing extraction is an essential process in all digital transmission systems. Since the statistical and timing description of timing extraction synchronization was first addressed (for an early example being (Bennett, 1958)), there have been a wealth of publications concerning timing extraction with regard to digital transmission systems (Bennett, 1958; Datta & Gangopadhyay, 1987; Franks, 1980; Gitlin & Salz, 1971; Takasaki, 1972). Other authors have considered the structure of the synchronizers (for example, (Gardner, 2005; Rosenberg, Chamzas, & Fishman, 1984)), while Gagliardi (R. Gagliardi, 1974) reported a means of using pulse edge tracking to feed an error signal to an oscillator operating at the slot frequency. Gagliardi's technique involved the removal of the DC component from the pulse train, integrated between 1/2 and 3/2 slot durations, with the average value being determined as an error signal. (Gol'dsteyn, 1980) subsequently developed an algorithm for the definition of digital PPM pulse position under non-ideal clock synchronization. Three years later, the synchronization of PPM systems was further studied by Gagliardi; a technique for establishing the error signal for correcting the oscillator was considered by Ling and Gagliardi

(Ling & Gagliardi, 1986). The spectral component is cancelled through the use of full width pulses by squaring the current of the photo detector prior to feeding the signal to a phase lock loop (PLL) (Chen & Gardner, 1986; Chen, Win, Marshall, & Lesh, 1991). Practical measurement of the timing component within the digital time frame was investigated by Sibley in 1986; in 1989, Davidson developed a successful timing recovery system using an APD receiver (F. M. Davidson & Sun, 1989).

In four papers of 1992, Elmirghani reported a number of properties of pseudo random binary sequence (PRBS) digital PPM data (J. Elmirghani, R. Cryan, & F. Clayton, 1992a, 1992b; J. Elmirghani, R. Cryan, & M. Clayton, 1992; J. M. Elmirghani, R. A. Cryan, & F. Clayton, 1992). In this work, Elmirghani presented a novel technique for frame synchronization in which increasing the timing component for high level coding systems was not dependent on the use of low modulation indexes. Furthermore, the authors reported an analytical solution for a given coding level and modulation index; the requirements for slot and frame synchronization were considered.

Therefore, there are many similarities between PPM synchronization and bit synchronization in PCM systems. However, differences between the two do exist, the principal ones being the long run of zeros in PPM format place additional demand on the PPM synchronizer, as a result of the PPM format structure being different.

There are four fundamental means of performing phrase synchronization of a PPM system. These are as follows:

1. The maximum likelihood detector has been commonly used to extract the clock, particularly in the case of optical space PPM. In this technique, periodic insertion of the synchronization sequences into the data stream as the frame phase is estimated ensures synchronization with the generated frame clock. The sensitivity of the system is reduced, as the inserted sequences do not contribute to the data and so represent redundant power. Moreover, as the

sequences must be added at the transmitter and subsequently removed from the receiver, the system operating bit rate is reduced.

2. Another method tracking pairs of back-to-back pulses has been used in space PPM; this method is advantageous in that it does not suffer from any limitations. Differences between optical fibre PPM and satellite PPM necessitates the use of higher coding levels in order to maintain optimum sensitivity. Natural acquisition sequences in optical fibre PPM have been defined (Sun & Davidson, 1990).
3. When used in timing synchronization, PLL has no effect on PPM sensitivity as the PPL generated clock is synchronized with the PPM signal; PLL can be used in the majority of PPM formats.
4. The maximum pulse deviation from the centre of the frame is restricted by the redundancy introduced by line code, which also estimates the frame phase (O'Reilly & Yichao, 1985). One disadvantage of this method is the additional complexity that the need for coders and decoders introduces both at the transmitter and at the receiver, thereby making implantation difficult.

2.3.1 Phase Locked Loops (PLL)

Phase Locked Loops are highly versatile systems that generate output signals that tracks external input signals in both phase and frequency. The frequency of the generated output signal is programmable and is a rational multiple of a fixed input frequency; it is phase locked to the input signal. In the situation where the frequency and phase of the input signal are synchronized, the PLL is said to be in the ‘locked’ condition and the phase difference between the output signal and the reference is a known value. (Best, 1999) described four different categories of PLL, according to their implementations: Linear PLL (LPLL), Classical Digital PLL (DPLL), All Digital PLL (ADPLL) and Software PLL (SPLL).

The uses of Phase Locked Loops are many and wide-ranging and they are commonplace in communication equipment and microprocessors. Their typical applications include motor speed control, frequency control and clock recovery (Sánchez, Moehlmann, Blinzer, & Ehlert, 2016). They have also been utilized in regenerating carrier from input signals whose carriers have been suppressed and in frequency modulation and demodulation, as well as synchronizing clocks with other signals. Applications of Clock and Data Recovery (CDR) in data communication systems include backplane routing, optical communication, chip-chip interconnects and disk drive read channels. An inherent benefit of digital transmission is the ability to regenerate binary data, which is frequently transmitted in Non Return-to-Zero (NRZ) format. Optimum timing of the received data sampling is necessary to minimize the bit errors in this regeneration process; this necessitates derivation of the sampling timing information from incoming data itself as transmission of the required sampling clock signal separately from the data is impractical. A clock must be extracted on account of the noisy, asynchronous nature of the random data received in systems such as these. Such clock and data recovery removes jitter and distortion from the data and, additionally, retimes it so that it may be processed further. The role of clock and data recovery is illustrated in figure (2.8) (Zhang, 2004).

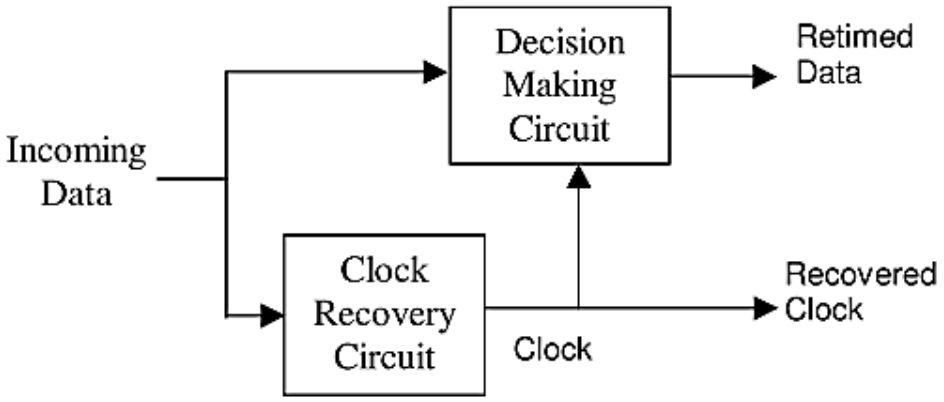


Figure 2-8 Simplified block diagram of a digital receiver

2.4 Digital Communication Errors and Error Correction

A. Bit Error Rate

The bit error rate (BER) in telecommunication transmission is the proportion of received bits that have errors and provides an indication of how frequently data must be retransmitted as a result of errors. For example, a BER of 10^{-3} would indicate that one bit out of 1,000 bits transmitted was in error. An excessively high BER might suggest that a slower data transfer rate would actually result in an improved (that is, lower) overall transmission time for a given quantity of data, as fewer packets would have to be resent. There are three principal means of improving the BER using a high signal strength, unless this results in cross-talk and so actually increases the BER, using slow and robust modulation or line coding schemes and through the application of channel coding schemes (for example, redundant forward error codes, the strength of which affect the information BER). The transmission BER is the number of detects bits that are incorrect prior to error correction divided by the total number of transferred bits, including redundant error codes and is generally greater than the information BER (Akaiwa, 2015).

B. Signal-To-Noise Ratio

In general, signal-to-noise ratio (SNR or S/N) is the ratio of the level of a signal to the level of background noise. It is a concept that is applicable to any type of signal – not just electrical signals – as a means of quantifying the extent to which a signal has been corrupted by noise. An SNR ratio of unity indicates equal levels of desired signal and background noise; the higher the SNR is above this, the stronger the signal is relative to the noise level. Therefore, the terms can be considered to be a measure of the relative quantities of useful information and extraneous or false information in an exchange of information. (Alam, Alam, Hu, & Mehrab, 2011) suggests that provide a useful means of viewing this as considering the extent to which the signal ‘stands out’ with respect to a noise reference level.

Dynamic range is a concept closely related to SNR as, in most situations; both quantify signals levels relative to noise levels. However, a channel's dynamic range is a measure of the maximum useful range of information that can be carried by a channel, being defined as the greatest undistorted signal on that channel to the minimum detectable signal, the latter generally being assumed to be the level of noise. In terms of digital electronics, the dynamic range is sometimes considered to be the ratio of the maximum signal level and minimum signal level required to maintain a certain bit error ratio (Ippolito & Ippolito Jr, 2017).

2.4.1 Maximum Likelihood Sequence Detection (MLSD)

Maximum Likelihood Sequence Detection (MLSD) is applied at the receiver side in order to minimize error rates. Should an erasure error occur in a block, the block received at the receiver will either contain all zeros or will contain a single pulse in a codeword (Maghrabi, Kumar, & Bakr, 2017). By way of example, the PPM codeword 1010 (which corresponds to OOK 110) could be considered. An erasure error affecting the first pulse (that is, an error in the first time slot) would result in the codeword 0010 (corresponding to OOK 100 – a 1 bit error). An erasure error affecting the second pulse would result in a PPM codeword 1000 (corresponding to OOK 100 – again in error by 1 bit). In both situations, the OOK error is one bit; the average error for this codeword across the two situations is one bit in three OOK bits. Figure (2.9) shows three types of errors which are enasure error, False alarm and wrong slot. False alarm errors are considered in the same fashion, considering the average bit errors, but accounting for the different mechanisms underlying these errors. For example, consider the transmitted 1010 codeword once more. In the case of a false alarm error, the code is received as either 1110 or 1011. The MLSD generates the four possible valid codewords; the average error for the three-bit OOK word is 0.75 bits, resulting in an overall OOK error of 0.25, as M=3. The same technique is used for other codewords and the average computed. Wrong slot errors and handled in a similar fashion to false alarm errors.

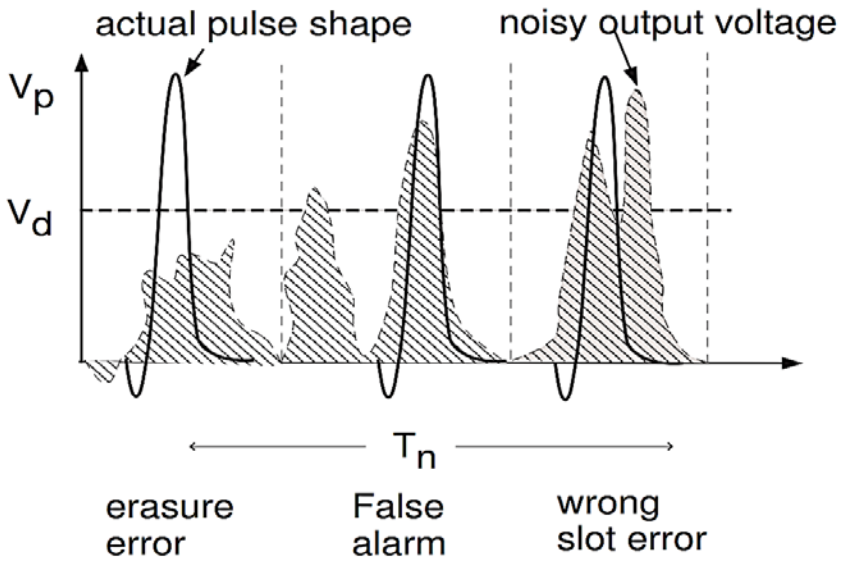


Figure 2-9 Generation of different types of error considering Gaussian type pulse shape

ISI and IFI terms are handled through the consideration of particular sequences. For example, the 11 sequence in which the second pulse is affected by ISI/IFI due to the first, which is generated when the preceding word is 0001 or 1011 (that is, there is a pulse in the final slot) and there is a pulse in the first slot of the following word (that is, 1XXX where X is the ‘don’t care’ condition). In this situation, the MSLD generates all possible sequences, calculating error probabilities in the same manner as it does with false alarms. Should MLSD not be used, the receiver would generate random errors. The process by which the MLSD generates the possible codewords in order to minimize errors is depicted in figure (2.10) (Ray, 2015).

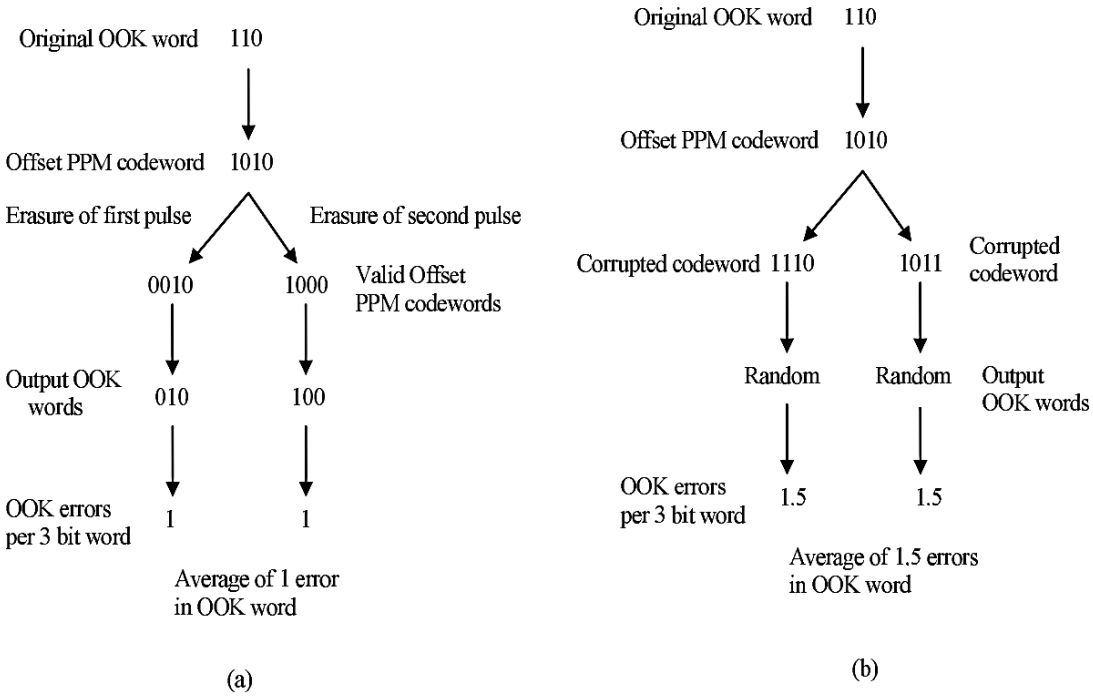


Figure 2-10 Shown how (a) erasures and (b) false alarms affect the decoding of offset PPM (M. J. Sibley, 2011)

2.5 Non-Return-To-Zero and Return-To-Zero Formats

Return-to-Zero (RZ) and Non-Return-to-Zero (NRZ) are the two most commonly used formats for the representation of digital pulse trains and are illustrated in figure (2.11). In the optical digital format, a light pulse represents the bit 1, while the absence of a pulse represents 0; the trains 10101101 are shown in figure (2.11) (Dakin & Brown, 2017).

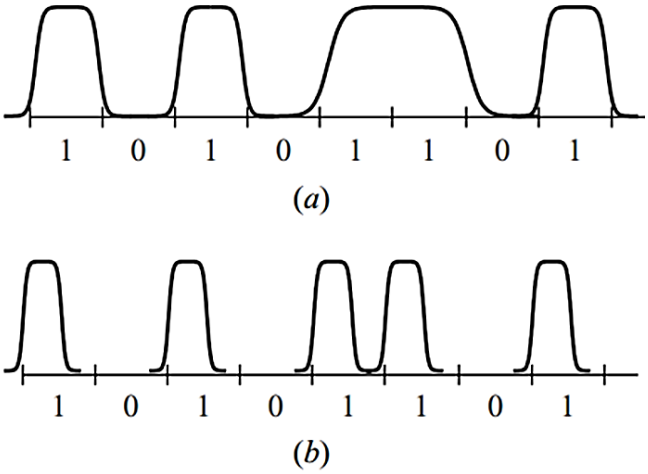


Figure 2-11 (a) NRZ and (b) RZ bit patterns corresponding to the bit sequence 10101101

The two formats differ in their behaviour in the presence of two consecutive pulses, as a result of the pulse durations. In the NRZ format, the pulse duration is equal to the period of the bit stream. Therefore, when there are two consecutive pulses, the signal does not return to zero (hence 'non-return-to-zero'), as shown in figure (2.11 a). In the RZ format, shown in figure (2.11 b), the pulse duration is a fraction of the period of the bit stream (generally one-half of the period), allowing the signal to fall back to zero between consecutive '1' pulses. The implication of this difference is that an RZ pulse sequence requires a significantly higher bandwidth, on account of the higher speed of the changes in intensity and the shorter pulses. This format is more immune to nonlinear effects and so is generally preferred when high bit rates are required (in the order of 40 Gb/2 and above) (KS Thyagarajan & Ghatak, 2007). The lower bandwidth requirement of the NRZ format makes it the more commonly used of the two formats.

2.6 (FPGA) and Microcontroller Comparison

Since the appearance of Small-Scale Integrated (SSI) circuits, containing fewer than 100 transistors on a chip, in the early 1960's, there has been a rapid development in the technology. Each decade has seen, broadly speaking, an order of magnitude increase in the number of transistors available on chips. In the late 1960's, Medium-Scale Integrated (MSI) circuit chips held several hundred

transistors, while chips in the Large-Scale Integrate (LSI) circuits of the mid-1970's contained several thousand transistors. This increase has continued through the Very Large-Scale Integrated (VLSI) circuits of the early 1980's (with 100,000 transistors per chip), the late 1980's seeing the milestone of one million transistors per chip; today, chips containing up to one billion transistors have been developed (Monmasson, 2017).

Digital logic circuits can all be constructed from three basic gates, the AND, NOT and OR gates. (NOR and NAND gates are more complex forms of gates, each containing four transistors; all such circuits can be built using only NOR or NAND gates.) The three basic gates were used in technologies such as Transistor-Transistor Logic (TTL) and supplied in chips in SSI and MSI circuits that were used throughout the early decades of digital technology for functions such as adding, decoding and multiplexing.

The advents of VLSIs enabled the provision of vast arrays of the three basic forms of gates on single chips with no predetermined functions. These enabled users to design and configure circuits to meet their individual needs, usually through the use of computer-aided applications. These chips were accordingly referred to as Programmable Logic Devices (PLDs). As technology developed, Complex Programmable Logic Devices (CPLDs) were produced, which were essentially numerous PLDs combined onto single chips.

In the 1980's, Field Programmable Gate Arrays (FGPAs) were produced to implement combinational logic. An entirely new approach to the task, they abandon the use of AND and OR gates in favour of configurable logic blocks within an array of Input/output (I/O) blocks (although two AND and two XOR gates are included for the arithmetic purposes) (Diehl, Farahmand, Yalla, Kaps, & Gaj, 2017). Digital Clock Managers (DCMs) are implemented to avoid clock distribution delays, with the additional benefit of enabling alterations in clock frequencies. Random Access Memory RAM-based FPGAs are advantageous in that they can implement significantly larger-scale

digital systems that CPLDs. FPGAs are powerful, offering equivalent capabilities to thousands of flips-flops and several million of gates (Haskell & Hanna, 2009).

2.7 VHSIC Hardware Description Language (VHDL)

A language used to describe the structure and behaviour of electronic circuitry, VHDL is the VHSIC (Very High Speed Integrated Circuits) Hardware Description Language. It was initially developed as a means of formulating standardized design practices for digital circuits in the 1980's and as a source of input to software packages intended to model the operation of digital circuits. The use of VHDL in the process of modelling circuits' operation is a benefit of its ability to simulate the behaviour of aspects of such circuits in varying levels of detail, from individual gates to the circuit as a whole. Furthermore, it is also used in the synthesis of gate level descriptions from design abstractions (such as Register Transfer Level descriptions). This enables its use in supporting the high-level design process, verifying electronic designs through simulation at high abstraction levels, prior to more detailed design using automatic synthesis. As a result of this, it has more recently found additional uses in CAD systems. The VHDL is used in design entry, the CAD system subsequently synthesizing the code into a hardware implementation of the circuit it describes (Stephen Brown, 2010; S. Brown, Brown, & Vranesic, 2008).

The original 1987 standard, IEEE Standard 1076, was significantly revised in 1993 to incorporate numerous major improvements-this was called IEEE Standard 1164 (Doulos, 2005). There have been three further revisions-in 2000, 2002 and 2008-reflecting developments in technology, of which only the most recent represented a significant revision. The result is a complex, powerful language.

2.8 Summary

- The overview of the existing literature has been reviewed to understand the concepts, implementation and performance of different types of PPM, and the corresponding encoder and decoder.
- The digital communication errors that affect the different types of PPM have been discussed.
- The difference between Non-Return-To-Zero (NRZ) and Return-To-Zero (RZ) Formats has been analysed.
- A historical improvement of Field Programmable Gate Array (FPGA) was reviewed, and a comparison with the Microcontroller has been presented.
- The VHSIC Hardware Description Language (VHDL) was discussed in this chapter as well.

3 Optoelectronics of Optical Fibre Communication System

3.1 Introduction

Optical fibre is a medium used for the data transfer that, unlike conventional copper wire-based systems, uses light rather than electricity to carry the information. As with all communication systems, fibre-optic systems range from basic, small-scale installations, such as local-area networks, to the highly sophisticated, such as national cable television networks (Lecoy, 2008). In its most simple form, a fibre-optic system comprises a transmitter that converts an electrical signal into light, a cable of optical fibres through which the light is carried and a receiver that converts the light back into an electrical signal.

3.2 Optical Transmitter

The transmitter is the first part of the communication system, from which the signal is sent. The input to an optical transmitter is an electrical signal. The transmitter contains an optical source, which converts the electrical signal into an optical signal in the form of pulses of light and inserts it into the optical fibre(s), through which it travels towards the receiver. The nature of optical fibre transmission requires the light source to be coupled to the fibre, to ensure that the signals pass into the fibre correctly.

In addition to high reliability, practicality (for example, cost and size), requirements of ideal optical sources for fibre-optic communication systems include the ability to produce light of the correct wavelength and over an area compatible with the small dimensions of optical fibre, high efficiency and the capability for modulation at high frequencies. The optical sources that best meet these requirements are semiconductor-based sources such as light emitting diodes (LEDs) and semiconductor lasers. Indeed, it has been their suitability for optical communication that has driven

the very development of semiconductor lasers since their use in practical conditions became possible after 1970 (Dakin & Brown, 2017).

3.2.1 Optical Source

The LEDs or Laser Diodes (LDs) used as sources in fibre-optic communication system transmitters are formed around semiconductor materials. Applying current to a semiconducting material causes the emission of light at a wavelength characteristic of the material. Certain wavelengths of light are more desirable for use in optical communication systems than others; the material most commonly used in sources for this purpose is gallium indium arsenide phosphide (GaInAsP), which produces light at 1.31 μm and 1.55 μm (Gallion, 2017; KS Thyagarajan & Ghatak, 2007).

While different applications impose their own specific requirements on system components, (Saleh, Teich, & Saleh, 1991) lists the most important factors of light sources for optical communication systems common to all:

- The power of the source must be sufficiently high. If the power is not high enough, the signal will have deteriorated before reaching the receiver to the extent that it cannot be accurately detected. Information will have been lost.
- The source must have a narrow spectral line width in order for the signal to maintain coherence as it travels through the optical fibre, minimizing the effect of chromatic dispersion.
- It must be possible to modulate the source power at the required speed.
- There must be no noise in the source – a lack of random fluctuations is of particular importance in coherent communication systems.
- The source must be robust, not only in terms of resilience to physical damage, but also in terms of performance. This includes insensitivity to temperature, pressure and humidity changes.

- The source must be low-cost and have good longevity.

3.2.2 Laser Diodes

Variously known as diode lasers, junction lasers or semiconductor lasers, these are one of the key forms of lasers in fibre-optic communications. Their lasing medium is one of a range of semiconductors, the material chosen for specific lasers depending on the requirements of the application. Laser diodes have characteristics that make them appropriate for use with optic-fibre communication. These include direct pumping and monolithic integration with conventional electronic circuitry and the capability of direct modulation in the gigahertz region. Moreover, they are cheap, small and, critically, compatible with optical fibres (Feng, 2017).

3.2.3 Light Emitting Diodes

Although LEDs do not meet some of the requirements of ideal characteristics of optical communications sources, it is possible to use them for this purpose. The wavelengths of the emitted light cover a relatively broad band, in the region of 30 nm to 50 nm, resulting in significant dispersion in communication systems.

In LEDs, photons are produced by electroluminescence, a process that occurs in Gallium Arsenide Phosphide (GaAsP) and Gallium Phosphide (GaP) diodes semiconductors – this is different from lasers, in which stimulated emission is the governing process. As a result, LEDS light lacks directionality, reducing the amount of light available for coupling into the small diameter of a single-mode optical fibre. Despite this, a reasonable coupling efficiency can be achieved with multi-mode fibres (for example, 4% compared to 1% for single-mode fibres). Modulation speeds achievable with LEDs are relatively low, in the order of 1 GHz. (KS Thyagarajan & Ghatak, 2007) quote the typical spectral bandwidth of a commercial 1310 nm LED as 100 nm to 170 nm and the power output -20 dBm for a 50 μm fibre.

3.3 Optical Receiver

Once the optical signal has travelled to its destination, it must be converted back to an electrical signal in order to be useful. The optical receiver accepts the signal and, in simplistic terms, performs reverses the actions performed by the transmitter – it demodulates the signal that the transmitter modulated. The signal may then undergo further processing or amplification prior to being passed to the equipment that will utilize it. A variety of classes of receivers exist, including photoconductive devices, Charge Coupled Detectors (CCDs), photomultiplier tubes and semiconductors (DeCusatis & DeCusatis, 2010).

As with the transmitter, there are a range of requirements of an effective receiver. Logistically, receivers must be compact, reliable, robust and as cost-effective as possible. However, the most fundamental requirement is that it must be able to receive the signal efficiently. This requires identification and detection of photons of the wavelength transmitted at the source. Most of the detector types previously mentioned are able to detect photons across the optical spectrum. The devices most commonly used for communication systems using optical fibres are solid state semiconductor detectors, such as the PIN photodiode (DeCusatis & DeCusatis, 2010), which is limited to certain wavelengths. The response of the receiver must be fast and it must introduce as little noise as possible into the electrical signal while receiving with as high sensitivity as possible. The receiver sensitivity is the minimum number of photons per bit required to ensure the bit error rate is below a certain value – typically 10^{-9}. As errors are generated from random variations in the numbers of photons detected as well as noise in the receiver, an ideal (noise-free) receiver requires a sensitivity of 10 photons per bit for a stabilized laser source (of at least 20 bits per pulse) in order to achieve that bit error rate.

3.3.1 Common Types of Photodetector

There are two broad categories of semiconductor photodetectors. The first category comprises those without internal gain, examples being pin, Schottky barrier, PN and MSM photodetectors. The second, used to improve the front-end photoreceiver's sensitivity, have internal gain and include photoconductors, APDs and phototransistors.

- **PN Photodiode**

They are p-n junction diodes operating under a reverse bias. Therefore, they convert light pulses into electric currents when incident photons of the appropriate wavelengths with sufficient energy to excite electrons across the material's bandgap are detected.

Receiver performance is dependent upon the optical power and the width of the depletion region in which the photons are absorbed. The optical power, determines the number of electron-hole pairs, which are separated in the depletion area; higher quantum efficiencies are achieved when the depletion region is greater. However, this is at the expense of longer drift times (and so reduced photodiode bandwidth). Therefore, the depletion zone should be chosen to achieve a suitable compromise between efficiency and speed (Fahs et al., 2017).

3.4 Photo Amplifier

The power of the signal attenuated as the signal travels through the optical fibre; the photo amplifier restores the power of optical signal without any electrical manipulation of the signal. The majority of optical amplifiers exploit the stimulated emission process used in lasers, but without the feedback process. Three methods, shown in the figure (3.1), are employed. The transmitter power can be boosted (a preferred method if adjusting for losses in the optical elements between the laser and the optical fibre) prior to the signal entering the optical fibre; this might be by means of Wavelength-Division Multiplexing (WDM), optical couplers or external optical modulators. The second method

that might be used is to use one or more in-line amplifiers in the optical fibre length – this method is used to compensate for any losses that occur during propagation (for example, over long distances). Finally, an optical pre-amplifier may be used after the optical fibre but immediately before the receiver; as the photodetector sensitivity is dependent on the signal power, this improves the performance of the receiver (Djordjevic, Ryan, & Vasic, 2010). In all three cases, the optical gain is population inversion achieved by optical or electrical amplifier pumping. In general, the gain is a function both of the local beam intensity and frequency.

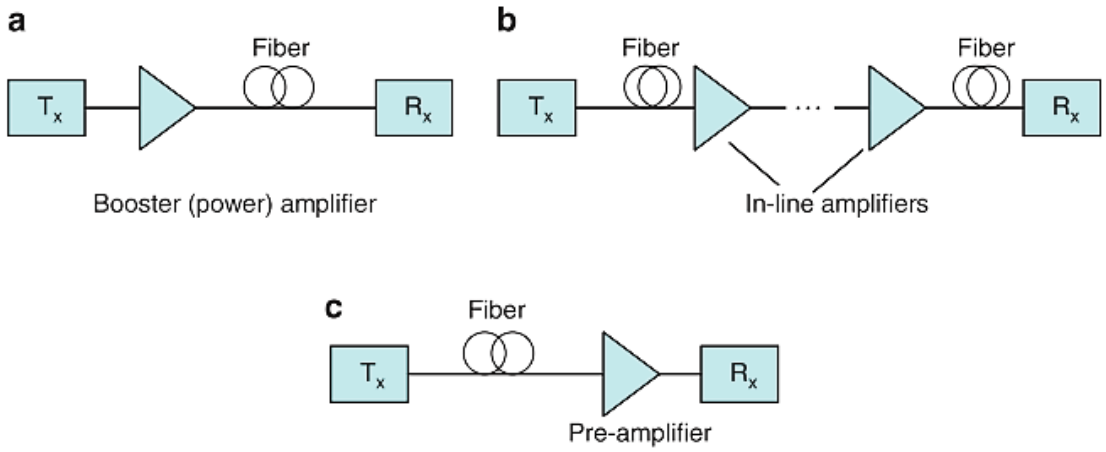


Figure 3-1 Possible applications of optical amplifiers (a) booster amplifier, (b) in-line amplifiers, and (c) preamplifier

3.5 Optical Fibre

Optical fibres depend on Total Internal Reflection (TIR); if light is inserted into the glass fibre at a sufficiently small angle, the refractive index is such that the light is reflected off the edge of the fibre rather than simply passing out of it. This phenomenon has been known since the 1850's and glass fibres been in existence for nearly a century. However, as they are not 100% efficient, practical use of optical fibres was not possible until the 1950's, following a proposal to add cladding to fibres. Prior to the 1970's, the principal use of optical fibres was medical as the signal losses over long distances in the order of 1000 dB/km were relatively unimportant in the short

distances required for such applications. In 1970, improvements in optical fibre technology, reduced losses below 20 dB/km [10] and ten years later, this had been reduced to 0.2 dB/km, initiating fibre-optic communications (Govind, 2002). Optical fibres comprise four concentric layers – the core, the cladding, the coating and the buffer as shown in figure (3.2).

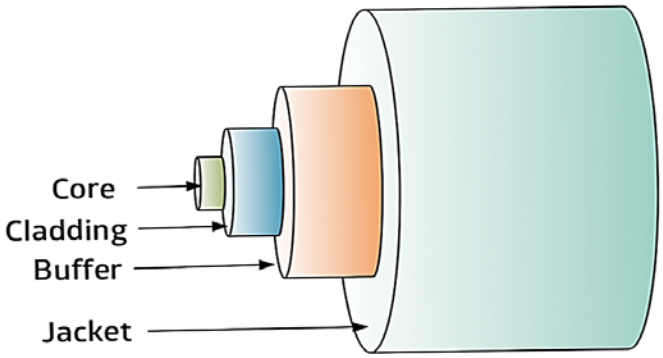


Figure 3-2 Optical fibre cable structure

The core is the glass fibre itself, in which the signal is carried. It is composed of silica or doped silica. The cladding immediately surrounds the core. As it, too, is composed of silica. Optical signals can travel in it. However, the composition of the cladding is different from that of the core. The cladding has a lower refractive index than the core, but as it higher than that of air, the cladding acts as a waveguide, the signal is better restricted to the core than it would be were the core directly surrounded by air as there is greater TIR at the core-cladding interface.

The coating comprises at least one polymer layer in which optical signals cannot travel. Its purpose is to protect the fibre and cladding from environmental and physical damage. The outermost layer, the buffer, is a little under a millimetre thick and protects the fibre during installation and termination.

3.5.1 Types of Optical Fibre

Optical fibre communication utilizes two forms of fibres –multimode and single-mode. As the name implies, in the former, light is propagated through the fibre following different paths, or ‘modes’

figure (3.3). In single-mode fibre, light follows just one mode as shown in figure (3.4). The former their different properties makes them suitable for different applications.

The core of single-mode optical fibre is thin (typically 8 microns to 9 microns) as shown in figure (3.5). This enables only one mode to travel through it, with the result that signal amplification is required only after the signals have travelled considerable distances. Therefore, single-mode fibre is used in the majority of long-haul, or long-distance, fibre-optic telephone lines.

By contrast, multimode fibres have a much thicker core – typically 50 micron or 62.5 micron as shown in figure (3.5) a core cladding ratio over six times greater than that of single-mode fibre. (Fibres of 100 microns and 140 microns are also used in some situations.) Light has greater room to move within the fibre as it propagates along its length which leads to greater distortion and loss of information. As a result, multimode cables are unsuitable for use in applications requiring the transfer of large amounts of data or high bandwidths. More frequent signal boosting is required for transfer over long distances. However, multimode cables are significantly cheaper to produce than single-mode cables (Ilyas & Mouftah, 2003).

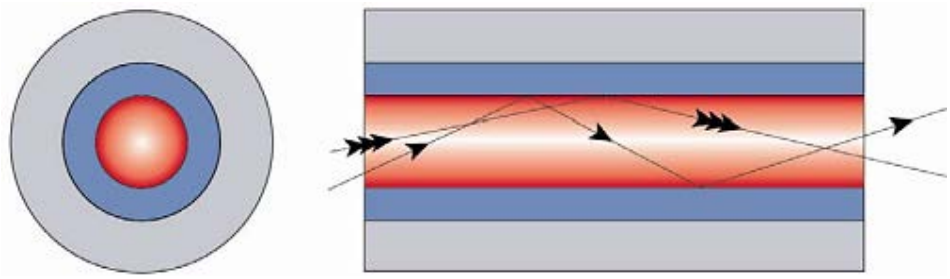


Figure 3-3 Multimode fibre light propagation

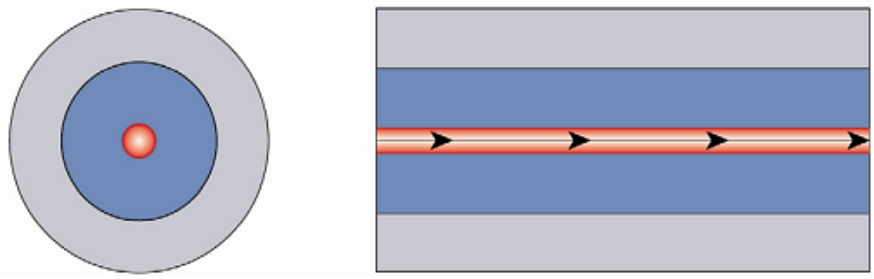


Figure 3-4 Single mode fibre light propagation

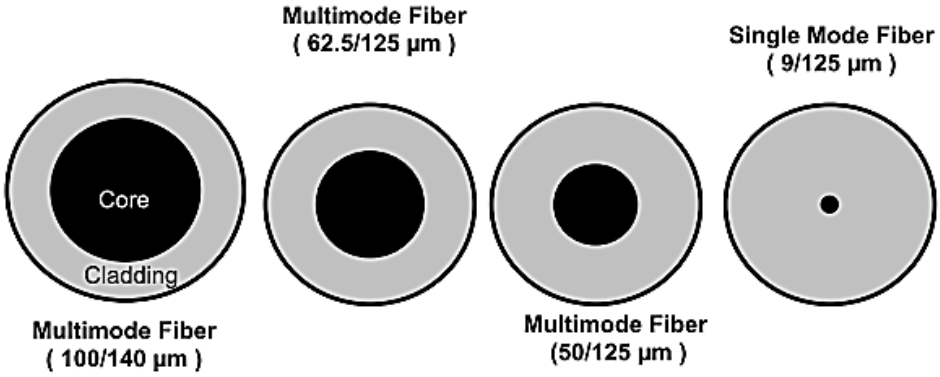


Figure 3-5 Multimode and singlemode fibres layout

3.5.2 Plastic Optic Fibre

Plastic optical fibres (POF) are generally composed of polymethyl methacrylate (PMMA) and have larger cores than silica glass multimode fibre in the order of 120 microns to 1,000 microns, which has the benefits of easy installation, as connector alignment is much easier. A further advantage is that visible and infra-red light is often used as a source. However, they are limited to short distances as the large core results in high losses in the order of several dB per kilometre.

Applications, both current and potential, of POF are, nonetheless, varied. Consumer electronics provide one of these given the particularly short distances involved, in both the home and the office contexts. For example, in entertainment systems, the ability to use infra-red sources is exploited by devices such as DVD players and the fibres can be used with both Optical Mini Jack and square connectors. They are suitable for use in the medical environment, transport control systems (such as motor vehicles and aircraft) and medical instrumentation is typical. In communications, transceiver testing requires optical loopbacks and feedbacks, for which the attenuation of POF might be useful as it lessens the likelihood of detector saturation.

Furthermore, POF can be used for short-distance communication links, with several types having been proposed as standards for this purpose. It is available both in single-mode and in multi-mode formats, a typical specification being shown in table (3.1). Lucina graded-index POF is one example (DeCusatis & DeCusatis, 2010). Constructed of CYTOP, a transparent fluoropolymer, it is

capable of transferring data at up to 1 Gbit/s over distances of 500 m. When transferring light of wavelength 850 nm (infra-red), the attenuation is in the order of 50 dB per kilometre and the bandwidth-distance product is between 200 MHz-km and 300 MHz-km.

Table 3.1 Typical specifications of plastic optical fibre used in communication applications

Parameter	***Specification***
Core diameter	980 μm
Cladding diameter	1000 μm (1 mm)
Jacket diameter	2.2 mm
Attenuation (at 850 nm)	<18dB/100mm (180dB/km)
Numerical aperture	0.30
Bandwidth (at 100 m)	Step index: 125 MHz Graded index: 500 MHz

3.5.3 Glass Optic Fibre

A laser (whose name is an acronym for Light Amplification by Stimulated Emission of Radiation) emits spatially coherent light; as described by (Svelto & Hanna, 1976), a laser beam remains confined to a small diameter over long distances traversed.

The underlying physics behind the operation of lasers is described by quantum physics. Atoms can exist only in discrete energy levels (Al-Azzawi, 2006). If an atom is excited, it moves to the state of being in a higher energy level. Atoms in the excited state can fall back to the lower energy level either spontaneously or when stimulated, releasing a photon whose energy is equal to the difference in energy between the two levels. Stimulated emission occurs when an incident photon with the same energy as the energy different between the states strikes an atom in the excited state; the released photon is identical to the incident photon (G. Agrawal, 2010). If a large number of these excited atoms are placed between two mirrors, a chain reaction is initiated when the incident photon arrives, creating a large number of these identical photons. These photons are released as a single coherent laser beam (K Thyagarajan & Ghatak, 2010).

3.6 Summary

- In this chapter, the optical transmitter, optical receiver, optical amplifier, and the optical fibre were discussed to give an introduction because they will used as an optical communication set working with Offset PPM implementation.
- Plastic Optic Fibre (POF) and Glass Optic Fibre as the main two kind of fibre optic were reviewed with useful details.

4 Offset PPM Theory

4.1 Introduction

This project concerns Offset PPM. This scheme is a new variant on the digital PPM scheme in which the line rate of a digital PPM signal is halved using the principle of a sign bit. This technique is commonly used in analogue to digital converters.

In table (4.1), the coding scheme for 3-bit PCM words is illustrated. The scheme is similar to digital PPM for PCM for words below 100 PCM; the one difference is that in Offset PPM, no pulse is transmitted for 000 PCM. For 100 PCM and higher, the 'sign' bit is introduced as the most significant bit (MSB) of the Offset PCM. Therefore, the sign bit indicates the source of the offset – that is, 000 PCM or 100 PCM. Coding continues as previously for 100 PCM and higher. Using this scheme, the Offset PPM's line rate is equal to one-half the line rate of digital PPM. The performance of the scheme is superior to that of digital PPM when applied to highly dispersive channels, despite the presence of a second pulse in some channels potentially suggesting a lower sensitivity. While similarities exist between Offset PPM and DH-PPM, the latter has a variable word length unlike the fixed word length of Offset PPM. Therefore, Offset PPM is capable of continuous data coding (M. J. Sibley, 2011).

The Offset PPM coder and receiver/decoder removes the MSB from the PCM word and delays it by 2^{M-1} time slots, as shown in the schematic in figure (4.1), generating the offset pulse as shown in table (4.1). The PCM bits that remain after the Most Significant Bit (MSB) is removed are loaded into a counter that counts down to zero. This counter generates a carry pulse; the position of this pulse in the frame varies according to the truncated PCM word. The receiver comprises a pre-amplifier and a post-amplifier. The signal is passed to a threshold crossing detector and is then decoded.

Table 4.1 Generating the offset pulse, the sign bit in offset PPM is shown in italics

Original PCM word	*Offset PPM codeword*
000	*0* 000
001	*0* 001
010	*0* 010
011	*0* 100
100	*1* 000
101	*1* 001
110	*1* 010
111	*1* 100

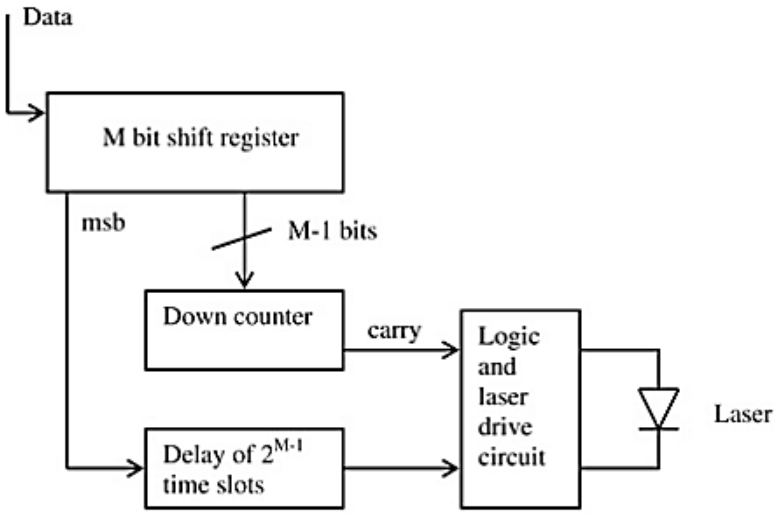


Figure 4-1 Offset PPM coder and transmitter system (M. J. Sibley, 2011)

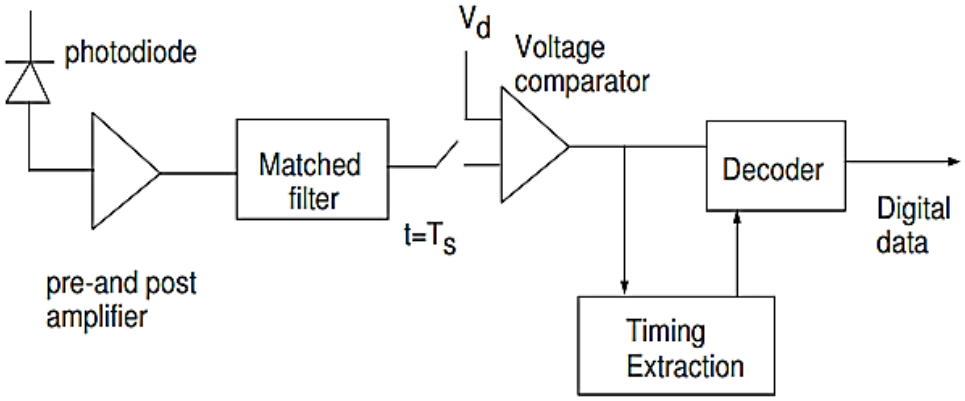


Figure 4-2 Schematic of an optical receiver system (M. J. Sibley, 2011)

This theory may be adapted to various channels. In this case, the optical channel chosen had a Gaussian impulse response such as that obtained from graded-index, plastic optical fibre, as described in (Gol'dsteyn, 1980).

4.2 Coding Scheme

There are similarities between the multiple PPM and Offset PPM, as indicated in table (4.1), which shows the coding scheme for three bits of data. Changes in the pulse position within slots are used to send information in the digital PPM scheme. Digital PPM uses twice the number of slots in one frame that are used in the equivalent Offset PPM scheme, which is similar to digital PPM except that a sign bit (most significant bit) is used. By introducing this sign bit, the line rate is reduced; in Offset PPM, no pulse is sent when the offset is taken from 0000, whereas in digital PPM, one pulse is always sent.

4.3 Errors affect Offset PPM

Offset PPM is impacted by false-alarm, wrong slot and erasure errors, as is the case with other PPM systems (McEliece, 1981). When operating with highly dispersive channels, these errors are affected by both inter-symbol interference (ISI) and inter-frame interference (IFI). The impact of ISI on a three-bit Offset PPM system, operating with 1 Gbit/s PCM data is considered in this original analysis, additionally comparing the performance with that of an equivalent digital PPM system. A maximum likelihood sequence detector, or MLDS, is implemented for digital PPM simulations, but not for the Offset PPM; this is discussed later.

In considering the probability of the three error types, the receiver output voltage noise is assumed to be a Gaussian random variable. Particular sequences are considered in investigating the impacts of ISI and IFI. First, both 0 and 1 are considered as isolated pulses. Additionally, sequences such as 01, 10, 10, 01, 11, 11, 101 and 110, in which the italicized numeral indicates the error position are considered. As described by (Ray, Sibley, & Mather, 2012), the derivations of the three types of errors (wrong slot, erasure and false alarm) are as follows.

4.3.1 Wrong slot errors

If noise on a pulse's leading edge results in a threshold crossing on an adjacent time slot, a wrong slot error occurs. The probability of a wrong slot error is given by:

$$P_s = 0.5\ erfc(\frac{Q_s}{\sqrt{2}}) \tag{4.1}$$

Where:

$$Q_s = (\frac{T_s}{2}\frac{slope(t_d)}{\sqrt{\langle n_o^2 \rangle}}) \tag{4.2}$$

Where T_s is the slot time, slope (t_d) is the slope of the received pulse at the decision time, t_d and $< n_o{}^2 >$ is the mean squared noise presented to the threshold detector. The threshold time is dependent on where the decision level is set on the received pulse. An error such as this is present when the bandwidth of the link is low; the resultant pulses have a pronounced slope.

4.3.2 Erasure errors

There is a possibility that noise will result in the output voltage crossing the threshold in an empty slot, thereby generating a false pulse. The probability of this occurring is given by:

$$P_r = 0.5\ erfc(\frac{Q_r}{\sqrt{2}}) \tag{4.3}$$

Where, T_s / τ_R is the number of uncorrelated noise samples per time slot, τ_R is the time at which the autocorrelation has become small and Q_t is given by:

$$Q_r = (\frac{v_{pk} - v_d}{\sqrt{\langle n_o^2 \rangle}}) \tag{4.4}$$

of which v_{pk} represents the peak signal voltage of a particular time slot and v_d represents the decision voltage.

4.3.3 False Alarm Errors

False alarm errors occur if any pulse is detected in the empty slot due to noise. This error can be minimized if the threshold voltage is increased and the corresponding error probability is given by:

$$P_f = (\frac{T_s}{\tau_R}) 0.5 erfc(\frac{Q_t}{\sqrt{2}}) \quad (4.5)$$

where the ratio $\frac{T_s}{\tau_R}$ represents the number of uncorrelated noise samples per time slot and τ_R is the time at which the autocorrelation function gives the minimum value.

$$Q_t = \frac{v_d - v_{ISI}}{\sqrt{\langle n_o^2 \rangle}} \quad (4.6)$$

Where v_{ISI} represents the signal voltage level at a particular time slot and depends upon the error sequences.

4.4 Summary

- In this chapter, the offset PPM design was discussed in detail in terms of theory and figures illustrated the principle of operation.
- The digital errors that affect Offset PPM were reviewed in section 4.3 with comprehensive details.

5 Offset PPM Encoder and Decoder Design, Implementation and Testing

5.1 Introduction

This chapter of the thesis presents the approach that adopted to the electronic design stage and implementation process of both the Offset PPM encoder and Offset PPM decoder. This process incorporates both the electronic components and PFGA board.

5.2 Parallel Offset PPM Encoder Design and Implementation

5.2.1 Offset PPM Encoder Design

The logic gate is either a physical or virtual device that is commonly used in the field of digital electronics. It operates using a Boolean function. The logic gate is able to generate a single logical output by performing a logical operation on a single logical input, and it can also generate a single logical output by performing a logical operation on multiple logical inputs.

The truth table for a digital circuit plays an important part in the design process. This is because the initial stage in the design of a digital circuit is to examine the truth table of the digital circuit for further information.

The truth table generated from the coding of the 3 bit Pulse Coding Modulation (PCM) to Offset Pulse Position Modulation (Offset PPM) schematic is illustrated in table (5.1). From examining the truth table, it is clear that the digital electronic circuit in question is designed with a 3-pin input. It is also evident from the table that the digital electronic circuit is designed with a 4-pin output. There are a total of eight states demonstrated by the inputs. These states begin with the binary code (000) and end with the binary code (111).

Table 5.1 Truth table of Offset PPM encoder

State #	Input/PCM (3 pin)			Output/Offset PPM (4pin)			
	A	B	C	D	E	F	G
1	0	0	0	0	0	0	0
2	0	0	1	0	0	0	1
3	0	1	0	0	0	1	0
4	0	1	1	0	1	0	0
5	1	0	0	1	0	0	0
6	1	0	1	1	0	0	1
7	1	1	0	1	0	1	0
8	1	1	1	1	1	0	0

The output of the encoder is a parallel 4 pin. Based on the data presented in the truth table, as shown above, a total of four Boolean equations have been developed in this test. These equations are outlined below, with each equation relating to each of the four pins:

$$D = A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC \tag{5.1}$$

$$E = \bar{A}BC + ABC \tag{5.2}$$

$$F = \bar{A}B\bar{C} + AB\bar{C} \tag{5.3}$$

$$G = \bar{A}\bar{B}C + A\bar{B}C \tag{5.4}$$

Based on the results of the four equations presented above, it is understood that in order for the coding circuit to be implemented, it is necessary to provide ten (3-input AND gate), one (4-input OR gate) and three (2-input OR gate). The Karnaugh map, or K-map, is a valuable tool that can be found online and helps to simplify Boolean equations so that they can be better worked with by researchers and other users. Therefore, in order to simplify the four aforementioned equations, the Karnaugh map method has been adopted in this study and will now be outlined in further detail.

This enabled the researcher to minimise the quantity of logic gates and the quantity of inputs in relation to the other gates. The application of the Karnaugh map method in the simplification of the four equations presented above is demonstrated in further detail in the following four diagrams, figure (5.1), figure (5.2), figure (5.3) and figure (5.4):

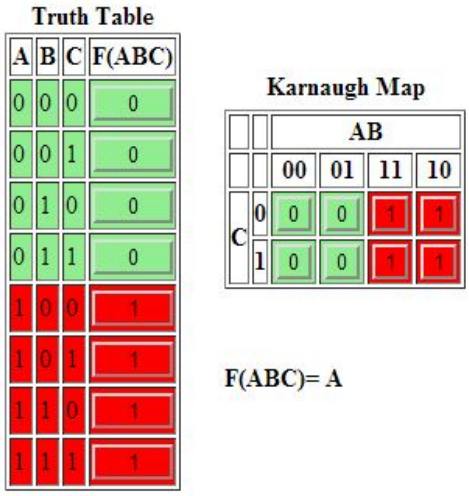


Figure 5-1 Karnaugh map application for pin (D)

The simplification of the equation for pin (D) using the Karnaugh map technique is illustrated in figure (5.1). This provides the following output:

$$D = A \tag{5.5}$$

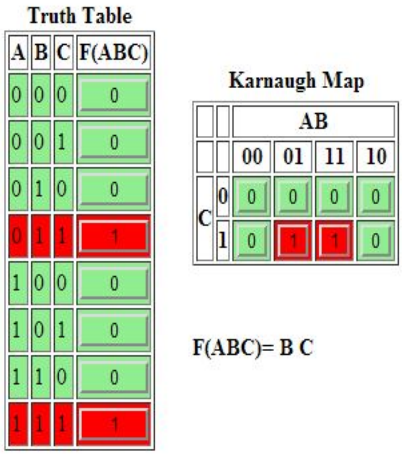


Figure 5-2 Karnaugh map application for pin (E)

The simplification of the equation for pin (E) using the Karnaugh map technique is illustrated in figure (5.2), this provides the following output:

$$E = BC \tag{5.6}$$

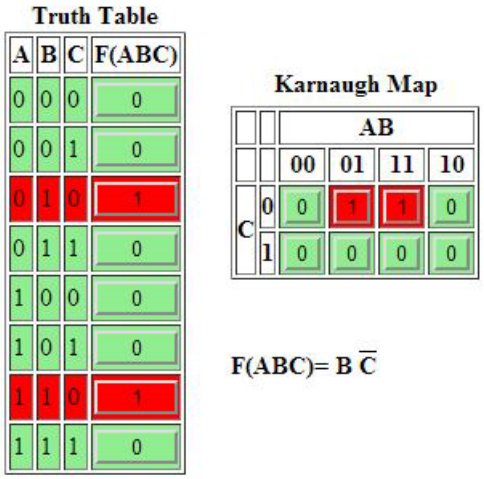


Figure 5-3 Karnaugh map application for pin (F)

The simplification of the equation for pin (F) using the Karnaugh map technique is illustrated in figure (5.3), this provides the following output:

$$F = B\bar{C} \tag{5.7}$$

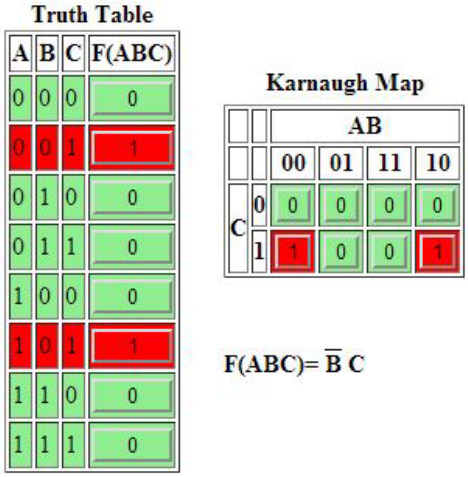


Figure 5-4 Karnaugh map application for pin (G)

The simplification of the equation for pin (G) using the Karnaugh map technique is illustrated in figure (5.4), this provides the following output:

$$G = \bar{B}C \tag{5.8}$$

Therefore, it is evident that three (2 input AND) gates and two inverters are required in order to complete the implementation of the Offset PPM encoder to code the (3 bit) PCM input to a (4 bit) output. The four equations outlined above have now been simplified as much as they can be, using the Karnaugh map application. A total of three (2-input AND) gates and two inverters are needed in order to implement the Offset PPM encoder designed to code a 3-input PCM. The hardware design for the Offset PPM encoder's electronic circuit is presented in figure (5.5).

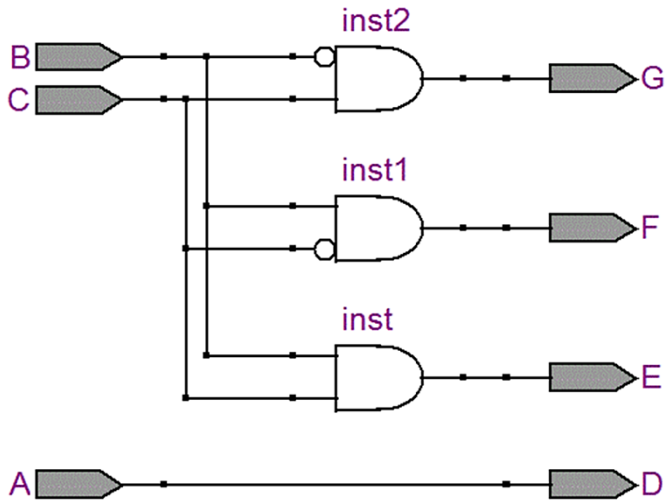


Figure 5-5 Offset PPM encoder Schematic

5.2.2 Offset PPM Encoder Hardware Implementation

This research adopts two different hardware configurations from the theoretical design literature in order to implement the offset PPM design. The first approach is the use of logic electronic components for hardware implementation, whilst the second approach is the use of Field Programmable gate Array (FPGA) for hardware implementation.

5.2.3 Encoder Hardware Implementation

The circuit used in this project was wired and connected using a Limrose board. The circuit contains two different types of chips. The first type of chip is used as an inverter, and is the DM74LS04; and the second type of chip is used as the triple 3-input AND Gate, and is the

DM74LS11. As noted earlier in this thesis, there are a total of eight possible states in a 3-input circuit. These states begin with (000) and end with (111). The incorporation of these eight states in the full implementation of the circuit is demonstrated in figure (5.6).

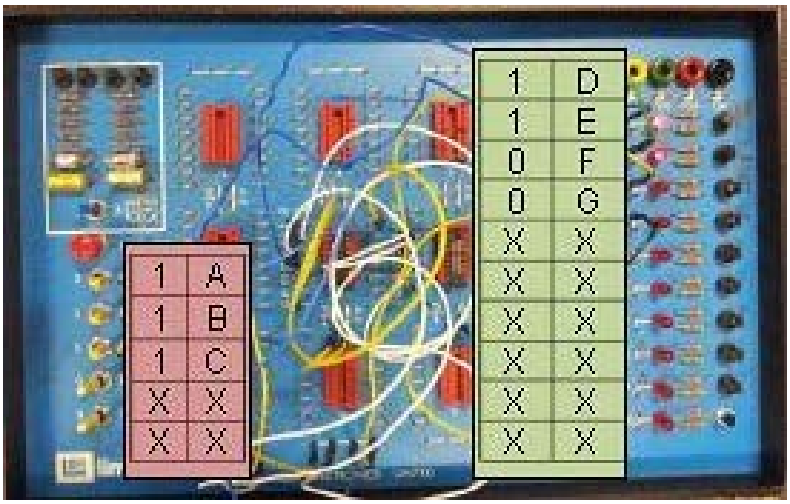


Figure 5-6 Offset PPM encoder implementation using a Limrose board

5.2.4 Offset PPM Encoder FPGA Implementation

The hardware implementation for the offset PPM encoder with the use of the FPGA approach is illustrated in figure (5.7). There are two different sets of switches contained within the FPGA. Either set can be utilised as an input to the FPGA board. There are various kinds of displays associated with the FPGA. One type of display is LED lights. In the current test, one of the two sets of dipswitches was utilised as the Pulse Position Modulation (PCM) input word. The eight states were produced using the first three witches, beginning with the digital word (000) and ending with the digital word (111). In this test, the green LED set was utilised as the output. The output of the Offset PPM encorder was shown by the output in the first four LEDs. Figure (5.7) illustrates all of the states.

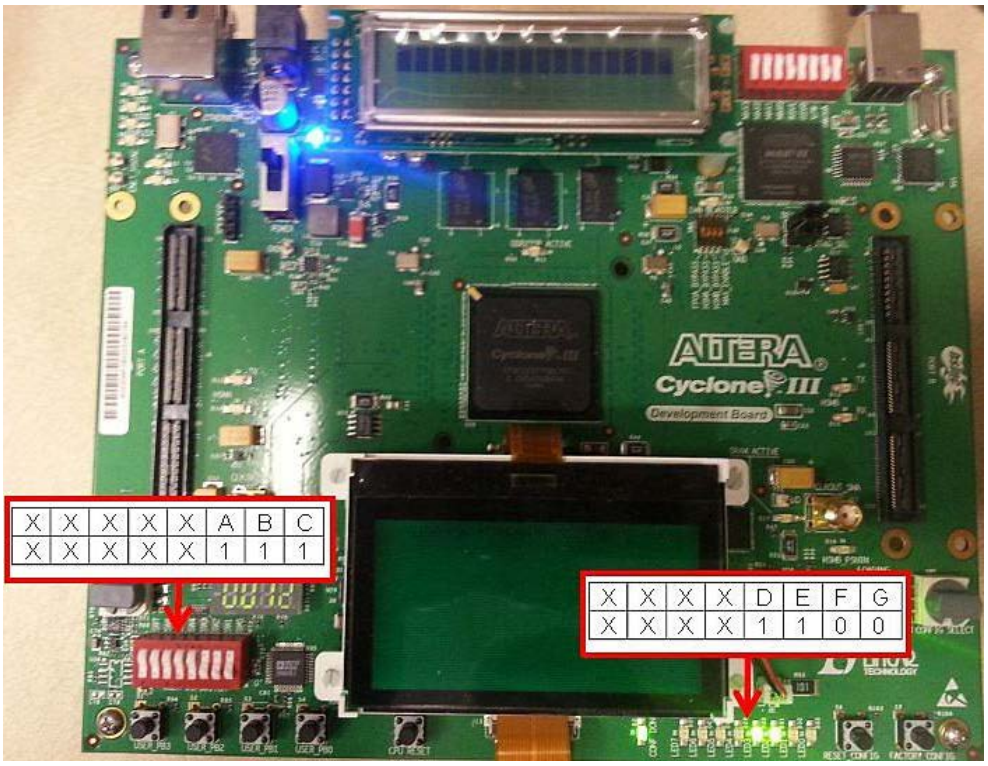


Figure 5-7 FPGA hardware implementation for the Offset PPM encoder

5.3 Parallel Offset PPM Decoder Design and Implementation

5.3.1 Offset PPM Decoder Design

Generally speaking, the Offset PPM Decoder design stage and implementation process are no different to the design and implementation approach for the Offset PPM Encoder. As with the design process for the Offset PPM Encoder, the first step that must be taken is to examine the truth table for the Offset PPM Decoder. In this case, the truth table shows 16 states, beginning with the binary word (0000) and ending with the binary word (1111).

Based on the data presented in the truth table shown table (4.1), a total of three equations have been established. These equations are outlined below, with each equation relating to each of the three output pins:

Table 5.2 Truth table for the Offset PPM Decoder

State #	Input/Offset PPM (4pin)				Output/PCM (3pin)		
	D	E	F	G	A	B	C
1	0	0	0	0	0	0	0
2	0	0	0	1	0	0	1
3	0	0	1	0	0	1	0
4	0	0	1	1	0	0	0
5	0	1	0	0	0	1	1
6	0	1	0	1	0	0	0
7	0	1	1	0	0	0	0
8	0	1	1	1	0	0	0
9	1	0	0	0	1	0	0
10	1	0	0	1	1	0	1
11	1	0	1	0	1	1	0
12	1	0	1	1	0	0	0
13	1	1	0	0	1	1	1
14	1	1	0	1	0	0	0
15	1	1	1	0	0	0	0
16	1	1	1	1	0	0	0

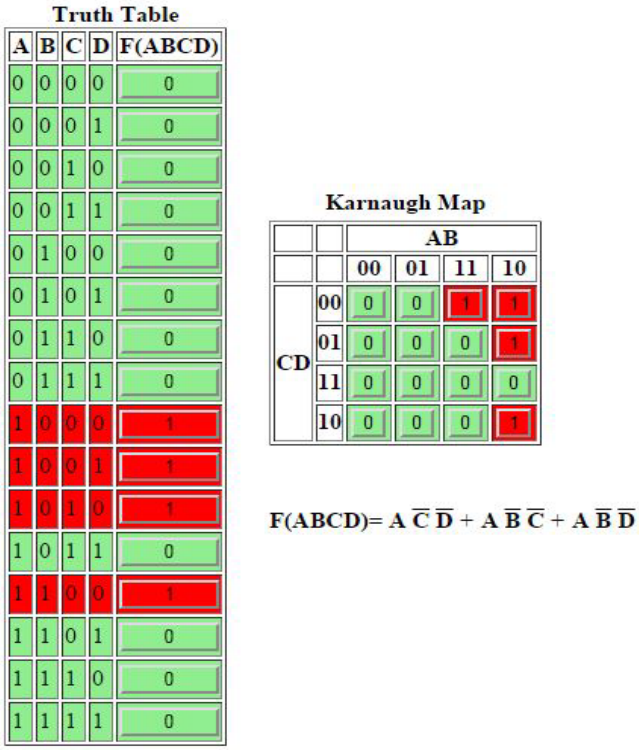
$$A = D\bar{E}\bar{F}\bar{G} + D\bar{E}\bar{F}G + D\bar{E}F\bar{G} + DE\bar{F}\bar{G} \tag{5.9}$$

$$B = \bar{D}\bar{E}FG + \bar{D}E\bar{F}\bar{G} + D\bar{E}F\bar{G} + DE\bar{F}\bar{G} \tag{5.10}$$

$$C = \bar{D}\bar{E}\bar{F}G + \bar{D}E\bar{F}\bar{G} + D\bar{E}\bar{F}G + DE\bar{F}\bar{G} \tag{5.11}$$

Based on the results of the three equations presented, it is understood that in order for the Offset PPM Decoder design to be fully implemented, it is necessary to incorporate twelve (4 pin AND gate) and three (4 pin OR gate). The Karnaugh map is used again in order to simplify the three aforementioned equations. The application of the Karnaugh map method in the simplification of the

three equations presented above is demonstrated in further detail in the following three diagrams, figure (5.8), figure (5.9) and figure (5.10):



Truth Table

A	B	C	D	F(ABCD)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Karnaugh Map

		AB			
		00	01	11	10
CD	00	0	0	1	1
	01	0	0	0	1
	11	0	0	0	0
	10	0	0	0	1

$F(ABCD) = A\,\overline{C}\,\overline{D} + A\,\overline{B}\,\overline{C} + A\,\overline{B}\,\overline{D}$

Figure 5-8 Karnaugh map for pin A

The simplification of the equation for pin A using the Karnaugh map technique is illustrated in Figure (5.8), this provides the following output:

$$A = D\bar{F}\bar{G} + D\bar{E}\bar{F} + D\bar{E}\bar{G} \qquad (5.12)$$

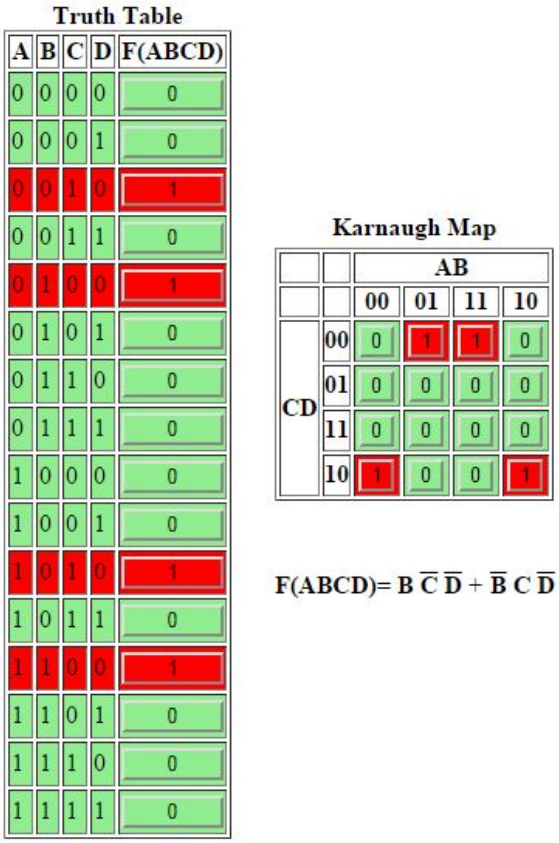


Figure 5-9 Karnaugh map for pin B

The simplification of the equation for pin B using the Karnaugh map technique is illustrated in Figure (5.9), this provides the following output:

$$B = E\bar{F}\bar{G} + \bar{E}F\bar{G} \tag{5.13}$$

Truth Table

A	B	C	D	F(ABCD)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Karnaugh Map

		AB			
		00	01	11	10
CD	00	0	1	1	0
	01	1	0	0	1
	11	0	0	0	0
	10	0	0	0	0

$F(ABCD) = B\,\overline{C}\,\overline{D} + \overline{B}\,\overline{C}\,D$

Figure 5-10 Karnaugh map for pin C

The simplification of the equation for pin C using the Karnaugh map technique is illustrated in figure (5.9), this provides the following output:

$$C = E\bar{F}\bar{G} + \bar{E}\bar{F}G \tag{5.14}$$

The design of the Offset PPM Decoder has been simplified as much as possible through the use of the Karnaugh map technique. Based on the results, it can be seen that seven (3 pin AND gates), four (2 pin OR gates) and one (3 pin OR gate) are needed. Figure (5.11) illustrates the circuit schematic for the Offset PPM Decoder:

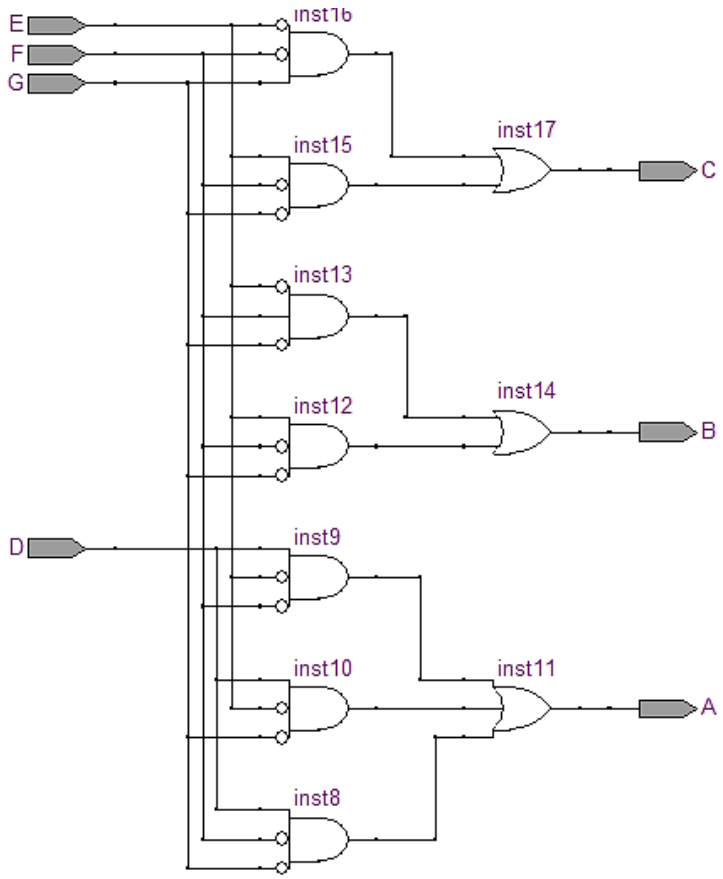


Figure 5-11 Offset PPM decoder schematic

5.3.2 Offset PPM Decoder Hardware Implementation

As with the implementation of the Offset PPM Encoder, the implementation process for the Offset PPM Decoder adopts two different hardware configurations based on the theoretical design literature. The first approach, again, is the use of logic electronic components for hardware implementation, whilst the second approach is, again, the use of Field Programmable gate Array (FPGA) for hardware implementation. Thus, there is no difference between the approaches used during the design implementation phase for the Offset PPM Decoder and the design implementation phase for the Offset PPM Encoder. With the three equations having been simplified as much as possible, the total quantity of logic gates needed to implement the design for the Offset PPM decoder in order to decode a (4 input offset PPM) code are seven (3 pin AND) gates, four (2 pin OR) gates, and one (3 pin OR) gate.

5.3.3 Offset PPM Decoder Hardware Implementation

The circuit used in this project was wired and connected using a Limrose board, as with the Offset PPM Encoder. Here, three different electronic components were used. The first type of component was an inverter, DM74LS04, as in the previous case. The second type of chip was used as the triple 3-Input AND Gate, and was the DM74LS11, as before. The third component was the DM7427 as the triple 3-input OR gate. As illustrated in the truth table for the Offset PPM Decoder, there are a total of 16 possible states. These states begin with the binary word (0000) and end with the binary word (1111). The incorporation of these 16 states in the full implementation of the circuit is demonstrated in figure (5.12):

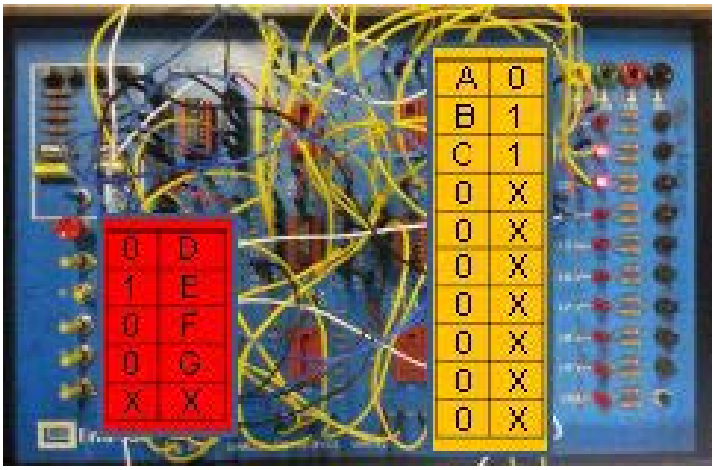


Figure 5-12 Offset PPM decoder implementation using a Limrose board

5.3.4 Decoder FPGA Implementation

The hardware implementation for the Offset PPM Decoder with the use of the FPGA approach is illustrated in figure (5.13). Again, there are two different sets of dipswitches contained within the FPGA. Either set can be utilised as an input to the FPGA board. There are various kinds of displays associated with the FPGA. One type of display is LED lights, as noted earlier. In the current test, one of the two sets of dipswitches was utilised as the Offset PPM input word. The eight states were produced using the first four switches, beginning with the digital word (0000) and ending with the

digital word (1111). In this test, the green LED set was utilised as the output. The output of the Offset PPM Decoder was shown by the output in the first three LEDs. Figure (5.13) illustrates all of the states.

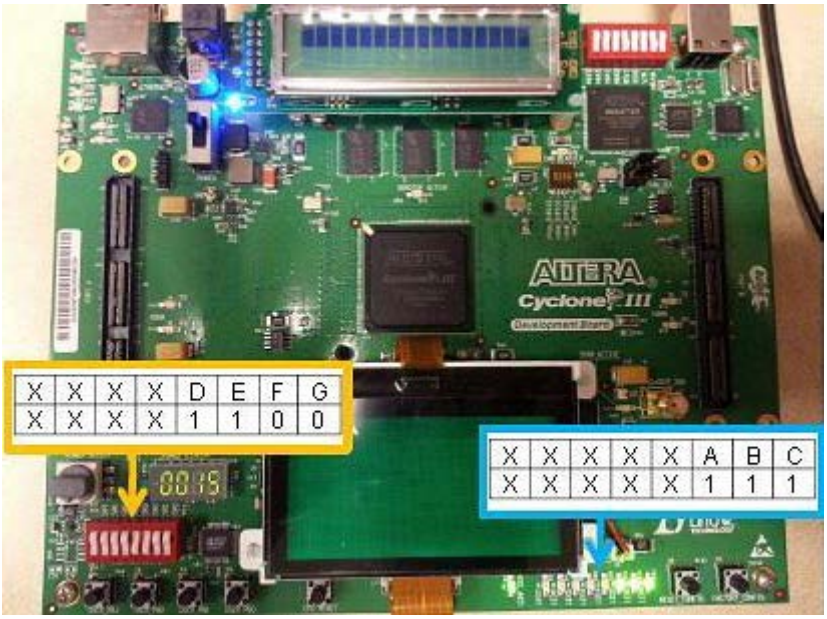


Figure 5-13 FPGA implementation for the Offset PPM decoder

5.4 Summary

- A full design of an Offset PPM encoder and Offset PPM decoder were presented in this chapter.
- Hardware implementations of Offset encoder and decoder were fully analysed using both the electronic components and FPGA.
- The tests of designs and implementations were found to be operating without any issues or errors.

6 VHDL Source Code, Simulation, and Implementation of Offset PPM

6.1 Introduction

This chapter describes the VHDL circuits that have been designed for the Offset PPM encoder and decoder system. All the VHDL designs have been listed in Appendix (9.1). Offset PPM encoder and decoder main section includes an FPGA PLL block for clock division and clock extraction, maximum length PRBS PCM input generator circuit, Offset PPM encoder system which has been implemented using schematic design technique, a (SIPO) register, finally the decoder for the system. The decoder has been designed using both schematic method using discrete logic gates in VHDL. An Altera © Quartus™ II design software has been used for all the VHDL design purposes.

6.2 VHDL and FPGA

6.2.1 VHDL

The Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) can be used for logic circuits. Unlike languages such as C or Java, which are general purpose languages, VHDL is specifically intended for designing digital systems that use hardware implementations. It is capable of supporting design hierarchies in different methodologies and is created under IEEE standards as shown in figure (6.1).

The design of a complete electronic system typically becomes increasingly complicated with higher numbers of gates and hardware implementation. This problem can be mitigated through the use of VHDL, which enables a top-down methodology for a given system. By writing a code in VHDL for a given system, a designer can test the system in real time before actually implementing the system in hardware. This assists in saving time and cost, as these simulations help to identify potential

errors in the system and so allow the system designer to take corrective action in advance (Hunter & Johnson, 1996).

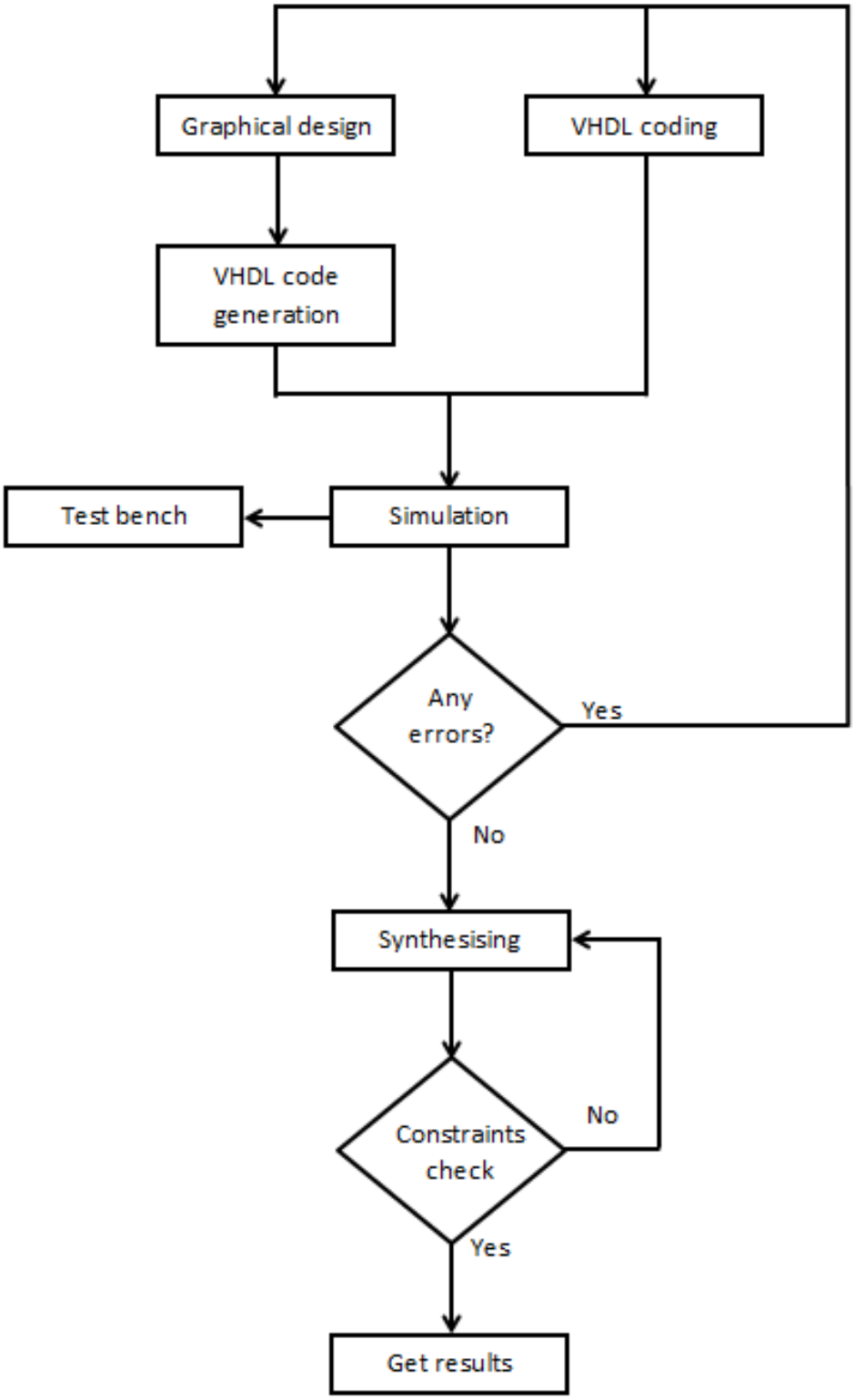


Figure 6-1 VHDL Implementation flow chart

The block diagram in figure (6.2) describes the complete design of the Offset-PPM through VHDL programming language and Altera Quartus II software.

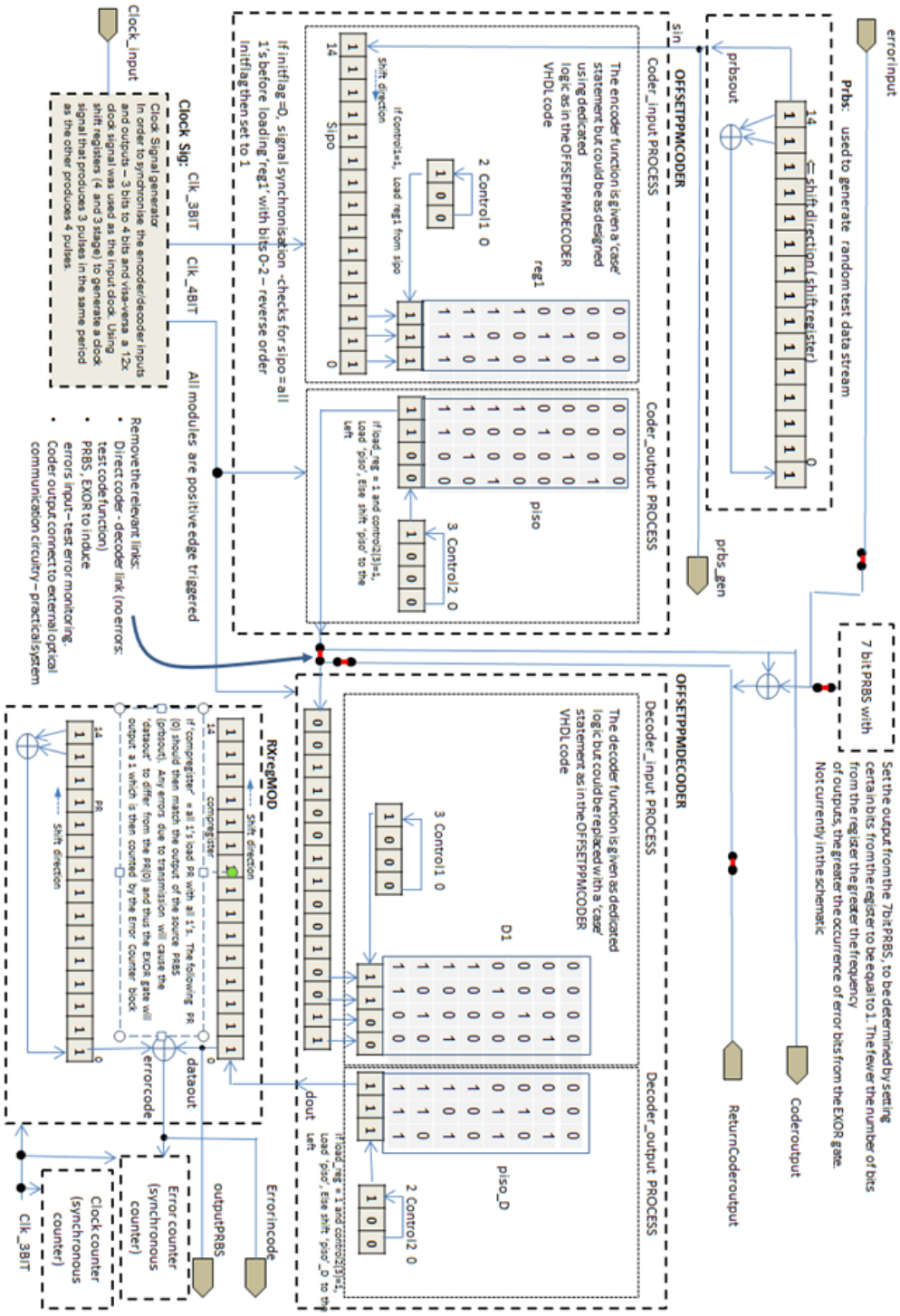


Figure 6-2 Offset PPM VHDL code sequence

6.2.2 Field Programmable Gate Arrays (FPGA)

(Altera, 2016) states that a Field Programmable Gate Array (FPGA) is a highly sophisticated hardware electronic board utilized in designing digital electronic circuitry. There are many benefits to the use of FPGAs in the design process. They are used to improve the performance of systems, irrespective of the degree of multiplication used, on account of the short delays in the transmission operations and low external noise levels. On a practical level, FPGAs are controllable by a range of software, including Xilinx and Quartus. Of the different models used in the hardware platform, one is the Cyclone III, which can be used as a transmission system interface unit in which bins are allocated and the entire design downloaded. The Cyclone III offers high efficiency and speed, low power consumption and a large memory interface. The FPGA includes a general-purpose microprocessor, which enables design models to be partitioned for a range of tasks, allowing simulators in cases such as these to test results in advance, as described by (Altera, 2016).

6.3 Cyclone III Development Board

The Cyclone III development board, shown in figure (6.3), presents hardware in setting up and developing high-volume, low-power and feature-supported designs. It can be used for several purposes, including wireless, image and video processing and high-bandwidth parallel processing systems. Altera (2013) lists are number of features of the board:

- 8 LEDs.
- Power use display.
- 4 push buttons.
- 256 MB dual channel DDR2 SDRAM (data width: 72 bit).
- High logic density (allows a large number of functions to be secured).
- Embedded memory (enables the support of high-bandwidth system designs).

- 2 Altera High-Speed-Mezzanine Card (HSMC) connectors for expansion.
- Support for dual-channel DDR SDRAM and low-power SRAM.
- Support for high-speed external memory.

The Cyclone III development board offers different benefits:

- Density-optimized FPGA and power-optimized FPGA at a lower cost.
- Industry leading FPGA in terms of multiplier-to-logic ratio efficiency.
- The power optimization feature of the Quartus II development software.
- The ability to secure memory-intensive and high-volume standards through the low-power, low-cost Cyclone III FPGA.

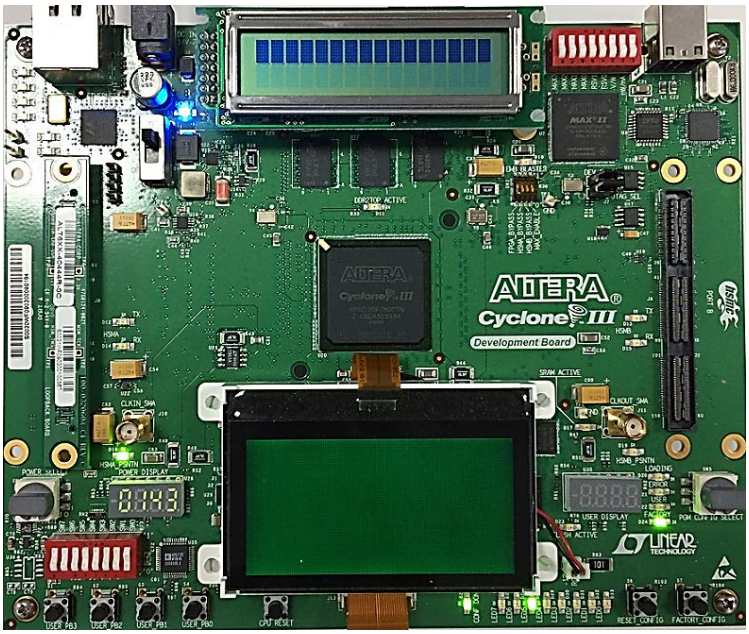


Figure 6-3 Cyclone III FPGA

6.3.1 SMA Breakout Cables

The two HSMC interfaces mentioned above enhance both the single-ended signalling and the differential signalling. (Connector part number: Samtec ASP-122953-01.) The interfaces, referred to as Ports A and B, support SM Bus, JTAG and clock outputs and inputs – including power for

compatible HSMC cards. Such HSMC daughter cards can be used to extend the coverage of the development board (Altera, 2016).

Three banks, Bank 1, Bank 2 and Bank 3 are contained within the system (Altera, 2016). Of the 172 pins in the HSMC connector, 39 are power pins, 120 signal pins and 13 ground pins. The grounds pins are seen between the shield and reference rows of signal and power pins. Bank 1 transceiver signals intended for PCI Express, Rapid I/O and other clock-data-recover (CDR systems) are not supported by the development board; rather, these 32 pins are allowed to float. Bank 2 and Bank 3, by contrast, are fully functional. They can, as shown in figure (6.4), be applied in either of two configurations.

Figure (6.5) illustrates a breakout cable produced by Altera and Samtec that is used to manage one bank of the HSMC connector to SMA cables using differential pins. This cable has high signal integrity and, when SMA connectors are used, offers a highly flexible connection system, although its use is not without its challenges.

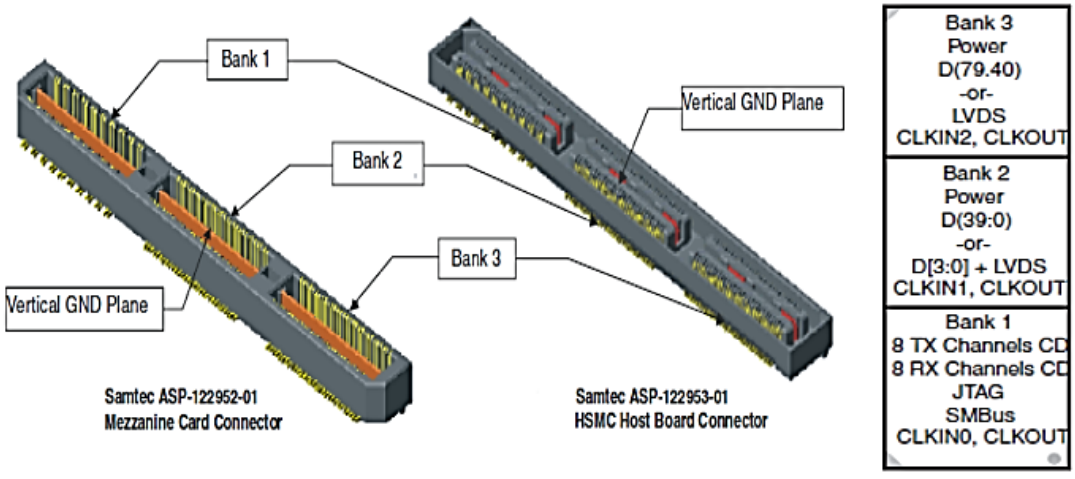


Figure 6-4 MC Connectors (Altera, 2015)

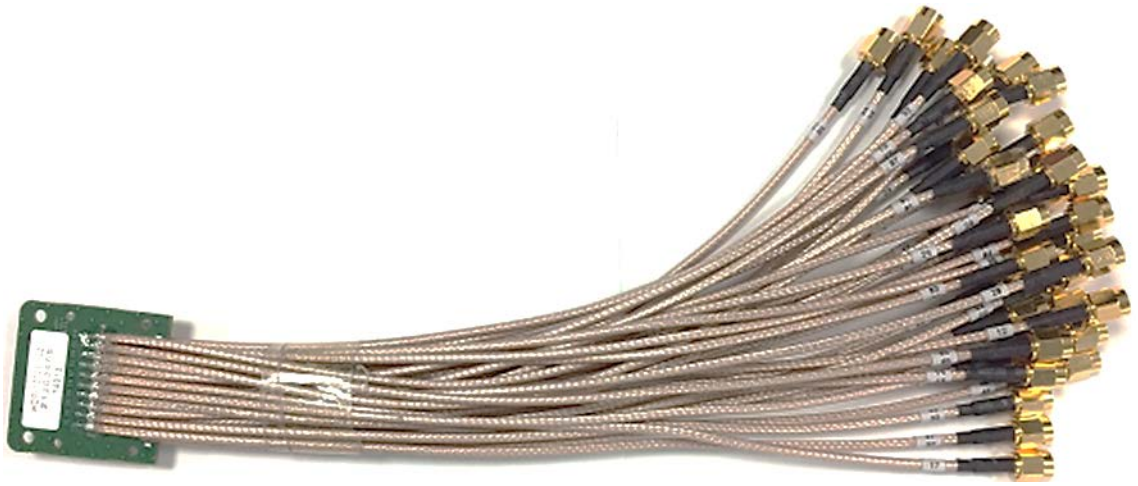


Figure 6-5 SMA Breakout Cable

6.4 System Schematic

The Offset PPM system implementation start with a parallel stage followed by two main stages, the third stage is the final implementation that an optimum with coding The PCM. Figure (6.6) shows the initial stage of implementation, this figure show a general schematic of the Offset PPM system. The parallel data block on the transmitter side generates a random parallel sequence, which is coded by the parallel Offset PPM encoder. At the receiver side, the Offset PPM data is received by the parallel Offset PPM decoder and converts in back into its initial format. This initial stage of implementation is to verify the results in chapter 5.

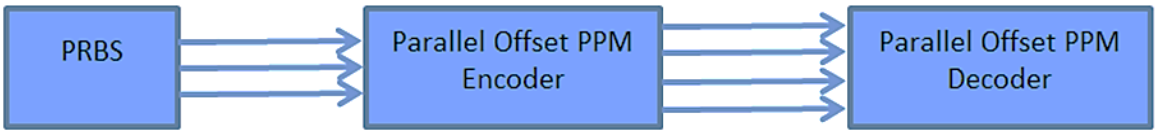


Figure 6-6 Block Diagram of Parallel Offset PPM coding

Figure (6.7) shows a schematic of first versions of serial Offset PPM encoder and serial Offset PPM decoder, the conversion between parallel and serial data was performed using the Parallel-In to Serial-Out (PISO) and Serial-In to Parallel-Out (SIPO) Convertors as shown in the figure below.

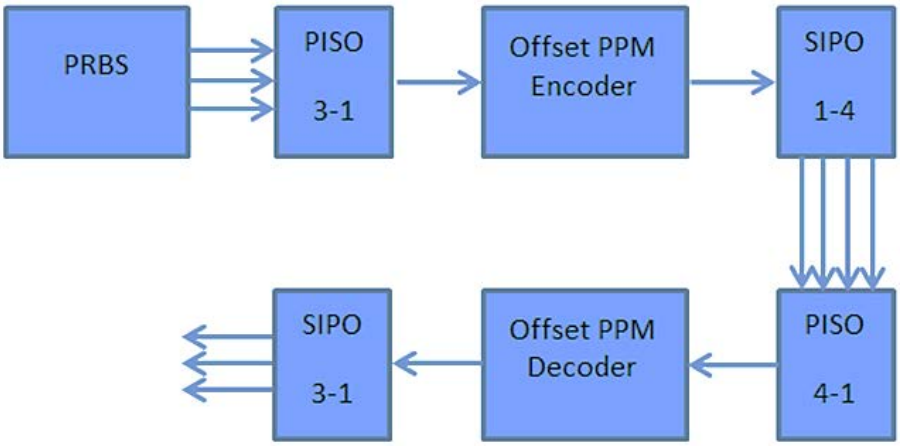


Figure 6-7 Block Diagram of First version of serial Offset PPM coding schematic

Figure (6.8) shows a final schematic of the Offset PPM system. The PRBS block on the transmitter side generates a random PCM sequence, which is coded by the Offset PPM encoder. At the receiver side, the Offset PPM data is received by the Offset PPM decoder and converts in back into PCM format.

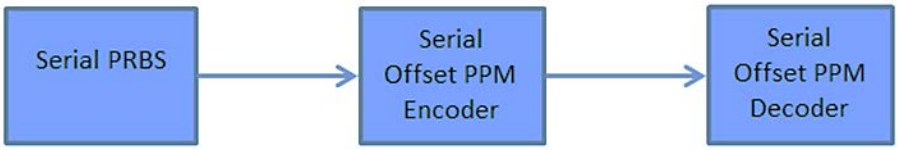


Figure 6-8 Block Diagram of Serial Offset PPM

6.5 Offset PPM system Components

The next step was to design and build the system of the Offset PPM testing, Different components are described in this section. The use of these components depends on the system implementation. There are two main projects to implement; the first one is a parallel Offset PPM. It is used to verify the results in chapter 5, and the second one is a serial Offset PPM that is the main task in this thesis.

6.5.1 Phase-locked Loop (PLL) Clock

Figure (6.9) illustrates the integration of PLLs into the FPGA in schematic block diagram form, a clock design method used to compensate for any latency in the Offset PPM system, reducing the

effects of delay and phase synchronization problems. The design in the diagram requires that the PLL block be operated with the manufacturer's clock control block in order for the Cyclone III's FPGAs, as it features a significant number of clock division ratios. It was necessary for the clock signals to be available to all parts of both circuits in the form of dedicated clock signals. This ensures that any clock delays are avoided.

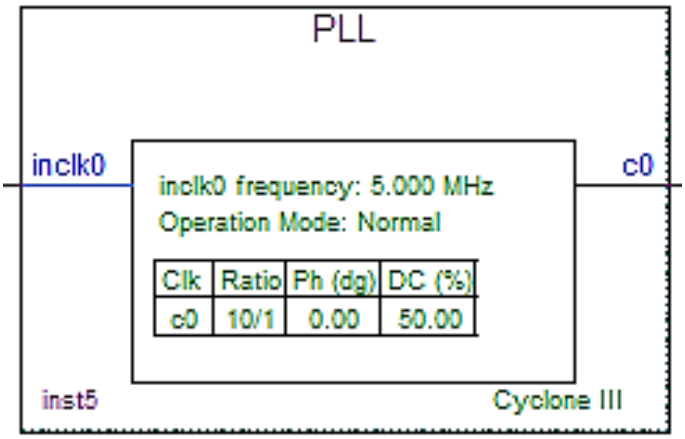


Figure 6-9 Offset PPM PLL design for clocking requirements

Figure (6.10) illustrates the results of the PLL clock generation simulation. The Master Clock is the PLL system input clock from either the external SMA clock or the internal 50 MHz source.

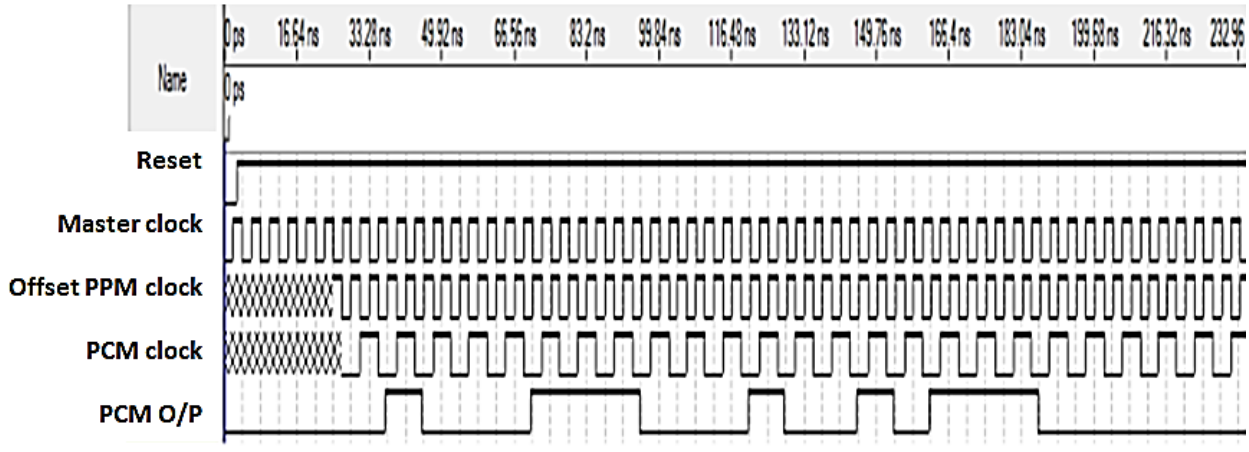


Figure 6-10 PLL clock generation simulation result

6.5.2 Pseudo Random Binary Sequence (PRBS)

The OOK PCM input to the Offset PPM encode system will be simulated by a shift register, implemented as a Pseudo-Random Binary Sequence (PRBS) generator. The result is that the system will be analysed more effectively and the PRBS sequences will be generated both in phase and appropriately for the BER test system. Figure (6.11) shows the main section of the PRBS generator VHDL code

```
ENTITY prbs IS
     GENERIC(n: natural := 7);     --(set to 7 or 15
     --this enables different sized PRBS generators
     PORT
      (  clk_3BIT       : IN STD_LOGIC;
         reset          : IN STD_LOGIC;
         prbsout     : OUT STD_LOGIC
         --trigger       : OUT STD_LOGIC
         );
    END prbs;

ARCHITECTURE behv OF prbs IS

SIGNAL  PR     :  STD_LOGIC_VECTOR (n-1 downto 0);

BEGIN
        PROCESS(clk_3bit, reset)
        BEGIN
```

Figure 6-11 Main section of the PRBS generator VHDL code

Figure (6.12) shows the annotated waveforms of the simulation results from the Offset PPM system's PRBS PCM data generation.

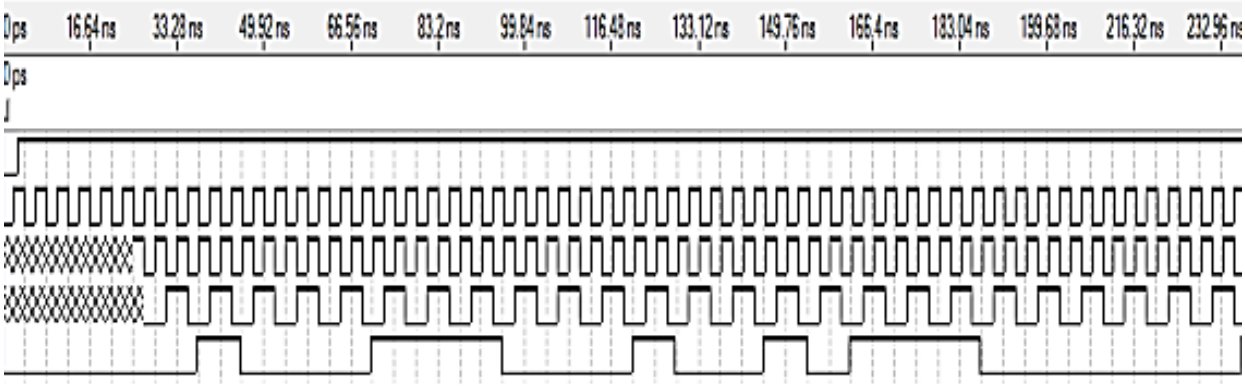


Figure 6-12 PRBS data generation in VHDL

6.5.3 Parallel Offset PPM Encoder

Figure (6.13) shows the main section of the parallel Offset PPM encoder code designed to acquire the theoretical output as described in section 4.1 (Table 4.1). This encoder converts the 3-bit sequences into 4-bit Offset PPM code sequences, as shown in that table. The 3-bit sequences used as the input to the parallel Offset PPM encoder were generated by the counter discussed in the previous section.

```
ENTITY OFFSETPPMCODER IS
port(    sin          : IN STD_LOGIC;
        clk_3bit   : IN STD_LOGIC;
      clk_4bit     : IN STD_LOGIC;
        dout       : OUT STD_LOGIC
       );
end OFFSETPPMCODER;
architecture behaviour of OFFSETPPMCODER IS

   SIGNAL    control1     : STD_LOGIC_VECTOR(2 downto 0); --:= "100";-- chan
since taking 6 blocks of 3 instead of 5.
   SIGNAL     sipo     : STD_LOGIC_VECTOR(14 downto 0) := "000000000000000";
   SIGNAL     piso     : STD_LOGIC_VECTOR(3 downto 0);
   SIGNAL     reg1     : STD_LOGIC_VECTOR(2 downto 0) := "000";
-- SIGNAL     D2          : STD_LOGIC_VECTOR(2 downto 0) := "000";
   SIGNAL     load_reg    : STD_LOGIC;
   SIGNAL    initflag1    : STD_LOGIC := '1';  -- used to initialise/sync in
```

Figure 6-13 Main section Parallel Offset PPM Encoder VHDL source code

Figure (6.14) shows the waveform from the simulation of the parallel Offset PPM encoder. The red box in the figure illustrates the start position of the input to a valid Offset PPM encoded output, indicating successful encoding into Offset PPM data; according to the theoretical table given in section 4.1 (see Table 4.1).

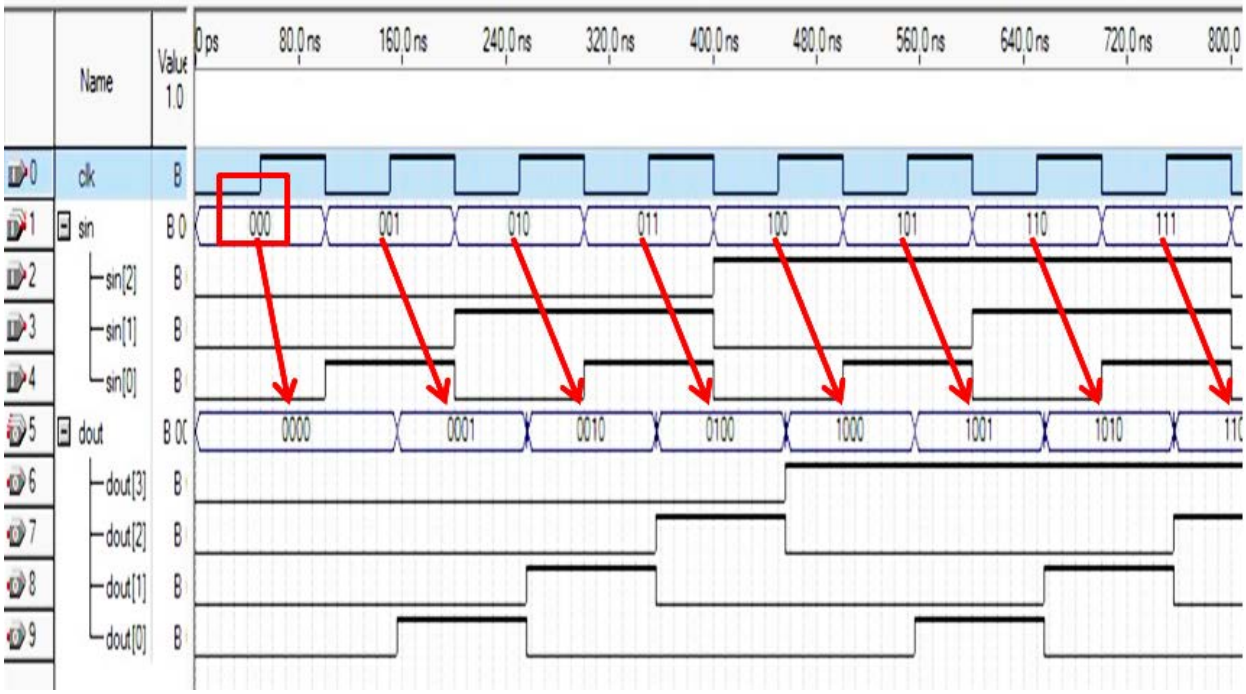


Figure 6-14 Offset PPM encoder VHDL simulation results

6.5.4 Parallel Offset PPM decoder

The corresponding code for the parallel Offset PPM decoder is shown in figure (6.15).

```
ENTITY OFFSETPPMdecoder IS
port(   sin        : IN std_logic;
        clk_3bit   : IN STD_LOGIC;
      clk_4bit     : IN STD_LOGIC;
        dout       : OUT std_logic
        --validflag  : OUT std_logic
        );
end OFFSETPPMdecoder;
architecture behaviour of OFFSETPPMdecoder IS
SIGNAL    control1     : STD_LOGIC_VECTOR(3 downto 0):="0001";
SIGNAL    control2     : STD_LOGIC_VECTOR(2 downto 0):="001";
SIGNAL     sipo     : STD_LOGIC_VECTOR(20 downto 0); --:="000000000";
SIGNAL     piso_D      : STD_LOGIC_VECTOR(2 downto 0):="000";
SIGNAL     D1          : STD_LOGIC_VECTOR(3 downto 0):="0000";
SIGNAL    initflag1    : STD_LOGIC := '1';  -- used to initialise/sync
```

Figure 6-15 Parallel Offset PPM decoder VHDL code

The waveforms for the simulation are shown in figure (6.16). The annotations indicate that the original data was retrieved from the Offset PPM data; this was according to the theoretical table shown in section 4.1 (Table 4.1).

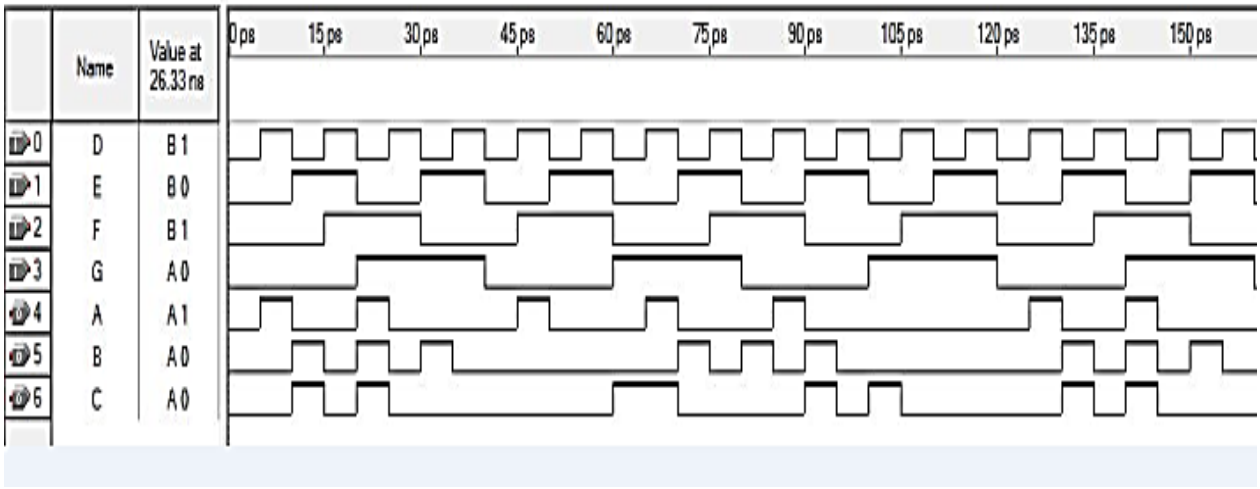


Figure 6-16 Offset PPM decoder VHDL simulation results

6.5.5 Parallel Input Serial Output (PISO)

The conversion from parallel data to serial data is performed by the shift register circuit known as the PISO. The complete set of shift register inputs simultaneously enter the parallel input pins, the data is read sequentially in a shift-right mode within the register (Miani, 2007). The data output occurs in synchrony with the clock, one bit being output on each cycle of the clock, figure (6.17) illustrates the SIPO top block view.

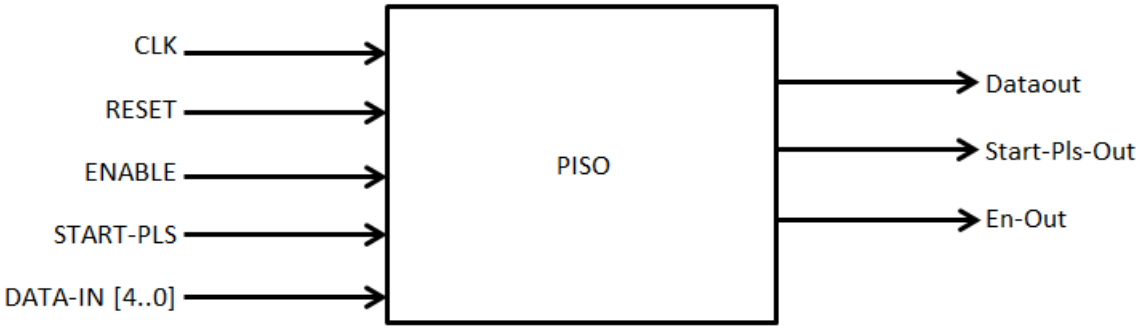


Figure 6-17 PISO top block view

6.5.6 Serial Input Parallel Output (SIPO)

The SIPO is a shift register performs the opposite operation, converting the serial data back into parallel data. Data is input sequentially, synchronized with the clock cycles and output simultaneously. For example, if four bits of data are shifted in over four clock pulses on a single wire, the data is output after the fourth clock pulse on four output wires simultaneously (Maini, 2007). Figure (6.18) illustrates the SIPO top block view.

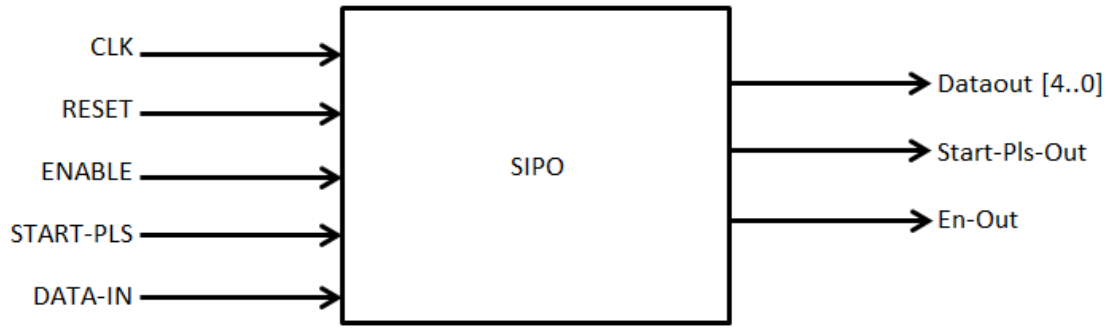


Figure 6-18 SIPO top block view

6.6 Parallel Offset PPM coding System Implementation

Figure (6.19) shows the parallel Offset coding scheme, it consist of PLL, counter, parallel offset encoder, and parallel Offset PPM decoder, theses blocks connected to each other directly. PLL output clock gives the synchronization to all system components. The counter generates a 3 bit parallel message that feeds to Offset PPM encoder as an input, therefore after coding this message and by the next clock the coded message enter the Offset PPM decoder as an input, by the third clock, the decoder generates the decided message again to return it to its original form.

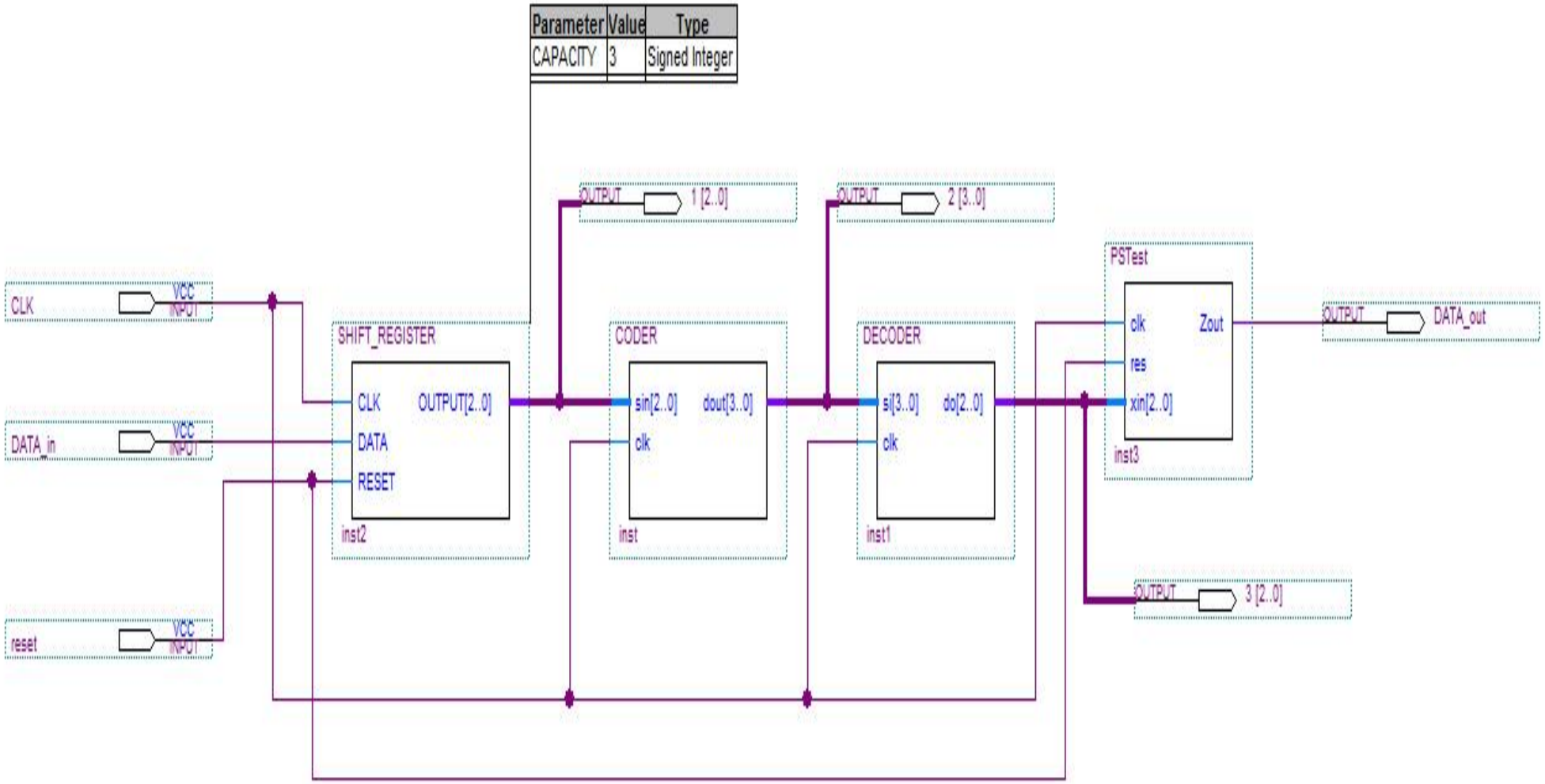


Figure 6-19 Parallel Offset PPM

Figure (6-20) shows the real time waveforms of the parallel Offset coding system

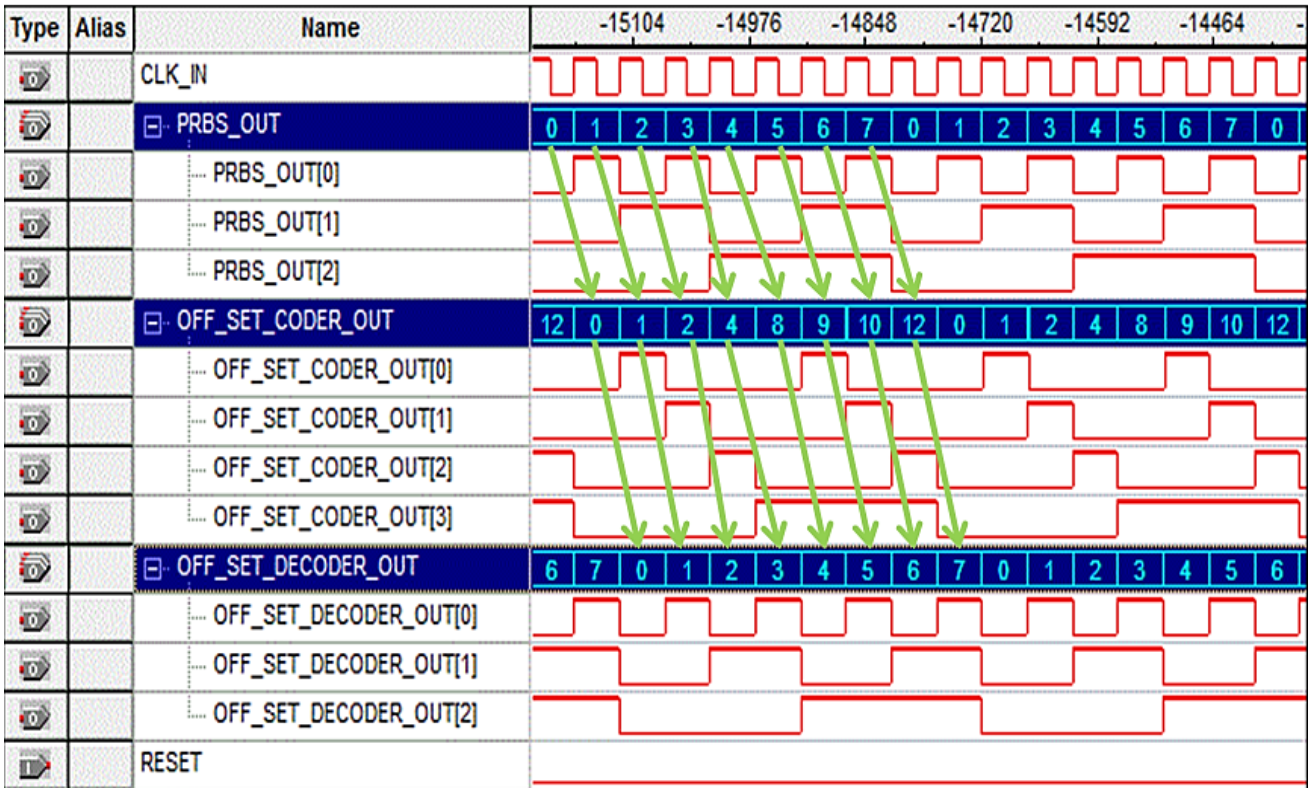


Figure 6-20 Real time waveform parallel Offset PPM

6.7 Serial Offset PPM Coding System Implementation

Completion of an integrated system design is the final step in the design and implementation of the VHDL and FPGA Offset PPM coding system. However, such compromises need not be required, given the processing power of modern FPGA and the high design capability of VHDL, if sufficient programming and design expertise be used in the design and coding, however complex the system. The Altera Quartus II software package was used for the first implementation of the Offset PPM system. A RESET signal was provided by one of the eight IP switched and the input clock was provided by a 50 MHz oscillator. Five stages constituted the transmitter side:

- PLL for the 1 MHz clock.
- PRBS generator.

- PISO for parallel PRBS output to serial conversion.
- Offset PPM encode.

The transmitter output is sent through a modelled channel.

At the receiver end, the data is processed in four steps. These included the Offset PPM decoder and the SIPO.

The following figure (6.21) shows a framework of Offset PPM layout. Figure (6.22) illustrates Offset PPM system.

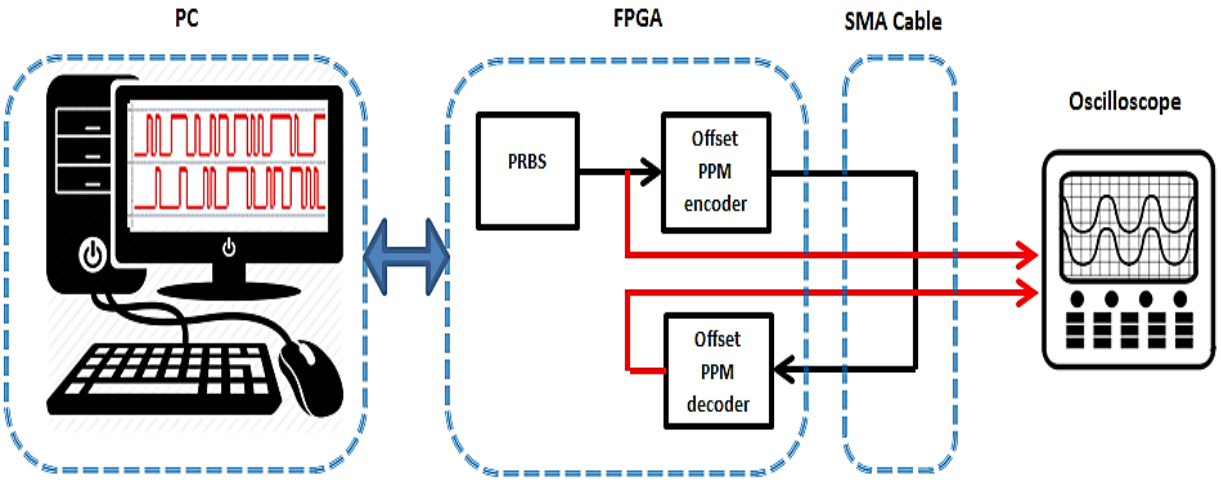


Figure 6-21 Serial Offset PPM system layout

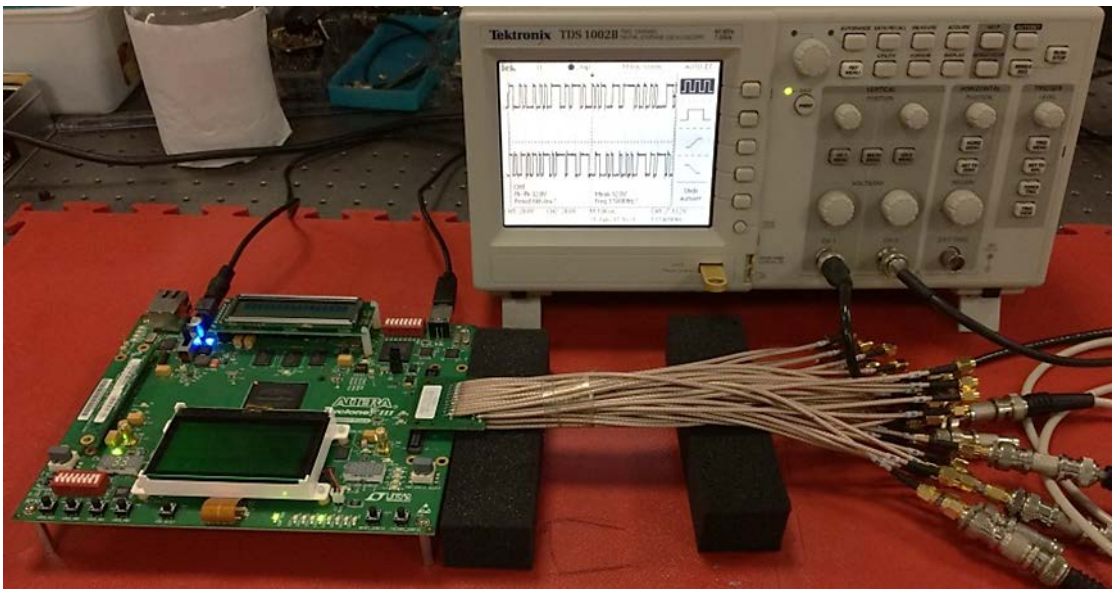


Figure 6-22 Offset PPM system without optical fibre links

The final stage of the design and implement of the Offset PPM coding system using VHSIC hardware description language (VHDL) and field programmable gate array (FPGA) required complete an integrated system design. Figure (6.23) shows the VHDL implementation of the full serial Offset PPM system. The first serial Offset PPM was implemented using the components that are described in the previous sections. Figure (6.24) illustrates the modification of serial Offset PPM system, this figure shows that serial Offset PPM encoder and decoder in one block. These serial encoder and decoder are consisting of SIPO and PISO together with the parallel Offset PPM encoder and decoder.

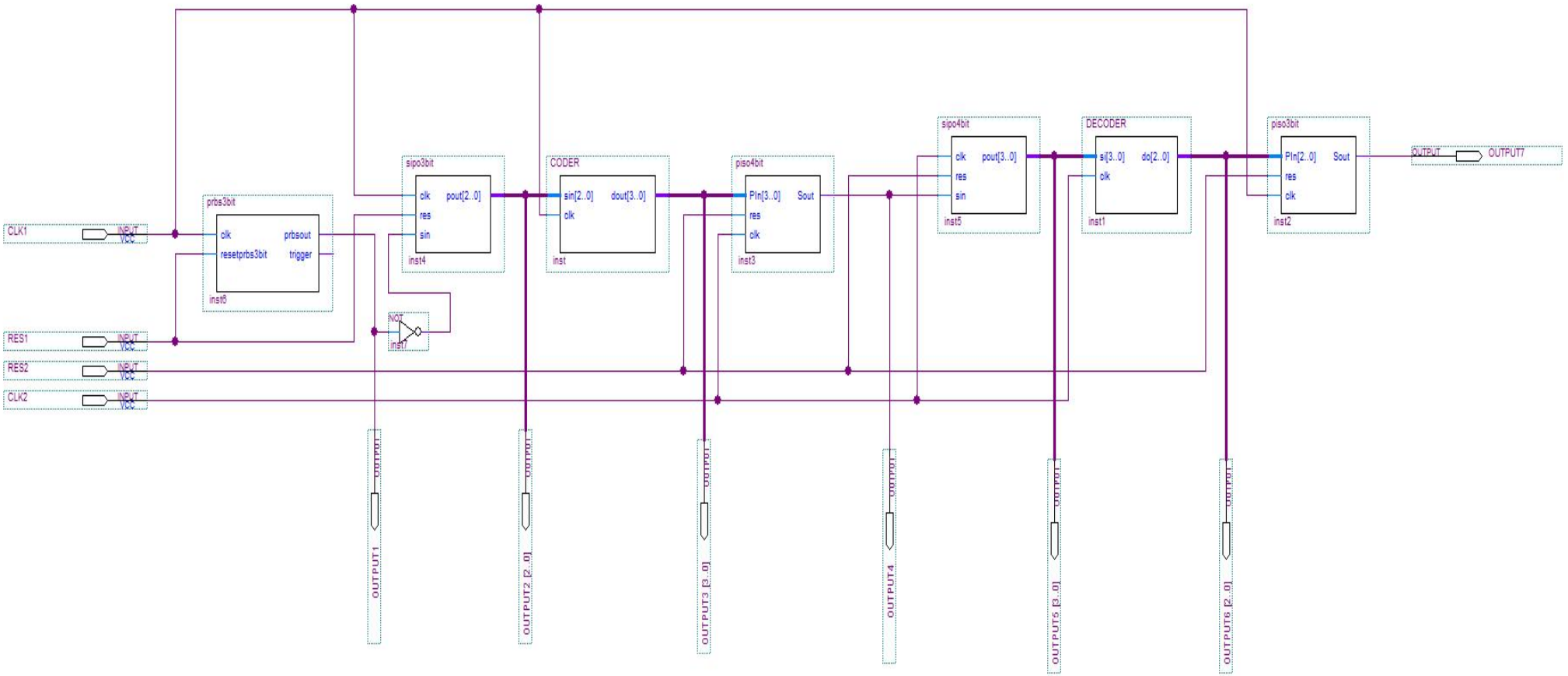


Figure 6-23 First version serial Offset PPM

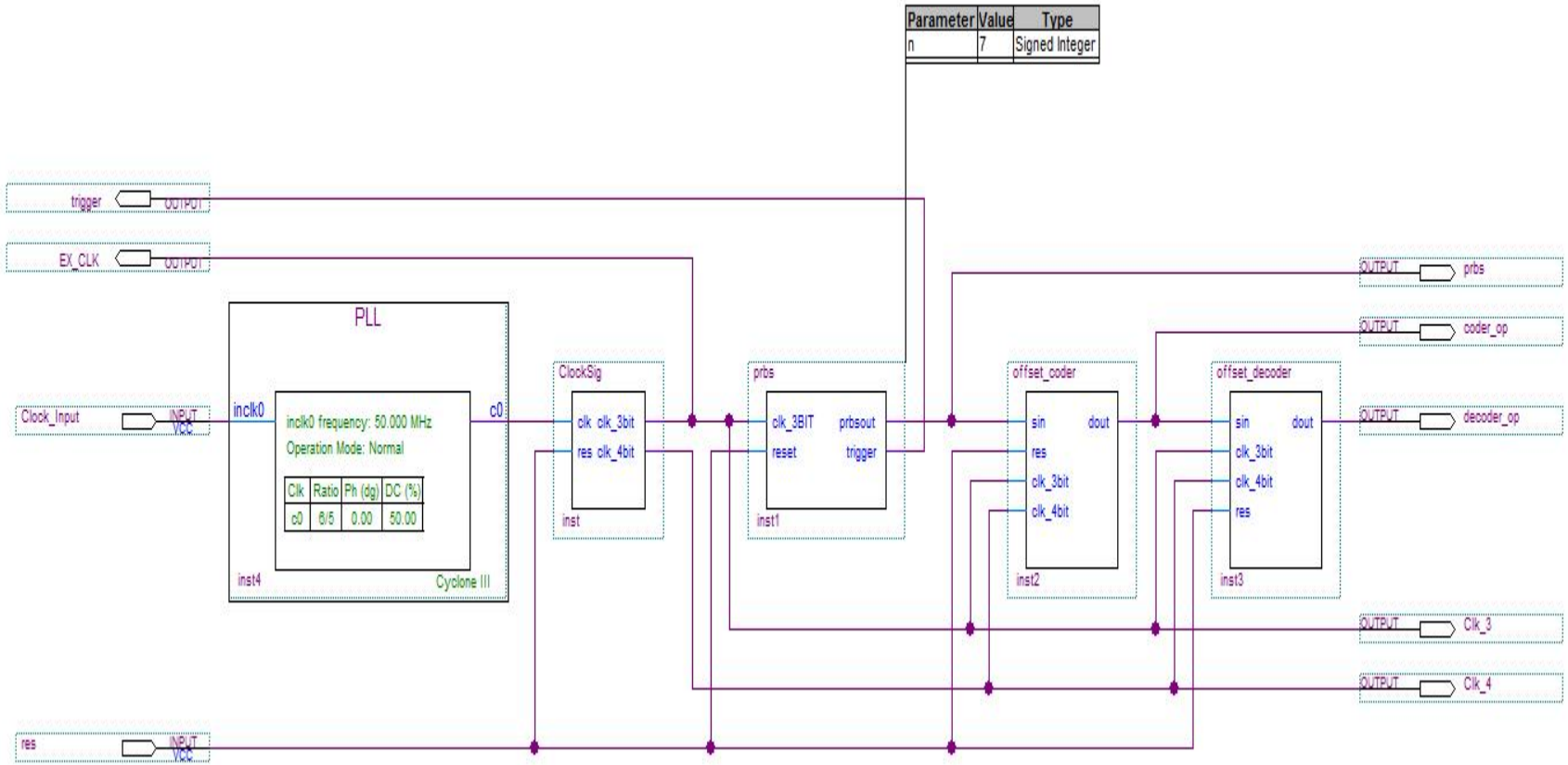


Figure 6-24 Serial Offset PPM schematic diagram

The simulation report was generated based on the same waveform file after the compilation of the modified circuit was completed. The simulation waveform of the Offset PPM system is given in figure (6.25). The waveform is annotated and it is clearly noticeable that the Offset PPM data has been successfully decoded into the original PCM data according to the theoretical table given in chapter 4 (Table 4.1). There is a delay between the input PCM and the output PCM as shown by the in the figure (6.25). The PCM input data is named (prbs), while the PCM output data named (decoder_op). The red arrow on the figure indicates a reference points on the two signals to show the similarity between them, and the delay which occurs.

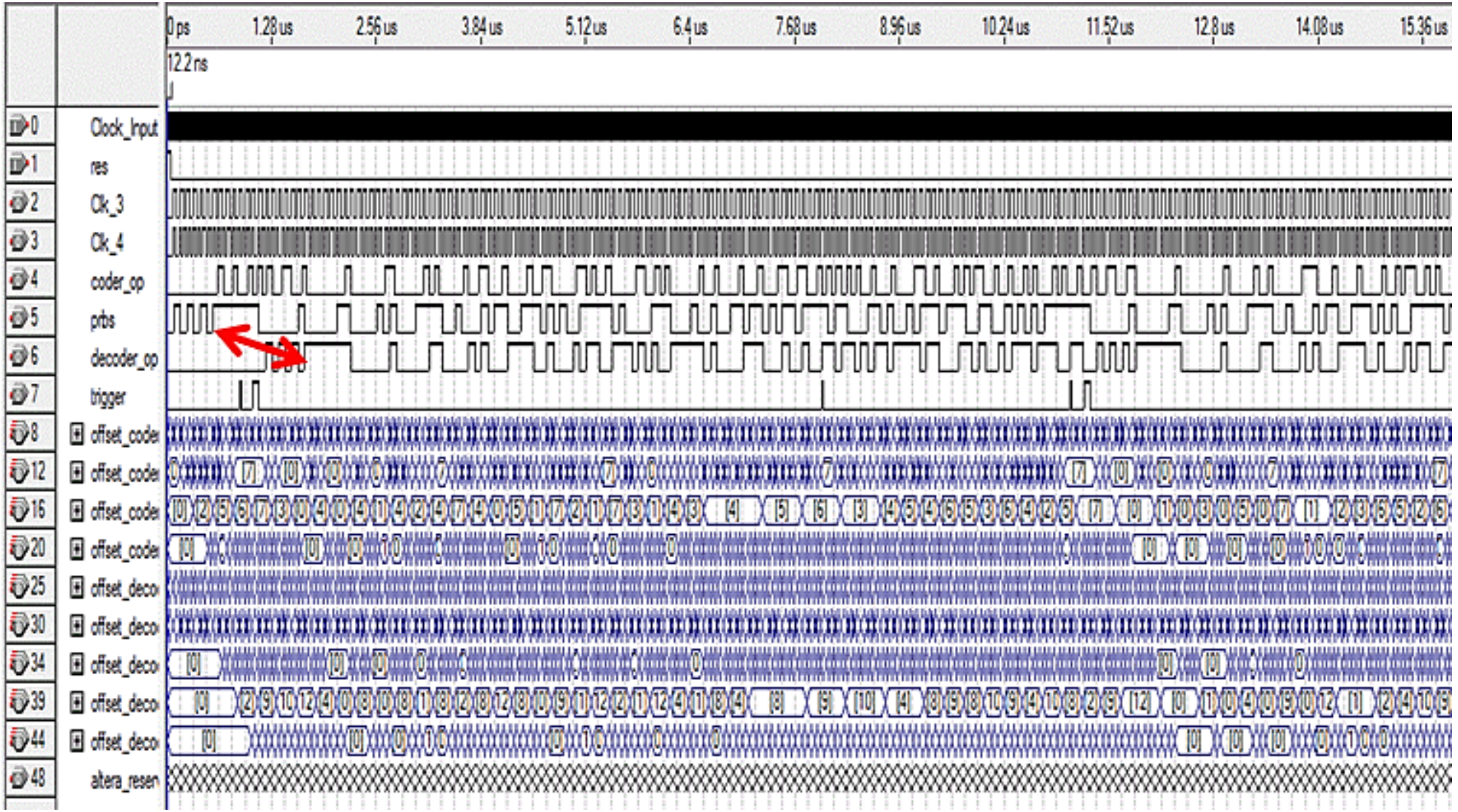


Figure 6-25 Serial Offset PPM simulation

Quartus® II software includes a system level debugging tool called Signal Tap Analyser (STA) that can be used to capture and display signals in real time in any FPGA design. STA Logic Analyser is scalable, easy to use, and is available as a stand-alone package or included with the Quartus® II software subscription. This logic analyser helps debug an FPGA design by probing the state of the internal signals in the design without the use of external equipment. After the program was successfully downloaded to the FPGA board through the programmer, the result of analysis to evaluate the practical performance was obtained once the analysis process was completed. There is a delay between the input PCM and the output PCM as shown by the in the figure (6.26).

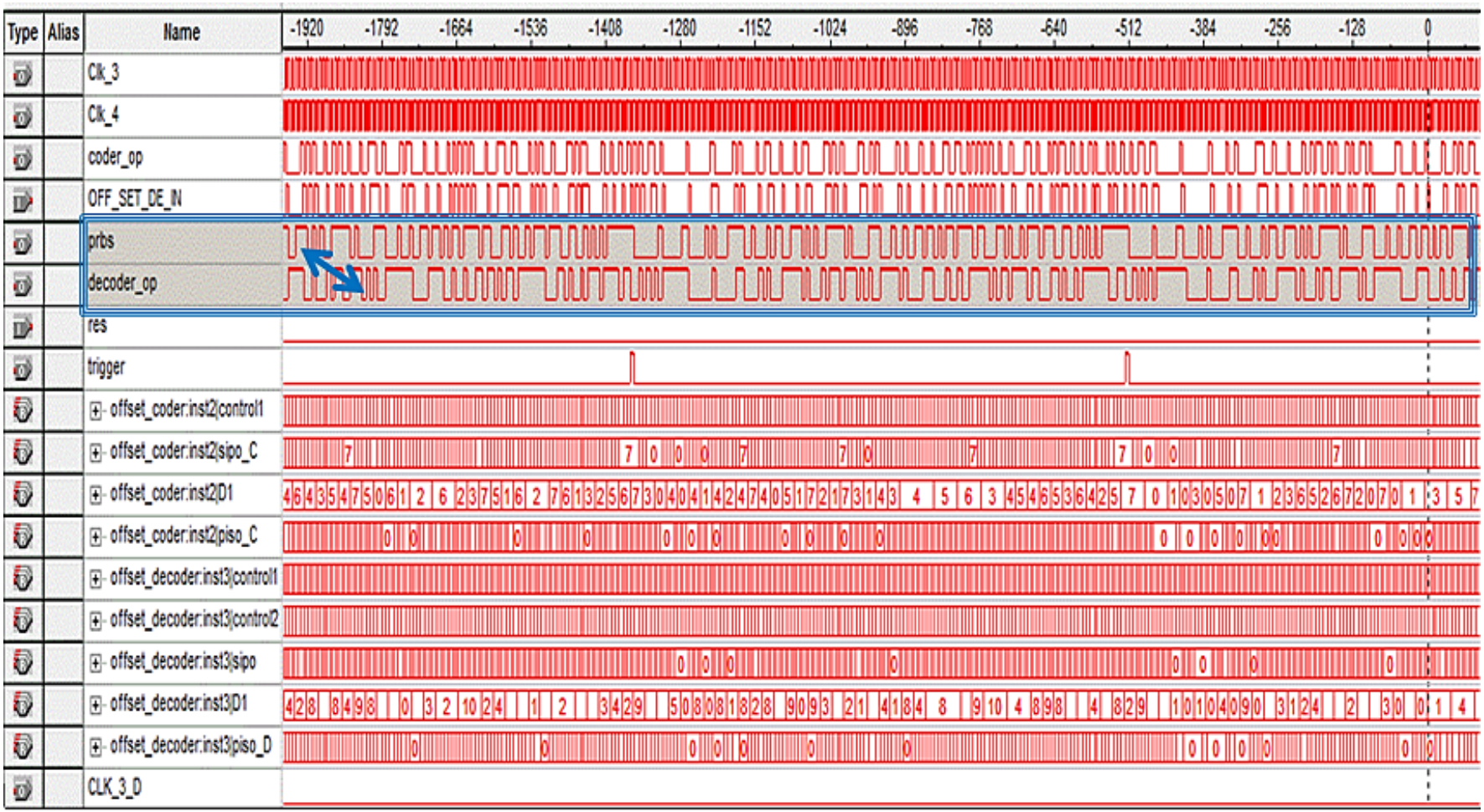


Figure 6-26 Real time waveform serial Offset PPM

Experimental verification results of the Offset PPM decoder are given in figure (6.27). There is a delay between the PCM output and decoded PCM similar to figure (6-26) in the previous page, the red boxes indicate reference points in the two signals to show waveforms clearly in the same screenshot.

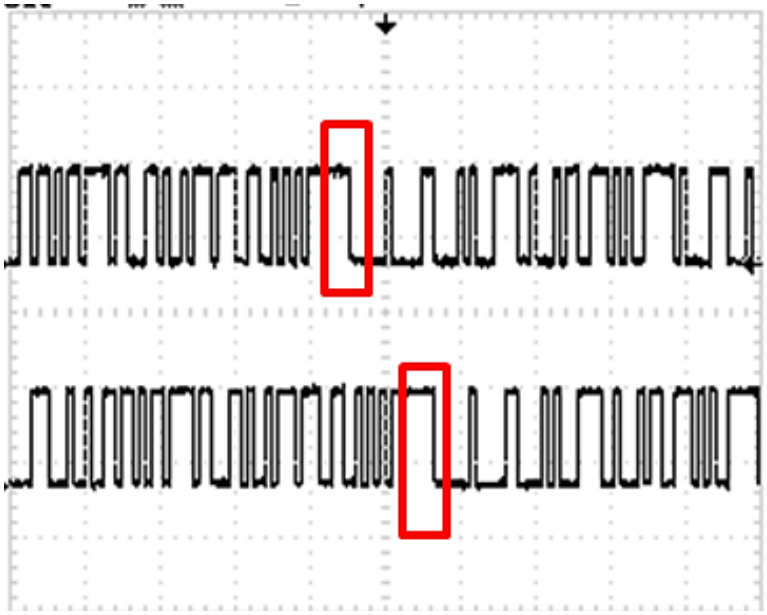


Figure 6-27 PRBS output (top trace), Offset PPM decoder (bottom trace)

6.8 Summary

- In this chapter, the Cyclone III development board and SMA Breakout Cable were described with the lists of features of the board and specific information.
- The Offset PPM system has been discussed and implemented using VHDL with fully successfully testing results in this chapter.
- This work was executed using VHDL on an FPGA. The encoder and decoder design and development have been described and the simulation waveforms and practical results of the implementation have all been presented in this chapter.

7 Optical Offset PPM Communication System

7.1 Introduction

Chapter 6 presented and discussed the design of the Offset PPM system's VHDL source code and the implementation of the system. In order to implement the full optical communication designed system, Altera Quartus II was used in conjunction with a Cyclone III Field Programmable Gate Array (PFGA) based DSP development board (Altera, 2015). The design stage for the voltage comparator, optical receiver and optical transmitter was completed and these entities were then created. In order to obtain the digital input signals and output signals from the FPGA, the author adopted the SMA breakout cable interface. Figure (7.1) illustrates the framework of the full Offset PPM communication system with optical communication set as a first test, while, figure (7.2) shows the second test for this communication system using an external PRBS generator. The test bench equipment is demonstrated in figure (7.3).

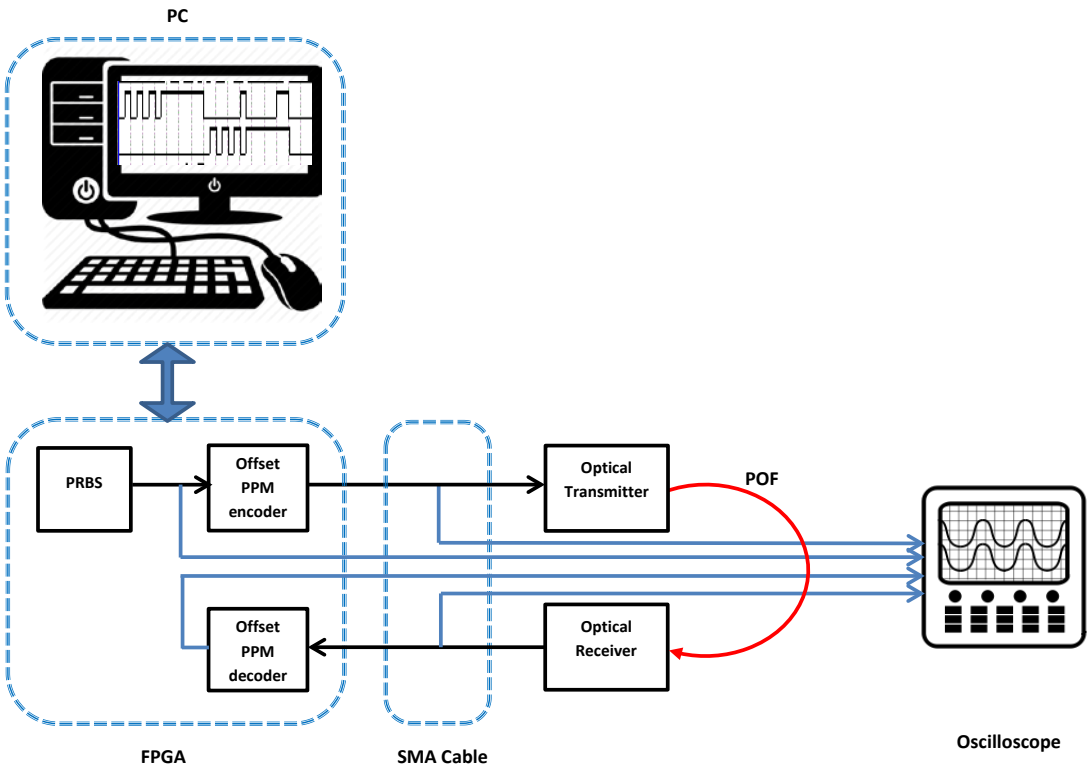


Figure 7-1 Frame work of the full Offset communication system

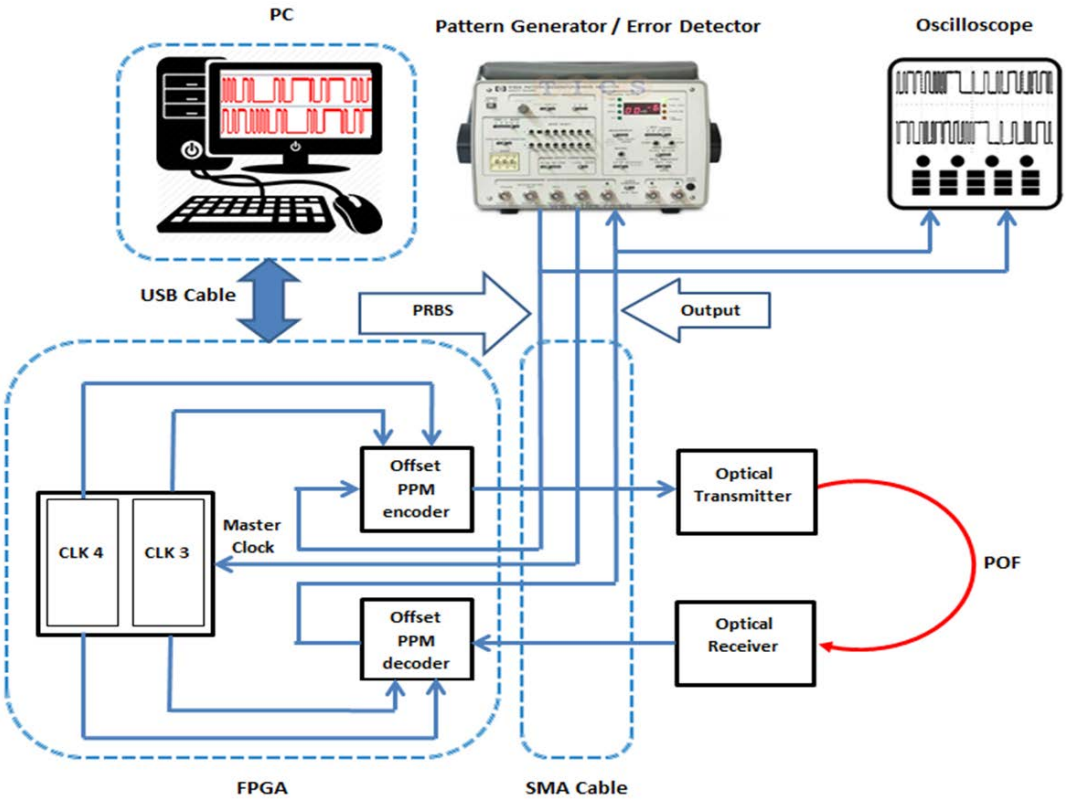


Figure 7-2 Frame work of the full Offset communication system with external PRBS

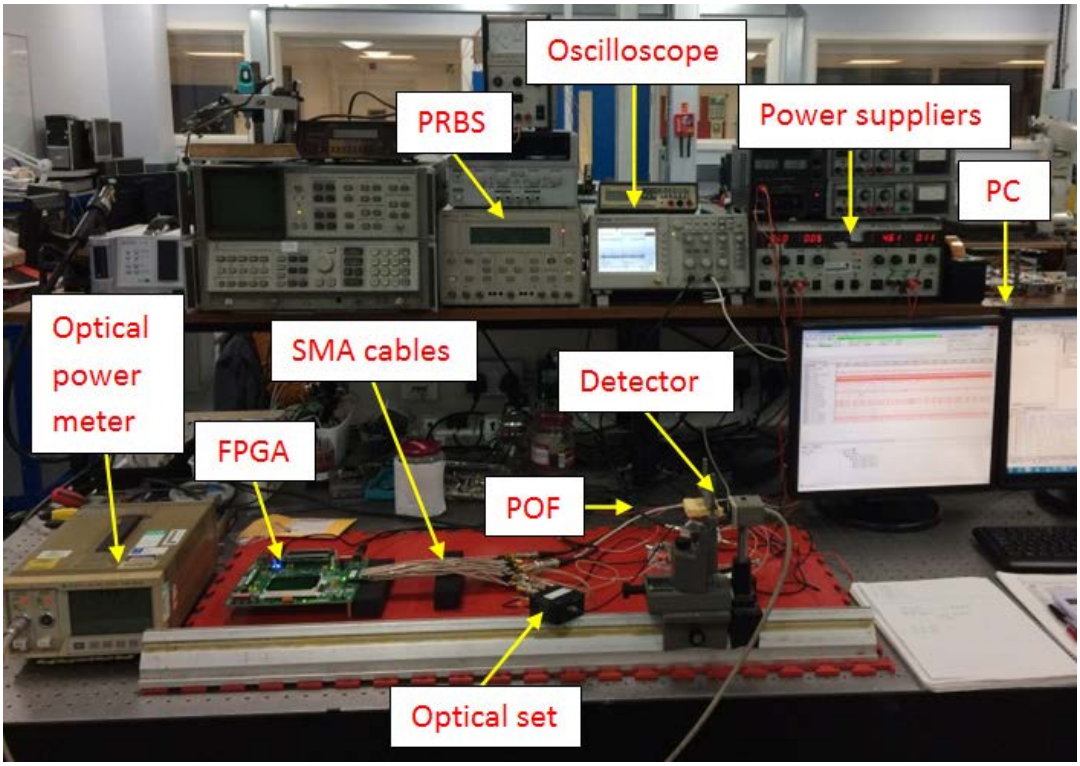


Figure 7-3 Test bench setup

7.2 Serial Set Offset PPM coding system with Optical Components and External PRBS

The complete system is illustrated in figure (7.3), along with the devices and tools used. A USB cable was used to connect the Personal Computer (PC) to the Cyclone III FPGA-based development board in order to download the software. The data stream was transmitted and received using the output and input pins. The optical transmitter and optical receiver were both attached to metal mounts and connected to the driver's circuit board in order to achieve optimum transmission. Figure (7.3) also depicts the configuration of the tools used, with the oscilloscope, pattern test set (pattern generator/error detector) and power suppliers on the test bench. All of the parts used were placed close together, using short cables to connect the components so as to minimise the errors.

7.3 Experiment Hardware and Software Resources

7.3.1 FPGA & VHDL

FPGA and VHDL design for Offset PPM system are described comprehensively in chapter 6.

7.3.2 Optical Fibre Communication System Components

In the context of the key components contained within the system, the optical fibre communication system is not markedly different to any other kind of communication system, the optical fibre communication system works through a light source that moves through a fibre channel before arriving at an optical receiver. Once received by the optical receiver, an electric signal is generated out of the modulated light.

7.3.2.1 Optical Transmitter

(Senior & Jamro, 2009) and (M. J. N. Sibley, 1995) explain that the optical transmitter is a source of light where the transmitter circuit's drive current is altered to result in on-off keying, which is

then used to modulate the optical transmitter's output. The optical output power of the transmitter is then altered to varying degrees. The core component within the transmitter is the semiconductor diode. The semiconductor diode can be either a laser diode or a light-emitting diode (LED). Senior and Jamro (2009) and Sibley (1995) add that the semiconductor diode is a forward-biased diode where an optical fibre is used to align the intensity of the output light with the diameter of the semiconductor.

In order to send data across the optical channel, the optical communication system depends upon a transmitting component which contains an LED photon source. This is the primary component of the transmitting block. LEDs are categorised based on the time it takes for them to respond as well as on their wavelength. As Komine and Nakagawa (Komine, Lee, Haruyama, & Nakagawa, 2009) explain, in most cases, LEDs have a longer response time than the rate at which data is transmitted. In other cases, the rate of data transmission is often equal to the response time of the LEDs.

The optical transmitter used in this project is the HFBR-15X7Z (Appendix 9.2). The HFBR-15X7Z transmitter is a high power 650 nm LED in a low cost plastic housing designed to efficiently couple power into 1 mm diameter plastic optical fibre and 200 μm Hard Clad Silica (HCS®) fibre. With the recommended drive circuit, the LED operates at speeds from 1-125 MB/s. Some of HFBR-15X7Z features are the data transmission at signal rates of 1 to 125 MB/s over distances of 100 meters, compatible with inexpensive, easily terminated plastic, optical fibre, and with large core silica fibre and high voltage isolation. These features allowed it to work perfectly on different applications like intra-system links, board-to-board, rack-to-rack, telecommunications switching systems, computer-to-peripheral data links, PC bus extension, industrial control, and medical instruments.

The optical transmitter system designed as part of this project is illustrated in figure (7.4), figure (7.5) and figure (7.6). In order to ensure that the system was able to achieve strong optical power able to manage a long POF cable, the author used the HFRB-15X7Z transmitter. The HFRB-15X7Z

transmitter achieves a signal rate of between 1 MB/s and 125 MB/s through either a plastic optical fibre with a diameter of 1mm or a hard clad silica glass optical fibre with a diameter of 200 µm.

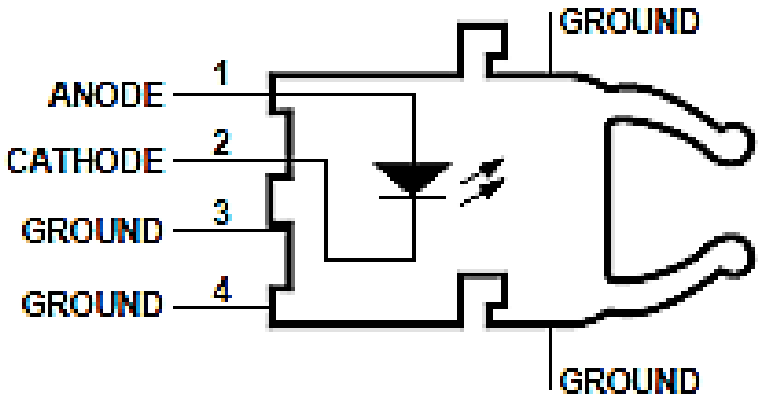


Figure 7-4 Optical transmitter layouts (Appendix 9.2)

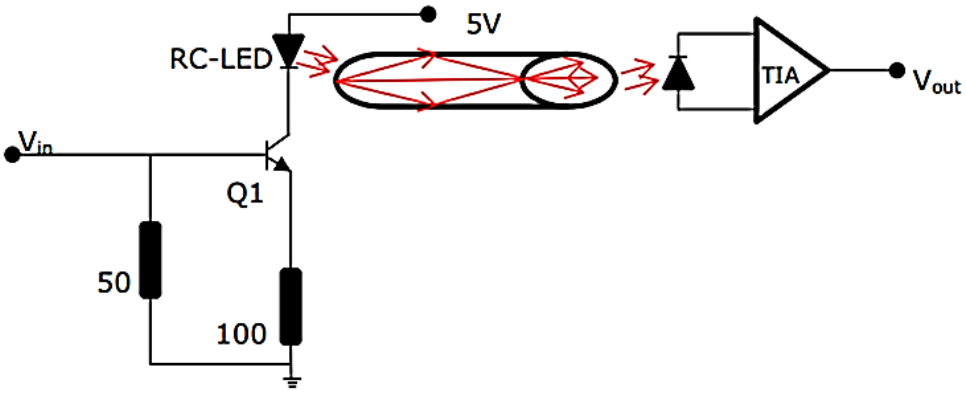


Figure 7-5 Optical Transmitter Circuit

Figure 7-6 Optical transmitter part

7.3.2.2 Optical Receiver

The key component in all optical communication systems is the optical receiver. This is because the optical receiver is responsible for detecting the level of optical power and converting this into an electrical current that is in line with the degree of change in optical power. As Sibley (1995) points out, it is common for the light close to the receiver to be weak. This is because of signal distortions and link loss. Therefore, it is important that the photodetector chosen is appropriate to the communication system being used. This includes considerations such as high performance quality, affordability, good reliability, minimum error / low noise, a rapid response time based on the data rate needed, high sensitivity at the wavelength needed, and good efficiency when converting photons (optical power) to electrons (electrical power).

(Brundage, 2010) adds that in most cases, optical receivers represent the final destination for data sent via an optical link channel. The optical receiver contains a photodetector, preamplifier and current-to-voltage circuitry. This being said, the optical energy received is converted by the optical receiver to an electrical signal that is strong enough for other electronic components to process the signal.

Senior and Jamro (2009) and Sibley (1995) explain that the photo detector serves as a demodulator that is able to convert the optical signal into an electrical signal. The photo detector is the core component of the optical receiver and must therefore meet a certain level of performance. Photo detectors come in a wide variety of different forms, constructed with a range of different materials, and they perform various functions. However, it is the nature of the system and the needs associated with it that should determine which photo detector is used.

The HFBR-25X6Z (Appendix 9.2) is used as an optical receiver in this project is a high bandwidth analogue receiver containing a PIN photodiode and internal transimpedance amplifier. With the recommended application circuit for 125 MB/s operation, the performance of the complete data link

is specified for 0-25 metres with plastic fibre and 0-100 meters with 200 μm HCS® fibre. A wide variety of other digitizing circuits can be combined with the HFBR- 25X6Z Series to optimize performance and cost at higher and lower data rates.

The HFBR-25X6Z receivers contain a PIN photodiode and transimpedance pre-amplifier circuit in vertical (HFBR-2536Z) blue housing, and are designed to interface to 1mm diameter plastic optical fibre or 200 μm hard clad silica glass optical fibres. The receivers convert a received optical signal to an analogue output voltage. Follow-on circuitry can optimize link performance for a variety of distance and data rate requirements. Electrical bandwidth greater than 65 MHz allows design of high speed data links with plastic or hard clad silica optical fibre.

The optical receiver system designed as part of this project is illustrated in figure (7.7), figure (7.8) and figure (7.9). The tests performed in the current study were carried out with the HFBR-2526Z optical receiver, which is appropriate for a POF cable.

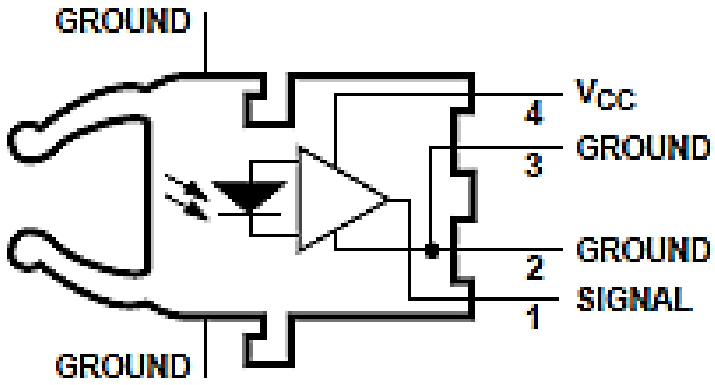


Figure 7-7 Optical receiver layouts

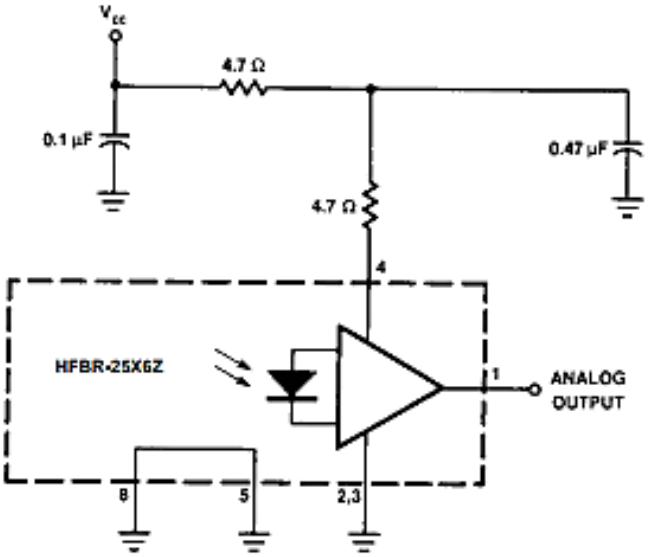


Figure 7-8 Power supply Circuit for Optical Receive (Appendix 9.2)

Figure 7-9 Optical receiver part

7.3.2.3 Plastic Optical Fibre (POF)

The core and cladding of the plastic optical fibre are made from organic polymers, which make manufacturing the optical fibre inexpensive and allow the product to be used without any difficulty. POF has been constructed out of Polymethyl Methacrylate and Fluorinated Acrylic (PMMA) more recently. This kind experiences 110 dB/km losses in the visible wavelength. As Senior and Jamro

(2009) and Sibley (1995) explain, due to absorption and Rayleigh scattering (linked to polymers' anisotropic structure and density fluctuations) its loss type is similar to that of glass fibre.

The HFBR (Appendix 9.3) fibre optic cable has been used in this project to transfer data between the optical (transmitter/receiver). The HFBR-R of plastic fibre optic cables is constructed of a single step-index fibre sheathed in a black polyethylene jacket. The HFBR fibre optic cable is compatible with Avago Versatile Link Family of connectors and fibre optic components. It has 1 mm diameter with 0.22 dB/m typical attenuation.

For the purposes of data transfer in this project, the author used 10 metres long cable in order to send data from the optical transmitter to the receiver. This is illustrated in figure (7.10).

Figure 7-10 HFBR-R optical fibre (Appendix 9.3)

7.3.3 Voltage Comparator

Brundage (2010) and Sibley (1995) assert that in the majority of cases where communication systems are being utilised, the comparator is installed in order to ensure zero receiver outputs. The comparator compares the input signal with the reference voltage; therefore, the comparator ensures that pre-set voltage present when the comparator receives the input signal. Following amplification processing, the data pulse received is added to the comparator's input. The data signal that has been received is converted into voltage within the comparator. This is typically a TTL signal. In most

cases, it is not possible to fulfil the circuit criteria of 0 and +5 volts unless the comparator output receives the TTL signal. This signal is influenced by the input signal's amplitude with regards to the comparator's reference signal. The TTL output is determined to be low when the input signal is weaker than the reference voltage, whilst it is determined to be high when the input signal is stronger than the reference voltage.

The comparator circuit identifies the larger of two voltages and outputs from 0 to a pre-set voltage determining the differences between them. As Senior and Jamro (2009) and Sibley (1995) point out, these are typically used so as to evaluate whether or not an input has reached a certain value that has already been set.

In this project, the voltage comparator used was the MAX941 (Appendix 9.4). The MAX941 is a single high-speed comparator optimized for systems powered from a 3V or 5V supply. This device combines high speed, low power, and rail-to-rail inputs. Propagation delay is 80ns, while supply current is only 350µA per comparator. The input common-mode range of the MAX941 extends beyond both power-supply rails. The outputs pull to within 0.4V of either supply rail without external pullup circuitry, making this device ideal for interface with both CMOS and TTL logic. All input and output pins can tolerate a continuous short circuit fault condition to either rail.

As shown in figure (7.11), the MAX941 comparator was connected as a simple line transceiver with a clean square wave signal as the output, at the same frequency as the input. The amplitude of the output is V+. Pin set-ups are outlined in figure (7.12), and a real picture of the voltage comparator is illustrated in figure (7.13).

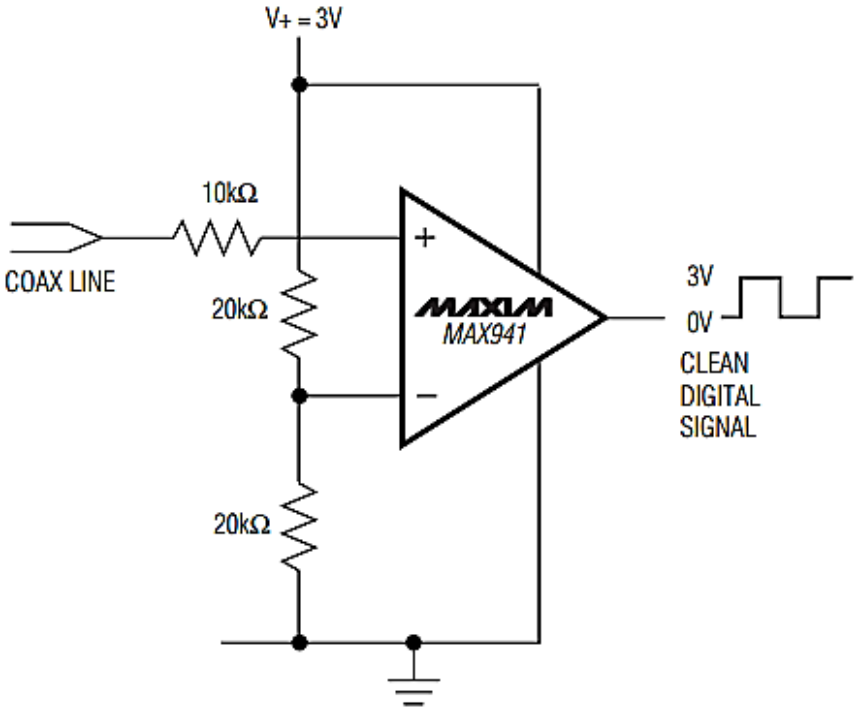


Figure 7-11 Voltage comparator circuit (Appendix 9.4)

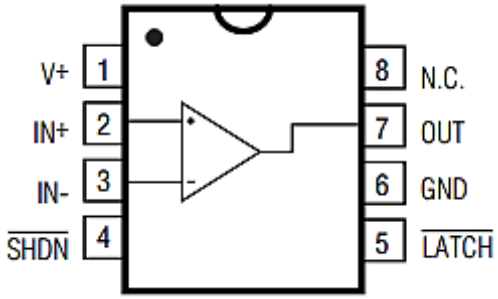


Figure 7-12 MAX941 Pin configuration

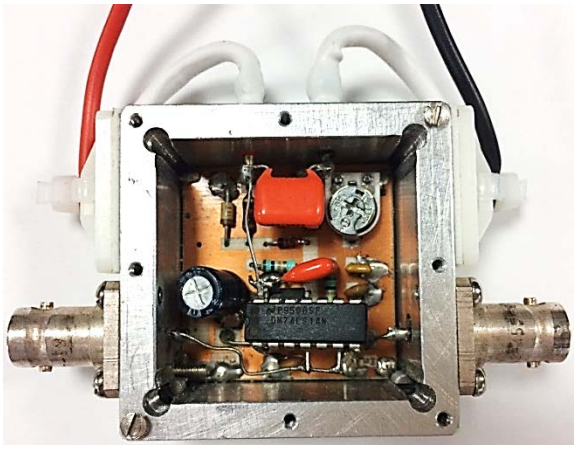


Figure 7-13 Voltage comparator part

Figure (7.14) presents the input comparator signal from the receiver (top trace), the TTL output signal after digitalize it by the comparator (lower trace).

Figure 7-14 Voltage comparator Input/Output

7.3.4 PRBS Generator

Data bits require binary data and are transmitted by all digital communication systems (Choudhary & Kumar, 2017). However, it is the way in which the data bits are created that is significant. As shown in figure (7.15), this project utilised the Hewlett-Packard HP 3780A as the (PRBS generator/error detector), comprising a serial data generator and a data receiver capable of achieving synchronisation. The PRBS generator also contains comparison circuitry able perform error detection by comparing data sequences that have been generated against data sequences received. Finally, the instrument bit error rate (BER) is displayed using the display and LEDs.

It is possible to generate two types of output through the data generator. The first is a pseudo-random bit sequence (PRBS). The second is a 16 bit pattern that is repeated on a loop and determined by the user. Either output is generated in a non-return-to-zero (NRZ) format. There are also alternatives, such as special formats (e.g. RZ) and the incorporation of zeros into the sequence

in order to test clock the system's recovery speed and level. It is also possible to purposefully introduce errors for the purpose of testing the receiver display.

The HP 3780A (pattern generator/error detector) is a comprehensive error measuring set in one portable package for use in manufacturing, commissioning, and maintenance of digital transmission terminal and link equipment. The instrument measures binary errors and code errors in digital transmission equipment operating at rates between 1kb/s and 50 Mb/s. A range of standard PRBS test patterns and automatic pattern recognition/synchronisation are provided for simple performance checks. Binary clock and data ternary coded interfaces can be selected with automatic equalisation at 2, 8, and 34 Mb/s on the receiver. Results are displayed as error COUNT or BER over a range of gating periods.

Figure 7-15 Hewlett-Packard HP 3780A PRBS generator

7.4 Implementation of Offset PPM System

The initial implementation of the optical Offset system was carried out during this test as part of the project. Both the Offset encoder and the Offset decoder were constructed through the use of the source code for the Offset PPM. As illustrated in figure (7.16), Altera Quartus II version 9.1 software was used by the researcher to achieve the complete design of the optical Offset PPM

system. The Altera Quartus software package is highly useful for the purposes of this research in that it provides a variety of MegaCore functions for engineers, allowing them to apply parameters to the specific function that is desired by the user or creator. As shown in figure (7.3), earlier in the chapter, a USB cable was used during this test to transfer the software from a PC and to gather data onto the PC. In order to obtain the input signals from the FPGA along with the output signals, the author used an SMA breakout cable as an interface between the development board and the other experiment equipment such as optical transmitter, optical receiver, (PRBS generator/error detector), and oscilloscope, during the test. In terms of the transmitter's attributes, input data were fed through a PRBS generator that was connected to the development board. Additionally, the optical transmitter and the output pin of the Offset PPM encoder were connected to one another. Finally, the data were transferred through the use of a plastic optical fibre (POF). The plastic optical fibre had a total length of 10 metres. Next, in terms of the receiver, the first step was to design a comparator. The reason for designing the comparator as the first step in the testing process is to ensure that the signal sent from the optical receiver could be successfully received. Once this had been achieved, the signal received from the optical receiver was then sent to the Offset PPM decoder. This then made it possible for the original PCM sequence to be regenerated.

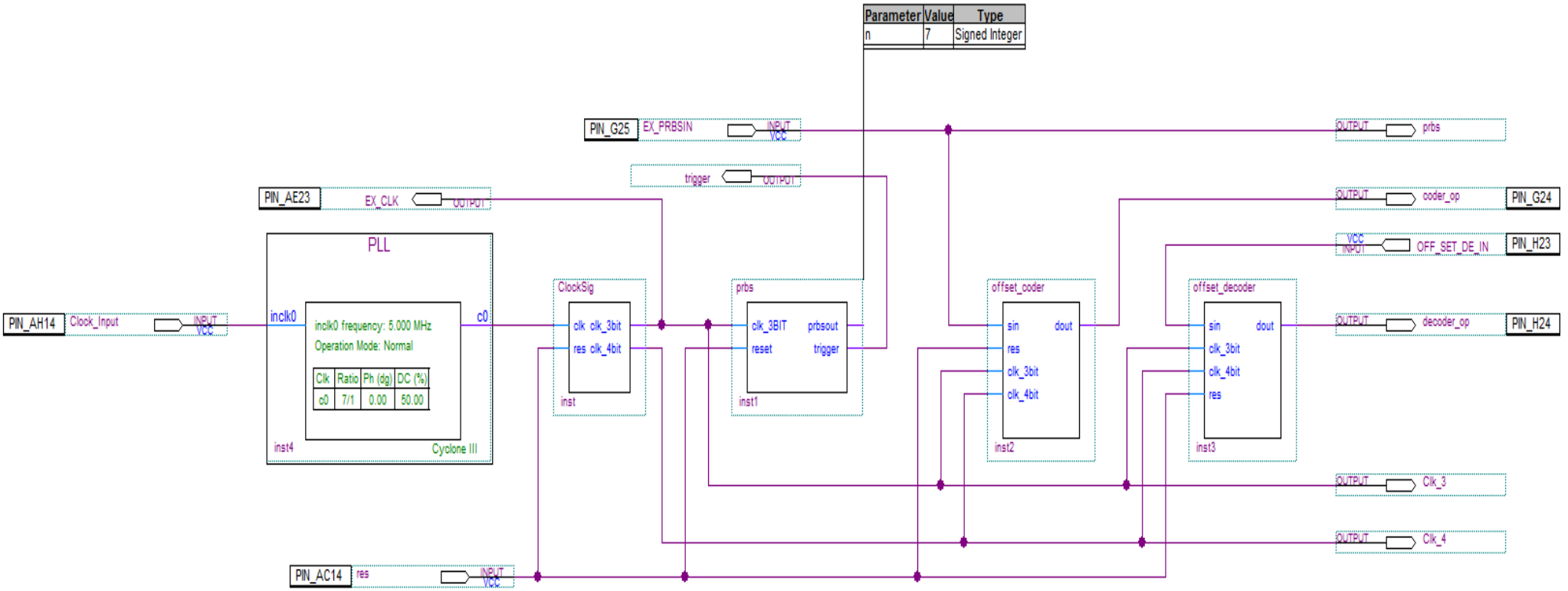


Figure 7-16 Optical Offset PPM system design using Altera Quartus II v. 9.1 software

7.4.1 Simulation Results

The results of the complete Offset PPM system simulation test are illustrated in figure (7.17) as shown below. As demonstrated in the figure, the signal sent from the Offset PPM Decoder is exactly the same as the PRBS output signal, with a delay. The output of the Offset PPM Encoder is also demonstrated in figure below. The signals from the two clocks (ck 3 and ck 4) allowed for synchronisation to be achieved between the parallel 3-bit word and the 4-bit word. The parallel output of the encoder and decoder (bottom traces) are both shown below.

In figure (7.17), the left red box is used as a reference. Signal 5 indicate the (prbs) sequence as the input signal to the Offset PPM encoder, while signal 6 is a (decoder_op) as the Offset PPM decoder output signal. The two other red boxes are used to indicate a reference between these two main signals. These two signals are identical in the shape. Signal 6 was shifted by a time delay compared to signal 5.

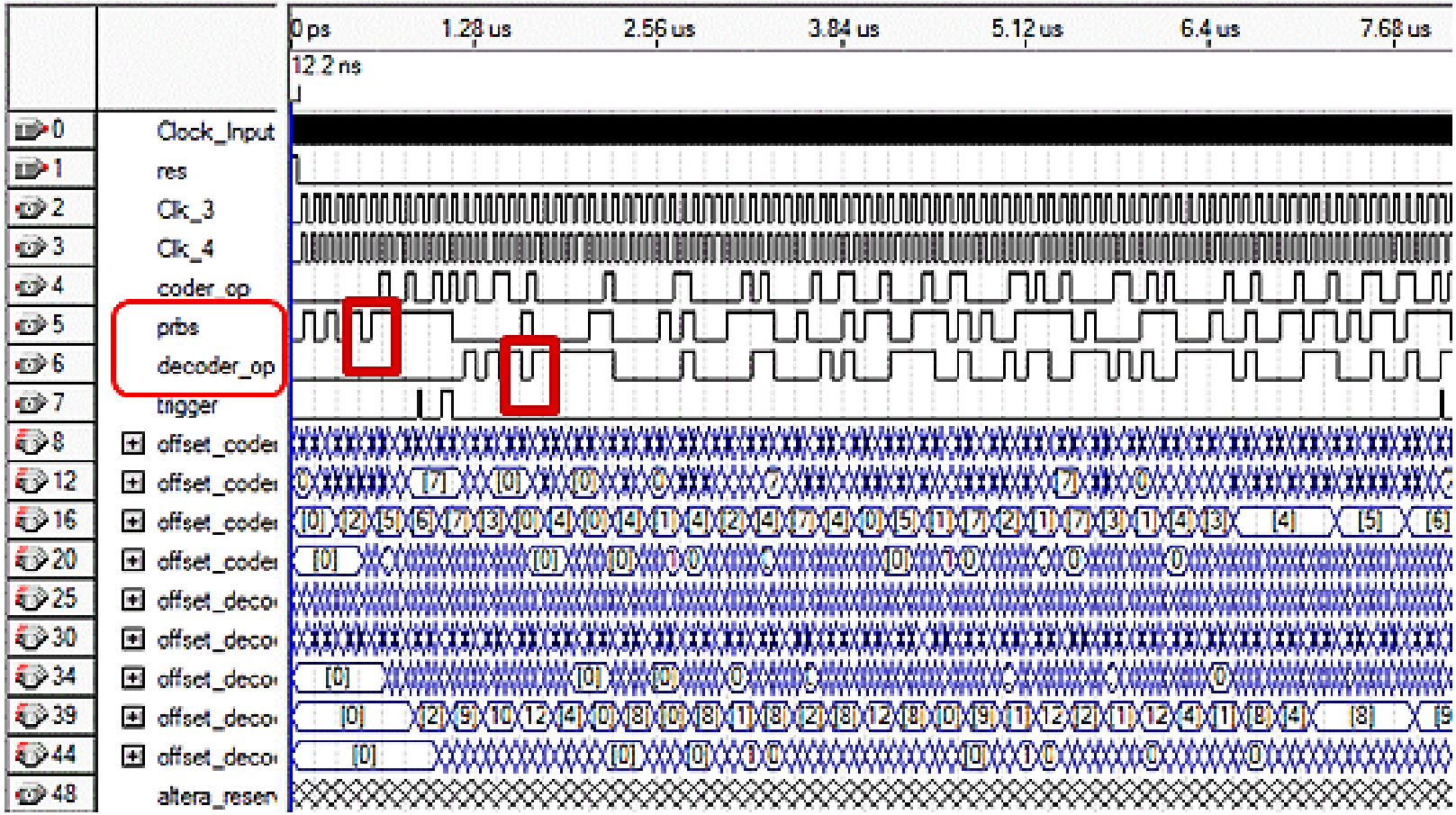


Figure 7-17 Offset PPM system simulation results

7.4.2 Real Time Results

An oscilloscope was utilised in conjunction with the (STA) tool through the use of the Altera Quartus II software package. This allowed the research to gather the PRBS generator waveform output. Consequently, the author was able to easily examine the parallel data. The external PRBS waveform output observed through the oscilloscope is illustrated in figure (7.18) as shown below. In addition, figure (7.18) also illustrates the Offset PPM decoder output that was observed through the use of the oscilloscope. The red arrow is used to indicate the shift between the two signals. Additionally, in figure (7.19) the two main signals were highlighted and two red boxes were used to indicate the shift between the signals. A time delay is seen between the input and output signals. The PRBS waveform output is illustrated in figure (7.18) alongside the Offset PPM decoder output which as obtained through the use of the Altera Quartus II software STA tool, including the parallel form.

The signal is sent to the pin in the Offset PPM decoder once it has been picked up by the optical receiver. The original encoder output waveform will be reconstructed by the Offset PPM decoder if possible. This allows the original PCM sequence to be regenerated with permission. As shown in figure (7.18) and figure (7.19), it is clear that despite the delay in the decoding process, the regeneration of the PCM data has been achieved by the Offset decoder in this test. The optical Offset PPM system designed in this project uses FPGA to generate the correct Offset PPM. Following this, the optical Offset PPM system then encounters a delay of just half a clock cycle when decoding the Offset PPM back to the original PCM. M Decoder output obtained via the oscilloscope.

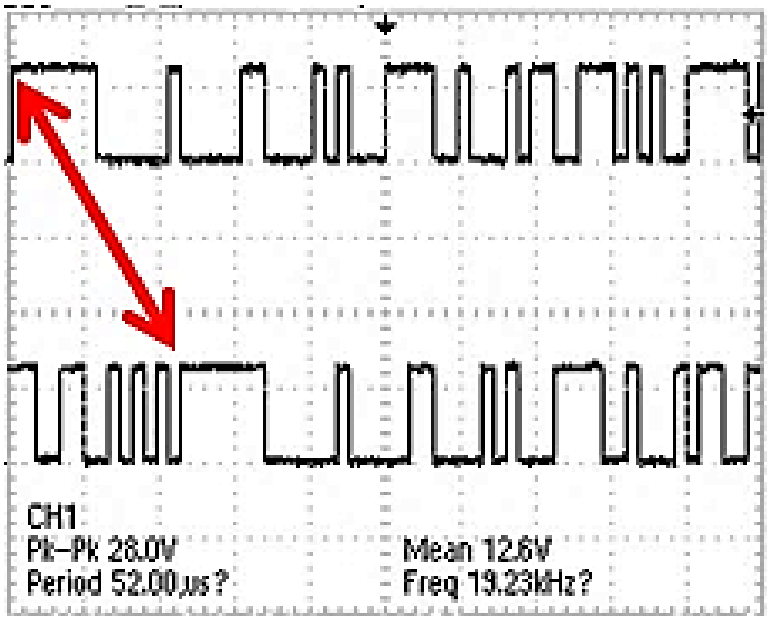


Figure 7-18 External PRBS output (upper trace) waveform and Offset PPM decoder output (bottom trace)

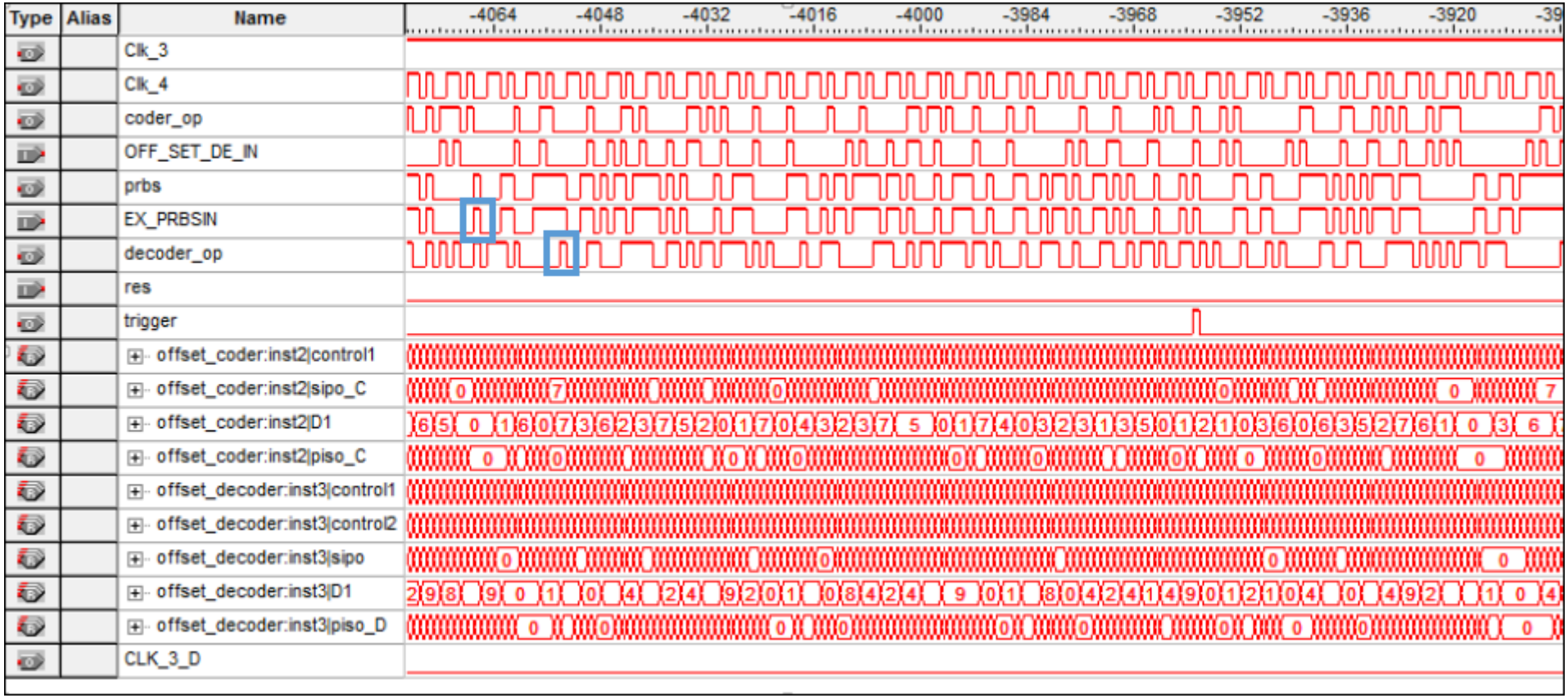


Figure 7-19 PRBS waveform output and Offset PPM Decoder output

7.5 Digital Transmission Measurements and Analysis

Two methods are used in this project to measure the errors that appear in this implementation. The first one is by using the facility of the HP 3780A as digital transmission analyser beside the main purpose of PRBS generator in this project.

The first test of transmission measurement for Offset PPM without optical set is used as a direct connection between the encoder and decoder, where the output of the offset encoder that goes directly to the Offset PPM decoder. BER has been measured in this test at the highest speed can be achieved by this instrument, the recorded results about 10^{-15} BER at a speed of 34 Mb/s.

The second test in this method was to measure the errors of full optical Offset PPM communication system. In this test the completed system was implemented with optical transmitter and optical receiver. The HP 3780A (PRBS generator/error detector) frequencies limitation of 2, 8, and 34 Mb/s, and the voltage comparator MAX941 speed limitation of 15Mb/s, therefore, the achieved at speed 10^{-12} is 8 Mb/s.

Figure (7.20) shows a minimum BER has been recorded by the device where the yellow LED with indicates <100 errors. This error shows that the offset PPM system is limited by optical set. The limitations of the optical set are inherent for instance; the length of the optical fibre, electronic noise such as the transmitter and receiver quality, and type of light source is used.

The analysis of Offset PPM system is described. Modifications to the standard two methods are suggested, which lead to averagely simple algebraic expressions for system operation. These results are used to investigate the relations between optical system performance and design parameters, and the conditions under which optimum performance may be obtained are investigated by using the first which is BER tester.

The output results were investigated shows that the first method has some limitation represent the speed of data circulation about 10 Mb/s.

Figure 7-20 Minimum BER recorded

However, a second method of digital transmission measurements has been used in order to improve the measurements of BER. The VHDL source code and FPGA were used together in order provide an improvement for BER measurements. Figure (7.21) shows the implementation of the digital transmission measurement based on the FPGA system.

The designed transmission measurement tester consists of two parts, the first part is a clock counter, which is used for to count the number of clock pulses per second, and the second part is introduced as an error counter. The output of the clock counter is a 40 parallel bit. In addition, the output of the error counter is the same number of clock counter and a same format as shown in figure (7.22). It is clearly representing a real time waveform of error and clock counters. Because of the voltage comparator speed limitation, the maximum speed data rate for Offset PPM system with optical set using the PRBS that which implemented by VHDL is 12 Mb/s with a 10^{-15} BER.

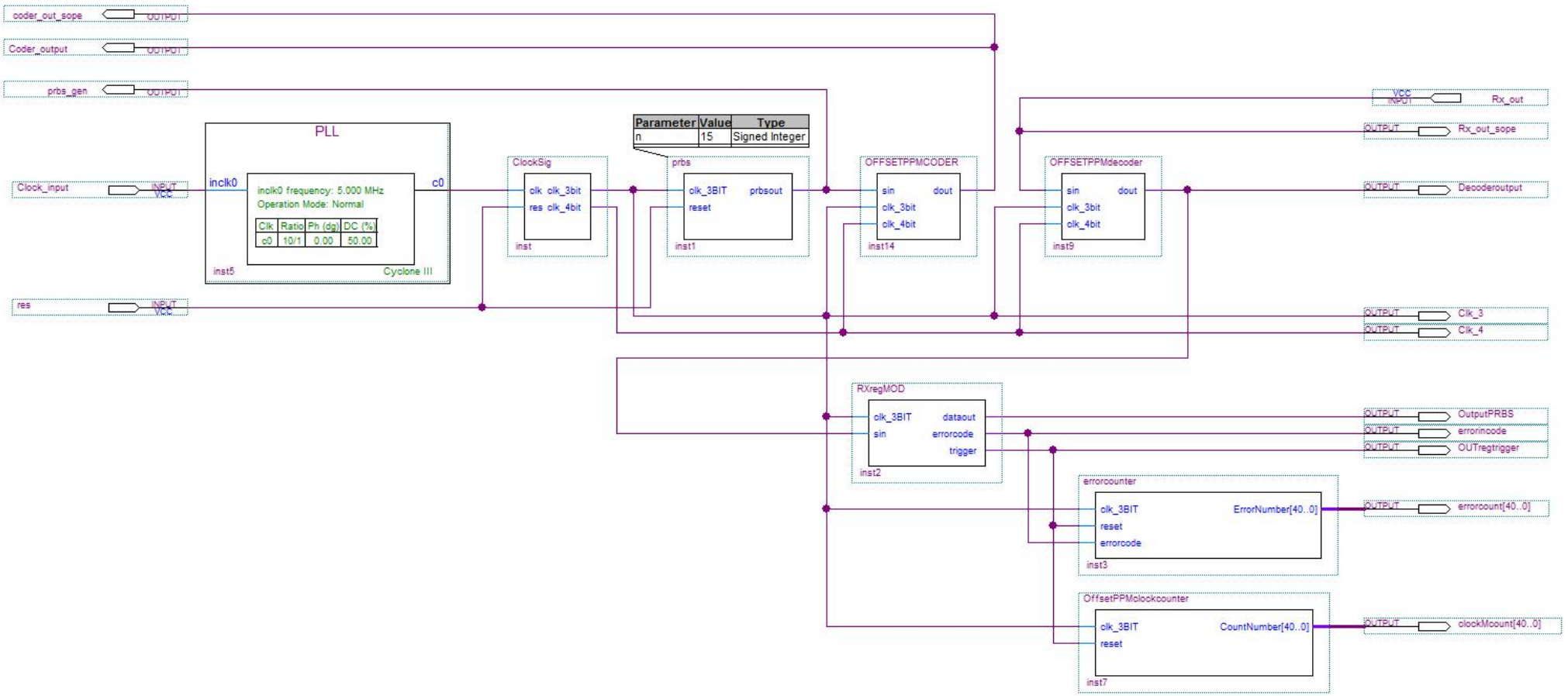


Figure 7-21 Digital transmission measurements and analysis based on FPGA

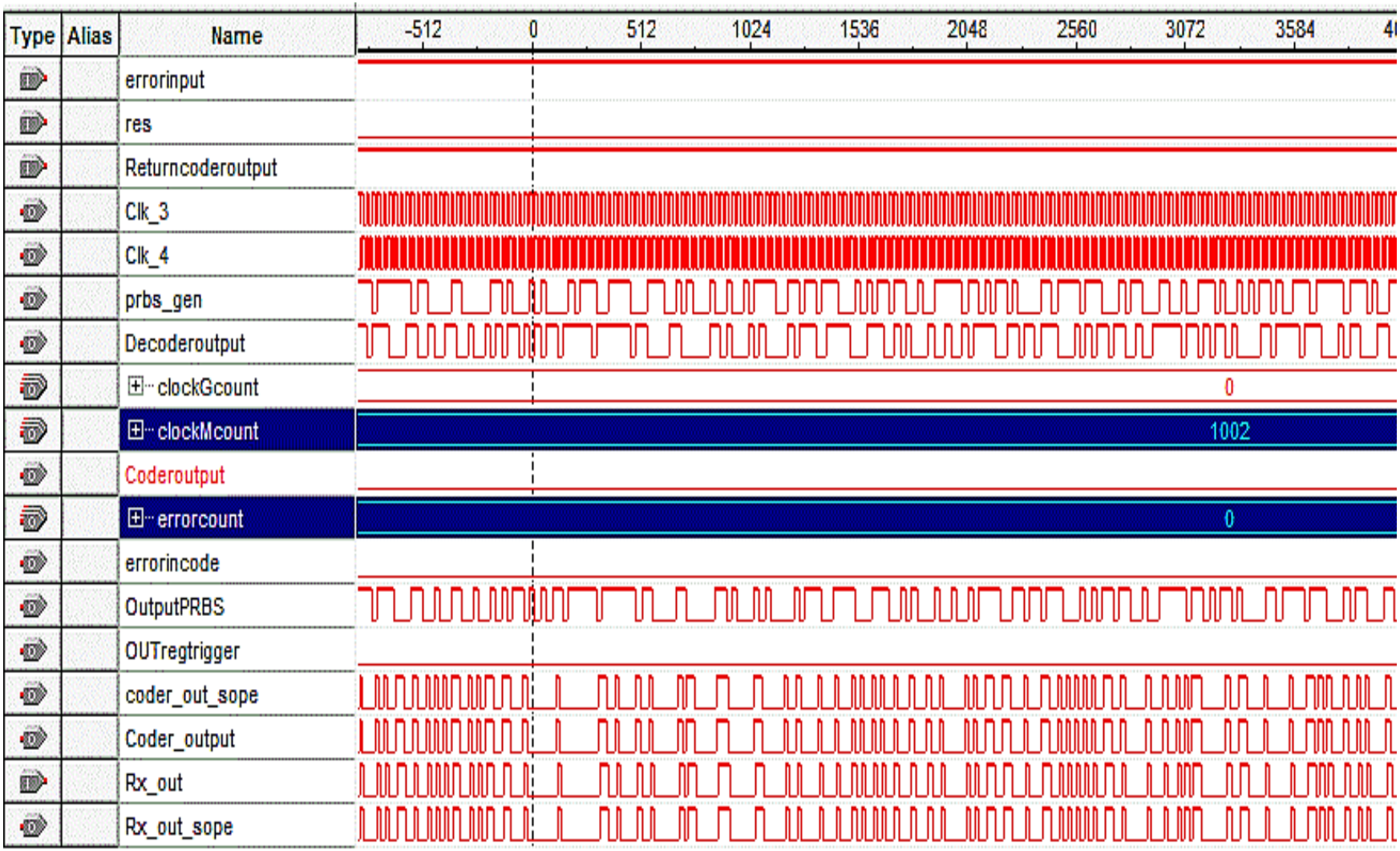


Figure 7-22 Real time waveform output error and clock counters

7.6 Summary

- This chapter described the full optical communication system that achieved to code an Offset PPM code.
- A discussion of POF that is used as an optical channel, and a description of the optical transmitter and receiver design and testing were being viewed with their specific parameters. Also a digital voltage comparator was described as well.
- The practical implementation of the system designed in this project has been outlined in detail, beginning with an introduction to the optical Offset PPM communication system, presenting the complete system and its components along with the hardware and software used.
- The PRBS generator that was used in this project as a sequence generator and a digital transmission measurement was discussed.
- Providing the simulation results, outlined the real-time results, and finally discussed the digital transmission measurements and analysis were being viewed with the achieved waveforms.
- As noted in this chapter, the implementation was achieved through the use of the Altera Quartus II software package alongside a DSP development board based on Cyclone III Field Programmable Gate Array (FPGA).
- The output results obtained through the practical implementation of the system designed in this project are in accordance with the results of the simulation test presented in Chapter 6, demonstrating a good level of similarity between the simulation test and the practical implementation procedure.

8 Conclusions and future work

8.1 Conclusions

Offset Pulse Position Modulation (Offset PPM) technique has been proposed as a novel coding scheme for applied over a fibre-optic link applications. The system has been implemented by verifying theoretical and practical testing methods. The simulation of the Offset PPM coding scheme is designed by Altera Quartus II with cyclone III. The simulations results show much agreement with practical results. The significant results of the first construction of Offset PPM encoder/decoder by using low cost electronic components improve that the system is easy and simple to use.

Moreover, the compactness and simplicity of any design is one of the important demands for embedded communication system. The Offset PPM coding system shows a high performance to introduce and can be used in optical fibre links applications. Results proved the theoretical proposal by showing that with the encoder generates correct Offset PPM sequences and that the decoder correctly decodes those sequences into Pulse Code Modulation (PCM).

The major aim of this work is to implement and increased the efficiency of optical fibre links systems in terms of BER, bandwidth of transferring data and optical system speed. This investigation of the performance of the Offset PPM achieved through optical fibre. Therefore, this system will be used to determine the performance of the Offset PPM waveforms through Plastic Optical Fibre (POF). Furthermore, a clock sequence will be required for this application in order to for Offset PPM decoding a PCM format.

A VHDL source code design downloaded on FPGA in order to implement a coding scheme, furthermore, an optical set together with this scheme is a full Offset PPM communication system.

In addition, the transmission measurements part implemented using VHDL based on FPGA has been designed and added to this Offset PPM scheme to measure the BER. This additional part added to the system significant features to measure a digital transmission performance. However, the coding scheme has some limitations in this application, for instance, FPGA clock limits. The digital transmission performance of Offset PPM is very high at 50 Mb/s of data rate has been achieved without any errors without using optical fibre set. Additionally, a digital transmission performance has been recorded of coding scheme with an optical transmission set, 12 Mb/s has been achieved without any errors. All the results of a novel system are recorded with laboratory environment.

8.2 Future Work

During the course of the research work all the key objectives that were set out in this thesis have been completed to a satisfactory extent. However, further improvements can be made in order to modify and optimised some of the objectives that have been completed. In addition, further investigations and testing need to be carried out for greater optimisation. This section discusses some of the main suggestions that have been made to improve the proposed coding scheme further.

- This work considers the optical fibre medium. Investigation on the performance of offset PPM in free space may be carried out in the future scope.
- Different types of transmitter/receiver sets may be used for future work.
- Clock and Data Recovery (CDR), this may be looked into in future scope.
- The complete VHDL Offset PPM system, with error corrector, to be loaded on an FPGA and the optical communication system (transmitter/receiver) connected. Errors will be introduced into the system by moving the optical transmitter away from the optical receiver.

Comparisons of different outcomes of the Offset PPM decoder and the Offset PPM error corrector decoder will be required to determine the accuracy and sensitivity.

9 Appendixes

9.1 VHDL codes

ClockSig

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY ClockSig IS
    PORT
   (
      clk                  : IN STD_LOGIC;--(Clock 12 time speed to enable 3 - 4 bit interface)
      clk_2bit   : OUT STD_LOGIC;
      clk_3bit   : OUT STD_LOGIC;
      clk_4bit   : OUT STD_LOGIC;
      res                     : IN STD_LOGIC
   );
END ClockSig;

ARCHITECTURE behv OF ClockSig IS
SIGNAL  divide2      :  STD_LOGIC_VECTOR (1 downto 0):="10";
SIGNAL  divide3      :  STD_LOGIC_VECTOR (2 downto 0):="100";
SIGNAL  divide4      :  STD_LOGIC_VECTOR (3 downto 0):="1000";
SIGNAL  clk_2                :  STD_LOGIC;
SIGNAL  clk_3                :  STD_LOGIC;
SIGNAL  clk_4                :  STD_LOGIC;

BEGIN

   PROCESS
      BEGIN
      WAIT UNTIL (clk'EVENT AND clk = '1');
         IF (res = '1') THEN
                  clk_2          <= '0';
                  clk_3          <= '0';
                  clk_4          <= '0';
                  clk_3bit       <= '0';
                  clk_4bit       <= '0';
         ELSIF (res = '0') THEN

                        IF divide2(0) ='1' THEN
                              clk_2  <= not(clk_2);
                        END IF;

         IF divide3(0) ='1' THEN
                              clk_4  <= not(clk_4);
```

```
                    END IF;

                    IF  divide4(0) ='1' THEN
                clk_3 <= not(clk_3);
                    END IF;
                    divide2 <= divide2(0) & divide2(1);
        divide3 <= divide3(1 downto 0) & divide3(2);
        divide4 <= divide4(2 downto 0) & divide4(3);
        clk_2bit <= clk_2;
                    clk_3bit <= clk_3;
                    clk_4bit <= clk_4;

    END IF;
   END PROCESS;
END behv;

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
prbs

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY prbs IS
    GENERIC(n: natural := 7);    --(set to 7 or 15 for PRBS bit size)
    --this enables different sized PRBS generators to be used
    PORT
        (       clk_3BIT                : IN STD_LOGIC;
                reset                   : IN STD_LOGIC;
                prbsout                 : OUT STD_LOGIC
        --trigger                 : OUT STD_LOGIC
        );
   END prbs;

ARCHITECTURE behv OF prbs IS

SIGNAL  PR          :  STD_LOGIC_VECTOR (n-1 downto 0);

BEGIN
      PROCESS(clk_3bit, reset)
      BEGIN

        IF reset ='1' THEN

                    IF n = 7 THEN
                    PR <= "1111111";
                    ELSIF n = 15 THEN
                    PR <= "111111111111111";
```

```
            END IF;

        ELSIF (clk_3bit'EVENT AND clk_3bit = '1') THEN
              PR <= PR(n-2 downto 0)&(PR(n-1)XOR PR(n-2));

        END IF;
   END PROCESS;

            prbsout <= PR(n-1);
        --trigger <= PR(9) AND PR(8) AND PR(7) AND PR(6) AND PR(5) AND PR(4) AND
PR(3) AND PR(2) AND PR(1) AND PR(0);

END behv;
```

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

OFFSET PPM encoder

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.STD_LOGIC_UNSIGNED.all;
ENTITY OFFSETPPMCODER IS
port(    sin                    : IN STD_LOGIC;
      clk_3bit   : IN STD_LOGIC;
         clk_4bit         : IN STD_LOGIC;
      dout               : OUT STD_LOGIC
     );
end OFFSETPPMCODER;
architecture behaviour of OFFSETPPMCODER IS

        SIGNAL   control1    : STD_LOGIC_VECTOR(2 downto 0); --:= "100";-- changing this
value 1 position changes the op as not synced 24 bit output since taking 6 blocks of 3 instead of 5.
        SIGNAL        sipo          :      STD_LOGIC_VECTOR(14      downto      0)      :=
"000000000000000";
        SIGNAL        piso          : STD_LOGIC_VECTOR(3 downto 0);
        SIGNAL        reg1          : STD_LOGIC_VECTOR(2 downto 0) := "000";
--      SIGNAL        D2                  : STD_LOGIC_VECTOR(2 downto 0) := "000";
        SIGNAL        load_reg      : STD_LOGIC;
        SIGNAL   initflag1    : STD_LOGIC := '1';  -- used to initialise/sync input stream- once
detected reset to 0 under synced operation
BEGIN

coder_input: PROCESS   -- loads the input data using the 3 bit clock

            BEGIN
            WAIT UNTIL (clk_3bit'EVENT AND clk_3bit = '1');
                  control1 <= (control1(0)) & (control1(2 downto 1));
               IF initflag1 ='1' THEN
```

```
                    IF sipo = "111111111111111" THEN
                   -- basic sync sequence from PRBS 111111111111111
                   -- 100011111110111    sync sequence produced from all 1's encoded by
15/11
                  -- note: the sequence needs to be input in reverse order in the waveform test
file
                  -- extra bit in reg to account for extra clocks
                          initflag1 <= '0';
                          reg1 <= "111";
                          control1 <= "001";
                    END IF;

                    ELSE                    --   ELSIF initflag1 ='0' THEN
                     IF control1(1) = '1'  THEN
                                reg1 <= sipo(0) & sipo (1) & sipo(2);
                          END IF;

                    END IF;
                  sipo <= sin & sipo(14 downto 1);
                  --D2 <= reg1 ; --(3 downto 1);
                   --sipo <= sipo(1 downto 0) & sin;

END PROCESS;

coder_output: PROCESS -- Outputs the code data using the 4 bit clock

                BEGIN
                WAIT UNTIL (clk_4bit'EVENT AND clk_4bit = '1');

                IF (control1(1) = '1') AND (load_reg = '1') THEN

                                load_reg <= '0';
                                --piso  <= D2(0) & (D2(1) AND D2(2)) & (D2(1) AND NOT D2(2))
& (NOT D2(1) AND D2(2));
                                --piso  <= D1(2) & (D1(1) AND D1(0)) & (D1(1) AND NOT D1(0))
& (NOT D1(1) AND D1(0));
                                -- the above coding is performed using logic, which automatically
assigns a valid code for data with errors
                                -- a case statement i.e a look-up table could also be used, as below.
                                 case reg1 is
                                        when "000"    => piso <= "0000";
                                        when "001"    => piso <= "0001";
                                        when "010"    => piso <= "0010";
                                        when "011"    => piso <= "0100";
                                        when "100"    => piso <= "1000";
                                        when "101"    => piso <= "1001";
                                        when "110"    => piso <= "1010";
                                        when "111"    => piso <= "1100";
```

```
                        when others => piso <= "0000";
                    end case;

                ELSE

                    --piso <= '0' & piso(3 downto 1); -- needs order cahnging
                    piso <= piso(2 downto 0) & '0'; -- needs order cahnging

                    load_reg <= '1';

                END IF;
                dout  <= piso (3);  --serial output

END PROCESS;
END behaviour;
```

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

Offset PPM decoder

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.STD_LOGIC_UNSIGNED.all;
ENTITY OFFSETPPMdecoder IS
port(   sin                     : IN std_logic;
      clk_3bit   : IN STD_LOGIC;
         clk_4bit         : IN STD_LOGIC;
      dout                : OUT std_logic
      --validflag         : OUT std_logic
      );
end OFFSETPPMdecoder;
architecture behaviour of OFFSETPPMdecoder IS
SIGNAL   control1    : STD_LOGIC_VECTOR(3 downto 0):="0001";
SIGNAL   control2    : STD_LOGIC_VECTOR(2 downto 0):="001";
SIGNAL        sipo          : STD_LOGIC_VECTOR(20 downto 0); --:="000000000";
SIGNAL        piso_D              : STD_LOGIC_VECTOR(2 downto 0):="000";
SIGNAL        D1                  : STD_LOGIC_VECTOR(3 downto 0):="0000";
SIGNAL   initflag1    : STD_LOGIC := '1';  -- used to initialise/sync input stream- once detected
reset to 0 under synced operation

BEGIN
decoder_input: PROCESS

        BEGIN
        WAIT UNTIL (clk_4bit'EVENT AND clk_4bit = '1');

                sipo <= sin & sipo(20 downto 1);
```

```
                IF initflag1 ='1' THEN

                        IF sipo(20 downto 1) = "00110011001100110011" THEN
                        --
                        --pre encodede using 15/11 IF sipo(20 downto 1) =
"11000100110010100001" THEN
                        -- sync sequence produced from all 1's encoded by 15/11
                        -- note: the sequence needs to be input in reverse order in the waveform test
file
                                initflag1 <= '0';
                                control1 <= "1000";
                        END IF;

                ELSE
                        IF control1(3) = '1'  THEN
                                D1 <= sipo (3 downto 0);
                        END IF;
                        control1 <= control1(0) & (control1(3 downto 1));
            END IF;
END PROCESS;

 decoder_output: PROCESS
         BEGIN
                WAIT UNTIL (clk_3bit'EVENT AND clk_3bit = '1');

                IF initflag1 ='1' THEN
                        control2 <= "100";
                ELSE
                        IF control2(2)= '1' THEN

                                piso_D <= D1(0) & (D1(2) OR D1(1)) & (D1(3) OR D1(1));
                                --piso_D <= D1(3) & (D1(1) OR D1(2)) & (D1(0) OR D1(2));
                                -- decode logic : this could also be performed using a case statement
(look-up table)
                                -- use reverse case statement as used for encoder
                    ELSIF control2(2)= '0' THEN

                                --piso_D <= '0' & piso_D(2 downto 1);
                                  piso_D <= piso_D(1 downto 0) & '0';
                        END IF;
                        control2 <= control2(0) & control2(2 downto 1);
                END IF;
                        dout <= piso_D(2);
                        --dout <= piso_D(0);
                  --validflag <= initflag1;
                        -- signals that the dout is synchronised when validflag = '0'
                        -- could use to signal 15/11 decoder to start
END PROCESS;
```

```
END behaviour;

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
Error counter
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
-- this code could be merged with the clock count and output bit errors per number of clocks
-- need to improve so doesn't output error count until after reset - currently counts errors until sync
ENTITY errorcounter IS
    PORT
        (       clk_3BIT                : IN STD_LOGIC;
                        reset                   : IN STD_LOGIC;
        errorcode               : IN STD_LOGIC;
                        ErrorNumber             : OUT STD_LOGIC_VECTOR (40 downto 0));
  END errorcounter;

ARCHITECTURE behv OF errorcounter  IS

  signal Count: std_logic_vector(40 downto 0);

begin

  PROCESS
  BEGIN
    WAIT UNTIL (clk_3bit'EVENT AND clk_3bit = '1');

     if reset = '1' then
        Count <= Count - Count;

     else
        if errorcode = '1' then
          Count <= Count + 1;
        end if;
     end if;
  end process;

  ErrorNumber          <= Count;

end behv;


XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

Clock counter


library IEEE;
```

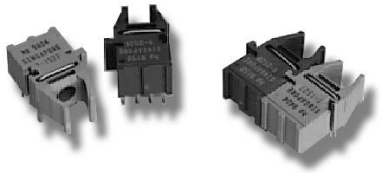
```
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
---------------------------------
--              Entity Declaration              --
---------------------------------
ENTITY OffsetPPMclockcounter IS
    PORT
        (       clk_3BIT                : IN STD_LOGIC;
                reset                   : IN STD_LOGIC;
                CountNumber : OUT STD_LOGIC_VECTOR (40 downto 0));
   END OffsetPPMclockcounter ;
---------------------------------
--      Architecture Declaration       --
---------------------------------
ARCHITECTURE behv OF OffsetPPMclockcounter   IS

   signal Pre_Count: std_logic_vector(40 downto 0);

begin
   process(clk_3BIT, reset, Pre_Count)
   begin
                if reset = '1' then
                        Pre_Count <= Pre_Count - Pre_Count;
                elsif (clk_3BIT='1' and clk_3BIT'event) then
                        Pre_Count <= Pre_Count + 1;
                end if;
   end process;
   CountNumber                  <= Pre_Count;
end behv;
```

9.2 Optical transmitter/receiver data sheet

HFBR-0507Z Series
HFBR-15X7Z Transmitters
HFBR-25X6Z Receivers

125 Megabaud Versatile Link

The Versatile Fiber Optic Connection



Data Sheet

Description

The 125 MBd Versatile Link (HFBR-0507Z Series) is the most cost-effective fiber-optic solution for transmission of 125 MBd data over 100 meters. The data link consists of a 650 nm LED transmitter, HFBR-15X7Z, and a PIN/ preamp receiver, HFBR-25X6Z. These can be used with low-cost plastic or silica fiber. One mm diameter plastic fiber provides the lowest cost solution for distances under 25 meters. The lower attenuation of silica fiber allows data transmission over longer distance, for a small difference in cost. These components can be used for high speed data links without the problems common with copper wire solutions, at a competitive cost.

The HFBR-15X7Z transmitter is a high power 650 nm LED in a low cost plastic housing designed to efficiently couple power into 1 mm diameter plastic optical fiber and 200 ∝ m Hard Clad Silica (HCS®) fiber. With the recommended drive circuit, the LED operates at speeds from 1-125 MBd. The HFBR-25X6Z is a high bandwidth analog receiver containing a PIN photodiode and internal transimpedance amplifier. With the recommended application circuit for 125 MBd operation, the performance of the complete data link is specified for of 0-25 meters with plastic fiber and 0-100 meters with 200 ∝ m HCS® fiber. A wide variety of other digitizing circuits can be combined with the HFBR-0507Z Series to optimize perfor-mance and cost at higher and lower data rates.

Features

10 RoHS-compliant

11 Data transmission at signal rates of 1 to 125 MBd over distances of 100 meters

12 Compatible with inexpensive, easily terminated plastic optical fiber, and with large core silica fiber

13 High voltage isolation

14 Transmitter and receiver application circuit schematics and recommended board layouts available

15 Interlocking feature for single channel or duplex links, in a vertical or horizontal mount configuration

Applications

1)Intra-system links: board-to-board, rack-to-rack

2) Telecommunications switching systems

3)Computer-to-peripheral data links, PC bus extension

4) Industrial control

5) Proprietary LANs

6) Digitized video

7) Medical instruments

8) Reduction of lightning and voltage transient susceptibility

HCS® is a registered trademark of Spectran Corporation.

HFBR-0507Z Series

125 MBd Data Link

Data link operating conditions and performance are specified for the HFBR-15X7Z transmitter and HFBR-25X6Z receiver in the recommended applications circuits shown in Figure 1. This circuit has been optimized for 125 MBd operation. The Applications Engineering Department in the Avago Optical Communication Division is available to assist in optimizing link performance for higher or lower speed operation.

Recommended Operating Conditions for the Circuits in Figures 1 and 2.

Parameter	Symbol	Min.	Max.	Unit	Reference
Ambient Temperature	T_A	0	70	°C	
Supply Voltage	V_{CC}	+4.75	+5.25	V	
Data Input Voltage – Low	V_{IL}	V_{CC} -1.89	V_{CC} -1.62	V	
Data Input Voltage – High	V_{IH}	V_{CC} -1.06	V_{CC} -0.70	V	
Data Output Load	R_L	45	55	Ω	Note 1
Signaling Rate	f_S	1	125	MBd	
Duty Cycle	D.C.	40	60	%	Note 2

Link Performance: 1-125 MBd, BER ≤ 10^{-9}, under recommended operating conditions with recommended transmit and receive application circuits.

Parameter	Symbol	Min.[3]	Typ.[4]	Max.	Unit	Condition	Reference
Optical Power Budget, 1 m POF	OPB_{POF}	11	16		dB		Note 5,6,7
Optical Power Margin, 20 m Standard POF	$OPM_{POF,20}$	3	6		dB		Note 5,6,7
Link Distance with Standard 1 mm POF	l	20	27		m		
Optical Power Margin, 25 m Low Loss POF	$OPM_{POF,25}$	3	6		dB		Note 5,6,7
Link Distance with Extra Low Loss 1 mm POF	l	25	32		m		
Optical Power Budget, 1 m HCS	OPB_{HCS}	7	12		dB		Note 5,6,7
Optical Power Margin, 100 m HCS	$OPM_{HCS,100}$	3	6		dB		Note 5,6,7
Link Distance with HCS Cable	l	100	125		m		

Notes:

1. If the output of U4C in Figure 1, page 4 is transmitted via coaxial cable, terminate with a 50 Ω resistor to V_{CC} - 2 V.

- Run length limited code with maximum run length of 10 µ s.
- Minimum link performance is projected based on the worst case specifications of the HFBR-15X7Z transmitter, HFBR-25X6Z receiver, and POF cable, and the typical performance of other components (e.g. logic gates, transistors, resistors, capacitors, quantizer, HCS cable).
- Typical performance is at 25° C, 125 MBd, and is measured with typical values of all circuit components.
- Standard cable is HFBR-RXXYYYZ plastic optical fiber , with a maximum attenuation of 0.24 dB/m at 650 nm and NA = 0.5. Extra low loss cable is HFBR-EXXYYYZ plastic optical fiber, with a maximum attenuation of 0.19 dB/m at 650 nm and NA = 0.5. HCS cable is HFBR-H/VXXYYY glass optical fiber, with a maximum attenuation of 10 dB/km at 650 nm and NA = 0.37.
- Optical Power Budget is the difference between the transmitter output power and the receiver sensitivity, measured after 1 meter of fiber.

The minimum OPB is based on the limits of optical component performance over temperature, process, and recommended power supply variation.

- The Optical Power Margin is the available OPB after including the effects of attenuation and modal dispersion for the minimum link distance: OPM = OPB - (attenuation power loss + modal dispersion power penalty). The minimum OPM is the margin available for longterm LED LOP degradation and additional fixed passive losses (such as in-line connectors) in addition to the minimum specified distance.

Plastic Optical Fiber (1 mm POF) Transmitter Application Circuit: Performance of the HFBR-15X7Z transmitter in the recommended application circuit (Figure 1) for POF; 1-125 MBd, 25° C.

Parameter	Symbol	Typical	Unit	Condition	Note
Average Optical Power 1 mm POF	P_{avg}	-9.7	dBm	50% Duty Cycle	Note 1, Fig 3
Average Modulated Power 1 mm POF	P_{mod}	-11.3	dBm		Note 2, Fig 3
Optical Rise Time (10% to 90%)	t_r	2.1	ns	5 MHz	
Optical Fall Time (90% to 10%)	t_f	2.8	ns	5 MHz	
High Level LED Current (On)	$I_{F,H}$	19	mA		Note 3
Low Level LED Current (Off)	$I_{F,L}$	3	mA		Note 3
Optical Overshoot - 1 mm POF		45	%		
Transmitter Application Circuit Current Consumption - 1 mm POF	I_{CC}	110	mA		Figure 1

Hard Clad Silica Fiber (200 ∝ m HCS) Transmitter Application Circuit: Performance of the HFBR-15X7Z transmitter in the recommended application circuit (Figure 1) for HCS; 1-125 MBd, 25° C.

Parameter	Symbol	Typical	Unit	Condition	Note
Average Optical Power 200 ∝ m HCS	P_{avg}	-14.6	dBm	50% Duty Cycle	Note 1, Fig 3
Average Modulated Power 200 ∝ m HCS	P_{mod}	-16.2	dBm		Note 2, Fig 3
Optical Rise Time (10% to 90%)	t_r	3.1	ns	5 MHz	
Optical Fall Time (90% to 10%)	t_f	3.4	ns	5 MHz	
High Level LED Current (On)	$I_{F,H}$	60	mA		Note 3
Low Level LED Current (Off)	$I_{F,L}$	6	mA		Note 3
Optical Overshoot - 200 ∝ m HCS		30	%		
Transmitter Application Circuit Current Consumption - 200 ∝ m HCS	I_{CC}	130	mA		Figure 1

Notes:

- Average optical power is measured with an average power meter at 50% duty cycle, after 1 meter of fiber.
- To allow the LED to switch at high speeds, the recommended drive circuit modulates LED light output between two non-zero power levels. The modulated (useful) power is the difference between the high and low level of light output power (transmitted) or input power (received), which can be measured with an average power meter as a function of duty cycle (see Figure 3). Average Modulated Power is defined as one half the slope of the average power versus duty cycle:

$$\text{Average Modulated Power} = \frac{[\text{Pavg @ 80\% duty cycle} - \text{Pavg @ 20\% duty cycle}]}{(2)\,[0.80 - 0.20]}$$

\emdash High and low level LED currents refer to the current through the HFBR-15X7Z LED. The low level LED “off” current, sometimes referred to as “hold-on” current, is prebias supplied to the LED during the off state to facilitate fast switching speeds.

Plastic and Hard Clad Silica Optical Fiber Receiver Application Circuit: Performance[4] of the HFBR-25X6Z receiver in the recommended application circuit (Figure 1); 1-125 MBd, 25° C unless otherwise stated.

Parameter	Symbol	Typical	Unit	Condition	Note
Data Output Voltage - Low	V_{OL}	V_{CC} -1.7	V	R_L = 50 Ω	Note 5
Data Output Voltage - High	V_{OH}	V_{CC} -0.9	V	R_L = 50 Ω	Note 5
Receiver Sensitivity to Average Modulated Optical Power 1 mm POF	P_{min}	-27.5	dBm	50% eye opening	Note 2
Receiver Sensitivity to Average Modulated Optical Power 200 µ m HCS	P_{min}	-28.5	dBm	50% eye opening	Note 2
Receiver Overdrive Level of Average Modulated Optical Power 1 mm POF	P_{max}	-7.5	dBm	50% eye opening	Note 2
Receiver Overdrive Level of Average Modulated Optical Power 200 µ m HCS	P_{max}	-10.5	dBm	50% eye opening	Note 2
Receiver Application Circuit Current Consumption	I_{CC}	85	mA	R_L = ∞	Figure 1

Notes:

1. Performance in response to a signal from the HFBR-15X7Z transmitter driven with the recommended circuit at 1-125 MBd over 1 meter of HFBR-RZ/EXXYYYZ plastic optical fiber or 1 meter of HFBR-H/VXXYYY hard clad silica optical fiber.
5. Terminated through a 50 Ω resistor to V_{CC} - 2 V.

- If there is no input optical power to the receiver, electrical noise can result in false triggering of the receiver. In typical applications, data encoding and error detection prevent random triggering from being interpreted as valid data. Refer to Applications Note 1066 for design guidelines.

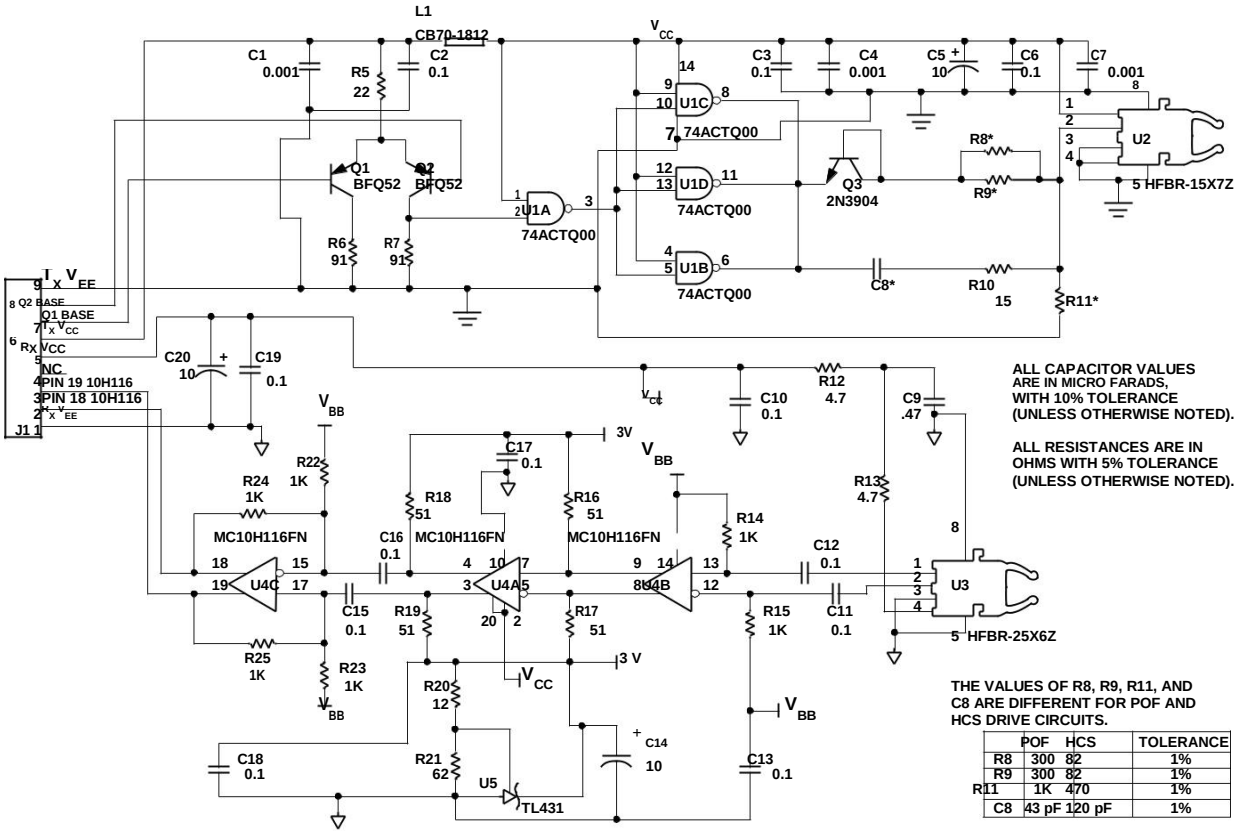


Figure 1. Transmitter and receiver application circuit with +5 V ECL inputs and outputs.

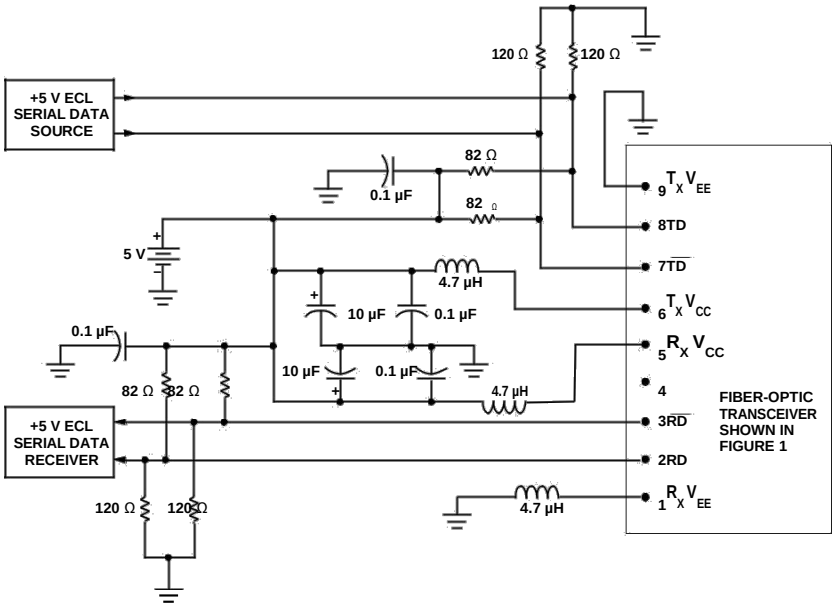


Figure 2. Recommended power supply filter and +5 V ECL signal terminations for the transmitter and receiver application circuit of Figure 1.

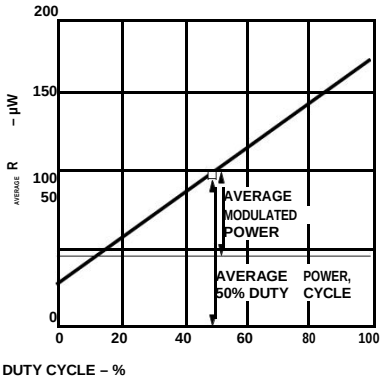


Figure 3. Average modulated power.

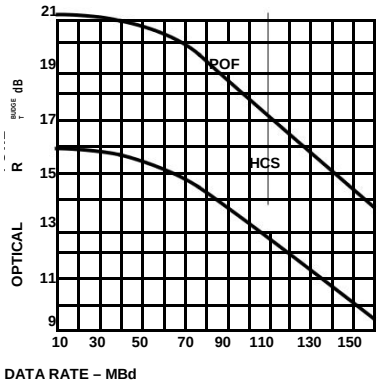


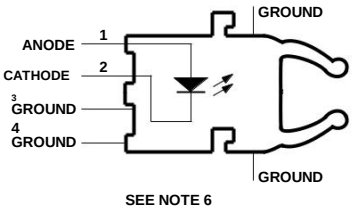
Figure 4. Typical optical power budget vs. data rate.

125 Megabaud Versatile Link
Transmitter

HFBR-15X7Z Series

Description

The HFBR-15X7Z transmitters incorporate a 650 nanometer LED in a horizontal (HFBR-1527Z) or vertical (HFBR-1537Z) gray housing. The HFBR-15X7Z transmitters are suitable for use with current peaking to decrease response time and can be used with HFBR-25X6Z receivers in data links operating at signal rates from 1 to 125 megabaud over 1 mm diameter plastic optical fiber or 200 ∝ m diameter hard clad silica glass optical fiber. Refer to Application Note 1066 for details for recommended interface circuits.



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Reference
Storage Temperature	T_S	-40	85	°C	
Operating Temperature	T_O	-40	70	°C	
Lead Soldering Temperature Cycle Time			260	°C	Note 1
			10	s	
Transmitter High Level Forward Input Current	$I_{F,H}$		120	mA	50% Duty Cycle ε 1 MHz
Transmitter Average Forward Input Current	$I_{F,AV}$		60	mA	
Reverse Input Voltage	V_R		3	V	

CAUTION: The small junction sizes inherent to the design of this component increase the component's suscepti-bility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

WARNING: WHEN VIEWED UNDER SOME CONDITIONS, THE OPTICAL PORT MAY EXPOSE THE EYE BEYOND THE MAXIMUM PERMISSIBLE EXPOSURE RECOMMENDED IN ANSI Z136.2, 1993. UNDER MOST VIEWING CONDITIONS THERE IS NO EYE HAZARD.

Electrical/Optical Characteristics 0 to 70° C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.[2]	Max.	Unit	Condition	Note
Transmitter Output Optical Power, 1 mm POF	P_T	-9.5 -10.4	-7.0	-4.8 -4.3	dBm	$I_{F,dc}$ = 20 mA, 25° C 0-70° C	Note 3
Transmitter Output Optical Power, 1 mm POF	P_T	-6.0 -6.9	-3.0	-0.5 -0.0	dBm	$I_{F,dc}$ = 60 mA, 25° C 0-70° C	Note 3
Transmitter Output Optical Power, 200 µ m HCS®	P_T	-14.6 -15.5	-13.0	-10.5 -10.0	dBm	$I_{F,dc}$ = 60 mA, 25° C 0-70° C	Note 3
Output Optical Power Temperature Coefficient	$\frac{\Delta P_T}{\Delta T}$		-0.02		dB/° C		
Peak Emission Wavelength	λ_{PK}	640	650	660	nm		
Peak Wavelength Temperature Coefficient	$\frac{\Delta \lambda}{\Delta T}$		0.12		nm/° C		
Spectral Width	FWHM		21		nm	Full Width, Half Maximum	
Forward Voltage	V_F	1.8	2.1	2.4	V	I_F = 60 mA	
Forward Voltage Temperature Coefficient	$\frac{\Delta V_F}{\Delta T}$		-1.8		mV/° C		
Transmitter Numerical Aperture	NA		0.5				
Thermal Resistance, Junction to Case	θ_{jc}		140		° C/W		Note 4
Reverse Input Breakdown Voltage	V_{BR}	3.0	13		V	$I_{F,dc}$ = -10 µ A	
Diode Capacitance	C_O		60		pF	V_F = 0 V, f = 1 MHz	
Unpeaked Optical Rise Time, 10% - 90%	t_r		12		ns	I_F = 60 mA f = 100 kHz	Figure 1 Note 5
Unpeaked Optical Fall Time, 90% - 10%	t_f		9		ns	I_F = 60 mA f = 100 kHz	Figure 1 Note 5

Notes:

1. 1.6 mm below seating plane.
2. Typical data is at 25° C.
3. Optical Power measured at the end of 0.5 meter of 1 mm diameter plastic or 200 µ m diameter hard clad silica optical fiber with a large area detector.
4. Typical value measured from junction to PC board solder joint for horizontal mount package, HFBR-1527Z. θ_{jc} is approximately 30° C/W higher for vertical mount package, HFBR-1537Z.
5. Optical rise and fall times can be reduced with the appropriate driver circuit; refer to Application Note 1066.
6. Pins 5 and 8 are primarily for mounting and retaining purposes, but are electrically connected; pins 3 and 4 are electrically unconnected. It is recommended that pins 3, 4, 5, and 8 all be connected to ground to reduce coupling of electrical noise.
7. Refer to the Versatile Link Family Fiber Optic Cable and Connectors Technical Data Sheet for cable connector options for 1 mm plastic optical fiber and 200 µ m HCS fiber.
8. The LED current peaking necessary for high frequency circuit design contributes to electromagnetic interference (EMI). Care must be taken in circuit board layout to minimize emissions for compliance with governmental EMI emissions regulations. Refer to Application Note 1066 for design guidelines.

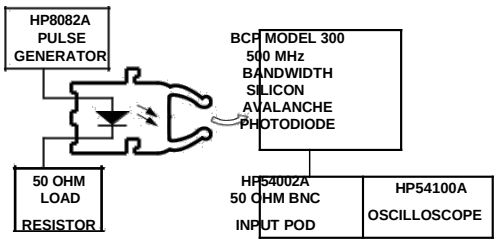


Figure 1. Test circuit for measuring unpeaked rise and fall times.

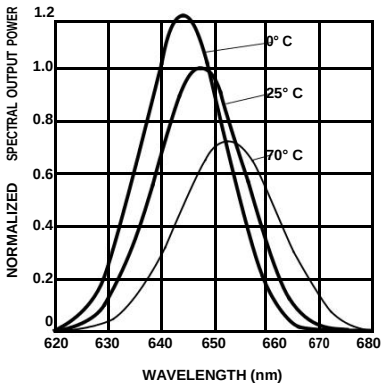


Figure 2. Typical spectra normalized to the 25° C peak.

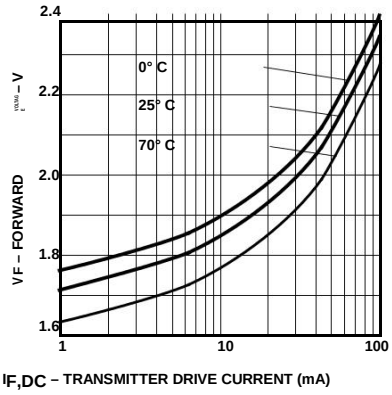


Figure 3. Typical forward voltage vs. drive current.

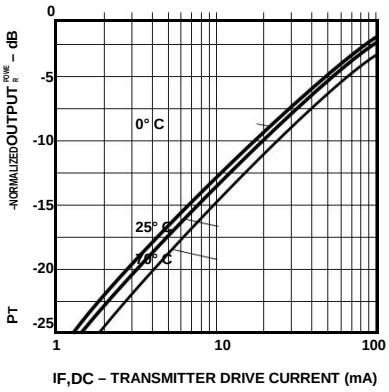


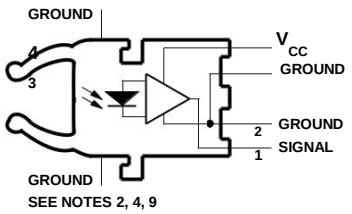
Figure 4. Typical normalized output optical power vs. drive current.

125 Megabaud Versatile Link Receiver

HFBR-25X6Z Series

Description

The HFBR-25X6Z receivers contain a PIN photodiode and transimpedance pre-amplifier circuit in a horizontal (HFBR-2526Z) or vertical (HFBR-2536Z) blue housing, and are designed to interface to 1mm diameter plastic optical fiber or 200 ∝ m hard clad silica glass optical fiber. The receivers convert a received optical signal to an analog output voltage. Follow-on circuitry can optimize link performance for a variety of distance and data rate requirements. Electrical bandwidth greater than 65 MHz allows design of high speed data links with plastic or hard clad silica optical fiber. Refer to Application Note 1066 for details for recommended interface circuits.



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Reference
Storage Temperature	T_S	- 40	+75	°C	
Operating Temperature	T_A	0	+70	°C	
Lead Soldering Temperature			260	°C	Note 1
Cycle Time			10	s	
Signal Pin Voltage	V_O	-0.5	V_{CC}	V	
Supply Voltage	V_{CC}	-0.5	6.0	V	
Output Current	I_O		25	mA	

CAUTION: The small junction sizes inherent to the design of this component increase the component's suscepti-bility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Electrical/Optical Characteristics 0 to 70° C; 5.25 V ≥ V_{CC} ≥ 4.75 V; power supply must be filtered (see Figure 1, Note 2).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Note
AC Responsivity 1 mm POF	$R_{P,APF}$	1.7	3.9	6.5	mV/µ W	650 nm	Note 4
AC Responsivity 200 µ m HCS	$R_{P,HCS}$	4.5	7.9	11.5	mV/µ W		
RMS Output Noise	V_{NO}		0.46	0.69	mV_{RMS}		Note 5
Equivalent Optical Noise Input Power, RMS - 1 mm POF	$P_{N,RMS}$		- 39	-36	dBm		Note 5
Equivalent Optical Noise Input Power, RMS - 200 µ m HCS	$P_{N,RMS}$		-42	-40	dBm		Note 5
Peak Input Optical Power - 1 mm POF	P_R			-5.8 -6.4	dBm dBm	5 ns PWD 2 ns PWD	Note 6
Peak Input Optical Power - 200 µ m HCS	P_R			-8.8 -9.4	dBm dBm	5 ns PWD 2 ns PWD	Note 6
Output Impedance	Z_O		30		Ω	50 MHz	Note 4
DC Output Voltage	V_O	0.8	1.8	2.6	V	P_R = 0 µ W	
Supply Current	I_{CC}		9	15	mA		
Electrical Bandwidth	BW_E	65	125		MHz	-3 dB electrical	
Bandwidth * Rise Time			0.41		Hz * s		
Electrical Rise Time, 10-90%	t_r		3.3	6.3	ns	P_R = -10 dBm peak	
Electrical Fall Time, 90-10%	t_f		3.3	6.3	ns	P_R = -10 dBm peak	
Pulse Width Distortion	PWD		0.4	1.0	ns	P_R = -10 dBm peak	Note 7
Overshoot			4		%	P_R = -10 dBm peak	Note 8

Notes:

c) 1.6 mm below seating plane.

d) The signal output is an emitter follower, which does not reject noise in the power supply. The power supply must be filtered as in Figure 1.

e) Typical data are at 25° C and VCC = +5 Vdc.

510 Ω with load capacitance less than 5 pF.4.Pin1shouldbeaccoupledtoaload

5. Measured with a 3 pole Bessel filter with a 75 MHz, -3dB bandwidth.
6. The maximum Peak Input Optical Power is the level at which the Pulse Width Distortion is guaranteed to be less than the PWD listed under Test Condition. $P_{R,Max}$ is given for PWD = 5 ns for designing links at ≤ 50 MBd operation, and also for PWD = 2 ns for designing links up to 125 MBd (for both POF and HCS input conditions).
7. 10 ns pulse width, 50% duty cycle, at the 50% amplitude point of the waveform.
8. Percent overshoot is defined at:

$$\frac{(V_{PK} - V_{100\%})}{V} \times 100\%$$

9. Pins 5 and 8 are primarily for mounting and retaining purposes, but are electrically connected. It is recommended that these pins be connected to ground to reduce coupling of electrical noise.
10. If there is no input optical power to the receiver (no transmitted signal) electrical noise can result in false triggering of the receiver. In typical applications, data encoding and error detection prevent random triggering from being interpreted as valid data. Refer to Application Note 1066 for design guidelines.

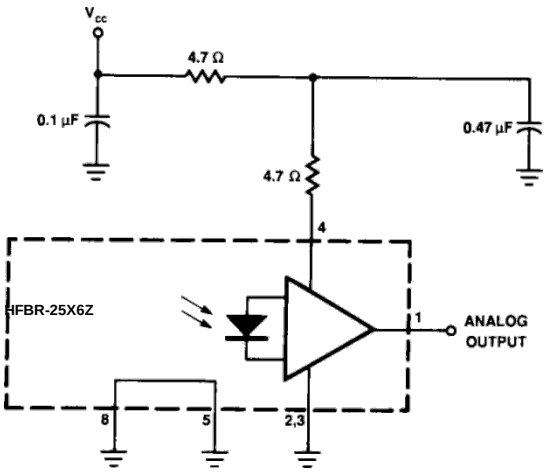


Figure 1. Recommended power supply filter circuit.

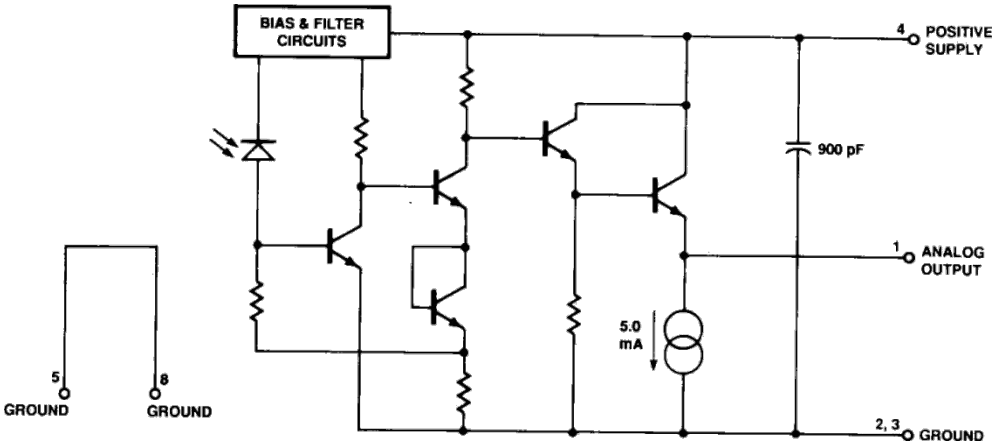


Figure 2. Simplified receiver schematic.

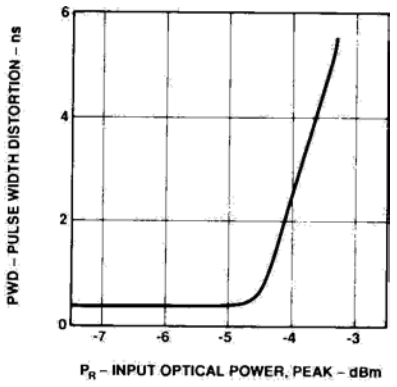


Figure 3. Typical pulse width distortion vs. peak input power.

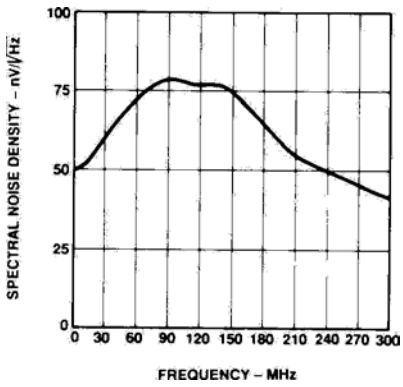


Figure 4. Typical output spectral noise density vs. frequency.

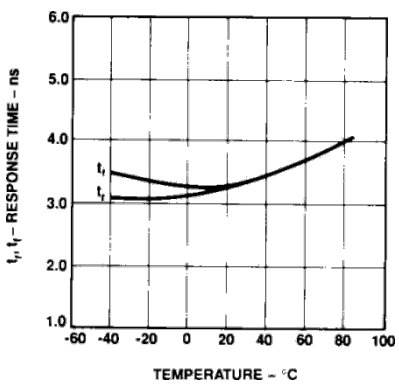
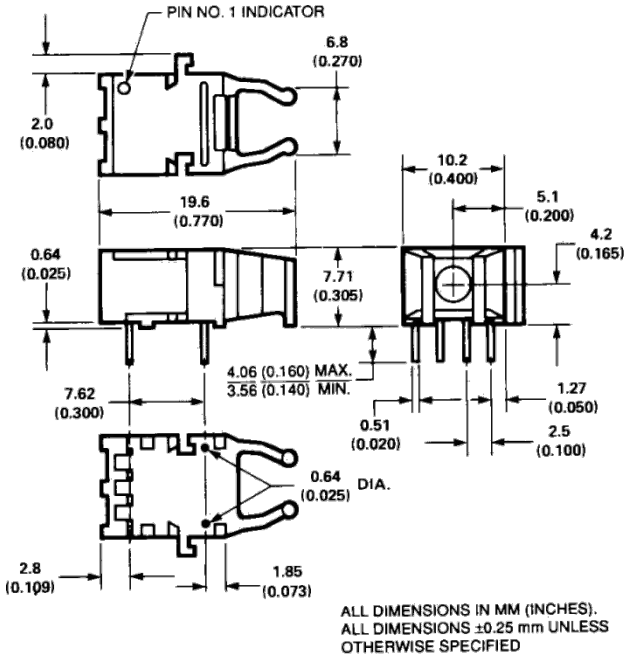


Figure 5. Typical rise and fall time vs. temperature.

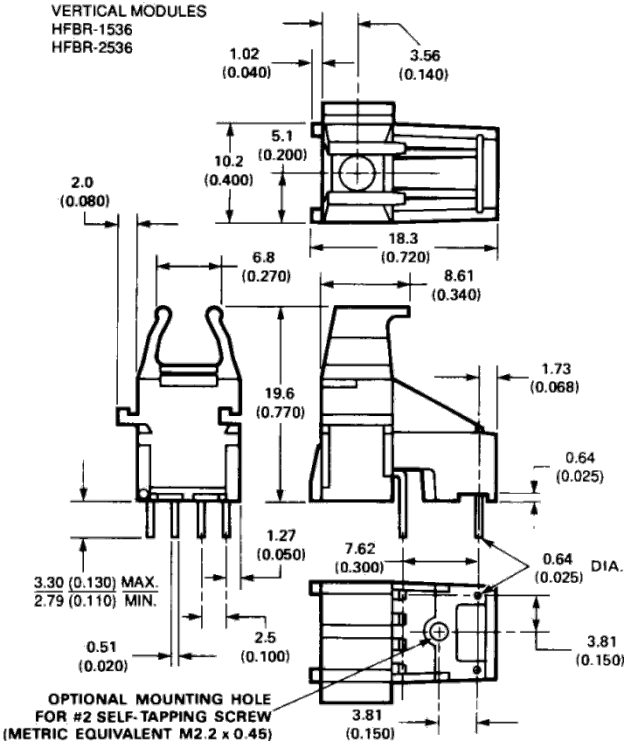
Versatile Link Mechanical Dimensions

HORIZONTAL MODULES
HORIZONTAL MODULES
HFBR-1526Z
HFBR-2526Z
HFBR-1526
HFBR-2526

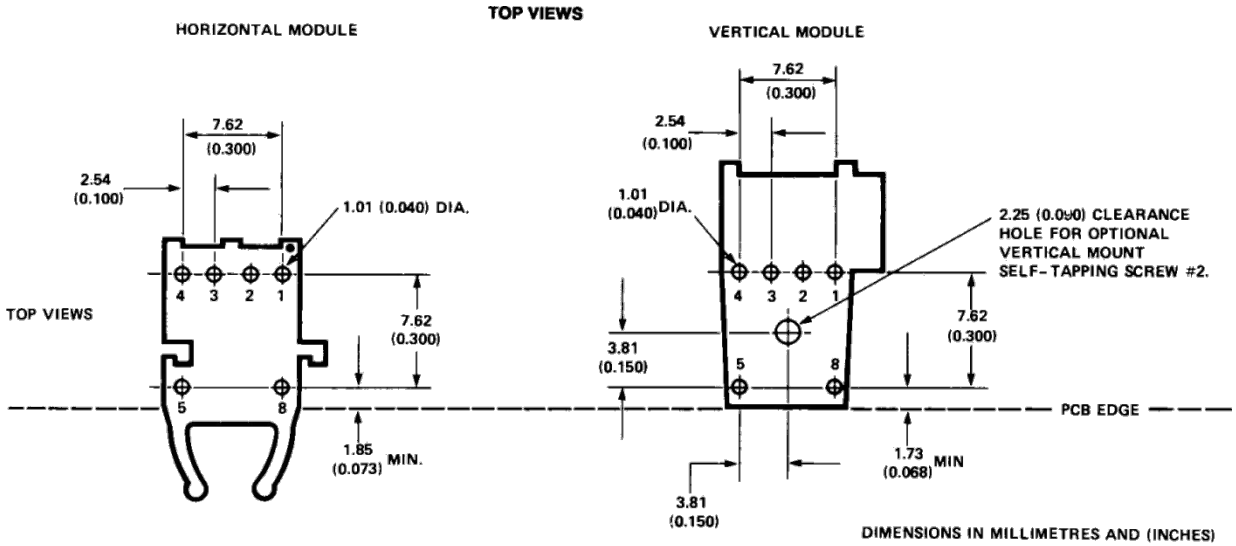
VERTICAL MODULES
HORIZONTAL MODULES
HFBR-1537Z
HFBR-2536Z
HFBR-2526Z



VERTICAL MODULES
HFBR-1536
HFBR-2536



Versatile Link Printed Circuit Board Layout Dimensions



ELECTRICAL PIN FUNCTIONS

PIN NO.	TRANSMITTERS HFBR-15x7Z	RECEIVERS HFBR-25x6Z
1	ANODE	SIGNAL
2	CATHODE	GROUND
3	GROUND*	GROUND
4	GROUND*	Vcc (+5 V)
5	GROUND**	GROUND**
8	GROUND**	GROUND**

*NO INTERNAL CONNECTION.
**PINS 5 AND 8 CONNECTED INTERNALLY TO EACH OTHER ONLY.

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

5989-4631EN September 11, 2006

9.3 POF data sheet

HFBR-RXXYYYZ Series (POF)
HFBR-EXXYYYZ Series (POF)

Plastic Optical Fiber Cable and Accessories for Versatile Link

Data Sheet

Cable Description

The HFBR-R/EXXYYYZ series of plastic fiber optic cables are constructed of a single step-index fiber sheathed in a black polyethylene jacket. The duplex fiber consists of two simplex fibers joined with a zipcord web.

Standard attenuation and extra low loss POF cables are identical except for attenuation specifications. Polyethylene jackets on all plastic fiber cables comply with UL VW-1 flame retardant specification (UL file # E89328).

Cables are available in unconnectored or connectored options. Refer to the Ordering Guide for part number information.

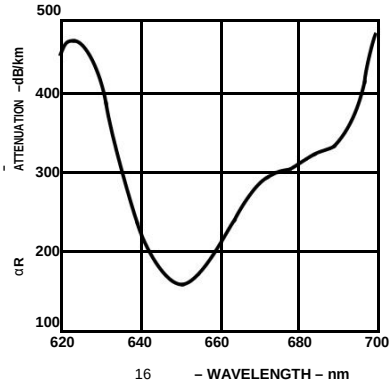


Figure 1. Typical POF attenuation vs. wavelength.

Features

9) Compatible with Avago Versatile Link family of connectors and fiber optic components

10) 1 mm diameter Plastic Optical Fiber (POF) in two grades: low cost standard POF with 0.22 dB/m typical attenuation, or high performance extra low loss POF with 0.19 dB/m typical attenuation

Applications

- **Industrial data links for factory automation and plant control**
- **Intra-system links; board-to-board, rack-to-rack**
- **Telecommunications switching systems**
- **Computer-to-peripheral data links, PC bus extension**
- **Proprietary LANs**
- **Digitized video**
- **Medical instruments**
- **Reduction of lightning and voltage transient susceptibility**
- **High voltage isolation**

Plastic Optical Fiber Specifications: HFBR-R/EXXYYYZ

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Note
Storage and Operating Temperature		$T_{S,O}$	-55	+85	°C	
Recommended Operating Temperature		T_O	-40	+85	°C	
Installation Temperature		T_I	-20	+70	°C	1
Short Term Tensile Force	Single Channel	F_T		50	N	2
	Dual Channel	F_T		100	N	
Short Term Bend Radius		r	25		mm	3, 4
Long Term Bend Radius		r	35		mm	
Long Term Tensile Load		F_T		1	N	
Flexing				1000	Cycles	4

Mechanical/Optical Characteristics, T_A = -40 to +85°C unless otherwise specified.

Parameter		Symbol	Min.	Typ.[5]	Max.	Unit	Condition
Cable Attenuation	Standard Cable, Type "R"	α_O	0.15	0.22	0.27	dB/m	Source is HFBR-15XXZ (660 mm LED, 0.5 NA)
	Extra Low Loss, Type "E"		0.15	0.19	0.23		=50 meters
Reference Attenuation	Standard Cable, Type "R"	α_R	0.12	0.19	0.24	dB/m	Source is 650 nm, 0.5 NA monochrometer,
	Extra Low Loss, Type "E"		0.12	0.16	0.19		=50 meters Note 7, Figure 1
Numerical Aperture		NA	0.46	0.47	0.50		>2 meters
Diameter, Core and Cladding		D_C	0.94	1.00	1.06	mm	
Diameter, Jacket		D_J	2.13	2.20	2.27	mm	Simplex Cable
Propagation Delay Constant		l/v		5.0		ns/m	Note 6
Mass per Unit Length/Channel				5.3		g/m	Without Connectors
Cable Leakage Current		I_L		12		nA	50 kV, = 0.3 meters
Refractive Index	Core	n		1.492			
	Cladding			1.417			

Notes:

- Installation temperature is the range over which the cable can be bent and pulled without damage. Below -20°C the cable becomes brittle and should not be subjected to mechanical stress.
- Short Term Tensile Force is for less than 30 minutes.
- Short Term Bend Radius is for less than 1 hour nonoperating.
- 90° bend on 25 mm radius mandrel. Bend radius is the radius of the mandrel around which the cable is bent.
- Typical data are at 25°C.
- Propagation delay constant is the reciprocal of the group velocity for propagation delay of optical power. Group velocity is v=c/n where c is the velocity of light in free space ($3xl0^8$ m/s) and n is the effective core index of refraction.
- Note that α_R rises at the rate of about 0.0067 dB/°C, where the thermal rise refers to the LED temperature changes above 25°C. Please refer to Figure 1 which shows the typical plastic optical fiber attenuation versus wavelength at 25°C.

Plastic Fiber Connector Styles

Connector Description

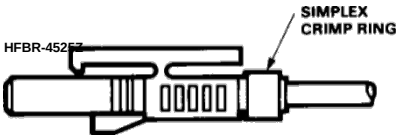
Four connector styles are available for termination of plastic optical fiber: simplex, simplex latching, duplex and duplex latching. All connectors provide a snap-in action when mated to Versatile Link components. Simplex connectors are color coded to facilitate identification of trans-mitter and receiver connections. Duplex connectors are keyed so that proper orientation is ensured during insertion. If the POF cable/ connector will be used at extreme operating temperatures or experience frequent and wide temperature cycling effects, the cable/connector attachment can be strengthened with an RTV adhesive (see Plastic Connector-ing Instructions for more detail). The connectors are made of a flame retardant VALOX UL94 V-0 material (UL file # E121562).

SIMPLEX CONNECTOR STYLES

HFBR-4501Z/4511Z – Simplex

The simplex connector provides a quick and stable connection for applications that require a component-to-connector retention force of 8 Newtons (1.8 lb.). These connectors are available in gray (HFBR-4501Z) or blue (HFBR-4511Z).

HFBR-4503Z/4513Z – Simplex Latching

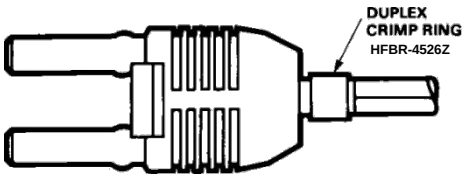


The simplex latching connector is designed for rugged applications requiring a greater retention force — 80 Newtons (18 lb.) — than provided by a simplex nonlatching connector. When inserting the simplex latching connector into a module, the connector latch mechanism should be aligned with the top surface of the horizontal modules, or with the tall vertical side of the vertical modules. Misalignment of an inserted latching connector into either module will not result in a positive latch. The connector is released by depressing the rear section of the connector lever, and then pulling the connector assembly away from the module housing.

The simplex latching connector is available in gray (HFBR-4503Z) or blue (HFBR-4513Z).

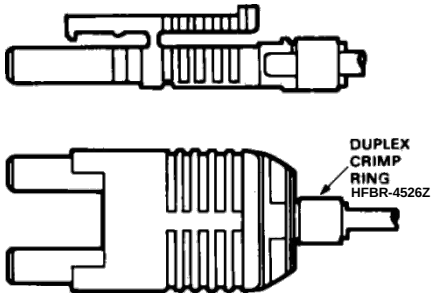
DUPLEX CONNECTOR STYLES

HFBR-4506Z – Duplex



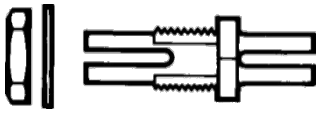
Duplex connectors provide con-venient duplex cable termination and are keyed to prevent incorrect insertion into duplex configured modules. The duplex connector is compatible with dual combina-tions of horizontal or vertical Versatile Link components (e.g., two horizontal transmitters, two vertical receivers, a horizontal transmitter with a horizontal receiver, etc.). The duplex non-latching connector is available in parchment, off-white (HFBR-4506Z).

HFBR-4516Z – Duplex Latching



The duplex latching connector is designed for rugged applications requiring greater retention force than the nonlatching duplex con-nector. When inserting the duplex latching connector into a module, the connector latch mechanism should be aligned with the top surface of the dual combination of horizontal or vertical Versatile Link components. The duplex latching connector is available in gray (HFBR-4516Z).

Feedthrough/Splice HFBR-4505Z/4515Z Bulkhead Adapter



The HFBR-4505Z/4515Z adapter mates two simplex connectors for panel/bulkhead feedthrough of HFBR-4501Z/4511Z terminated plastic fiber cable. Maximum panel thickness is 4.1 mm (0.16 inch). This adapter can serve as a cable in-line splice using two simplex connectors. The adapters are available in gray (HFBR-4505Z) and blue (HFBR-4515Z). This adapter is not compatible with POF duplex, POF simplex latching, or HCS connectors.

Plastic Optical Fiber Connector Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage and Operating Temperature	$T_{S,O}$	-40	85	°C	1
Recommended Operating Temperature	T_O	-40	85	°C	1
Installation Temperature	T_I	0	70	°C	1
Nut Torque	T_N		0.7	N-m	2
HFBR-4505Z/4515Z Adapter			100	OzF-in.	

Notes:

2. Storage and Operating Temperatures refer to the ranges over which the connectors can be used when not subjected to mechanical stress. Installation Temperature refers to the ranges over which connectors may be installed onto the fiber and over which connectors can be connected and disconnected from transmitter and receiver modules.
3. Recommended nut torque is 0.57 N-m.

Plastic Optical Fiber Connector Mechanical/Optical

Characteristics T_A = -40 to +85°C, Unless Otherwise Specified.

Parameter	Part Number	Symbol	Min.	Typ.[1]	Max.	Units	Temp. °C	Note
Retention Force, Connector to	Simplex, HFBR-4501Z/4511Z	F_{R-C}	7 3	8		N	+25 -40 to +85	2
Versatile Link Transmitters and Receivers	Simplex Latching, HFBR-4503Z/4513Z		47 11	80			+25 -40 to +85	
	Duplex, HFBR-4506Z		7 4	12			+25 -40 to +85	
	Duplex Latching, HFBR-4516Z		50 15	80			+25 -40 to +85	
Tensile Force, Connector to Cable	Simplex, HFBR-4501Z/4511Z	F_T	8.5	22		N		3
	Simplex Latching, HFBR-4503Z/4513Z		8.5	22				
	Duplex, HFBR-4506Z		14	35				
	Duplex Latching, HFBR-4516Z		14	35				
Adapter Connector to Connector Loss	HFBR-4505Z/4515Z with HFBR-4501Z/4511Z	α_{CC}	0.7	1.5	2.8	dB	25	4, 5
Retention Force Connector to Adapter	HFBR-4505Z/4515Z with HFBR-4501Z/4511Z	F_{R-B}	7	8		N		
Insertion Force, Connector to Versatile	Simplex, HFBR-4501Z/4511Z	F_I		8	30	N		6
Link Transmitters and Receivers	Simplex Latching, HFBR-4503Z/4513Z			16	35			
	Duplex, HFBR-4506Z			13	46			
	Duplex Latching HFBR-4516Z			22	51			

Notes:

- Typical data are at +25°C.
- No perceivable reduction in retention force was observed after 2000 insertions. Retention force of non-latching connectors is lower at elevated temperatures. Latching connectors are recommended for applications where a high retention force at high temperatures is desired.
- For applications where frequent temperature cycling over temperature extremes is expected, please contact Avago Technologies for alternate connectoring techniques.
- Minimum and maximum limit for αCC for 0°C to +70°C temperature range. Typical value of αCC is at +25°C.
- Factory polish or field polish per recommended procedure.
- Destructive insertion force was typically at 178 N (40 lb.).

Step-by-Step Plastic Cable Connectoring Instructions

The following step-by-step guide describes how to terminate plastic fiber optic cable. It is ideal for both field and factory installation. Connectors can be easily installed on cable ends with wire strippers, cutters and a crimping tool.

Finishing the cable is accomplished with the Avago HFBR-4593Z Polishing Kit, consisting of a Polishing Fixture, 600 grit abrasive paper and 3 ∝m pink lapping film (3M Company, OC3-14). The connector can be used immediately after polishing.

Materials needed for plastic fiber termination are:

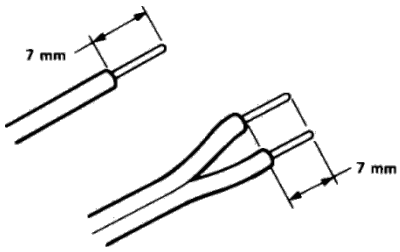
9. Avago Plastic Optical Fiber Cable (Example: HFBR-RUS500Z, HFBR-RUD500Z, HFBR-EUS500Z, or HFBR-EUD500Z)
10. Industrial Razor Blade or Wire Cutters
11. 16 Gauge Latching Wire Strippers (Example: Ideal Stripmaster^{TM} type 45-092).
12. HFBR-4597Z Crimping Tool
13. HFBR-4593Z Polishing Kit
14. One of the following connectors:
    a) HFBR-4501Z/4503Z Gray Simplex/Simplex Latching Connector and HFBR-4525Z Simplex Crimp Ring
    b) HFBR-4511Z/4513Z Blue Simplex/Simplex Latching Connector and HFBR-4525Z Simplex Crimp Ring
    f) HFBR-4506Z Parchment (off-white) Duplex Connector and HFBR-4526Z Duplex Crimp Ring
    g) HFBR-4516Z Gray Latching Duplex Connector and HFBR-4526Z Duplex Crimp Ring

Step 1

The zip cord structure of the duplex cable permits easy separation of the channels. The channels should be separated a minimum of 100 mm (4 in) to a maximum of 150 mm (6 in) back from the ends to permit connectoring and polishing.

After cutting the cable to the desired length, strip off approximately 7 mm (0.3 in.) of the outer jacket with the 16 gauge wire strippers. Excess webbing on the duplex cable may have to be trimmed to allow the simplex or simplex latching connector to slide over the cable.

When using the duplex connector and duplex cable, the separated duplex cable must be stripped to equal lengths on each cable. This allows easy and proper seating of the cable into the duplex connector.



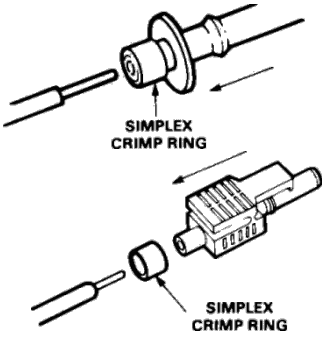
Step 2

Place the crimp ring and connector over the end of the cable; the fiber should protrude about 3 mm (0.12 in.) through the end of the connector. Carefully position the ring so that it is entirely on the connector with the rim of the crimp ring flush with the connector, leaving a small space between the crimp ring and the flange. Then crimp the ring in place with the crimping tool. One crimp tool is used for all POF connector crimping requirements.

For applications with extreme temperature operation or frequent temperature cycling, improved connector to cable attachment can be achieved with the use of an RTV (GE Company, RTV-128 or Dow Corning 3145-RTV) adhesive. The RTV is placed into the connector prior to insertion of the fiber and the fiber is crimped normally. The connector can be polished after the RTV has cured and is then ready for use.

Note: *By convention, place the gray connector on the transmitter cable end and the blue connector on the receiver cable end to maintain color coding (different color connectors are mechanically identical).*

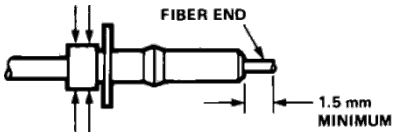
Simplex connector crimp rings cannot be used with duplex connectors and duplex connector crimp rings cannot be used with simplex connectors because of size differences. The simplex crimp has a dull luster appearance; the duplex ring is glossy and has a thinner wall.



Step 3

Any excess fiber protruding from the connector end may be cut off; however, the trimmed fiber should extend at least 1.5 mm (0.06 in) from the connector end.

Insert the connector fully into the polishing fixture with the trimmed fiber protruding from the bottom of the fixture. This plastic polish-ing fixture can be used to polish two simplex connectors or simplex latching connectors simultane-ously, or one duplex connector.



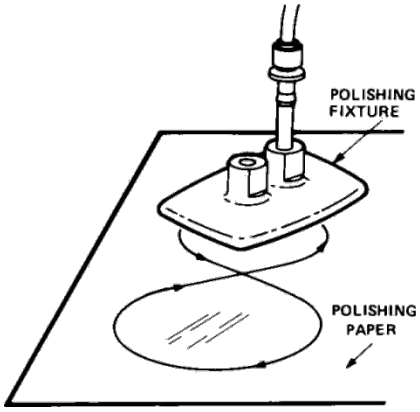
Note: The four dots on the bottom of the polishing fixture are wear indicators. Replace the polishing fixture when any dot is no longer visible. Typically, the polishing fixture can be used 10 times; 10 duplex connectors or 20 simplex connectors, two at a time.

Place the 600 grit abrasive paper on a flat smooth surface, pressing down on the connector, polish the fiber and the connector using a figure eight pattern of strokes until the connector is flush with the bottom of the polishing fixture. Wipe the connector and fixture with a clean cloth or tissue.

Step 4

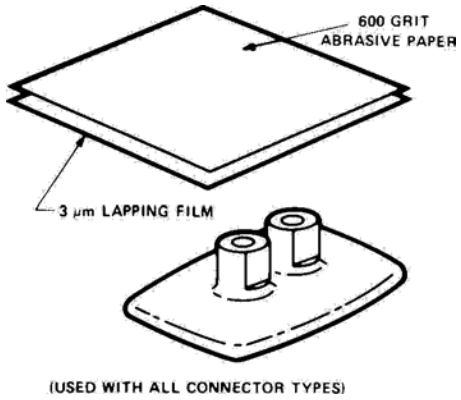
Place the flush connector and polishing fixture on the dull side of the 3 ∝m pink lapping film and continue to polish the fiber and connector for approximately 25 strokes. The fiber end should be flat, smooth and clean.

This cable is now ready for use.



Note: Use of the pink lapping film fine polishing step results in approximately 2 dB improvement in coupling performance of either a transmitter-receiver link or a bulkhead/splice over a 600 grit polish alone. This fine polish is comparable to the Avago factory polish. The fine polishing step may be omitted where an extra 2 dB of optical power is not essential, as with short link lengths. Proper polishing of the tip of the fiber/ connector face results in a tip diameter between 2.5 mm (0.098 in.) minimum and 3.2 mm (0.126 in.) maximum..

HFBR-4593Z Polishing Kit



Ordering Guide for POF Connectors and Accessories

Plastic Optical Fiber Connectors

HFBR-4501Z Gray Simplex Connector/Crimp Ring HFBR-4511Z Blue Simplex Connector/Crimp Ring HFBR-4503Z Gray Simplex Latching Connector with Crimp Ring HFBR-4513Z Blue Simplex Latching Connector with Crimp Ring HFBR-4506Z Parchment Duplex Connector with Crimp Ring HFBR-4516Z Gray Duplex Latching Connector with Crimp Ring HFBR-4505Z Gray Adapter (Bulkhead/Feedthrough) HFBR-4515Z Blue Adapter (Bulkhead/Feedthrough)

Plastic Optical Fiber Accessories

HFBR-4522Z 500 HFBR-0500Z Products Port Plugs
HFBR-4525Z 1000 Simplex Crimp Rings
HFBR-4526Z 500 Duplex Crimp Rings
HFBR-4593Z Polishing Kit (one polishing tool, two pieces 600 grit abrasive paper, and two pieces 3 ∝m pink lapping film)
HFBR-4597Z Plastic Fiber Crimping Tool

Ordering Guide for POF Cable For Example:

HFBR-RUD500Z is a Standard Attenuation, Unconnectored, Duplex, 500 meter cable.

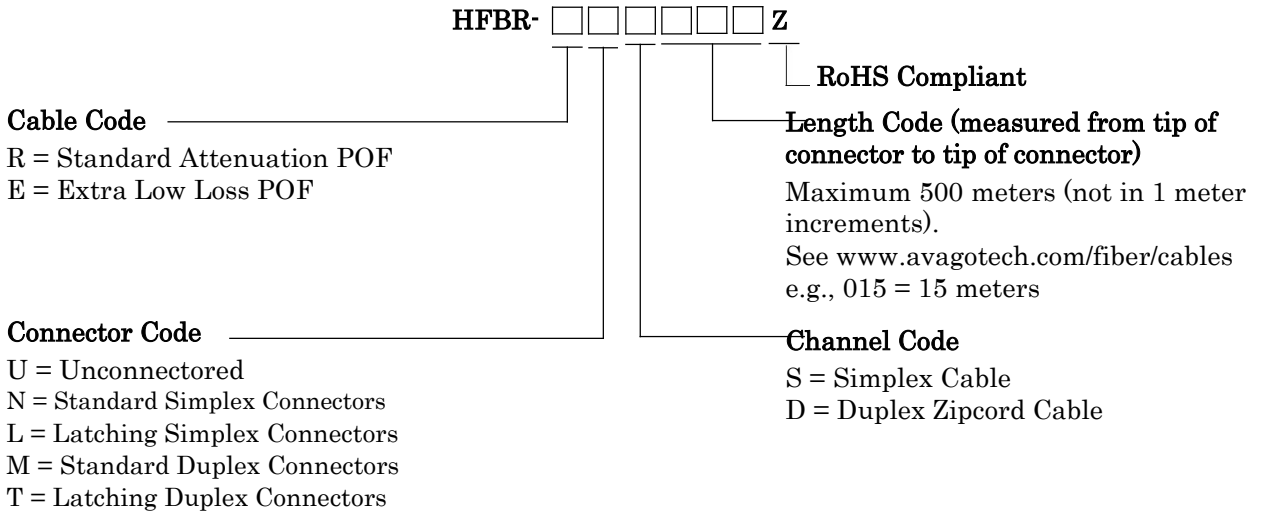
HFBR-RLS001Z is a Standard Attenuation, Latching Simplex Connectored, Simplex, 1 meter cable.

HFBR-RMD010Z is a Standard Attenuation, Standard Duplex Connectored, Duplex, 10 meter cable.

HFBR-RMD100Z is a Standard Attenuation, Standard Duplex Connectored, Duplex, 100 meter cable.

Cable Length Tolerances:
The plastic cable length tolerances are: +10%/-0%.

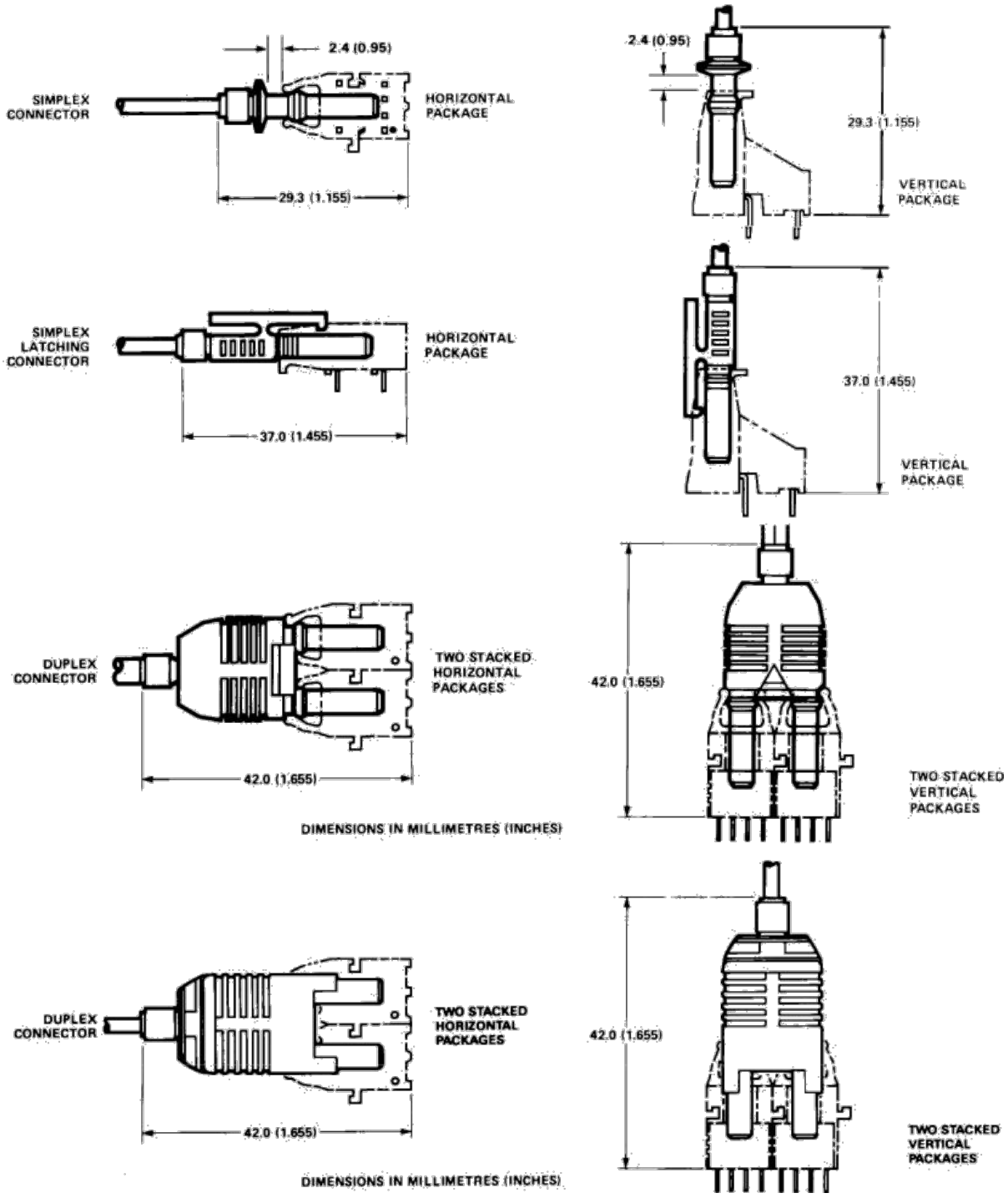
NOTE: By convention, pre-connectored simplex POF cables have gray and blue colored connectors on the opposite ends of the same fiber; although oppositely colored, the connectors are mechanically identical. Duplex POF cables with duplex connectors use color-coded markings on the duplex fiber cable to differentiate between the channel.



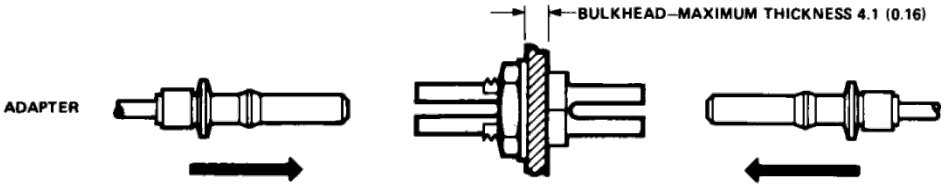
Note: Not all possible combinations reflect available part numbers. Please contact your local Avago representative for a list of current available cable part numbers.

Connector Applications

Attachment to Avago Versatile Link Fiber Optic Components



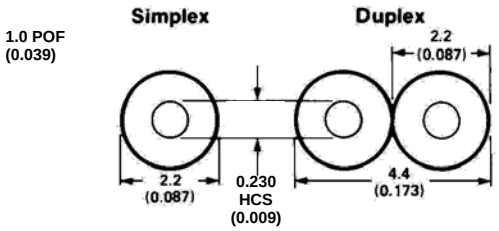
Bulkhead Feedthrough or Panel Mounting for HFBR-4501Z/4511Z Simplex Connectors



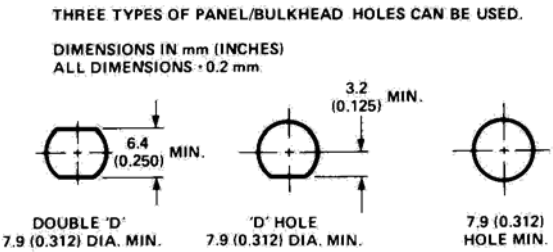
Versatile Link Mechanical Dimensions

All dimensions in mm (inches).
All dimensions ± 0.25 mm unless otherwise specified.

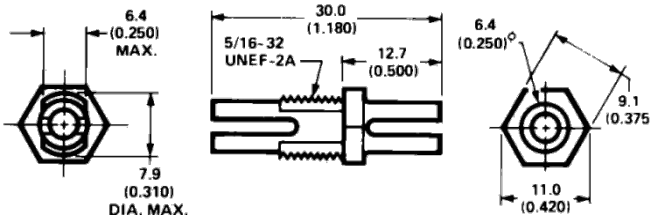
Fiber Optic Cable Dimensions



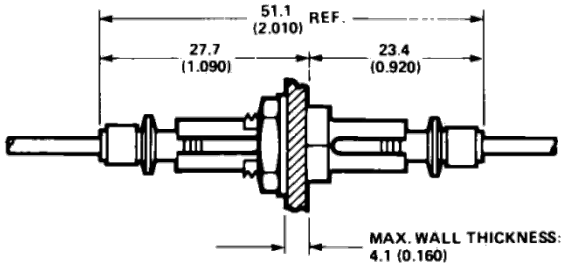
Panel Mounting – Bulkhead Feedthrough



HFBR-4505Z (Gray)/4515Z (Blue) Adapters

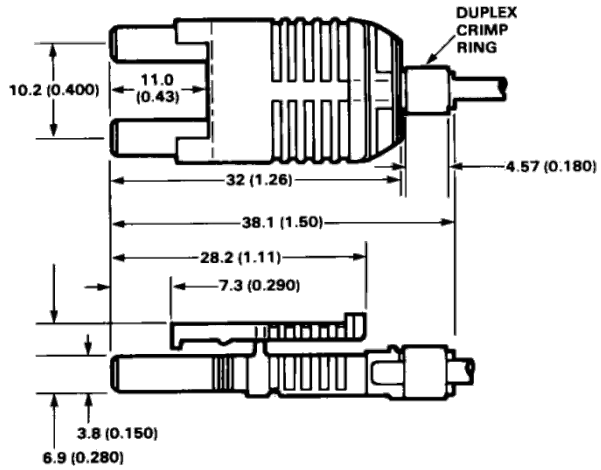


Bulkhead Feedthrough with Two HFBR-4501Z/4511Z Connectors

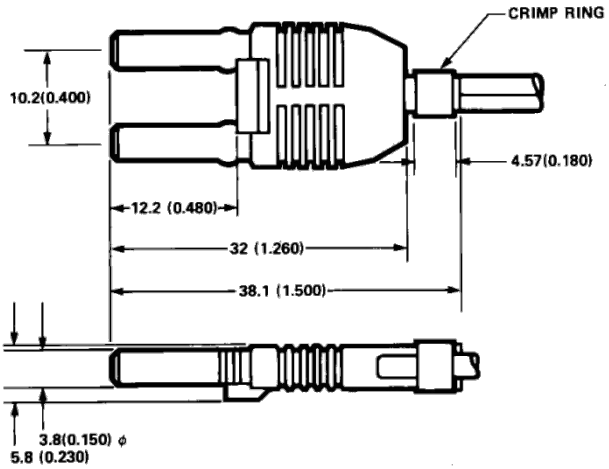


Versatile Link Mechanical Dimensions, continued

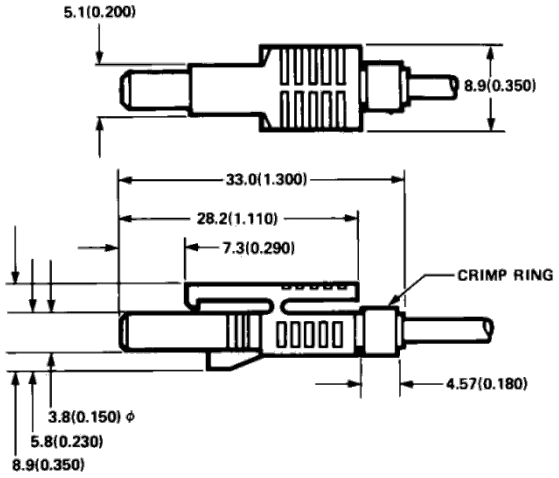
HFBR-4516Z (Parchment) Duplex Latching Connector



HFBR-4506Z (Parchment) Duplex Connector



HFBR-4503Z (Gray)/4513Z (Blue) Simplex Latching Connector



HFBR-4501Z (Gray)/4511Z (Blue) Simplex Connector

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

AV01-0150EN May 14, 2006

9.4 Comparator data sheet

MAX941/MAX942/ MAX944

High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

General Description

The MAX941/MAX942/MAX944 are single/dual/quad high-speed comparators optimized for systems powered from a 3V or 5V supply. These devices combine high speed, low power, and rail-to-rail inputs. Propagation delay is 80ns, while supply current is only 350µA per comparator.

The input common-mode range of the MAX941/MAX942/ MAX944 extends beyond both power-supply rails. The outputs pull to within 0.4V of either supply rail without external pullup circuitry, making these devices ideal for interface with both CMOS and TTL logic. All input and output pins can tolerate a continuous short-circuit fault condition to either rail. Internal hysteresis ensures clean output switching, even with slow-moving input signals. The MAX941 features latch enable and device shutdown.

The single MAX941 and dual MAX942 are offered in a tiny µMAX® package. Both the single and dual MAX942 are available in 8-pin DIP and SO packages. The quad MAX944 comes in 14-pin DIP and narrow SO packages.

Applications

●● 3V/5V Systems
●● Battery-Powered Systems
●● Threshold Detectors/Discriminators
●● Line Receivers
●● Zero-Crossing Detectors
●● Sampling Circuits

Features

●● Available in µMAX Package
●● Optimized for 3V and 5V Applications (Operation Down to 2.7V)
●● Fast, 80ns Propagation Delay (5mV Overdrive)
●● Rail-to-Rail Input Voltage Range
●● Low 350µA Supply Current per Comparator
●● Low, 1mV Offset Voltage
●● Internal Hysteresis for Clean Switching
●● Outputs Swing 200mV of Power Rails
●● CMOS/TTL-Compatible Outputs ●● Output Latch (MAX941 Only)
●● Shutdown Function (MAX941 Only)

Ordering Information

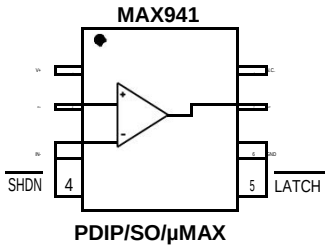
PART	TEMP RANGE	PIN-PACKAGE
MAX941CPA	0°C to +70°C	8 PDIP
MAX941CSA	0°C to +70°C	8 SO
MAX941EPA	-40°C to +85°C	8 PDIP
MAX941ESA	-40°C to +85°C	8 SO
MAX941EUA-T	-40°C to +85°C	8 µMAX
MAX941AUA-T	-40°C to +125°C	8 µMAX

T = Tape and reel.

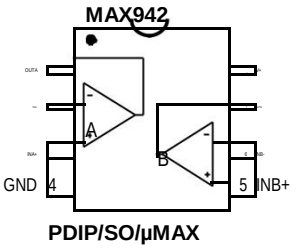
Ordering Information continued at end of data sheet.

Pin Configurations

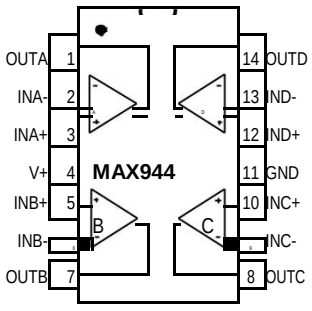
TOP VIEW



PDIP/SO/µMAX



PDIP/SO/µMAX



PDIP/SO

Absolute Maximum Ratings

Power-Supply Ranges
Supply Voltage V+ to GND..... +6.5V
Differential Input Voltage..... -0.3V to (V+ + 0.3V)
Common-Mode Input Voltage..... -0.3V to (V+ + 0.3V)
LATCH Input (MAX941 only)..... -0.3V to (V+ + 0.3V)
SHDN Control Input (MAX941 only) ..... -0.3V to (V+ + 0.3V)
Current Into Input Pins..... ±20mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C)... 727mW
8-Pin SO (derate 5.88mW/°C above +70°C)..... 471mW
8-Pin µMAX (derate 4.1mW/°C above +70°C)..... 330mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)... 800mW
14-Pin SO (derate 8.33mW/°C above +70°C)..... 667mW
Operating Temperature Ranges
MAX94_C_ _..... 0°C to +70°C
MAX94_E_ _..... -40°C to +85°C
MAX94_AUA..... -40°C to +125°C
MAX942MSA..... -55°C to +125°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s)..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V+ = 2.7V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 14)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Positive Supply Voltage	V+				2.7		5.5	V
Input Voltage Range	V_{CMR}	(Note 1)			-0.2		V+ + 0.2	V
Input-Referred Trip Points	V_{TRIP}	V_{CM} = 0V or V_{CM} = V+ (Note 2)	T_A = +25°C	MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA		1	3	mV
				MAX941_UA/MAX942_UA		1	4	
			$T_A = T_{MIN}$ to T_{MAX}	MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA			4	mV
				MAX941_UA/MAX942_UA			6	
Input Offset Voltage	V_{OS}	V_{CM} = 0V or V_{CM} = V+ (Note 3)	T_A = +25°C	MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA		1	2	mV
				MAX941_UA/MAX942_UA		1	3	
			$T_A = T_{MIN}$ to T_{MAX}	MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA			3	mV
				MAX941_UA/MAX942_UA			5.5	
Input Bias Current	I_B	V_{IN} = V_{OS}, V_{CM} = 0V or V_{CM} = V+ (Note 4)		MAX94_C		150	300	nA
				MAX94_E/A, MAX942MSA		150	400	
Input Offset Current	I_{OS}	V_{IN} = V_{OS}, V_{CM} = 0V or V+				10	150	nA
Input Differential Clamp Voltage	V_{CLAMP}	Force 100µA into IN+, IN- = GND, measure V_{IN+} - V_{IN-}, Figure 3				2.2		V
Common-Mode Rejection Ratio	CMRR	(Note 5)		MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA		80	300	µV/V
				MAX941_UA/MAX942_UA		80	800	
Power-Supply Rejection Ratio	PSRR	2.7V ≤ V+ ≤ 5.5V, V_{CM} = 0V		MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA		80	300	µV/V
				MAX941_UA/MAX942_UA		80	350	
Output High Voltage	V_{OH}	I_{SOURCE} = 400µA			V+ - 0.4	V+ - 0.2		V
		I_{SOURCE} = 4mA			V+ - 0.4	V+ - 0.3		
Output Low Voltage	V_{OL}	I_{SINK} = 400µA				0.2	0.4	V
		I_{SINK} = 4mA				0.3	0.4	
Output Leakage Current	I_{LEAK}	(Note 6)					1	µA

Electrical Characteristics (continued)

(V+ = 2.7V to 5.5V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 14)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current per Comparator	I_{CC}	V+ = 3V	MAX941		380	600	µA
			MAX942/MAX944		350	500	
		V+ = 5V	MAX941		430	700	
			MAX942/MAX944		400	600	
		MAX941 only, shutdown mode (V+ = 3V)			12	60	
Power Dissipation per Comparator	PD	(Note 7)	MAX941		1.0	4.2	mW
			MAX942/MAX944		1.0	3.6	
Propagation Delay	t_{PD+}, t_{PD-}	(Note 8)	MAX94_C		80	150	ns
			MAX94_E/A, MAX942MSA		80	200	
Differential Propagation Delay	dtPD	(Note 9)			10		ns
Propagation Delay Skew		(Note 10)			10		ns
Logic-Input Voltage High	V_{IH}	(Note 11)		V+/2 + 0.4			V
Logic-Input Voltage Low	V_{IL}	(Note 11)				V+/2 - 0.4	V
Logic-Input Current	I_{IL}, I_{IH}	VLOGIC = 0V or V+ (Note 11)			2	10	µA
Data-to-Latch Setup Time	tS	(Note 12)			20		ns
Latch-to-Data Hold Time	tH	(Note 12)			30		ns
Latch Pulse Width	t_{LPW}	MAX941 only			50		ns
Latch Propagation Delay	t_{LPD}	MAX941 only			70		ns
Shutdown Time		(Note 13)			3		ns
Shutdown Disable Time		(Note 13)			10		ns

Note 1: Inferred from the CMRR test. Note also that either or both inputs can be driven to the absolute maximum limit (0.3V beyond either supply rail) without damage or false output inversion.

Note 2: The input-referred trip points are the extremities of the differential input voltage required to make the comparator output change state. The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis zone (see Figure 1).

Note 3: VOS is defined as the center of the input-referred hysteresis zone (see Figure 1).

Note 4: The polarity of IB reverses direction as VCM approaches either supply rail. See *Typical Operating Characteristics* for more detail.

Note 5: Specified over the full common-mode range (VCMR).

Note 6: Applies to the MAX941 only when in shutdown mode. Specification is for current flowing into or out of the output pin for VOUT driven to any voltage from V+ to GND.

Note 7: Typical power dissipation specified with V+ = 3V; maximum with V+ = 5.5V.

Note 8: Parameter is guaranteed by design and specified with VOD = 5mV and CLOAD = 15pF in parallel with 400µA of sink or source current. VOS is added to the overdrive voltage for low values of overdrive (see Figure 2).

Note 9: Specified between any two channels in the MAX942/MAX944.

Note 10: Specified as the difference between tPD+ and tPD- for any one comparator.

Note 11: Applies to the MAX941 only for both SHDN and LATCH pins.

Note 12: Applies to the MAX941 only. Comparator is active with LATCH pin driven high and is latched with LATCH pin driven low (see Figure 2).

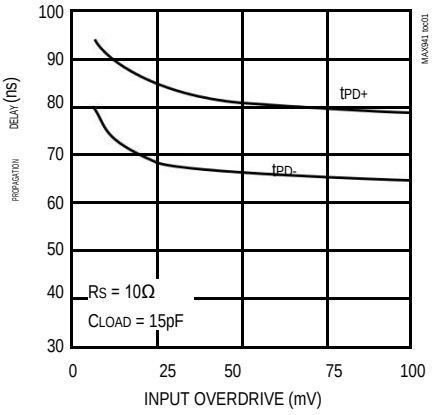
Note 13: Applicable to the MAX941 only. Comparator is active with SHDN pin driven high and is in shutdown with SHDN pin driven low. Shutdown disable time is the delay when SHDN is driven high to the time the output is valid.

Note 14: The MAX941_UA and MAX942_UA are 100% production tested at TA = +25°C. Specifications over temperature are guaranteed by design.

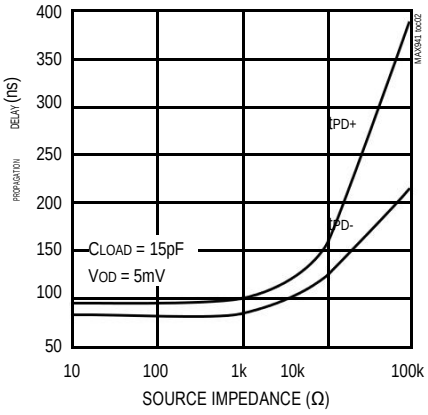
Typical Operating Characteristics

(V+ = 3.0V, TA = +25°C, unless otherwise noted.)

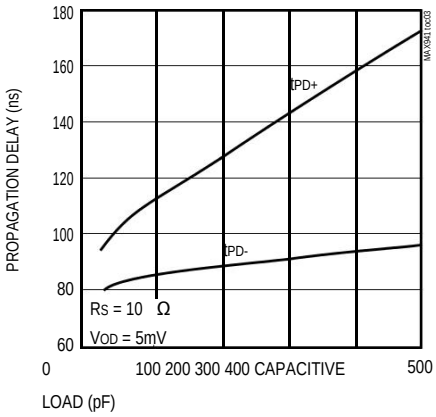
PROPAGATION DELAY vs.
INPUT OVERDRIVE

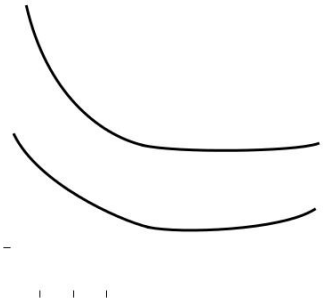


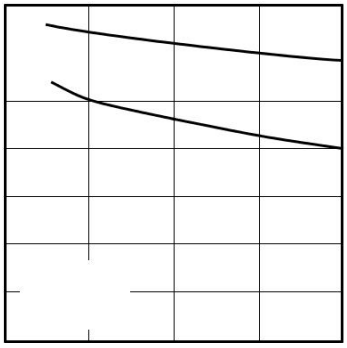
PROPAGATION DELAY vs.
SOURCE IMPEDANCE

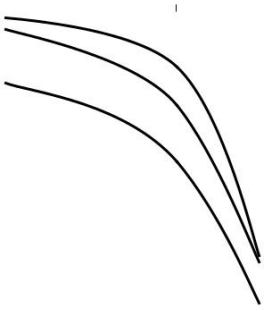


PROPAGATION DELAY vs.
CAPACITIVE LOAD

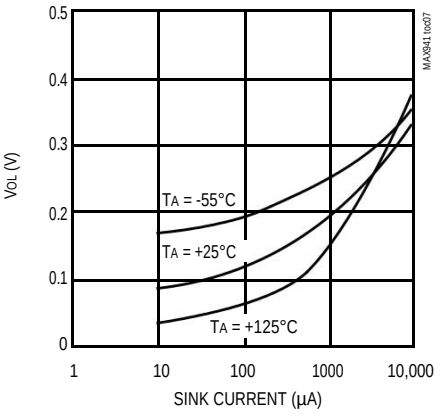




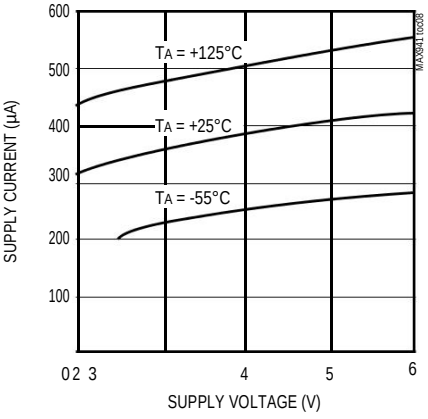




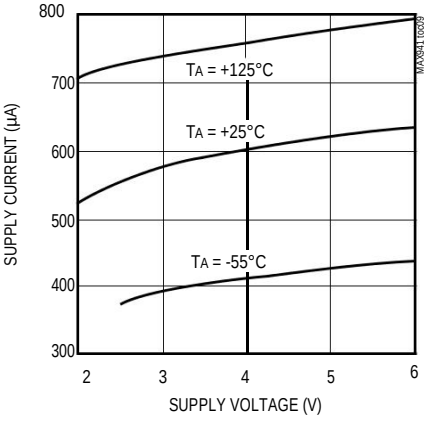
OUTPUT LOW VOLTAGE
vs. SINK CURRENT



MAX941 TOTAL SUPPLY CURRENT
vs. SUPPLY VOLTAGE



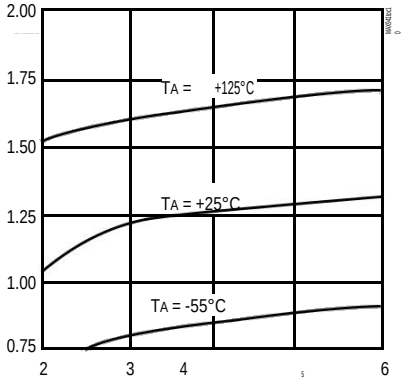
MAX942 TOTAL SUPPLY CURRENT
vs. SUPPLY VOLTAGE



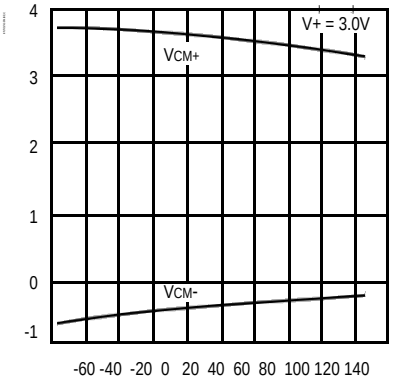
Typical Operating Characteristics (continued)

(V+ = 3.0V, TA = +25°C, unless otherwise noted.)

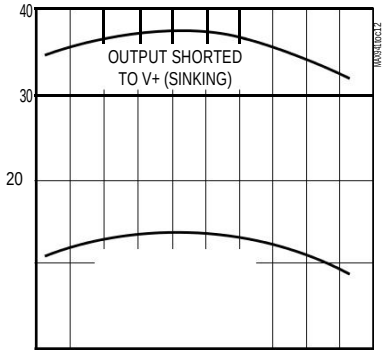
MAX944 TOTAL SUPPLY CURRENT
vs. SUPPLY VOLTAGE



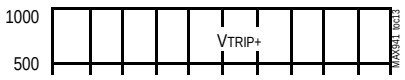
INPUT VOLTAGE RANGE
vs. TEMPERATURE

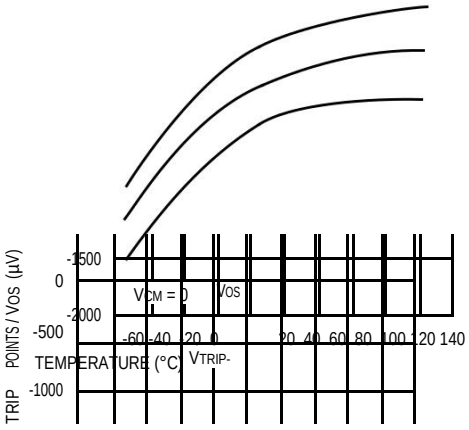


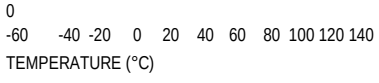
SHORT-CIRCUIT OUTPUT CURRENT
vs. TEMPERATURE



VOLTAGE TRIP POINTS/INPUT OFFSET
VOLTAGE vs. TEMPERATURE



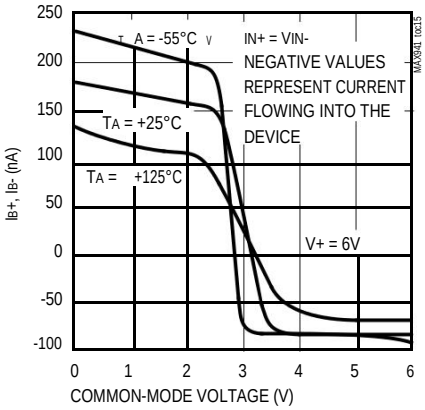




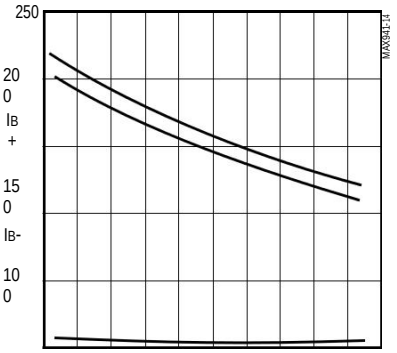
INPUT BIAS / OFFSET CURRENT (nA)

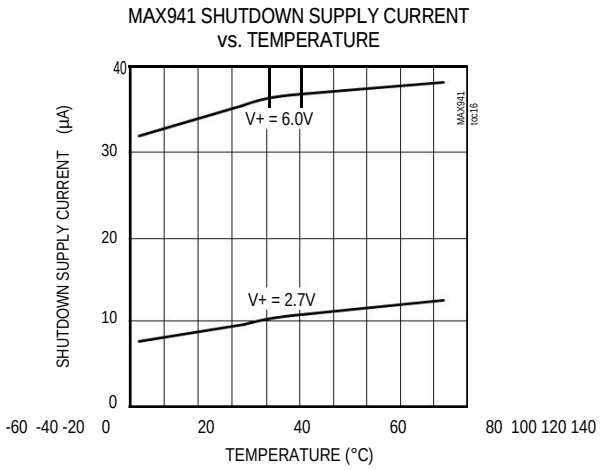
40 60 80 100 120 140 TEMPERATURE (°C)

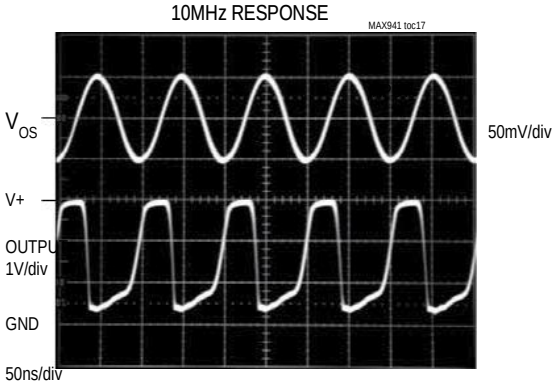
INPUT BIAS CURRENT (IB+, IB-)
vs. COMMON-MODE VOLTAGE



INPUT BIAS CURRENT/INPUT OFFSET CURRENT vs. TEMPERATURE



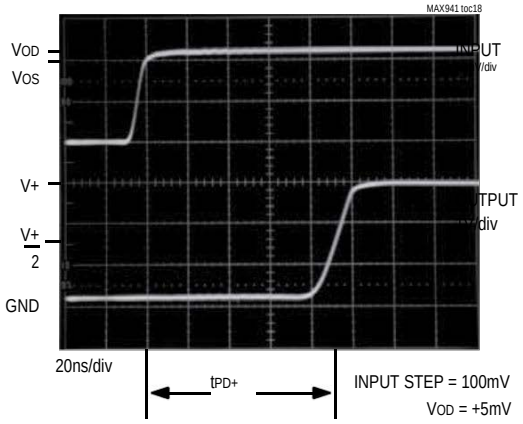

MAX941 SHUTDOWN SUPPLY CURRENT
vs. TEMPERATURE
SHUTDOWN SUPPLY CURRENT (µA)
TEMPERATURE (°C)
V+ = 6.0V
V+ = 2.7V
MAX941 toc16
40
30
20
10
0
-60 -40 -20 0 20 40 60 80 100 120 140


10MHz RESPONSE
MAX941 toc17
VOS
50mV/div
V+
OUTPU
1V/div
GND
50ns/div

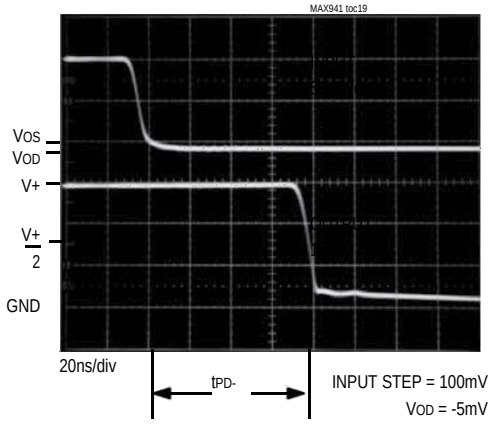
Typical Operating Characteristics (continued)

(V+ = 3.0V, TA = +25°C, unless otherwise noted.)

PROPAGATION DELAY (t_{PD+})



PROPAGATION DELAY (t_{PD-})



Pin Description

PIN			NAME	FUNCTION
MAX941	MAX942	MAX944		
—	1	1	OUTA	Comparator A Output
—	2	2	INA-	Comparator A Inverting Input
—	3	3	INA+	Comparator A Noninverting Input
1	8	4	V+	Positive Supply (V+ to GND must be ≤ 6.5V)
—	5	5	INB+	Comparator B Noninverting Input
—	6	6	INB-	Comparator B Inverting Input
—	7	7	OUTB	Comparator B Output
—	—	8	OUTC	Comparator C Output
—	—	9	INC-	Comparator C Inverting Input
—	—	10	INC+	Comparator C Noninverting Input
6	4	11	GND	Ground
—	—	12	IND+	Comparator D Noninverting Input
—	—	13	IND-	Comparator D Inverting Input
—	—	14	OUTD	Comparator D Output
2	—	—	IN+	Noninverting Input
3	—	—	IN-	Inverting Input
4	—	—	SHDN	Shutdown: MAX941 is active when SHDN is driven high; MAX941 is in shutdown when SHDN is driven low.
5	—	—	LATCH	The output is latched when LATCH is low. The latch is transparent when LATCH is high.
7	—	—	OUT	Comparator Output
8	—	—	N.C.	No Connection. Not internally connected.

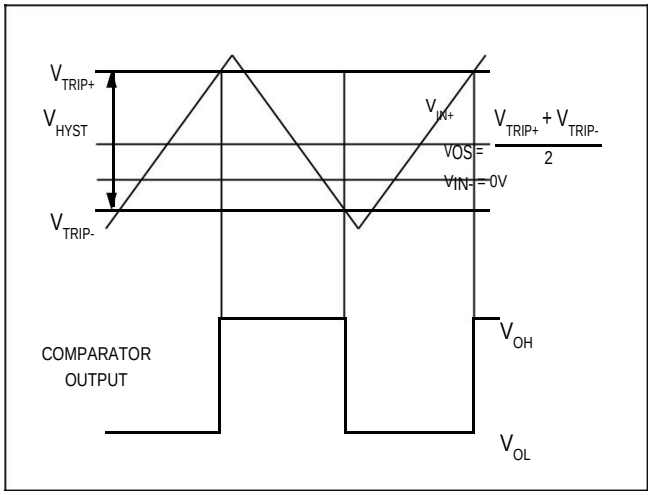


Figure 1. Input and Output Waveform, Noninverting Input Varied

Detailed Description

The MAX941/MAX942/MAX944 single-supply comparators feature internal hysteresis, high speed, and low power. Their outputs are guaranteed to pull within 0.4V of either supply rail without external pullup or pulldown circuitry. Rail-to-rail input voltage range and low-voltage single-supply operation make these devices ideal for portable equipment. The MAX941/MAX942/MAX944 interface directly to CMOS and TTL logic.

Timing

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the MAX941/MAX942/ MAX944 have internal hysteresis.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one com-parator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The MAX941/MAX942/MAX944's fixed internal hysteresis eliminates these resistors and the equations needed to determine appropriate values.

Figure 1 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

The MAX941 includes an internal latch that allows storage of comparison results. The LATCH pin has a high input impedance. If LATCH is high, the latch is transparent (i.e., the comparator operates as though the latch is not present). The comparator's output state is stored when LATCH is pulled low. All timing constraints must be met when using the latch function (Figure 2).

Shutdown Mode (MAX941 Only)

The MAX941 shuts down when SHDN is low. When shut down, the supply current drops to less than 60µA, and the three-state output becomes high impedance. The SHDN pin has a high input impedance. Connect SHDN to V+ for normal operation. Exit shutdown with LATCH high; other-wise, the output will be indeterminate.

Input Stage Circuitry

The MAX941/MAX942/MAX944 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of two back-to-back diodes between IN+ and IN- as well as two 4.1kΩ resistors (Figure 3). The diodes limit the differential voltage applied to the internal circuitry of the comparators to be no more than $2V_F$, where V_F is the forward voltage drop of the diode (about 0.7V at +25°C).

For a large differential input voltage (exceeding $2V_F$), this protection circuitry increases the input bias current at IN+ (source) and IN- (sink).

$$\text{Input Current} = \frac{(IN+ - IN-) - 2V_F}{2 \times 4.1k\Omega}$$

Input current with large differential input voltages should not be confused with input bias current (I_B). As long as the differential input voltage is less than $2V_F$, this input cur-rent is equal to I_B. The protection circuitry also allows for the input common-mode range of the MAX941/MAX942/ MAX944 to extend beyond both power-supply rails. The output is in the correct logic state if one or both inputs are within the common-mode range.

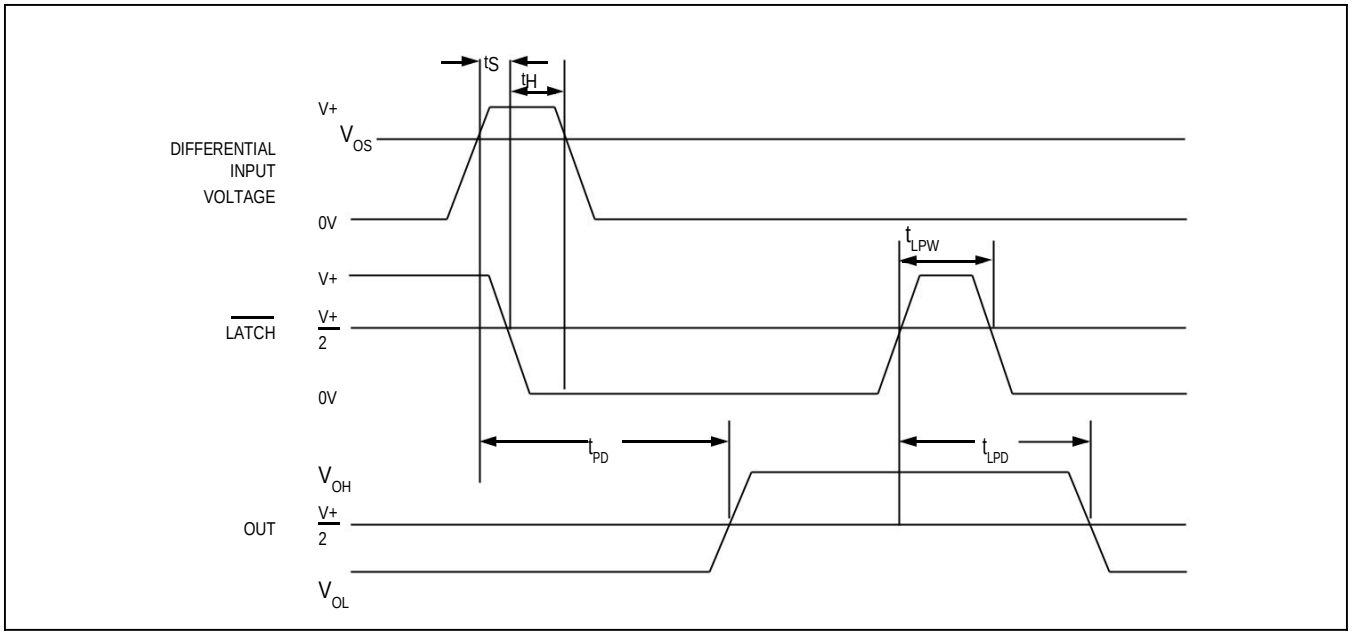


Figure 2. MAX941 Timing Diagram with Latch Operator

Output Stage Circuitry

The MAX941/MAX942/MAX944 contain a current-driven output stage as shown in Figure 4. During an output transition, I_{SOURCE} or I_{SINK} is pushed or pulled to the output pin. The output source or sink current is high during the transition, creating a rapid slew rate. Once the output voltage reaches V_{OH} or V_{OL}, the source or sink current decreases to a small value, capable of maintaining the V_{OH} or V_{OL} static condition. This significant decrease in current conserves power after an output transition has occurred.

One consequence of a current-driven output stage is a linear dependence between the slew rate and the load capacitance. A heavy capacitive load will slow down a voltage output transition. This can be useful in noisesensitive applications where fast edges may cause interference.

Applications Information

Circuit Layout and Bypassing

The high gain bandwidth of the MAX941/MAX942/MAX944 requires design precautions to realize the comparators' full high-speed capability. The recommended precautions are:

11) Use a printed circuit board with a good, unbroken, low-inductance ground plane.
12) Place a decoupling capacitor (a 0.1µF ceramic capaci-tor is a good choice) as close to V+ as possible.
13) Pay close attention to the decoupling capacitor's band-width, keeping leads short.
14) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the comparators.
15) Solder the device directly to the printed circuit board instead of using a socket.

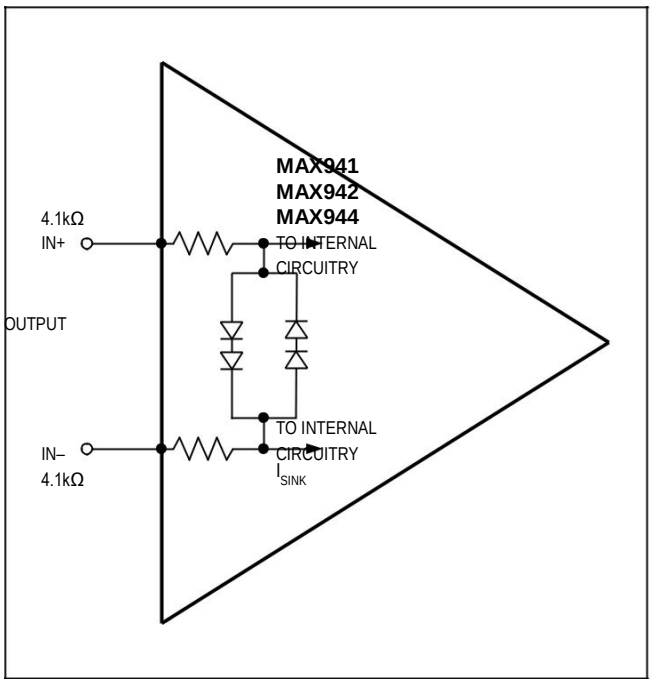


Figure 3. Input Stage Circuitry

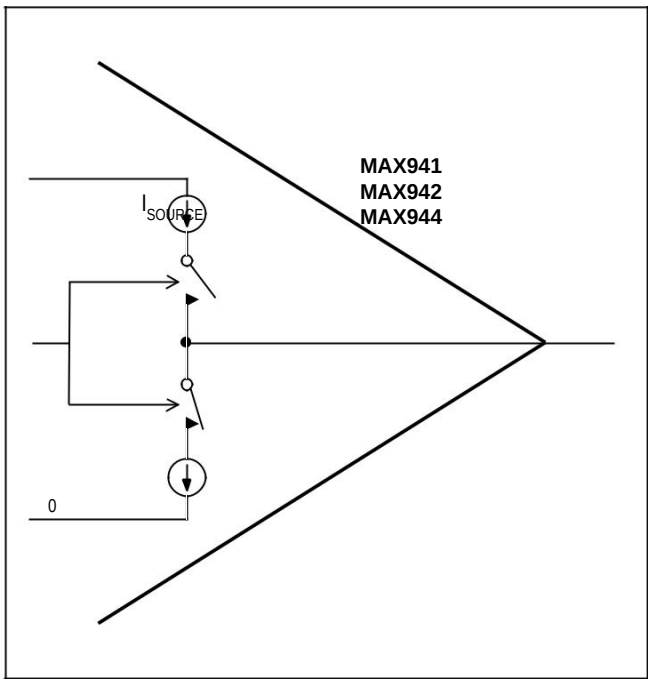


Figure 4. Output Stage Circuitry

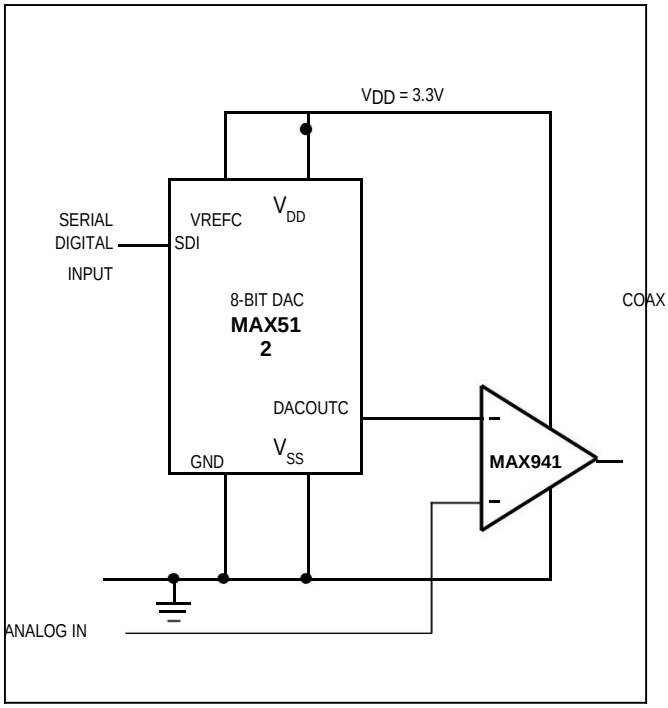


Figure 5. 3.3V Digitally Controlled Threshold Detector

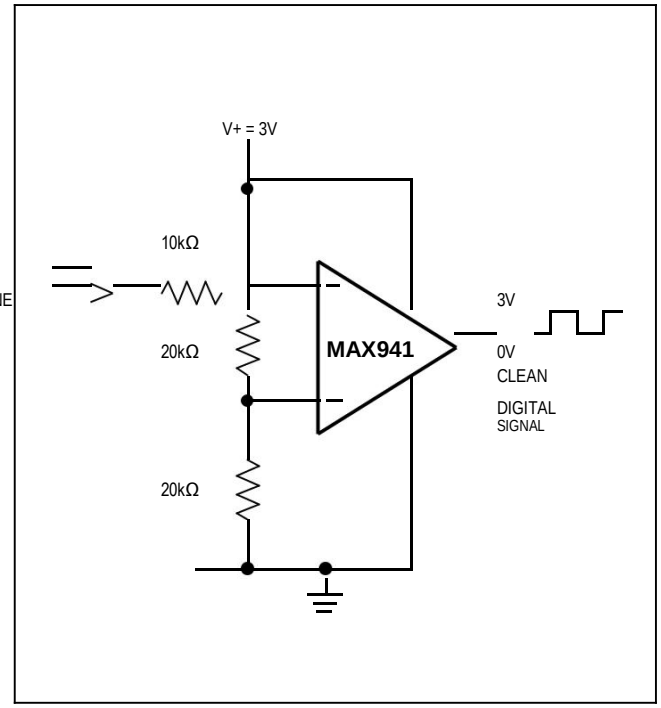


Figure 6. Line Transceiver Application

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX942MSA/PR	-55°C to +125°C	8 SO
MAX942CPA	0°C to +70°C	8 PDIP
MAX942CSA	0°C to +70°C	8 SO
MAX942EPA	-40°C to +85°C	8 PDIP
MAX942ESA	-40°C to +85°C	8 SO
MAX942EUA-T	-40°C to +85°C	8 µMAX
MAX942AUA-T	-40°C to +125°C	8 µMAX
MAX944CPD	0°C to +70°C	14 PDIP
MAX944CSD	0°C to +70°C	14 SO
MAX944EPD	-40°C to +85°C	14 PDIP
MAX944ESD	-40°C to +85°C	14 SO

T = Tape and reel.

Chip Information

PROCESS: BIPOLAR

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 µMAX	U8-1	**21-0036**	**90-0092**
8 PDIP	P8-1	**21-0043**	**—**
8 SO	S8-2	**21-0041**	**90-0096**
14 PDIP	P14-3	**21-0043**	**—**
14 SO	S14-1	**21-0041**	**90-0112**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
8	12/08	Added SO package diagram and removed transistor count	10
9	3/09	Corrected *Ordering Information* for MAX944ESD	10
10	9/14	Corrected *Electrical Characteristics* and removed automotive reference from Features	1, 3

10 References

Agrawal, G. (2010). *Applications of nonlinear fiber optics*: Academic press.

Agrawal, G. P. (2002). Optical receivers. *Fiber-Optic Communication Systems, Fourth Edition*, 128-181.

Akaiwa, Y. (2015). *Introduction to digital mobile communication*: John Wiley & Sons.

Al-Azzawi, A. (2006). *Fiber optics: principles and practices*: CRC Press.

Al-Nedawe, B. M. (2014). *Microelectronic Implementation of Dicode PPM System Employing RS Codes.* PhD Thesis, The University of Huddersfield.

Alam, S. J., Alam, M. R., Hu, G., & Mehrab, M. Z. (2011). Bit error rate optimization in fiber optic communications. *International Journal of Machine Learning and Computing, 1*(5), 435.

Altera. (2015). High Speed Mezzanine Card (HSMC) Specification.

Altera. (2016). Cyclone III FPGA development kit.

Babar, Z., Nguyen, H. V., Botsinis, P., Alanis, D., Chandra, D., Ng, S. X., & Hanzo, L. (2017). Unity-Rate Codes Maximize the Normalized Throughput of ON–OFF Keying Visible Light Communication. *IEEE Photonics Technology Letters, 29*(3), 291-294.

Bennett, W. (1958). Statistics of regenerative digital transmission. *Bell System Technical Journal, 37*(6), 1501-1542.

Best, R. E. (1999). Phase-locked loops: Design. *Simulation and Applications, 4*.

Brown, S. (2010). Fundamentals of digital logic design with VHDL.

Brown, S., Brown, S. D., & Vranesic, Z. G. (2008). *Fundamentals of Digital Logic with VHDL Design*: McGraw-Hill.

Brundage, H. (2010). *Designing a wireless underwater optical communication system.* Massachusetts Institute of Technology.

Calderbank, A., & Georghiades, C. (1993). *Coding for the unsynchronized optical OPPM channel.* Paper presented at the Communications, 1993. ICC'93 Geneva. Technical Program, Conference Record, IEEE International Conference on.

Calvert, N., Sibley, M. J., & Unwin, R. T. (1988). Experimental optical fibre digital pulse-position modulation system. *Electronics letters, 24*(2), 129-131.

Chen, C.-C., & Gardner, C. (1986). Performance of PLL synchronized optical PPM communication systems. *IEEE Transactions on Communications, 34*(10), 988-994.

Chen, C.-C., Win, M. Z., Marshall, W. K., & Lesh, J. R. (1991). *Low-data-rate coherent optical link demonstration using frequency-stabilized solid-state lasers.* Paper presented at the Optics, Electro-Optics, and Laser Applications in Science and Engineering.

Choudhary, K., & Kumar, S. (2017). Design of pseudorandom binary sequence generator using lithium-niobate-based Mach–Zehnder interferometers. *Optical Engineering, 56*(5), 057104-057104.

Cryan, R., & Unwin, R. (1993). Optimal and suboptimal detection of optical fibre digital PPM. *IEE Proceedings J (Optoelectronics), 140*(6), 367-375.

Cryan, R., Unwin, R. T., Garrett, I., Sibley, M. J., & Calvert, N. (1990). Optical fibre digital pulse-position-modulation assuming a Gaussian received pulse shape. *IEE Proceedings J-Optoelectronics, 137*(2), 89-96.

Cryan, R. A. (2010). Spectral characterisation of shortened pulse position modulation format. *Electronics letters, 46*(5), 355. doi: 10.1049/el.2010.2667

Dai, L., Wang, Z., & Yang, Z. (2012). Next-generation digital television terrestrial broadcasting systems: Key technologies and research trends. *IEEE Communications Magazine, 50*(6).

Dakin, J. P., & Brown, R. G. (2017). *Handbook of Optoelectronics: Enabling Technologies (Volume Two)*: CRC Press.

Datta, D., & Gangopadhyay, R. (1987). Simulation studies on nonlinear bit synchronizers in APD-based optical receivers. *IEEE Transactions on Communications, 35*(9), 909-917.

Davidson, F. (1985). Direct-detection optical communication with color coded pulse position modulation signaling. *IEEE Transactions on Communications, 33*(3), 273-276.

Davidson, F., & Bayoumi, M. (1987). Theoretical performance of direct detection optical communication with AlGaAs laser transmitters, avalanche photodiode detectors, and color-coded PPM signaling. *Journal of lightwave technology, 5*(11), 1574-1583.

Davidson, F. M., & Sun, X. (1989). Slot clock recovery in optical PPM communication systems with avalanche photodiode photodetectors. *IEEE Transactions on Communications, 37*(11), 1164-1172.

DeCusatis, C., & DeCusatis, C. J. S. (2010). *Fiber optic essentials*: Academic Press.

Diehl, W., Farahmand, F., Yalla, P., Kaps, J.-P., & Gaj, K. (2017). *Comparison of hardware and software implementations of selected lightweight block ciphers.* Paper presented at the Field Programmable Logic and Applications (FPL), 2017 27th International Conference on.

Djordjevic, I., Ryan, W., & Vasic, B. (2010). *Coding for optical channels*: Springer Science & Business Media.

Doulos, P. (2005). The VHDL Golden Reference guide: Book.

Elmirghani, J., Cryan, R., & Clayton, F. (1992a). *Frame synchronisation for optical fibre digital PPM.* Paper presented at the Singapore ICCS/ISITA'92.'Communications on the Move'.

Elmirghani, J., Cryan, R., & Clayton, F. (1992b). *Spectral properties of optical fibre digital PPM'.* Paper presented at the IEE Fourth Bangor Comm. Symp., Bangor, UK.

Elmirghani, J., Cryan, R., & Clayton, M. (1992). Spectral characterisation and frame synchronisation of optical fibre digital PPM. *Electronics letters, 28*(16), 1482-1483.

Elmirghani, J. M., Cryan, R. A., & Clayton, F. (1992). *Optical fiber n-ary PPM: the question of slot synchronization.* Paper presented at the Fibers' 92.

Fahs, B., Chowdhury, A. J., Zhang, Y., Ghasemi, J., Hitchcock, C., Zarkesh-Ha, P., & Hella, M. M. (2017). Design and Modeling of Blue-Enhanced and Bandwidth-Extended PN Photodiode in Standard CMOS Technology. *IEEE Transactions on Electron Devices, 64*(7), 2859-2866.

Feng, Z. C. (2017). *Handbook of Solid-State Lighting and LEDs*: CRC Press.

Franks, L. (1980). Carrier and Bit Synchronization in Data Communication--A Tutorial Review. *IEEE Transactions on Communications, 28*(8), 1107-1121. doi: 10.1109/tcom.1980.1094775

Gagliardi, R. (1974). Synchronization using pulse edge tracking in optical pulse-position modulated communication systems. *IEEE Transactions on Communications, 22*(10), 1693-1702.

Gagliardi, R. M., & Kim, Y. (1988). System design for optical PPM communications with diode combining. *IEEE Transactions on Communications, 36*(2), 186-190.

Gallion, P. (2017). Applications to Optical Communication. *Micro-and Nanophotonic Technologies*, 291-332.

Gardner, F. M. (2005). *Phaselock techniques*: John Wiley & Sons.

Garrett, I. (1983). *Digital pulse-position modulation over slightly dispersive optical fibre channels.* Paper presented at the Int. Symp. Information Theory, St. Jovite.

Garrett, I. (1983). Pulse-position modulation for transmission over optical fibers with direct or heterodyne detection. *IEEE Transactions on Communications, 31*(4), 518-527.

Ghassemlooy, Z., & Popoola, W. O. (2010). *Terrestrial free-space optical communications*: InTech.

Gitlin, R., & Salz, J. (1971). Timing recovery in PAM systems. *Bell System Technical Journal, 50*(5), 1645-1669.

Gol'dsteyn, A., Frezinskiy B. Ya. (1980). Statistical estimation of the time of arrival of a sequence of optical PPM pulses. *Telecommun. Radio Eng, 2*, 35.

Govind, P. A. (2002). Fiber-optic communication systems. *John Wiley, New York.*

Greefkes, J., & Riemens, K. (1970). Code modulation with digitally controlled companding for speech transmission. *Philips Technical Review, 31*(11-1), 335-&.

Haskell, R. E., & Hanna, D. M. (2009). *Introduction to Digital Design: Using Digilent FPGA Boards, Block Diagram, VHDL Examples [30 VHDL*.

Hunter, R., & Johnson, T. T. (1996). *Introduction to VHDL*: Springer Science & Business Media.

Ilyas, M., & Mouftah, H. T. (2003). *The Handbook of optical communication networks*: CRC Press.

Ippolito, L. J., & Ippolito Jr, L. J. (2017). *Satellite communications systems engineering: atmospheric effects, satellite link design and system performance*: John Wiley & Sons.

Keiser, G. (2003). *Optical fiber communications*: Wiley Online Library.

Komine, T., Lee, J. H., Haruyama, S., & Nakagawa, M. (2009). Adaptive equalization system for visible light wireless communication utilizing multiple white LED lighting equipment. *IEEE Transactions on Wireless Communications, 8*(6).

Lecoy, P. (2008). Fiber-Optic Transmission Systems. *Fiber-Optic Communications*.

Li, H., Fang, J., Chen, S., Wang, K., & Tang, Y. (2017). Pulse Density Modulation for Maximum Efficiency Point Tracking of Wireless Power Transfer Systems. *IEEE Transactions on Power Electronics*.

Ling, G., & Gagliardi, R. (1986). Slot synchronization in optical PPM communications. *IEEE Transactions on Communications, 34*(12), 1202-1208.

Liu, A. (2002). *The Mathematical Theory of Communication*.

Maghrabi, M. M., Kumar, S., & Bakr, M. H. (2017). Dispersion compensation of fiber optic communication system with direct detection using artificial neural networks (ANNs). *Optics Communications*.

Massarella, A. J., & Sibley, M. J. (1992). Experimental error correction results for optical digital pulse-position modulation. *Electronics letters, 28*(18), 1684-1686.

Mazzini, M., Traverso, M. J., & Nowell, M. (2017). PULSE AMPLITUDE MODULATION (PAM) OVER MULTI-MODE LINK WITH RECEIVER SPATIAL FILTERING: US Patent 20,170,272,164.

McEliece, R. (1981). Practical codes for photon communication. *IEEE transactions on information theory, 27*(4), 393-398.

Monmasson, E. (2017). FPGAs: Fundamentals, Advanced Features, and Applications in Industrial Electronics [Book News]. *IEEE Industrial Electronics Magazine, 11*(2), 73-74.

Mostafa, K. (2015). *Theoretical Analyses and Practical Implementation of Duobinary Pulse Position Modulation Using Mathcad, VHDL, FPGA and Purpose-built Transceiver.* PhD Thesis, The University of Huddersfield.

Mostafa, K., Sibley, M. J., & Mather, P. J. (2014). Duobinary pulse position modulation–a novel coding scheme for the dispersive optical channel. *IET optoelectronics, 8*(6), 264-269.

Nikolaidis, K., & Sibley, M. J. (2007). Investigation of an optical multiple PPM link over a highly dispersive optical channel. *IET optoelectronics, 1*(3), 113-119.

Nikolaidis, K., & Sibley, M. J. (2010). Investigation of higher order optical multiple pulse position modulation links over a highly dispersive optical channel. *IET optoelectronics, 4*(2), 85-94.

O'Reilly, J. J., & Yichao, W. (1985). Line code design for digital pulse-position modulation. *IEE Proceedings F Communications, Radar and Signal Processing, 132*(6), 441. doi: 10.1049/ip-f-1.1985.0084

Ray, I. (2015). *Analysis of Offset Pulse Position Modulation.* PhD Thesis, University of Huddersfield.

Ray, I., Sibley, M. J., & Mather, P. J. (2012). Performance analysis of offset pulse-position modulation over an optical channel. *Journal of lightwave technology, 30*(3), 325-330.

Rosenberg, R., Chamzas, C., & Fishman, D. (1984). Timing recovery with SAW transversal filters in the regenerators of undersea long-haul fiber transmission systems. *IEEE journal on selected areas in communications, 2*(6), 957-965.

Saleh, B. E., Teich, M. C., & Saleh, B. E. (1991). *Fundamentals of photonics* (Vol. 22): Wiley New York.

Sánchez, A. M., Moehlmann, U., Blinzer, P., & Ehlert, M. (2016). *Practical design considerations for an all-digital PLL in a digital car radio reception SoC.* Paper presented at the Central American and Panama Convention (CONCAPAN XXXVI), 2016 IEEE 36th.

Senior, J. M., & Jamro, M. Y. (2009). *Optical fiber communications: principles and practice*: Pearson Education.

Shalaby, H. (1993). *Performance of uncoded overlapping PPM under communication constraints.* Paper presented at the Communications, 1993. ICC'93 Geneva. Technical Program, Conference Record, IEEE International Conference on.

Shalaby, H. M. (1999). A performance analysis of optical overlapping PPM-CDMA communication systems. *Journal of lightwave technology, 17*(3), 426-433.

Sibley, M. (2004). Analysis of multiple pulse position modulation when operating over graded-index plastic optical fibre. *IEE Proceedings-Optoelectronics, 151*(6), 469-475.

Sibley, M. J. (1993). *Design implications of high-speed digital PPM.* Paper presented at the SPIE's 1993 International Symposium on Optics, Imaging, and Instrumentation.

Sibley, M. J. (2003). Dicode pulse-position modulation: a novel coding scheme for optical-fibre communications. *IEE Proceedings-Optoelectronics, 150*(2), 125-131.

Sibley, M. J. (2004). Suboptimal filtering in a zero-guard, dicode PPM system operating over dispersive optical channels. *IEE Proceedings-Optoelectronics, 151*(4), 237-243.

Sibley, M. J. (2011). Analysis of offset pulse position modulation-a novel reduced bandwidth coding scheme. *IET optoelectronics, 5*(4), 144-150.

Sibley, M. J., & Massarella, A. J. (1993). *Detection of digital pulse position modulation over highly/slightly dispersive optical channels.* Paper presented at the Berlin-DL tentative.

Sibley, M. J. N. (1995). Optical Communications: Components and Systems. (Second edition UK, The Macmillan Press LTD).

Sugiyama, H., & Nosu, K. (1989). MPPM: A method for improving the band-utilization efficiency in optical PPM. *Journal of lightwave technology, 7*(3), 465-472.

Sun, X., & Davidson, F. M. (1990). Word timing recovery in direct detection optical PPM communication systems with avalanche photodiodes using a phase lock loop. *IEEE Transactions on Communications, 38*(5), 666-673.

Svelto, O., & Hanna, D. C. (1976). *Principles of lasers*: Springer.

Takasaki, Y. (1972). Timing extraction in baseband pulse transmission. *IEEE Transactions on Communications, 20*(5), 877-884.

Thyagarajan, K., & Ghatak, A. (2007). *Fiber optic essentials* (Vol. 10): John Wiley & Sons.

Thyagarajan, K., & Ghatak, A. (2010). *Lasers: fundamentals and applications*: Springer Science & Business Media.

Uddin, S., Ansari, I. R., & Naaz, S. (2016). Low Bit Rate Speech Coding Using Differential Pulse Code Modulation. *Advances in Research, SCIENCEDOMAIN International, 8*(3), 2348-0394.

Westbrook, L., & Moodie, D. (1996). Simultaneous bi-directional analogue fibre-optic transmission using an electroabsorption modulator. *Electronics letters, 32*(19), 1806-1807.

Zerek, A. R., Elfituri, M. M., & Emhimid, A. A. (2017). *Improving design of the 2 nd order high pass sigma delta modulation.* Paper presented at the Green Energy Conversion Systems (GECS), 2017 International Conference on.

Zhang, R. (2004). *Clock and data recovery circuits.* Citeseer.

Zwillinger, D. (1988). Differential PPM has a higher throughput than PPM for the band-limited and average-power-limited optical channel. *IEEE transactions on information theory, 34*(5), 1269-1273.