Theoretical Analyses and Practical Implementation of Duobinary Pulse Position Modulation Using Mathcad, VHDL, FPGA and Purpose-built Transceiver

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Abstract

Duobinary pulse-position modulation (PPM), a novel channel coding scheme, has been proposed in this thesis as an alternative method of improving bandwidth utilisation efficiency and sensitivity over existing coding schemes such as digital PPM, dicode PPM, multiple PPM and offset PPM while operating over slightly or highly dispersive graded-index (GI) plastic optical fibre (POF) channels of limited bandwidth. Theoretical investigation based on simulations of mathematical models with maximum likelihood sequence detection (MLSD) at 1 Gbps on-off keying (OOK) data shows that duobinary PPM significantly outperforms optimised digital PPM at low fibre bandwidths by 8.7 dB while only operating at twice the original pulse code modulation (PCM) data rate. It has also been shown at high fibre bandwidth duobinary PPM gives a sensitivity of -42.2 dBm which is favourably comparable to digital PPM seven-level coding sensitivity of -44.1 dBm. Results presented in the thesis also demonstrate that at very low normalised fibre bandwidths (below 1 and down to 0.43) duobinary PPM outperforms dicode PPM by 1.2 dB requiring 27 x 10^3 photons per pulse compared to 40.3 x 10^3 required by Dicode PPM. Due to the use of MLSD at low bandwidths, wrong-slot errors are completely eliminated, and the effect of erasure and false-alarm errors are significantly reduced thus resulting in significantly improved sensitivity.

Successful VHSIC hardware description language (VHDL) and field programmable gate array (FPGA) implementation of duobinary PPM coder, decoder and MLSD as a single system has been presented in the thesis. An FPGA embedded bit error rate (BER) test device has also been implemented for sensitivity measurements purposes and all the designs have been tested successfully with back-to-back testing. A purpose-built VCSEL 850 nm wavelength based transceiver system has been designed and successful functional tests have been carried out. Maximum operational data rate of the transceiver is currently 622 Mbps to match the maximum operating frequency of the FPGA, however, it has the capability to operate up to 3.2 Gbps. Further work on receiver characterisation and slot and frame synchronisation of duobinary PPM is required.

All the results and analyses indicate that duobinary PPM is an ideal alternative to be considered for highly dispersive optical channels, and performance evaluation for higher bandwidths also favourably compares to existing coding schemes with only twice the expansion of original PCM data rate.

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Abbreviations	Meaning
ADC	Analogue-to-digital Converter
APD	Avalanche Photodiode
ASIC	Application-specific Integrated Circuit
BER	Bit Error Rate
BERT	Bit Error Rate Test
BPPM	Binary Pulse Position Modulation
CATV	Community Antenna Television
CDMA	Code Division Multiple Access
CMOS	Complementary Metal-oxide Semiconductor
CML	Current Mode Logic
D2B	Domestic Digital Bus
DAC	Digital-to-analogue Converter
DFT	Design for Test
DH-PIM	Dual Header – Pulse Interval Modulation
DiPPM	Dicode Pulse Position Modulation
DPPM	Differential Pulse Position Modulation
DuoPPM	Duobinary Pulse Position Modulation
EMI	Electro-Magnetic Interference
FEC	Forward Error Correction
FPGA	Field Programmable Gate Array
FSO	Free-space Optical Communication
GI	Graded-Index

GI-POF	Graded-Index Plastic Optical Fibre
GPIO	General-purpose Input/output
HDL	Hardware Description Language
HDTV	High Definition Television
IPTV	Internet Protocol Television
ISI	Inter-symbol Interference
IC	Integrated Circuits
LA	Limiting Amplifier
LAN	Local Area Network
LASER	Light Amplification by Stimulated Emission of Radiation
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LVTTL	Low-voltage Transistor-transistor Logic
LVDS	Low-voltage Differential Signal
MLSD	Maximum Likelihood Sequence Detection
MM	Multi-mode
MMF	Multi-mode Fibre
MPPM	Multiple Pulse Position Modulation
MSB	Most Significant Bit
NMOS	N-type Metal-oxide Semiconductor
NRZ	Non-Return to Zero
OOK	On-Off Keying
OPPM	Overlapping Pulse Position Modulation
PCB	Printed Circuit Board
PCM	Pulse Code Modulation

PCS	Plastic Clad Silica
PD	Photodiode
PDD	Proportional Derivative Delay
PF-GI-POF	Perfluorinated Graded-index Plastic Optical Fibre
PIM	Pulse Interval Modulation
PISO	Parallel-in-Serial-out
PIN-FET	Positive-intrinsic-negative Field Effect Transistor
PLL	Phase-locked Loop
PMMA	Polymethyl Methacrylate
POF	Plastic Optical Fibre
PPM	Pulse Position Modulation
PRBS	Pseudo Random Binary Sequence
PSD	Power Spectral Density
QAM	Quadrature Amplitude Modulation
RCLED	Resonant Cavity Light Emitting Diode
RS	Reed-Solomon
RTL	Register Transfer Level
SI	Step-Index
SIPO	Serial-in-Parallel-out
SM	Single-Mode
SMF	Single-Mode Fibre
SMD	Surface-mount Device
SMA	Sub Miniature version A
ST	Straight Tip
SoC	System-on-chip

TTL	Transistor-transistor Logic
TIA	Transimpedance Preamplifier
VCO	Voltage Controller Oscillator
VCSEL	Vertical Cavity Surface Emitting Laser
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VoIP	Voice over Internet Protocol

Chapter 1

1.1 Introduction

Ever since the proposal of Digital Pulse Position Modulation (DPPM) as a very attractive method of modulation for optical fibre links by Garett [1] in 1983, a new window of channel coding techniques was opened for the research. In the original DPPM the key proposal was made to use the vast bandwidth that was available compared to the data transmission rates in the early 80s in order to significantly improve the receiver sensitivity. Hence, the DPPM scheme has been proposed as a method of utilising the bandwidth available in optical fibres, with a 5-11 dB improvement in sensitivity being achieved compared to an equivalent Pulse Code Modulation (PCM) system [2]. However, this improvement comes at a cost. A number of key PPM based coding schemes have been proposed in recent years to improve the channel performance while reducing bandwidth utilisation and improving sensitivity at the same time. Every coding scheme that has been proposed[1] has advantages and improves the existing techniques to a certain extent. However, all the channel coding schemes inevitably come with their limitations as well as advantages.

Some improved coding schemes have some features which make them difficult to implement such as increased data rate. For example, if digital PPM is used, the final data rate can be almost 23 times that of the original PCM [1] and this makes implementation difficult by a greater order of magnitude. In addition, there is always room for further development regarding error detection and correction at the receiver as no existing PPM coding scheme is completely error free and the requirement of data security is ever increasing. All these have to be done without causing unwanted additional traffic in the channel and compromising speed thus there is a

[1] Channel coding schemes will be discussed in detail later in Chapter 2 – Literature Review.

greater need for improved error detection and correction algorithm. The special mention of compromised data rate is relevant because some of key channel coding schemes that are relevant to this research project have been developed to improve sensitivity and bandwidth utilisation in relatively low bandwidth and highly dispersive optical fibre channels. There are already existing and operational channel coding schemes that are very successfully deployed all over the world for the fibre channel line coding purpose such as 8B/10B, 5B/6B, 7B/8B, 9B/10B, 64B/66B etc. [3-4] where the first number signifies the original data bits and the last number denotes the number of bits the original data will be coded into. These are deployed in most fibre channels where bandwidth restriction is not much of a deterrent and the error detection and correction properties of these line coding schemes have significant room for improvement. Since the advent of fibre optic networks full deployment as digital data transmission medium, the actual physical optical fibre, especially the silica-glass fibre [5] types have gone through exponential level of improvement through research and investment. Therefore, even in modern day and age bandwidth, distance and speed are not something to be excessively concerned with when using silica based glass fibre.

However, the catch is that they are expensive and the hardware required to implement the links and maintaining are extremely expensive compared to any other contemporary transmission medium. Therefore, they are only used for large scale commercial purposes such as broadband, telecommunication, intercontinental data channels or government projects where cost is not a major issue. At the turn of the century, it is fair to say that electronics and communications have become consumer products, thus there is a need for cheaper alternative of silica-glass based optical fibre links. Plastic Optical Fibre (POF) [6] has become the main alternative cost effective way to still have high speed networks over the last decade. POFs have wide variety of uses such as any short distance networks in industrial premises, manufacturing plants,

automobile intra-communication, home networks, high-speed media interface just to name a few of the highly potential future deployment. Automobile and manufacturing networks using POFs are very much a reality now as many robotics arms in manufacturing plants are connected to POF networks and the electronics, media and data in some of the most advanced cars [7] are delivered by POF networks. For the aviation industry, it is highly useful due to optical links being immune to Electro-Magnetic Interference (EMI) which can cause catastrophic issues in any aircraft communication system.

The key attraction of POFs is that they are a much cheaper alternative to the classic glass fibre and the transceiver systems are significantly less complicated than its glass counterparts. However, all these advantages that can bring greater opportunities at low cost comes at a price. The bandwidth of the POF is limited compared to the glass fibre and the channel is highly dispersive which means that light can only travel very short distances through these channels before it is dispersed and detection becomes highly problematic at the receiver end. The main reason is that the POF is many years behind in development compared to traditional fibres as the use of it is becoming more and more popular only in recent years due to the exponential drive in consumer electronics. However, academics, engineers and manufacturing industries are now spending significant time and budget to improve the quality of the POFs such as achieving more bandwidth, less dispersion, thus improving sensitivity and many other features[2].

[2] Developments in Plastic Optical Fibres are discussed in greater details later in Chapter 2 – Literature review.

1.2 Background

As the development of the physical nature of Plastic Optical Fibre (POF) is gathering pace for full commercialisation and consumer use, researchers are also improving the understanding of channel coding for this particular medium of optical communications where coding schemes that are high performing over very dispersive channels and utilisation of less bandwidth are mandatory requirements. In the initial years of POF data transmission, the Resonant Cavity Light Emitting Diode (RCLED) was used with a wavelength of 650nm. However, improvement in Vertical Cavity Surface-Emitting Lase (VCSEL) [8] means that it is currently the most logical transmitter to be used for POF links design.

The actual POF has gone through drastic improvements over the years as well. POFs are currently available in 50/125 µm and 62/125 µm [6] which instantly means a major improvement regarding the light loss aspects for transmitter coupling and receiver photodiode light reception. Various channel coding schemes are in existence for optical communication links. Use of channel coding has also been implemented in high speed data links with various degree of success [9]. High-speed links typically refer to backplane or chip-to-chip interconnects that operate at very high data rates (~10 Gbps), low bit-error rate (~10^{-15}) and with high energy efficiency [9-10]. Depending on the channel characteristics of the high speed optical communications link, it has similar data rates and bit-error rate as high-speed back plane links. POFs are highly dispersive channels thus more efficient coding scheme and error detection and correction algorithm required for improved sensitivity and bandwidth reduction for bandwidth limited POF optical channels. Many variants of PPM have been proposed for the required improvements over the channel [11-17] but most of them are suited for long distance and high-speed optical communications link where bandwidth is not a concern and

the channel has low dispersion characteristics. These coding schemes are not useful for bandwidth limited short-distance POF channels where innovative coding schemes are required in order to effectively use the available bandwidth while improving the sensitivity and low data rate. Dicode PPM operates at a speed of four times that of the original PCM because it adds two guard slots, thus increasing the data rate [2, 18-24].

Like other technologies, scalability and speed of hardware are of great importance when commercial feasibility of any new technologies is concerned. System on chip (SoC) has become increasing popular with the increased complexity of new devices as they have certain advantages such as greater functionality, embedded characteristics, lower system cost, reduced time to market, scalability, ability to reconfigure and many more. VHSIC hardware description language (VHDL) is a C program based field programmable gate array (FPGA) simulation and programming software [25] that is perhaps the most popular complex high speed processor level programming software that is available for the engineers and researchers for any SoC designs. Signal integrity of high speed communication signals can be maintained due to the package size, many useful features such as Phase-locked Loops (PLL) are readily available in the FPGA which can be very easily programmed for operations such as clock division, clock extraction, clock generation and regeneration or any type of timing events that may be necessary for the transceiver designs and the complete coder, decoder, MLSD, Bit Error Rate Test circuits, Analogue to Digital (ADC) or Digital to Analogue (DAC) conversions that may be required by any coding schemes. FPGA implementation of the complete coding scheme is the future of optical data transmission.

Duobinary Pulse Position Modulation (DuoPPM) has been proposed as an alternative novel coding scheme which manifests many advantages over currently existing PPM formats according to the preliminary results obtained from theory and simulations [26-27][3]. It combines the bandwidth reduction of the three-level duo-binary code with the dispersion characteristics of conventional PPM. This coding scheme is intended to be implemented using VHDL (VHSIC hardware description language) and an FPGA (Field-programmable gate array) over plastic optical fibre (POF) thus making it an ideal SoC candidate with all the advantages that come with the SoC technologies. DuoPPM intends to run at the speed twice that of the original PCM with zero guard slots and with improved sensitivity and MLSD algorithm.

Nevertheless, if the preliminary promises of this new coding scheme are fulfilled upon successful implementation, it may be adapted to high-speed optical communications links potentially exceeding the speed of 10 Gbit/s. In addition to further reduction in bandwidth and greater dispersion characteristics, a novel MLSD error detection and correction algorithm will be implemented that completely eliminates wrong-slot errors and reduces the effects of false alarms and erasures and these performance improvements will be achieved only with twice the data rate of the original PCM. A cost effective VCSEL 850 nm wavelength based laser transceiver will be designed to form a single communication link with the FPGA development board for practical implementation of the DuoPPM coding scheme. The designed transceiver can also be easily used for Free Space Optical Communications (FSO) with few modification of the power and safety parameters.

[3] Published papers and papers submitted for publication that are being reviewed are listed in Appendix 1.

1.3 Aim and Objectives

1.3.1 Aim

The main aim of the research has been to develop, analyse and verify the coding methods and Maximum Likelihood Sequence Detection (MLSD) of Duobinary Pulse Position Modulation (DuoPPM) through three key stages: Mathcad modelling and simulations, VHDL and FPGA implementation of the coding scheme and finally design and implement VCSEL 850 nm based transceiver to be used with Plastic Optical Fibre (POF) channel for DuoPPM.

1.3.2 Objectives

The following objectives have been achieved during the course of the research:

- A wide ranging research has been undertaken to gather information about the relevant literature of channel coding schemes, specifically the channel coding schemes that are used for highly dispersive POF links. The main reason to carry out this exercise was to understand the advantages and limitations of the currently researched schemes and to be able to make comparisons of how these can be improved with the proposed novel DuoPPM.

- The second objective was to create a Mathcad[4] simulation model that closely resembles a POF link in terms of bandwidth and dispersion which was then to be used to simulate the DuoPPM to obtain the theoretically simulated confirmations of the viability and performance improvements of DuoPPM over comparable coding schemes. Mathcad software simulations obtain theoretically simulated sensitivity of the DuoPPM and

[4] Mathcad trademark of PTC Corporation.

compares with relevant POF coding schemes as well as the performance analysis of the MLSD of the DuoPPM itself.

- A complete design solution of the DuoPPM system need to be designed using VHDL programming language and Altera™ Quartus II software solution. The designs are to be tested for functional output verifications, and thereafter for timing analyses of the internal and external signals to ensure all the signals are in correct phase to produce the required outputs that have been verified by functional simulations when the designs are programmed on to a Field Programmable Gate Array (FPGA).

- Terasic™ DE2-115 FPGA[5] development board has been used to implement the VHDL designs for FPGA. It uses Cyclone™ IV E series FPGA EP4CE115F29C7N. The complete design will include: FPGA clock control block, Phase-locked Loop (PLL) for clock generation, division and recovery, Pseudo Random Binary Sequence (PRBS) PCM data generation, DuoPPM encoder, MLSD implementation and decoder, and finally a Bit Error Rate Test (BERT) system which will regenerate the original sent PRBS data sequence and use logic gates to check if any errors have occurred by comparing the original sequence with the regenerated data sequence.

- Transceiver design of the DuoPPM needs to be completed to operate over a highly dispersive POF link. VCSEL of 850 nm wavelength to be used to the transmission of data. As slightly higher power is required for the transmission, the VCSEL driver has been equipped with safety features such as over-current and over-power protection and constant VCSEL power so that regardless of any loss of power the receiver sensitivity will remain constant. The photodiode (PD) receiver to be used with Transimpedance Preamplifier (TIA) and Limiting Amplifier (LA) for the receiver.

[5] Terasic develops FPGA development boards for Altera Corporation FPGAs.

1.4 Thesis Organisation and Structure

The thesis has been organised and structured in a clear and coherent manner which makes it very easy to follow from the beginning to end. Footnotes have been added wherever necessary to provide further relevant information and clearly organised appendices have been provided after the conclusions of the main sections for further relevant and significant information. Appendix 1 is a very important part of the thesis as it contains two published papers on the research carried out and another paper [27] that has been submitted for publication to IET Optoelectronics journals. Two further papers are currently being written on the tasks completed for chapter 7, and 8 which will be completed shortly after submission of the thesis. Clear guidance is given in the chapters of the thesis regarding which publications they correspond to.

The thesis has been divided into 10 chapters and a brief description of what each chapter contains is given in the following points:

- Chapter 1 an introduction and background of the research project along with aims and objectives. It also provides a description of how the thesis is structured and the publications made by the author during the research project.
- Chapter 2 contains a literature review for the project. Some of the key research papers that have been reviewed are: relevant digital PPM based coding schemes, Plastic Optical Fibres (POF) and their physical properties and applications, VHDL and FPGA programming techniques, VCSEL transceiver designs for both POF and FSO links, Bit Error Rate Test (BERT) methods, Power Spectral Density (PSD) analysis, clock recovery systems for self-extracting coding schemes.
- Chapter 3 gives an overview of DuoPPM coding scheme. It shows how the data is coded and decoded and the theory of the errors that can occur in this coding scheme.

- Chapter 4 and 5 contain detailed analyses of how the MLSD of the DuoPPM has been developed and insight into the sequence correction procedure that needs to employed in case any errors in a sequence are detected.
- Chapter 6 explains the Mathcad modelling and simulation results of DuoPPM.
- Chapter 7 describes the VHDL designs of the complete DuoPPM system with both functional and timing analyses of all the designed circuit blocks. It also provides the results of FPGA implementation of the VHDL designs with final output waveforms shown from the oscilloscope for DuoPPM system.
- Chapter 8 details the transceiver design procedure and calculations for VCSEL POF transceiver that has been designed along with output waveforms.
- Chapter 9 discusses the complete thesis, and chapter 10 concludes the thesis with suggestions for further work that should be carried out to enhance the performance and practicality of DuoPPM coding scheme.

The appendices have six main parts and they are well structured. Appendix 1 contains all the published works along with the papers that have been submitted for publications and are currently being reviewed. Appendix 2 contains the Mathcad simulation model code of the DuoPPM and the relevant tables and graphs that may be of interest to the readers. Appendix 3 lists all the VHDL code and schematic diagrams that make the DuoPPM system in its entirety. Appendix 4 provides diagrams, PCB designs and other relevant information for the Transceiver designs. Appendix 5 contains the theoretical error sequences for the coding scheme that have been analysed to achieve the MLSD algorithm which has been implemented. Datasheets for VCSEL transmitter and receiver, and all the packaged ICs are provided at the very end of the thesis. A project Gantt chart has been provided in appendix 6.

1.5 Conclusions

In conclusion, an introduction to the thesis and the work completed for the project has been provided in this section. Background and brief literature about the key topics such as optical fibre and plastic optical fibre communications, channel coding schemes for dispersive and bandwidth limited channels, optical fibre links design, VHDL programming and FPGA implementation have also been provided. These key literature and research will be presented in more detail in the following chapter 2. The key aims and objectives for the thesis have been clearly stated and the organisation of the thesis through each chapter has been described in order to make it easier to follow and read the contents presented in the thesis.

Chapter 2

Literature Review

2.1 Pulse Position Modulation (PPM)

Pulse Position Modulation (PPM) schemes have been established as a leading method of utilising bandwidth available in the optical fibres, with significant improvement in sensitivity compared to equivalent pulse code modulation (PCM) [1, 11-13]. Various schemes of PPM have been proposed and investigated in recent past for use in optical communications links [1, 11-17]. The final data rate of some PPM systems can be almost 23 times that of the original PCM [2], thus making implementation difficult and expensive. Some of these PPM schemes can be attractive and suitable to implement for use in glass fibre or direct line of sight networks where bandwidth is not a concern, but unfortunately these optical communications links are expensive and not suitable for everyday use such as home networks, industrial networks and many other potentially direct consumer applications.

Monomode fibres are being used for many applications, as they offer greater repeater spacing and the possibility of upgrading the system in future by multiplexing at a higher bit rate [1]. However, PCM systems do not exploit the bandwidth shown by experimental monomode fibre links near the wavelength of minimum chromatic dispersion, which is orders of magnitude greater than that required for binary PCM systems at any data rate proposed for operational systems. Various PPM coding schemes have been investigated in order to effectively use available fibre bandwidth to improve channel performance in terms of sensitivity while reducing the complexity of the receiver design.

2.2 Existing Channel Coding Schemes

2.2.1 Digital Pulse Position Modulation

Digital PPM is one of the earliest coding schemes that was investigated and analysed by Garrett et al. [1, 11-13]. They have shown that the abundance in bandwidth available in the best monomode fibres may be exchanged for improved receiver sensitivity by employing digital PPM. It was shown for a 50 Mbit/s, 1.3 µm wavelength digital PPM system that provided the fibre bandwidth is several times that of the data rate, digital PPM can outperform commercially available PIN-BJT binary PCM systems [13]. The work was analysed for digital PPM systems operating over slightly dispersive optical channels using direct detection PIN-FET receivers and coherent receivers. They showed that there was a 5-11 dB theoretical improvement in sensitivity compared to standard Non-Return to Zero (NRZ) On-Off Keying (OOK) data. In digital PPM, M bits of information are transmitted using a single pulse by positioning it in one of 2^M time slots, figure 1 [1].

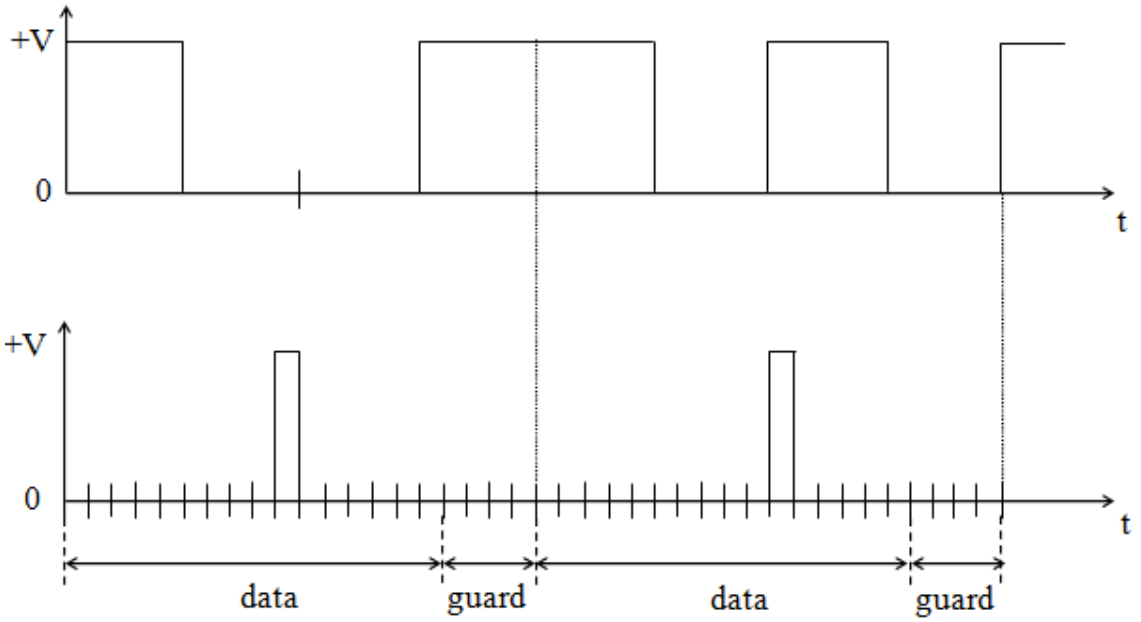


Fig. 2.1: Conversion of 4 bits of PCM (top trace) to digital PPM (bottom trace).

There is a significant improvement in sensitivity over NRZ OOK because a single pulse is used to transmit M bits of information. Therefore, by virtue of the lower mark: space ratio, increasing M means improving the sensitivity. However, in order to synchronise equivalent data throughput with NRZ OOK, the same amount of data must be transmitted within the same time frame. Therefore, for a data time frame of MT_b, where T_b is the bit period, there must be 2^M PPM time slots which means that the PPM slot rate is $2^M/M$ faster than the PCM bit rate in order to maintain the same information throughput. This large bandwidth expansion can make the final line rate prohibitively high.

2.2.2 Multiple Pulse Position Modulation (MPPM)

Sibley and Nikolaidis [28-30] have investigated Multiple Pulse Position Modulation (MPPM) for dispersive optical channels, however, MPPM was first proposed by Sugiyama and Nosu [31] as a viable method to improve the bandwidth utilisation efficiency in optical PPM. By virtue of the coding technique as shown by them, MPPM optical pulses are transmitted in multiple slots in one single block as shown by the figure 2.2 below [28].

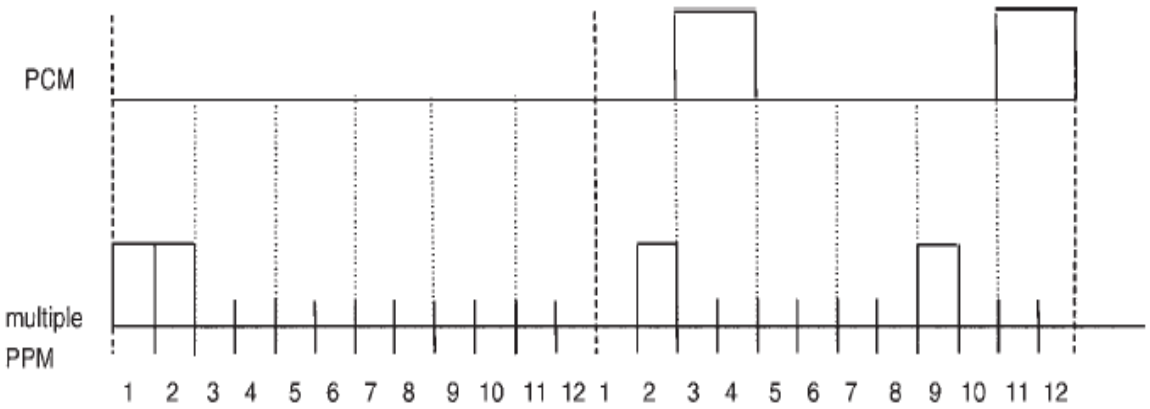


Fig. 2.2: Conversion of PCM (top trace) to multiple PPM double pulses per frame (bottom trace).

This method reduces the required transmission bandwidth in optical PPM to about half with the same transmission efficiency, thus increasing the band-utilisation efficiency. Sibley analysed and presented results of MPPM when operating over graded-index plastic optical fibre. It showed that the MPPM is one of the most bandwidth-efficient PPM coding schemes as it offers the sensitivity of digital PPM without the large bandwidth expansion. This scheme uses a number of pulses in a frame, with the pulse positions being determined by the original PCM word. Figure 2.2 (in previous page) shows (12/2) multiple PPM in which a 12-slot frame uses two data pulses to code 6 bits of PCM. Linear mapping is used in this instance and so the PCM word 000000 translates to pulses in slots 1 and 2 – referred to as 1,2 – whereas the PCM word 010001 results in 2,9. The line rate for this (12/2) code is twice that of the PCM. Further reductions can be achieved by using higher order codes [31] such as (15/4) which can code 10 bits of PCM resulting in a line rate of 1.5 times the PCM rate.

Sugiyama and Nosu [31] analysed the error performance and introduced the maximum likelihood detection (MLD) scheme and the prediction of error performance was simplified by the use of bounds. They concluded that multiple PPM is more efficient than digital PPM in terms of power and bandwidth utilisation. The best predicted sensitivity was 0.58 bits/photon compared to 0.5 bits/photon for digital PPM (both operating at an error rate of 1 in10^9). MPPM suffers from the usual PPM errors such as wrong-slot, erasure and false alarm errors due to either dispersion of the photons through the transmission channel or optical pulse detection errors at the receiver end or it may also be a combination of both and suitable MLSD can be applied to improve the sensitivity of MPPM.

2.2.3 Dicode Pulse Position Modulation (DiPPM)

Sibley and Charitopoulos [2, 18-24] proposed DiPPM which is another highly bandwidth-efficient PPM scheme that has been investigated and analysed extensively in recent years. This coding scheme combines dicode, a tertiary code sometimes used in magnetic recording, and digital PPM to form dicode PPM. They showed that DiPPM gives receiver sensitivity greater than digital PPM while operating at only four times the original data rate when coded with two guard slots and two times the original data rate when coded without the guard slots. The bandwidth efficiency of this coding scheme can be particularly useful when operating over band-limited channels such as plastic optical fibres. They showed that a high fibre bandwidth dicode PPM system can give sensitivities of -50.44 dBm and -44.27 dBm when operating with 155.52 Mbit/s and 1 Gbit/s PCM data rate, respectively, compared to typical PCM sensitivities of -38 dBm and -28 dBm. They also showed that DiPPM outperforms digital PPM at low fibre bandwidths by 3.02 dB.

In DiPPM coding scheme, both data transitions from logic zero to logic one and logic one to logic zero are coded as pulses in DiPPM slots SET and RESET respectively as shown in figure 2.3 (following page) [2], a zero signal (no pulses in either SET or RESET slots of the DiPPM) is transmitted if there is no change in the PCM signal. In DiPPM, these SET and RESET signals are converted into two pulse positions in a data frame. Thus a PCM transition from zero to one produces a pulse in slot S and a one to zero transition generates a pulse in slot R. In case of constant PCM data of either 1 or 0, no signal is transmitted. Although two guard slots have been used in this system, to reduce the effects of inter-symbol interference (ISI), this depends on the channel characteristics. If there is minimal inter symbol interference (ISI), zero guard slots could be used [32].

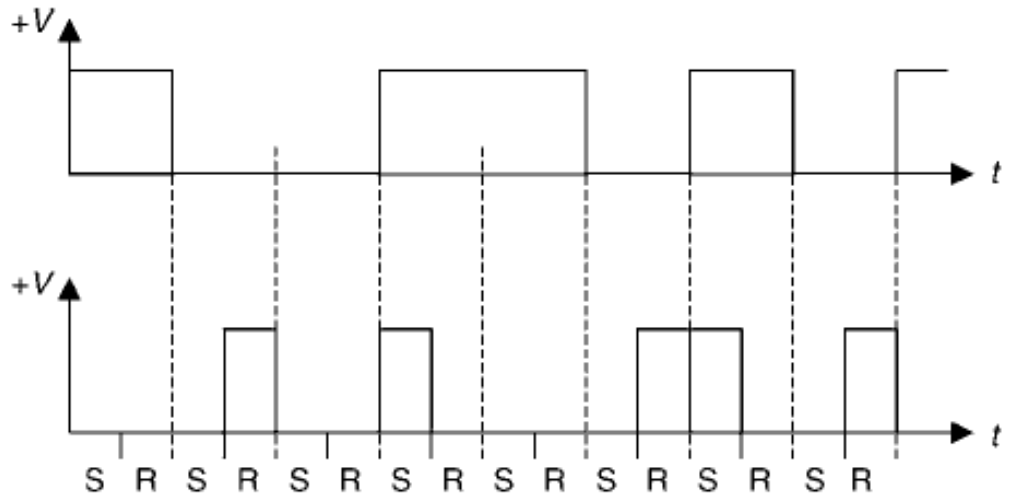


Fig. 2.3: Conversion of PCM data (top trace) into DiPPM.

PCM	Probability	Dicode PPM	Symbol
00	1 /4	No pulse	N
01	1 /4	SET	S
10	1 /4	RESET	R
11	1 /4	No pulse	N

Table 2.1: DiPPM symbol alphabet and probability.

2.2.4 Offset Pulse Position Modulation (Offset PPM)

One of the forerunners of research into restricted bandwidth coding schemes to improve performance and sensitivity Sibley [33-34] also proposed offset-PPM that offers increase in sensitivity over digital PPM and operate at half the line rate of digital PPM. Table 2.2 [33] in the following page how the offset coding scheme works with 3-bits of PCM input data and how 3-bit PCM data is coded into offset PPM word and compares that with the digital PPM word. Sibley showed that below 100_{PCM} the scheme is similar to digital PPM except that no pulse is transmitted for $000_{PCM.}$ When 100_{PCM} is reached, the 'sign' bit is introduced and coding continues as before. In effect the most significant bit (MSB) (the sign bit) shows whether the

offset is to be taken from 000_{PCM} or 100_{PCM}. In this way the line rate of offset PPM is exactly half that of digital PPM. It might initially be thought that there is a drop in sensitivity because some frames contain two pulses instead of just one for digital PPM; however, as Sibley showed, this novel technique offers a better performance than digital PPM when operating over highly dispersive channels.

Original PCM Word	Offset PPM Codeword	Digital PPM Codeword
000	0 000	0000 0001
001	0 001	0000 0010
010	0 010	0000 0100
011	0 100	0000 1000
100	1 000	0001 0000
101	1 001	0010 0000
110	1 010	0100 0000
111	1 100	1000 0000

Table 2.2: Coding table from original PCM to offset PPM and digital PPM when coding three bits of data.

A comparative generation of digital PPM, multiple PPM and dicode PPM from PCM data is shown below in figure 2.4 [18].

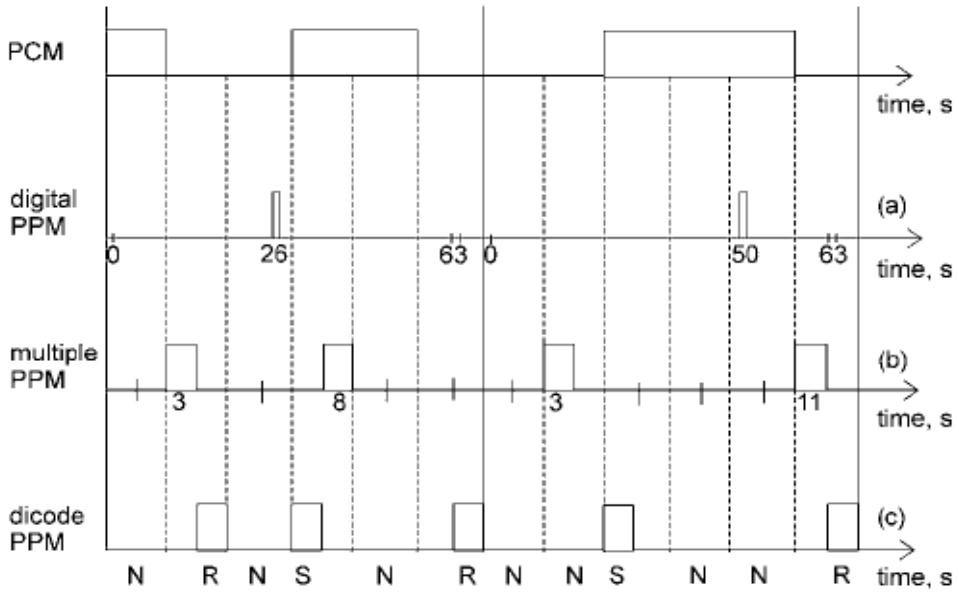


Fig. 2.4: Generation of (a) digital PPM, (b) multiple PPM and (c) dicode PPM from PCM data.

2.2.5 Differential PPM and Overlapping PPM

The last three decades significant amount of research has been conducted to overcome the various difficulties of digital pulse-position modulation (PPM) and the trend is to continue in order to find more suitable solutions. Digital PPM uses one pulse in one frame and requires a large number of slots to transmit one code word. Increasing the number of slots narrows the pulse width and that expands the bandwidth. Making a trade-off between bandwidth, line rate, and sensitivity becomes difficult as has been discussed in the earlier sections. Other than multiple PPM and dicode PPM many alternative coding systems have been proposed including differential PPM [16, 35] and overlapping PPM [17]. All of these aim to reduce the line rate while maintaining the receiver sensitivity.

Zwillinger [16] and Shiu and Kahn [35] proposed differential PPM coding scheme which can have a higher throughput of data than digital PPM because its line rate can be less than an equivalent digital PPM system. This increase in throughput comes from reducing the word length by suppressing the empty slots following a pulse. This results in a word that varies in length but whose average is less than the equivalent digital PPM word. An example of differential PPM coding is given in the table 2.3 below [35].

Source Bits	**Corresponding 4-PPM Chips (nominal mapping)**	**Corresponding 4-DPPM Chips (nominal mapping)**	**Corresponding 4-DPPM Chips (nominal mapping)**
00	1000	1	0001
01	0100	01	001
10	0010	001	01
11	0001	0001	1

Table 2.3: Mapping examples between source bits and transmitted chips of 4-PPM and 4-DPPM[6].

[6] DPPM here denotes Differential PPM, not to be confused with digital PPM.

Shalaby [17] also proposed a direct-detection optical code-division multiple access (CDMA) systems employing overlapping PPM (OPPM). In overlapping PPM, described by Shalaby, adjacent pulse positions are allowed to overlap, resulting in a line rate reduction. Shalaby restricted the upper and lower bound for the overlapping index such that overlapping PPM outperformed digital PPM. The performance characteristics were compared to optical CDMA systems employing traditional ON-OFF keying (OOK) and PPM schemes. Using OPPM it was shown that under fixed data rate and chip time, the OPPM-CDMA system outperforms both traditional OOK and PPM systems. Shalaby also showed that the throughput limitation of OPPM-CDMA is almost 6.7 times greater than that of OOK-CDMA.

2.2.6 M-Ary PPM, Reed-Solomon Coded PPM and Binary PPM

Alternative methods of PPM have also been investigated for free-space optical (FSO) links. Coding schemes such as M-ary PPM [36], Reed Solomon coded PPM [37], Binary PPM [38] have been proposed for FSO links for improved performance over existing modulation techniques.

Yan et al. [36] proposed M-ary PPM to improve the performance of a FSO communication system which is limited by light intensity fluctuations induced by atmospheric turbulence by using Forward Error Correction (FEC). They showed that power-efficiency of PPM scheme can be effectively employed in FSO systems to improve performance. The FEC scheme for M-ary PPM is based on Reed-Solomon (RS) codes. It was shown that FEC can reduce the required average signal light intensity for a high bit rate FSO system to keep a bit error rate (BER) below

$1x10^{-9}$, and that with the FEC scheme, the system is tolerant of the noise resulting from a background light that is stronger than the desired signal light.

Atmospheric attenuations and weather dependence remain major hurdles in the wide scale acceptability of the FSO communications technology. Muhammad et al. [37] proposed performance enhancement using higher state modulation schemes (i.e. 16 and 256-PPM) which promise a gain up to 25 dB when combined with Reed-Solomon (RS) codes and the results were compared to the widely used 2-state modulation mechanism. It was shown that the RS-coded PPM is an extremely robust and well-performing coded-modulation scheme for future FSO systems using a novel approach to terrestrial FSO channel modelling.

Kim [38] proposed the combined Binary Pulse Position Modulation (BPPM)/Biorthogonal Modulation for the direct-sequence Code Division Multiple Access (CDMA) systems in 1999. In direct comparison with M-ary orthogonal modulation the results of BPPM were found to be near identical, however, BPPM has the advantage of a much simpler receiver structure thus reducing complexity. Tahir et al. [39] also conducted simulations on BPPM in FSO communication systems in both weak and strong atmospheric turbulence to analyse the performance in terms of Bit Error Rate (BER) and eye diagrams with an Avalanche Photodiode (APD) receiver. In BPPM two bits are transmitted in block instead of one at a time and this block is called the BPPM frame. Their simulation results were encouraging as they matched the ideal calculated results.

2.3 Errors in PPM

In common with digital PPM, most of the PPM schemes are subject to three main error sources [32].

Erasure error where, due to negative noise spike, the amplitude of the pulse falls below the detection threshold. It occurs whenever noise destroys the pulse thus preventing detection. The probability of an erasure error P_r, assuming the receiver output noise voltage is a Gaussian random variable is

$$P_r = 0.5erfc\left(\frac{Q_r}{\sqrt{2}}\right) \qquad (2.1)$$

Where Q_r^2 is,

$$Q_r{}^2 = \left(\frac{(V_p - V_d)^2}{<n_0(t)^2>}\right) \qquad (2.2)$$

In the equation 2.2 above, $< n_0(t)^2 >$ is the mean square receiver output noise, V_d is the receiver output at the threshold crossing time t_d, and V_p is the peak receiver output at time t_p [32].

Wrong-slot error where, due to noise, the rising edge of the pulse is shifted into either the preceding or following slot, (the impact of this is pattern dependent). It occurs when noise on the leading edge of the pulse produces a threshold crossing in the time slot immediately preceding or following that containing the pulse. The probability of a wrong slot error,P_s, is given by

$$P_s = erfc\left(\frac{Q_s}{\sqrt{2}}\right) \qquad (2.3)$$

Where Q_s^2 is,

$$Q_s{}^2 = \left(\frac{t_s}{2}\right)^2 \left(\frac{1}{<n_0(t)^2>}\right)\left(\frac{dV_0(t)}{dt}\Big|_{t_d}\right)^2 \qquad (2.4)$$

and t_s is the slot time [32]

False-alarm error, where, due to a positive noise spike, the detection threshold is crossed in an empty slot that, depending upon the actual slot, may lead to a decoding error. It occurs when noise causes a threshold violation in a slot in which no pulse is present. The probability of this happening in a given timeslot is

$$P_f = \frac{t_s}{\tau_R} erfc\left(\frac{Q_f}{\sqrt{2}}\right) \quad (2.5)$$

Where Q_f^2 is,

$$Q_f{}^2 = \left(\frac{(V_d - V_{oISI})^2}{<n_0(t)^2>}\right) \quad (2.6)$$

$\frac{t_s}{\tau_R}$ is the number of uncorrelated samples per time slot and is the time at which the autocorrelation function of the receiver filter has become small [32].

2.4 Maximum Likelihood Sequence Detection (MLSD)

Applying Maximum Likelihood Sequence Detection (MLSD) techniques [40] to non-directed, indoor, FSO channels has been considered in recent work [18, 24, 26-27, 33], because sequence errors result from the large degree of Intersymbol Interference (ISI) introduced by these channels. In an MLSD scheme, only certain words or sequences are used for data transmission. At the receiver, the detected data word is compared to all valid words to find a match. If noise and ISI corrupt the received word so that it is invalid, the MLSD decoder determines the most likely word and uses that to generate the decoded data. Sibley [18] showed for dicode PPM system that using MLSD algorithm completely eliminates wrong-slot errors, and reduces the effects of false alarms and erasures.

MLSD has also been considered and applied to other modulation codes operating over free space channels, such as differential PPM [16], Pulse-Interval Modulation (PIM) and Dual-Header PIM (DH-PIM). Simple alternatives to MLSD such as Trellis-coded modulation and decision-feedback equalisation [41-42] have also been proposed but MLSD is very simple to implement thus simplifying decoder design.

Sibley showed that implementing a novel MLSD algorithm in dicode PPM system, operating over dispersive medium such as graded-index POF (GI-POF), with a wide-bandwidth receiver and classical matched filter corresponds to a 12.2 dB increase in sensitivity compared to a dicode PPM system without MLSD.

2.5 Channel Bandwidth and Attenuation Characteristics

In optical communications links, the optical fibre provides the transmission channel. The fibre consists of a solid cylindrical core of transparent material, surrounded by a cladding of similar material [42]. Light waves propagate down the core in a series of plane wavefronts i.e. modes. For this propagation to occur, the refractive index of the core must be larger than that of cladding and there are two basic structures which have this property: Step-Index (SI) and Graded-Index (GI) fibres. Multi-mode (MM) fibres allow many modes to propagate and single-mode (SM) fibres only allow one mode to propagate. Step-index types are generally available as both MM and SM fibres; although graded-index fibres are normally MM, some SM fibres are available. The three fibre types, together with their respective refractive index profiles are shown below in figure 2.5 [43]. In the figure, n is refractive index of the material, the cross-hatched area represents the cladding, the diameter of which ranges from 125 μm to a typical maximum of 1 mm. The core diameter can range from 8 μm, for some fibres, up to a typically 50 μm for large core MM fibres.

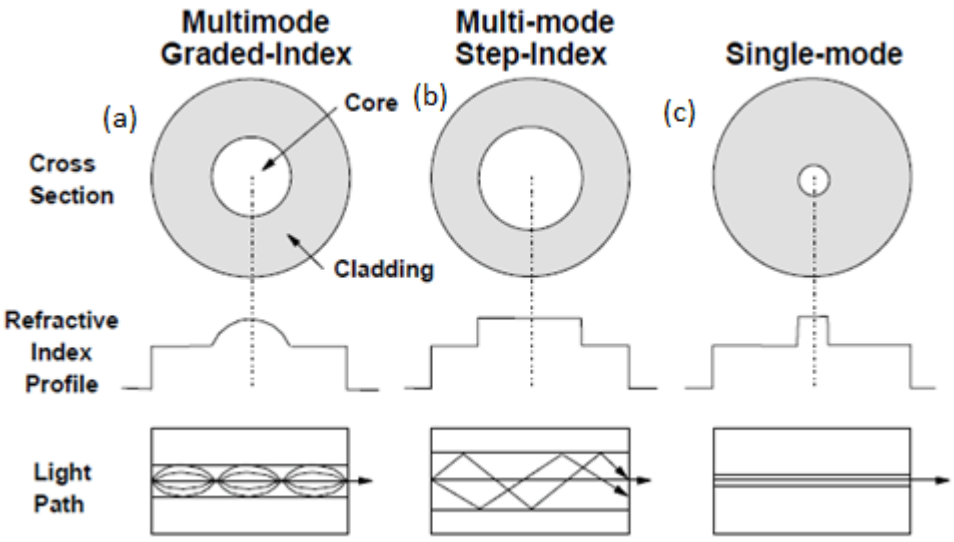


Fig. 2.5: Typical refractive index profiles of (a) graded-index multimode, (b) step-index multimode-mode, and (c) step-index single mode fibres.

Nowadays most of the optical fibres in use are made of either silica glass (SiO_2) or plastic/polymer. The change in refractive index, between the core and cladding, is achieved by the addition of certain dopants to the glass; all-plastic fibres use different plastics for the core and cladding. All-glass, SM fibres exhibits very low losses and high bandwidths, which make them ideal for use in long-haul telecommunications routes. Unfortunately such fibres are expensive to produce and so they are rarely used in short-haul (less than 500m length) industrial links.

The fibres with large core, for use in medical and industrial applications, and also for home and office networking nowadays, are generally made of plastic, making them more robust than all-glass types and much cheaper to manufacture. However, the very high attenuation and low bandwidth of these fibres tend to limit their use in communications links. Medium-haul routes, between 500 m and 1 km lengths, generally use plastic cladding/glass core fibre, otherwise as Plastic Clad Silica (PCS). All-plastic and PCS fibres are almost exclusively step-index, multi-mode types.

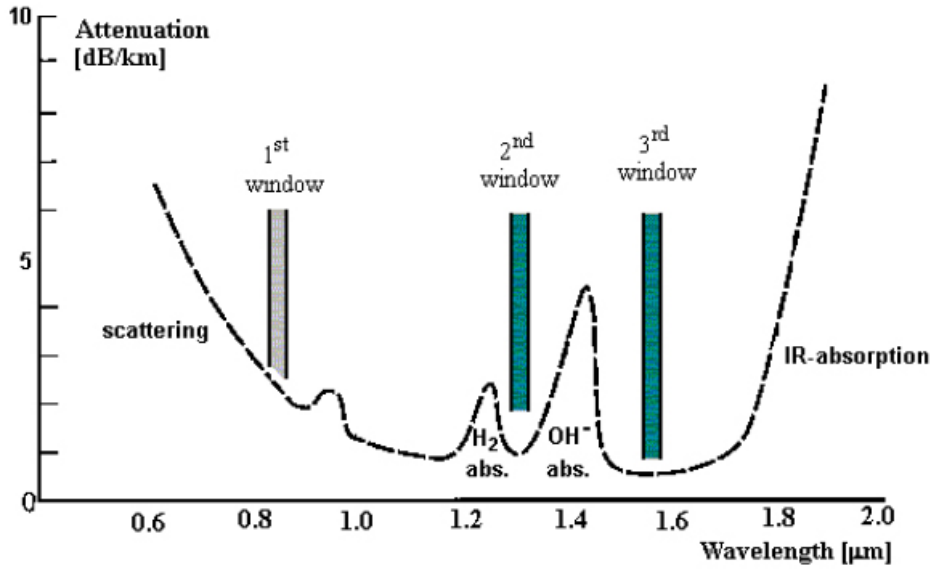


Fig. 2.6: Attenuation and wavelength characteristic of a silica-based glass fibre [42].

The attenuation and bandwidth of an optical fibre determines the maximum distance that signals can be transmitted. Attenuation is usually expressed in dB/km, while bandwidth is usually quoted in terms of the bandwidth length product, which has units of GHz km, or MHz km [42]. Attenuation also depends on impurities in the core and so the fibre must be made from very pure materials. To some extent bandwidth also depends on the core impurities; however the bandwidth is usually limited by the number of propagation modes. This explains why single SM fibres have a very large bandwidth.

2.6 Plastic Optical Fibre (POF)

All-plastic fibres are exclusively of the MM step-index type with large core and cladding diameters. These fibres are usually cheaper to produce and easier to handle than the corresponding silica-based glass variety. However, their performance (especially for optical transmission in the infrared) is restricted, giving them limited use in communication applications. All plastic fibres, however, generally have large numerical apertures which allow easier coupling of light into the fibre from a multimode source [42-43]. Early plastic fibres fabricated with a Polymethyl Methacrylate (PMMA) and a fluorinated acrylic cladding exhibited very high losses but with subsequent development in the fabrication process losses as low as 110 dB/km were achieved in the visible wavelength region. These all-plastic fibres exhibit both intrinsic and extrinsic loss mechanisms including Rayleigh scattering which results from density fluctuations and the anisotropic structure of the polymers.

In recent years, there has been increasing interest for using perfluorinated graded-index (GI) POF (PF-GI-POF) for high-speed ≥10-Gb/s short-reach applications such as low-cost interconnects in data centres, local area networks (LAN), and supercomputers. For such

applications, MM fibres (MMF) are preferred above SM fibres (SMF) due to their large core diameter and numerical aperture. Especially the PF-GI-POF, with core diameters of 50-62.5µm up to 120 µm, is very attractive for such applications. Due to the large alignment tolerances in transceiver components and fibre splices, the PF-GI-POF is attractive for in-building networks as its installation is easy and low cost [44-45].

Plastic-clad fibres are multimode and have either a SI or a GI profile. They have a plastic cladding (often a silicone rubber) and a glass core which is frequently silica. The PCS fibres exhibit lower radiation-induced losses than silica-clad silica fibres and, therefore, have an improved performance in certain environments.

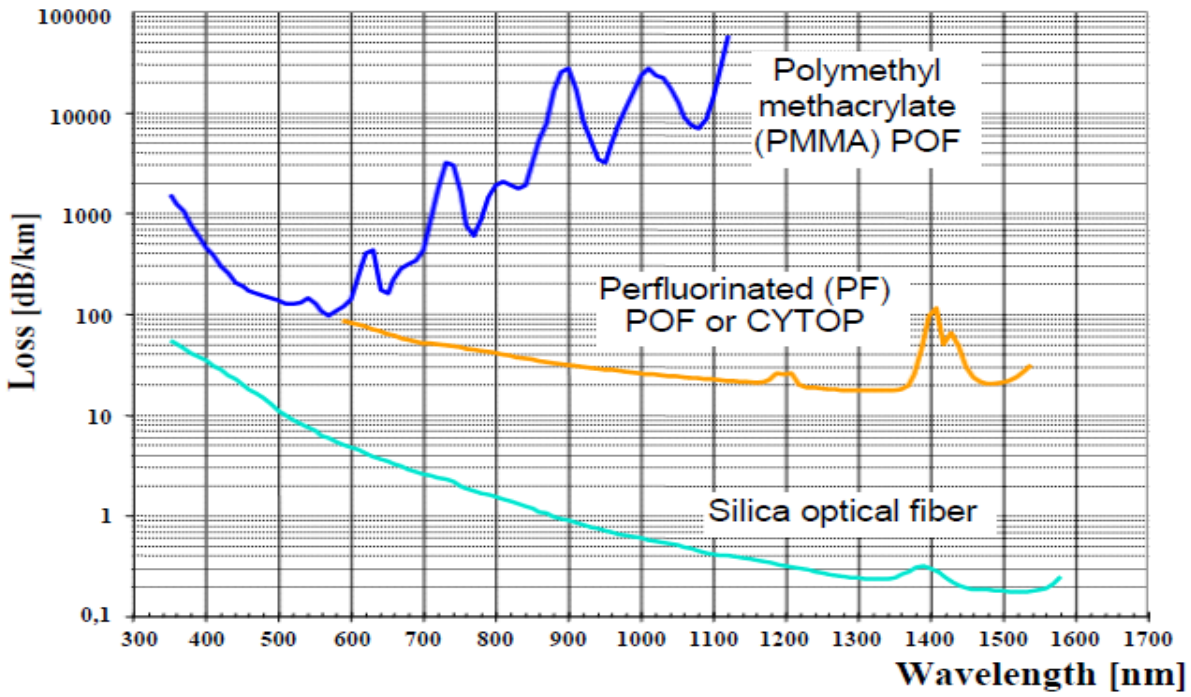


Fig. 2.7: Attenuation characteristics of POF and silica fibre [46].

In PCS fibres, the main absorption peaks are due to the O-H bond resonance, identical to all glass fibres, and the C-H bond resonances are due to the plastic cladding. The net result is that

PCS fibres exhibit a transmission window at 870 nm with a typical attenuation of 8 dB/km, so PCS links can use relatively cheap near infrared light sources. In view of the relatively low attenuation, and the fact that PCS fibre is SI MM, most PCS links are dispersion limited rather than attenuation limited. All-plastic fibres exhibit very high attenuation due to the presence of C-H bonds in the core materials. These bonds result in a transmission window at 670 nm, with a typical attenuation of 200 dB/km. As well as the high attenuation peaks caused by the complex C-H bonds, there's a large amount of Rayleigh scattering in all-plastic fibres. This is due to scattering from the large chain molecules that make up the materials. Although plastic fibres exhibit very low bandwidth-length products and very high attenuation, there is considerable interest in using such fibres for localised distribution systems and computer installations [42].

2.7 Potential Future Applications of the Research

DuoPPM operates at only two times faster than that of the original PCM data rate [26], thus reducing the bandwidth, making it a potentially attractive coding scheme for plastic optical fibre (POF) which suffers from low bandwidth; and high dispersion and attenuation because of the material [42-46]. Due to significant research and development in the material and fabrication of POF, it is fast becoming a consumer product, with applications such as low-speed, short distance (up to 100 meters) home media appliances, home networks, industrial networks, car networks, VoIP, IPTV, HDTV where the requirement for a relatively high-speed central distribution network inside buildings and homes is emerging. Siemens AG (2007) [46] claimed to successfully achieve 1 Gbit/s data rate over POF for 100 meter long distance using quadrature amplitude modulation (QAM). This claim may prove to be significant as it proves that with the rapid development in POF material and related technologies, it can achieve

sufficiently high bandwidth to cater for increasingly high speed consumer demands. The authors propose that further bandwidth reduction is achievable by combining duo-binary coding technique, first invented by Lender [47-50] in 1963, with dibit PPM. Sinsky et al (2005) [10] presented that high-speed data transmission is achievable using this three-level correlative coding technique by reducing bandwidth of transmission. Using similar technique shown by Cryan and Sibley (2006) [32], by moving from slope detection to central decision detection, dibit PPM receiver can be significantly simplified with equivalent sensitivity performance in the higher fibre bandwidths and considerably improved performance at lower bandwidths.

As discussed earlier, today plastic fibres are mostly used for very-short distance communication systems, such in a car. One of the main advantages of plastic fibre is ease of connection but it has yet to prove itself in terms of cost, bandwidth, and attenuation and long term thermal stability. General Motors and Daimler-Chrysler are developing plastic fibre-based automotive radio, video and data distribution systems such as D2B (domestic digital bus) for use in cars, the next generation of aircraft may opt for plastic fibre for rear-back video distribution. Any use of optical fibre in an aircraft offers massive weight saving over the equivalent copper cable solution [7, 45].

There is considerable interest in using POFs for localised distribution systems and computer installations. Due to the large alignment tolerances in transceiver components and fibre splices, the PF-GI-POF is attractive for in-building networks as its installation is easy and low cost; they are also commonly used for much higher-speed applications such as data centre wiring and building LAN wiring. Faster and more cost effective industrial automation and distribution networks can also be realised with POFs.

As the number of new services offered is increasing rapidly, such as VoIP, IPTV and HDTV, the need for a central distribution network inside buildings and homes can be effectively catered for using POFs. These networks will ideally combine large bandwidth with robustness, easy installation and cost effectiveness. This network should not only be able to distribute various new services, but also traditional ones such as CATV, voice telephony, high-speed internet, etc., making transparency also an important issue to consider. Particularly, plastic optical POF is attractive because it is easy to install due to its large core diameter. Moreover, POF offers large flexibility and ductility, which further reduces installation costs in often less accessible customer locations. The large diameter of POF allows relaxation of connector tolerances without sacrificing optical coupling efficiency. This simplifies the connector design and permits the use of low cost plastic components [44].

2.8 VHDL Programming and Design Methodology

It has been stated in section 1.3 that one of the key goals of the research is to develop the required system using VHSIC Hardware Description Language (VHDL), and implement the designs on to a Field Programmable Gate Array (FPGA) thereafter. Therefore, this section briefly describes the need for HDLs, design methodologies and hierarchies used to reduce complexity in VHDL, different VHDL models; and the design methodology used for this project in particular.

2.8.1 Designing on Multiple Levels

VHDL does not restrict the designers to use the same design level at all times unlike some other HDL software that are currently available commercially. The HDL designs are achievable on multiple levels and depending on the size, complexity or any other given requirements and specifications required and dictated by the designs, a system designer can choose to work on any level that fits. The key levels of design available in the VHDL are given below [51].

- System level.
- Algorithmic, or behavioural level.
- Data flow, or Register Transfer (RTL) level.
- Gate level.
- Switch, or transistor level.
- Electrical, or continuous mode (integral-differential) level.

2.8.2 VHDL Design Management

VHDL has clear and well defined design management structure that is easy to follow and intuitive in nature. It satisfies all the requirements of complex designs such as this DuoPPM system with highly structured design management. A VHDL design management structure is shown in the figure 2.8 below [51].

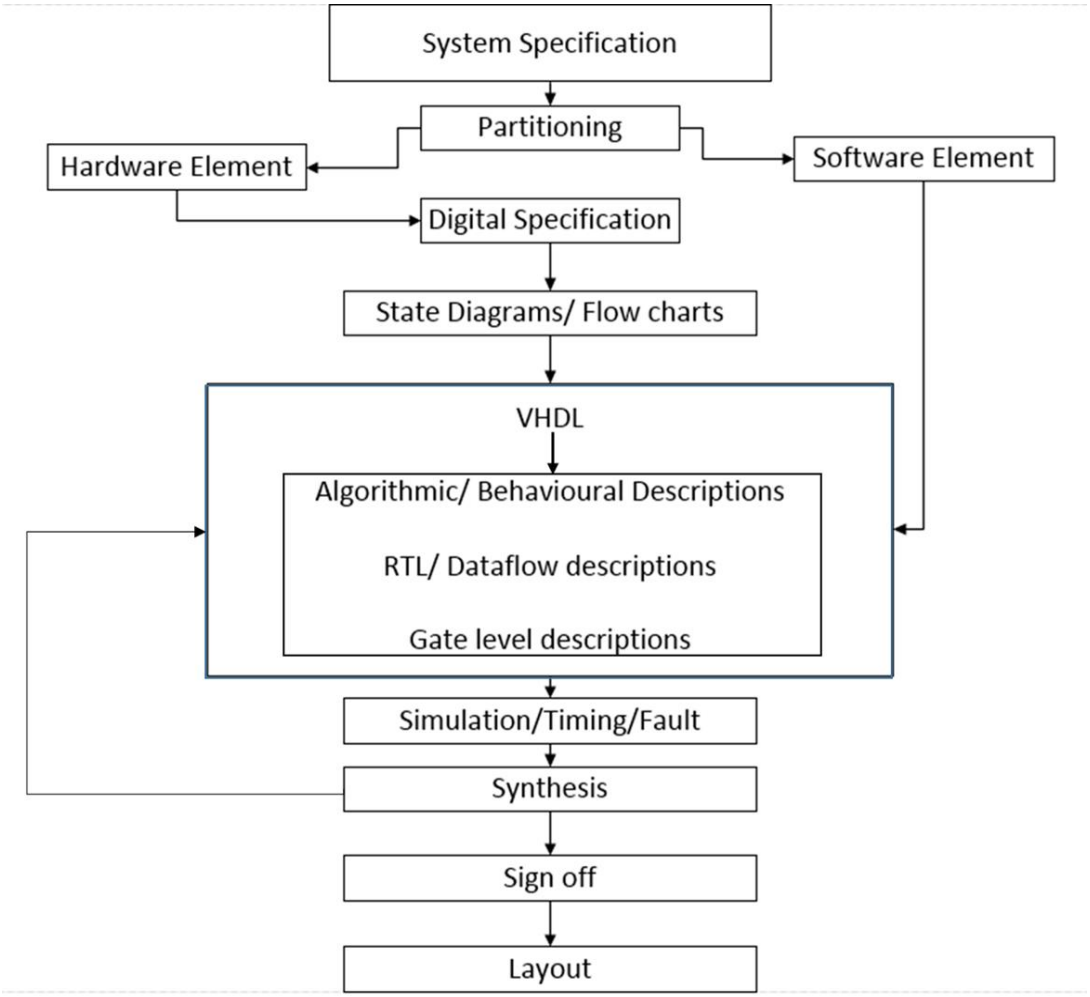


Fig. 2.8: Design structure flow diagram of VHDL capabilities.

It is clear from the diagram above that there is support for both hardware and software capabilities on equally structured level and every aspect of a design is separated thus making design changes and debugging simpler tasks.

2.8.3 Design Methodology

Both top-down and bottom-up design methodologies are available in the software design process. Top-down design flow of VHDL (shown in figure 2.9[7] [52]) will seek to solve the problem by deconstruction from system level to gate level, or electrical, or continuous mode (which could include layout), whereas bottom-up design will seek to solve it by building up the system in reverse manner to that of top-down flow or, in extremis, from level 6 (full custom design).'This project has been completed using top-down methodology. As Sjoholm & Lindh [51-52] mention that the design methodology which most people now given prominence to and try to follow is top-down. Bottom-up approach to the design could also be implemented depending on the design of the circuit. Following are the few key advantages of the top-down design methodology.

- It can handle significantly complex designs.
- Due to built-in features the designs times are significantly reduced.
- Increased quality of the designs.
- Rapid prototyping with FPGA is a very attractive feature.
- Recyclability is increased.

Verification of designs are also integrated in the top-down design flow structure in VHDL and they are as follows:

- Behavioural model.
- Register Transfer Level (RTL) VHDL model
- Gate level both before and after layout.

[7] Figure 2.9 is in the following page.

The component can be verified as follows in all three of the above verification steps that has been mentioned previously by using the following methods that are readily available in the software package:

- Creation of test vectors in the simulators internal language.
- VHDL testbench creation.
- System level simulation.

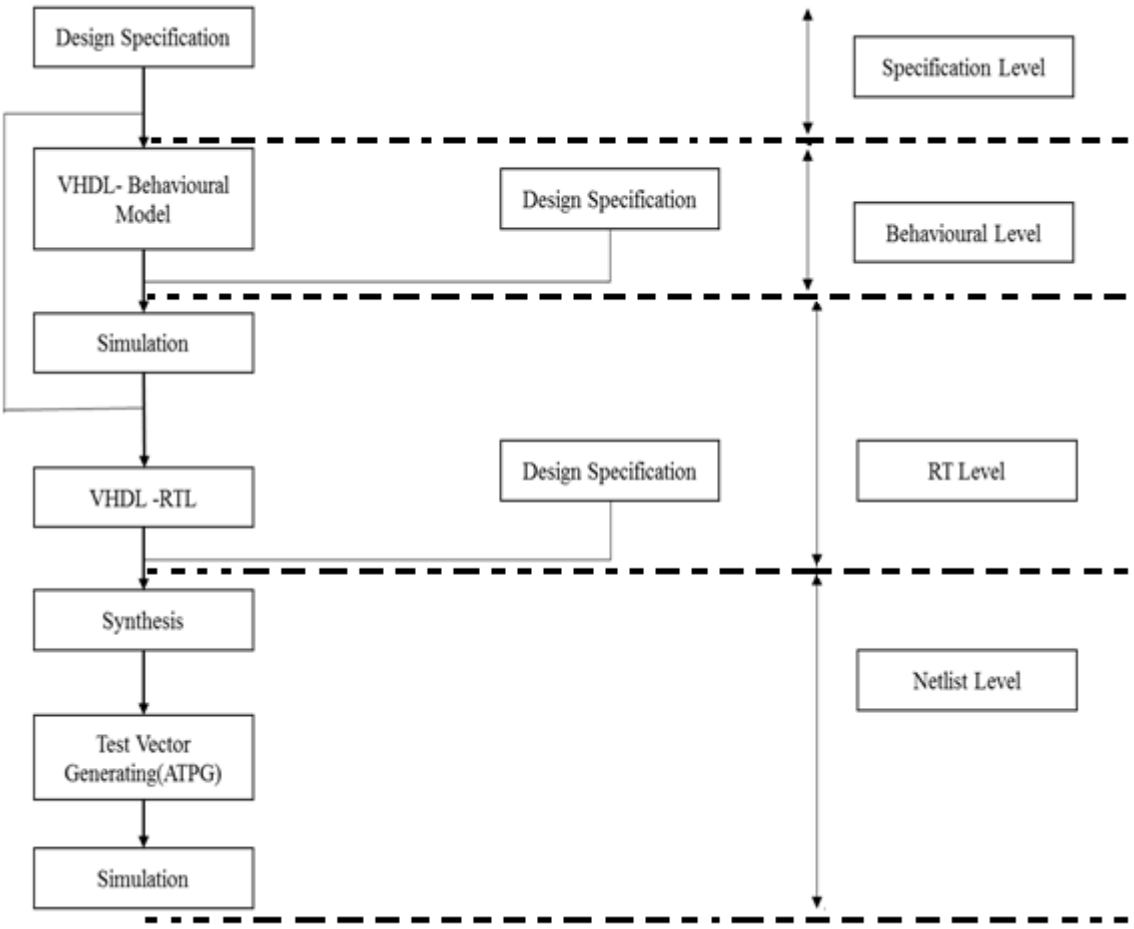


Fig. 2.9: Top-down design flow of VHDL design methodology.

2.8.4 Program Model and Simulation Choices

A general design model of VHDL programming design code can be described by the figure 2.10 below.

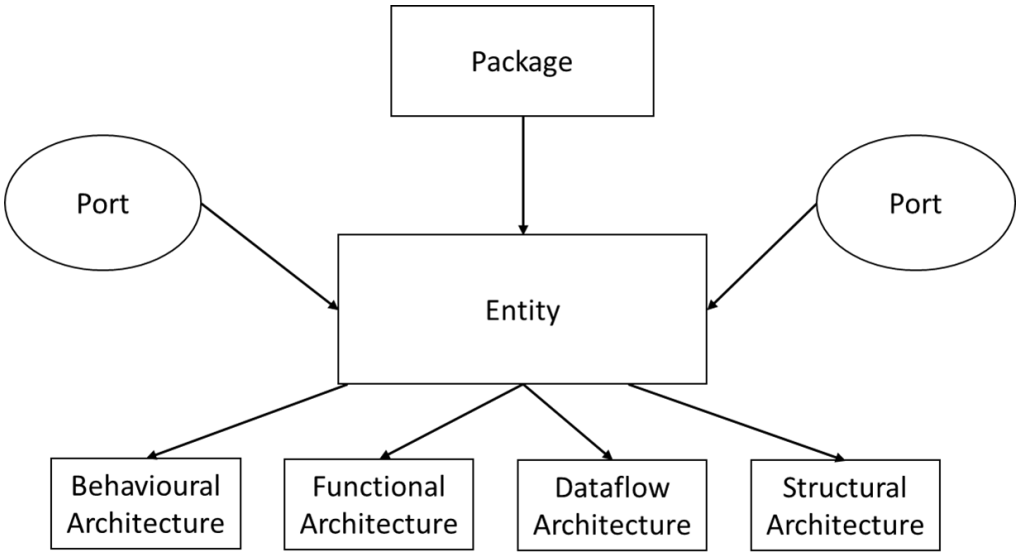


Fig. 2.10: Standard VHDL model of programming designs.

After completion of designs on either HDL level or Schematic, the design can be very easily verified in VHDL using input and output vectors for both functional and timing simulation that are necessary. State of internal signals and registers can also be observed in order to optimise the design to the required pre-defined specifications. There are two levels of simulations available in VHDL.

- High level simulation: provides information about functionality.
- Low level simulation: determines detailed information about timing. But these simulations are much slower.

To avoid high costs of low level simulation, high level simulations should be used to detect design flaws as early as possible. VHDL supports these multi-level simulations.

2.8.5 Key Advantages of Using VHDL Package

Some of the main advantages of using VHDL can be described by the points below [52]:

- Public availability: VHDL developed under US. Government contract, IEEE standard, government has interest in maintaining VHDL as a standard.
- Supports many methodologies: top-down, bottom-up, library based.
- Technology independent: i.e. CMOS, NMOS, but a design can be forced to a technology or process.
- Range of descriptive levels: behavioural to gate, so the same component can be described and simulated at different levels.
- Design exchange: as a standard components can be sub-contracted out.
- Large scale design and reusability: similar to programming languages. Multiple mechanisms to support design hierarchy.
- Versatile design reconfiguration support.
- Support for multiple level of abstractions.

2.9 FPGA Development Kits

2.9.1 Quartus II: Integrated VHDL Development Environment

Altera© Corporation[8] are pioneers of developing educational, research and industrial level FPGA development software and hardware [53]. The Quartus II software range developed by Altera has wide range and variety of VHDL and Verilog software and hardware development capabilities and is extensively used worldwide for various purposes. All levels and abstraction of VHDL design and methodology have been made possible in a simple manner in the Quartus II software package. There are a number of versions of Quartus II software are available as they have been through numerous development stages of the software. The versions vary depending on the support of FPGA in the design development process.

As the company develops FPGAs, they have the capability to modify and alter their software development environment to cater for them. There is a wide range of FPGAs to choose from providing all kinds of designs solution from semi-custom to full-custom application-specific integrated circuit (ASIC) designs. FPGAs differ in the number of logic gates available, PLL modules, operating frequency and speed, various integrated features that can be utilised for a complete design solution, interface blocks available on chip and many more. Therefore, it is up to the system designer to choose according to the specifications and choose the FPGA and development software wisely. Budgeting costs for any enterprise are vital and choice of wrong FPGA and design development can signify the difference between project success and failure.

[8] Altera, Terasic and Quartus are registered trading names for the companies and software mentioned.

2.9.2 DE2-115 FPGA Development Board

Altera© Corporation is collaborating with Terasic Inc. to develop the FPGA development boards for educational and research purpose [54-56]. There is a wide variety of development kits available with various different FPGA solutions. This project has used the DE2-115 board which satisfies the budget and requirement of the research. The board layout with key features identified is given in the figure 2.11 below [56].

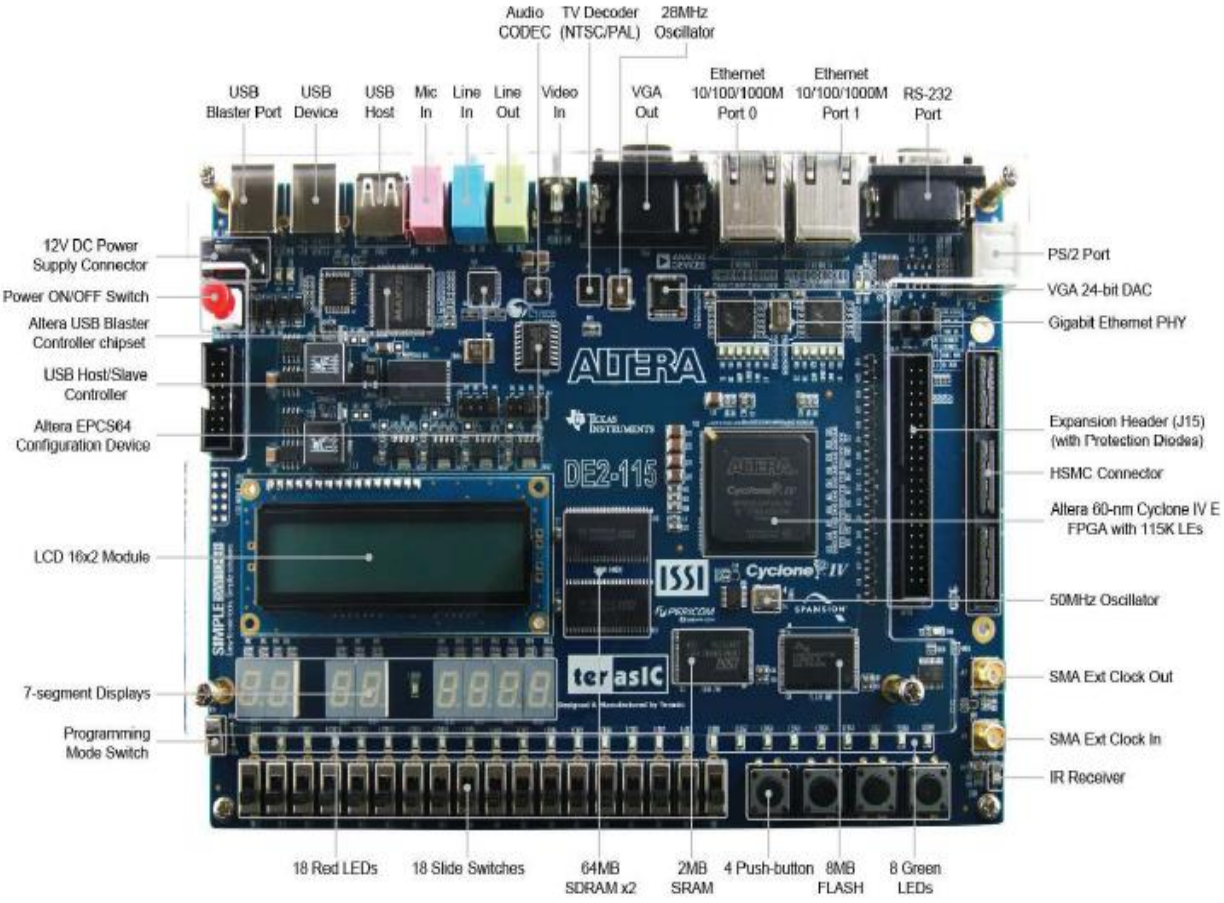


Fig. 2.11: DE2-115 Terasic FPGA development board layout [56].

The key features of the DE2-115 board that was considered for this project can be identified as given below [56]:

- Cyclone® IV EP4CE115 FPGA.
- 4 general purpose PLLs.
- SMA I/O Clock interface pins.
- 528 User I/Os including GPIO, HSMC, LCD and Switches.
- 50 MHz on-board clock.
- Configurable I/O standards (Levels: 3.3/2.5/1.8/1.5V).

There are many more key features available as well such as capabilities of adding various daughter boards using the HSMC I/O interface module for many types of designs. Current daughter cards available for the board are:

- HDMI Receiver card.
- HDMI Transmitter card.
- Card for video and image processing applications.
- AD/DA data conversion card.
- Transceiver channel connectors.
- Multi-touch LCD module for touch-screen application development.
- TV encoder and decoder capabilities.
- Sensor adaptor card.
- 5-megapixel digital camera package just to name a few of the additional features available.

2.10 Optical Fibre Links and VCSEL Transceiver Design

2.10.1 Optical Fibre Link Characteristics

A typical optical fibre link can be illustrated by figure 2.12 below.

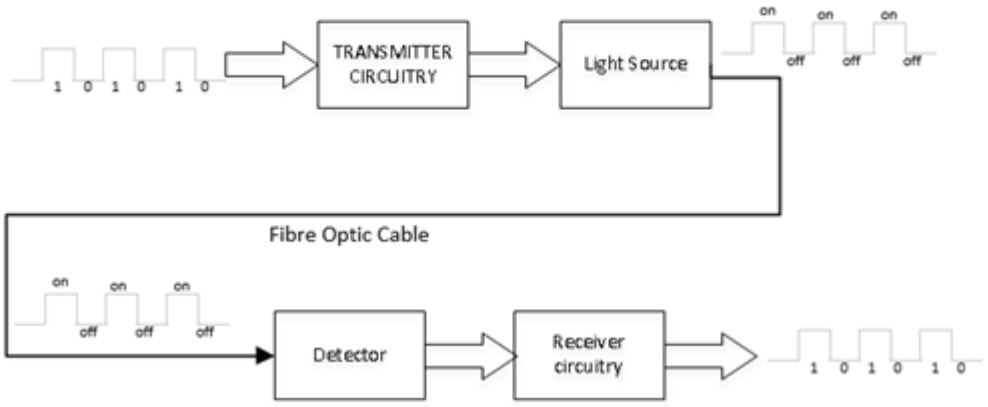


Fig. 2.12: A simplified optical fibre link.

It is clear from the figure above that, after the channel coding has been completed [11-12, 57-58], the next stage is to transmit the data using the light source. A light source usually either a Light Emitting Diode (LED) or LASER (Light amplification by stimulated emission of radiation)[9]. The light sources come in various wavelengths thus their dispersion characteristics vary as well [59-60]. The laser is particularly suitable for optical fibre communication as the fibre diameter is in µm range and the wavelength of the laser is suitable for this purpose. It makes laser coupling with fibre easier and significantly less coupling loss. LEDs usually have diffused light therefore if coupled with small fibre cores there will be a significant amount of light loss during coupling which makes the LED unsuitable for optical fibre communications [61]. However, in recent years some improvement has been made in LED technology which contributed to RC-LED (Resonant Cavity – LED) of 650 nm wavelength which has been used

[9] Commonly known as laser and will be denoted as 'laser' from hereafter.

for POF of higher core diameter as a cheaper alternative to laser. This is most notably used for short distance dispersive channels in MM fibres. However, as has been discussed earlier, the MM POF technology has significantly improved thus it is more widely used than before. VCSEL (Vertical Cavity Surface Emitting Laser) of 850 nm wavelength is now mostly replacing the use of RC-LED in POF links.

Glass fibre links very commonly use lasers of 1.3 µm and 1.55 µm wavelength [61-62]. The choice of laser for such links mainly depend on power budget and the link characteristics. Three dispersion characteristics of the links: material, modal and wavelength dispersion need to be taken into account when deciding on the choice of either light source or channel or both. The main reason of operation at 1.3 µm is that single-mode (SM) fibres are optimised for operation of 1.3 µm wavelength where they exhibit zero-dispersion and SM fibres are the main contender when it comes to long-haul communication. However, research showed that [62] by modifying fibre design the zero-dispersion point can be shifted towards the 1.55 µm wavelength where lowest losses occur in silica based fibre.

The channel for the research will be a highly dispersive GI-POF channel thus VCSEL has been chosen over RC-LED as the most suitable light source with better coupling, lower diffusion and dispersion and the single mode capability. VCSEL also comes at 650 nm wavelength, however, the most appropriate for the research would be 850 nm VCSEL. As the figure 2.12 in the previous page showed, a photo detector is necessary at the receiver end along with suitable receiver circuitry.

Cyran et al. [11-14] proposed a simple APD (Avalanche Photodiode) based receiver system as shown in figure 2.13 below. APD combined with pre-amplifier, post amplifier and predetection filter makes up the receiver for the proposed receiver.

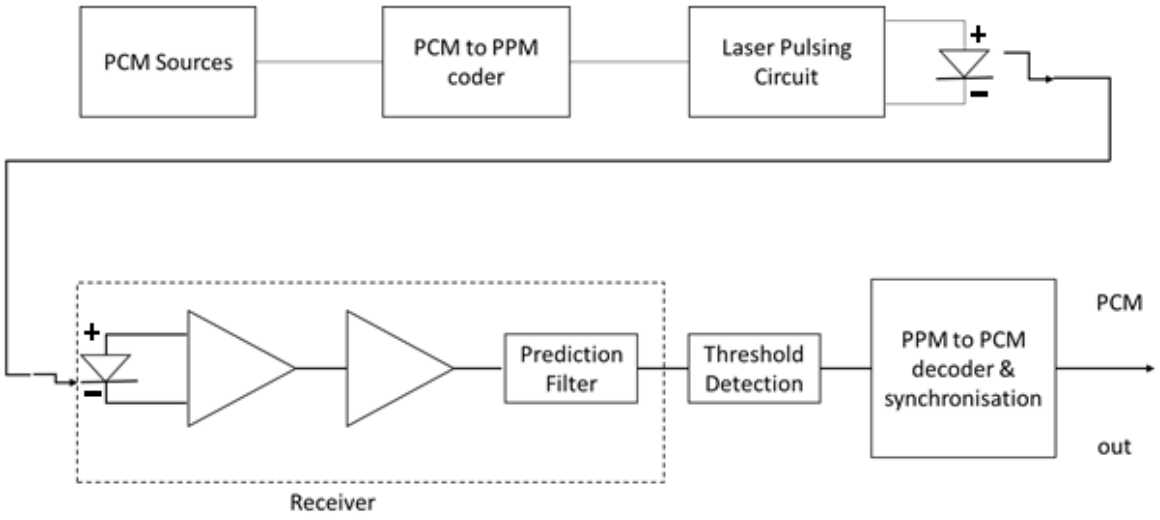


Fig. 2.13: Proposed digital PPM link diagram.

Neuhauser et al. [63] showed by design and implementation that low-noise and high-gain Si-bipolar transimpedance preamplifiers could be used for 10 Gbps data rate system in low cost optical fibre communications links.

2.10.2 VCSEL Based Transceiver Design

It has been discussed in the previous section that slowly the high-speed graded-index POF links are moving from LED based transceiver to VCSEL based transceiver. Siemens [46] has achieved gigabits data rate using VCSEL over POF in recent times. It also means that the use of POF is no longer limited to slower optical fibre data rates. Recent publications [65-67] have reported very high data rate achieved using POF and VCSEL in various conditions. Wipiejewski et al. [65] designed and manufactured VCSEL in visible red spectrums between 650 nm and 690 nm with a modulation bandwidth of devices in excess of 3 GHz and the output power is only limited by the eye-safety conditions. It has very high reliability in the 100,000 hours in operating use conditions. This is now a common trait of GaAs based VCSEL.

Polley et al. [66] have also published results of 10 Gbps VCSEL based transmission over 100m distance with large core graded-index POF. The experiments also demonstrates the VCSELs are very much compatible with highly alignment tolerant POFs. Park et al. [67] also showed simple medium data-rate 150 Mbps data rate is very easily achievable as well as high data-rate shown by the other publications. This bodes well for the early promise of the Duobinary PPM as claimed earlier that depending on applicable viability 10 Gbps data rate can be achieved with DuoPPM system. One key issue is that for a given wavelength of VCSEL, the receiver photodiode must be tuned to receive that particular wavelength for maximum optimisation [68-69]. However, as shown by Chang and Cordova [64] that it is also possible for a VCSEL based transceiver to communicate with existing LED based systems for hassle-free scalability which will also allow external electronic circuits to interact. Receiver designs are standard as any optical fibre links and there is a number of manufacturers currently producing packaged ICs, most notably Maxim Semiconductor, Analogue Devices and Avago Technologies.

2.11 Slot and Frame Synchronisation of PPM

Most of the optical PPM systems have self-extracting capabilities for clock recovery from the data frames that are being received [70-79] therefore no additional clock signals need to be associated with the data frame. Charitopoulos and Sibley [23] propose a slot and frame synchronisation for dicode PPM system. They have used a Phase-locked Loop (PLL) circuit in order to recover the timing information from the received data frame, with the use of a second-order PLL system which consists of a phase detector, an active low-pass filter, a voltage controller oscillator (VCO) and an amplifier. It has been shown that the clock can be reconstructed from the data, however, further investigation is needed in order to synchronise the recovered clock with the frame.

Elmirghani and Cryan et al. [76-79] have also previously investigated slot and frame synchronisation properties of digital PPM systems. They showed that in order to maintain frame and slot synchronisation, a scheme can be developed to generate phase bearing events. In general terms, it relies upon the presence of a pulse in the last slot of one frame followed by a pulse in the first slot of the next frame. This is a relatively simple method which can be achieved by adding two additional guard slots for extra pulses or modify the coding scheme to accommodate for two pulses. However, if no guard slots are used this is not possible to implement for Duobinary PPM because DuoPPM only consists of two slots in a frame and both are used for data pulses. In addition, DuoPPM intends to operate without any guard slots in order to maximise the bandwidth efficiency. Therefore, other forms of solution must be sought for the coding scheme. Although, dicode PPM can achieve clock recovery, effective frame synchronisation of the clock remains open for further development.

Various other investigations have gone into timing extraction in digital data transmission systems, especially in the domain of self-extracting clock [70-71] and also on the structure of the synchroniser [72-74]. It is fair to say that for most of these coding schemes, extracting the clock has not been of any major concern for designers, however, synchronisation with frames has been a significant issue, especially when no additional clock data has been sent. Gagliardi [72-73] presented a method which uses pulse edge tracking to feed the error signal to an oscillator running at the slot frequency. He also investigated the time synchronisation problem in PPM systems and proposed a method using a correlator to establish the error signal that corrects the oscillator.

2.12 Conclusions

In conclusion, literature review of the relevant topics has been presented in this chapter. Research with regards to original PPM and the channel coding schemes that have originated from the PPM such as digital PPM, multiple PPM, dicode PPM, offset PPM has been conducted, and findings are analysed and presented here for greater context and understanding. Advantages and disadvantages of the coding schemes that have been researched are analysed to develop understanding of how duobinary PPM will significantly improve the sensitivity and bandwidth utilisation in multimode dispersive plastic optical fibres. Typical error sources in PPM have also been investigated which is applicable for the project and the theories regarding the estimation of the probabilities of errors have been studied. POF channel bandwidth and attenuation characteristics have been researched along with VDHL hardware programming and FPGA implementation using VHDL to solidify key understandings. Optical fibre link designs, and slot and frame synchronisation of PPM have also been studied and presented in this section.

Chapter 3

Duobinary PPM Coding System

Duobinary PPM[10] has been proposed as a novel coding scheme which is the main focus of the research that has been carried out. This chapter will introduce the underlying theories of the DuoPPM coding scheme. A paper has been published [26] in IET Optoelectronics journal from the work done for this section. Therefore, there will be similarities between this chapter and the aforementioned publication.

3.1 Introduction to DuoPPM

DuoPPM, the subject of the research, is a novel coding scheme that combines the duobinary technique and digital PPM to form DuoPPM. In this signalling format, a signal is only transmitted when the data is constant at either logic one or logic zero and no signal is transmitted for data transitions from logic one to logic zero or logic zero to logic one – the change condition [26]. As will be shown later in chapter 3, the use of a novel MLSD technique allows for the elimination of wrong-slot errors and a reduction in the effects of erasure and false-alarm errors. In addition, DuoPPM achieves this performance with only a twofold increase in speed. Thus the increased sensitivity of digital PPM is made available without the adverse effects and added complications of excessive bandwidth expansion.

[10] The coding scheme will be called DuoPPM henceforth for the rest of the thesis for ease of reading.

3.2 DuoPPM Coding System

In the DuoPPM signalling technique, data transitions are coded into DuoPPM pulse positions as follows: a constant stream of data of logic zero produces a pulse in slot zero of the DuoPPM frame and a constant stream of data of logic one produces a pulse in slot one of the DuoPPM frame. No pulses are transmitted in the frame when the data is in transition from logic one to zero and logic zero to one (figure 3.1).

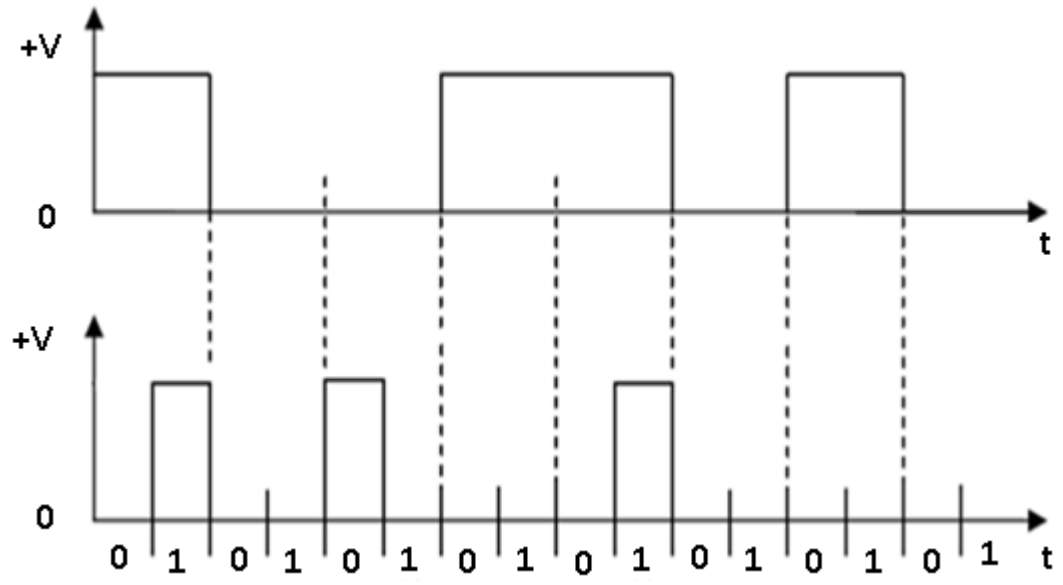


Fig. 3.1: Conversion of PCM data (top trace) into DuoPPM (bottom trace).

No guard slots are required for this coding scheme as the Inter-symbol Interference (ISI) will be significantly reduced by virtue of the inherent properties of the coding scheme. In addition, a novel MLSD and correction technique ensures that a particular error type can be completely eliminated. As can be seen from figure 3.1, the line rate is twice that of the original NRZ OOK data which is a considerable reduction in bandwidth expansion compared to digital PPM.

Table 3.1 below shows the DuoPPM signal representation.

Data	**Probability**	**DuoPPM**	**Symbol**
00	1/4	Pulse in slot 0	0
01	1/4	No pulse	C – change
10	1/4	No pulse	C – change
11	1/4	Pulse in slot 1	1

Table 3.1: DuoPPM coding and signal representations.

It can be seen from Table 3.1 that each symbol has a probability of 1/4. However, the DuoPPM no-pulse signal (C) occurs for both 01 and 10 sequences and therefore has a total probability of 1/2. Thus, the probability of a 1 occurring in the first instance is 1/4 and the probability of a subsequent C or 1 immediately following it is 1/2 (given that a 1 has occurred and the current coder state is one). Likewise, the probability of a 0 occurring initially is 1/4 and the probability of a C or 0 immediately following it is 1/2. If it can be assumed that the original PCM data is line coded so that the run of no-pulse signals (C) is limited to n, the maximum DuoPPM run would be 1, nC, 0/1. With this condition, the final pulse will be a 0 if n is an odd number or, if n is an even number, the final pulse will be a 1. This is because the coding technique dictates that a sequence will end with the same symbol as the first one if n is an even number, otherwise it will end with the opposite symbol (considering 0 is the opposite of 1 and vice versa). Some typical examples of valid DuoPPM sequences are 1C0, 0C1, 1CC1, 0CC0, 11, 00 etc.

3.3 DuoPPM Errors and Probabilities

Three sources of pulse detection errors affect PPM systems: wrong-slot, erasure and false alarm [11, 12]. The following sections develop expressions for the probability of these errors and discuss their impact on the error performance of DuoPPM.

3.3.1 Wrong-slot Errors

These errors occur when noise on the leading edge of a pulse can cause it to appear either before or after the current slot. This error is minimised if detection occurs at the centre of a slot of width T_s. Thus errors are generated when the edge moves by$|T_s/2|$. The probability of a wrong-slot error, P_s, is

$$P_{ws} = 0.5 erfc\left(\frac{Q_{ws}}{\sqrt{2}}\right) \tag{3.1}$$

where

$$Q_{ws} = \frac{T_s}{2}\frac{slope(t_d)}{\sqrt{< n_o{}^2 >}} \tag{3.2}$$

in which $< n_0{}^2 >$ is the mean square noise of the receiver, and $slope(t_d)$ is the slope of the received pulse at the threshold crossing instant, t_d. The threshold time is dependent on where the decision level is set on the received pulse. This form of error is present when the bandwidth of the link is low, thus giving a pronounced slope to the pulses.

3.3.2 Erasure Errors

Erasure error occurs when the noise is large enough to reduce the peak signal voltage to below the threshold level. The probability of an erasure error, P_{er}, is

$$P_{er} = 0.5 erfc\left(\frac{Q_{er}}{\sqrt{2}}\right) \tag{3.3}$$

where

$$Q_{er} = \frac{v_{pk} - v_d}{\sqrt{< n_o^{\,2} >}} \tag{3.4}$$

with v_{pk} being the peak signal voltage within the time slot at the output of the receiver and v_d is the threshold crossing voltage.

3.3.3 False-alarm Errors

Noise present in an empty slot could cause a threshold violation, or false-alarm error. The probability of this happening is

$$P_t = 0.5\, erfc\left(\frac{Q_t}{\sqrt{2}}\right) \tag{3.5}$$

where

$$Q_t = \frac{v_d}{\sqrt{< n_o^{\,2} >}} \tag{3.6}$$

v_d is the threshold crossing voltage. The number of uncorrelated samples per time slot can be approximated to T_s/τ_1 where τ_1 is the time at which the autocorrelation function of the receive filter has become small.

The probability of a false alarm error then becomes

$$P_f = \frac{T_s}{\tau_R} 0.5\, erfc\left(\frac{Q_f}{\sqrt{2}}\right) \tag{3.7}$$

where

$$Q_f = \frac{v_d - v_{ISI}}{\sqrt{< n_o{}^2 >}} \tag{3.8}$$

with v_{ISI} being the ISI-induced voltage in the empty time slot, caused by pulse dispersion in highly dispersive channels, leading to some signal voltage being present.

3.4 Equivalent PCM Data Errors in DuoPPM

In DuoPPM, a wrong-slot event can cause four possible errors. If the pulse is in the 0 slot, noise can cause the edge to appear in the preceding 1 slot or in the following 1 slot. In the case of a 0 pulse appearing in the following 1 slot, no detection error occurs as the pulse is still present in the 0 slot it will be detected correctly and for the edge appearing in the following 1 slot; it will not be detected as the decoder stops as soon as a pulse is received. However, a detection error occurs in the instance of a 0 pulse appearing in the preceding 1 slot of a C signal. This causes an immediate PCM error and the previous bit will also be in error but these errors will be completely detected and corrected using MLSD scheme shown in Table 2 ($1 \leftarrow 0$). In the case of a 0 pulse appearing in the preceding 1 slot of a 0 pulse (It is assumed that the probability of two errors occurring in a particular sequence is small) there will be no detection error as the 0 pulse will be detected first and the decoder will stop when a pulse is received thus no PCM errors will be generated.

Due to wrong-slot error a 1 pulse may appear in the preceding 0 slot or the following 0 slot. If the 1 pulse appears in the following 0 slot then the detection error is gives the same number of errors as $1 \leftarrow 0$ error and similarly it can be accurately detected and corrected using MLSD (Table 3.2: $1 \rightarrow 0$) thus there will be no PCM errors at the output of the decoder. In the instance of a 1 pulse appearing in the preceding 0 slot, a detection error will occur and this will cause an immediate PCM error, and all the following bits will be in error until a 0 (for odd number of C signal/0) or 1 (for even number of C signals) is received. If the number of the following C signals is *x*, then the number of PCM errors is $x + 1$. However, for $0 \leftarrow 1$, the effect of this wrong-slot error can be completely eliminated using MLSD similar to the other three possible wrong-slot errors as shown in the table 3.2 below.

$1 \leftarrow 0$	Transmitted	1	C	0	C	C	0	
	Received	1	**1**	0	C	C	0	Invalid sequence
	MLSD	1	C	0	C	C	0	error corrected
$0 \leftarrow 1$	Transmitted	0	C	1	C	C	1	
	Received	0	C	**0**	C	C	1	Invalid sequence
	MLSD	0	C	1	C	C	1	error corrected
$1 \rightarrow 0$	Transmitted	0	C	1	C	C	1	
	Received	0	C	1	**0**	C	1	Invalid sequence
	MLSD	0	C	1	C	C	1	error corrected
$0 \rightarrow 1$	Transmitted	1	C	0	C	C	0	
	Received	1	C	**1**	C	C	1	Invalid sequence
	MLSD	1	C	0	C	C	0	error corrected

Table 3.2: Showing the operation of the MLSD with wrong-slot errors. The symbol in error is shown in bold.

In a DuoPPM system, erasure of a 0 or a 1 pulse generates the same number of PCM errors and as previously mentioned, line coding results in a maximum number of consecutive C signals of *n*. With this condition, the PCM error probability for erasure is given by [2]

$$P_{erDuoPPM} = 2\left(\sum_{x=0}^{n-1}\left(1/2\right)^{x+3} P_{er}(x+1) + \left(1/2\right)^{n+2} P_{er}(n+1)\right) \tag{3.9}$$

Erasure of a 0 or a 1 pulse results in the change symbol C. This has the effect of generating an invalid DuoPPM sequence and so the MLSD acts to minimise the data error as in Table 3.3. The MLSD inserts a pulse of the correct polarity such that the sequences preceding and following the erasure event are valid. So, in the first entry in Table 3.3 – erasure of a 0 – the faulty sequence has eight C symbols between the 1 and 0. This is clearly at fault since the start and final pulses should be the same given an even number of C symbols. The MLSD detects the faulty sequence and inserts a 1 pulse as close to the centre of the run of Cs as possible. (As the MLSD has no information as to where the erasure has occurred, the mid-point in a run of Cs will yield the lowest error.) A similar mechanism occurs in the second example in Table 3.3 in which a 1 pulse is erased.

Erasure of 0	Transmitted	1	C	C	C	0	C	C	C	C	0
	Received	1	C	C	C	**C**	C	C	C	C	0
	Corrected	1	C	C	C	C	1	C	C	C	0
Erasure of 1	Transmitted	1	C	C	1	1	C	C	C	0	-
	Received	1	C	C	**C**	1	C	C	C	0	-
	Corrected	1	C	0	C	1	C	C	C	0	-

Table 3.3: Transmitted and received sequences with an erasure error.

In case of a false-alarm error, if a pulse is received in slot 0, a false alarm could occur in the following 1 slot but as the decoder stops when a pulse is received, no PCM errors will be generated. However, a detection error will happen if a false alarm occurs in the following string of C signals. The severity of the error depends on the position of the false alarm occurrence in a given sequence, as Table 3.4 shows. The false-alarm occurs on the *k*th C signal in a run of *x*C signals, and so the PCM error is ($x + 1 - k$) [2]. In this case, x must be greater than zero because when a 0 pulse is transmitted, a false-alarm error in the 1 slot has no bearing on the detection accuracy. A similar situation applies to false alarm errors with a 1 pulse. However, a false alarm could occur in the 0 slot immediately before the 1 pulse but the error will be detected and completely eliminated using MLSD the same as in 0 ← 1 wrong-slot error. Therefore, x must be greater than zero in this instance as well because when a 1 pulse is transmitted, a false-alarm error in the preceding 0 slot has no effect as the error will be eliminated. Thus the PCM error probability for both conditions is given by

$$P_{efDuoPPM} = 2\left(\sum_{x=1}^{n-1}\sum_{k=1}^{x}\left(1/2\right)^{x+3}P_f\left(x+1-k\right) + \sum_{k=1}^{n}\left(1/2\right)^{n+2}P_f\left(n+1-k\right)\right) \qquad (3.10)$$

The total equivalent PCM error probability is found by adding together equations (3.9) and (3.10) for DuoPPM. The performance criterion is that these error probabilities should be the same as for the PCM.

	Transmitted	0	C	C	C	C	C	C	C	C	0
FA of 0	Received	0	C	C	C	**0**	C	C	C	C	0
	Corrected	0	C	**1**	C	0	C	C	C	C	0
FA of 1	Received	0	C	C	C	C	C	C	**1**	C	0
	Corrected	0	C	C	C	1	C	C	1	C	0

Table 3.4: Transmitted and received sequences with a false-alarm error.

3.5 DuoPPM Receiver and Clock Extraction

In common with digital PPM, the optimum filter for a DuoPPM receiver consists of a noise-whitened matched filter and a PDD network, as shown in figure 3.2 below [26]. Following the PDD (Proportional Derivative Delay) network, a voltage comparator is used to slice the data and the resulting pulses are applied to a decoding logic circuit which is programmed according to appropriate decoding rules. To maintain frame synchronisation, a slot clock can be extracted from the data received and used to decode the DuoPPM signals, figure 3.3.

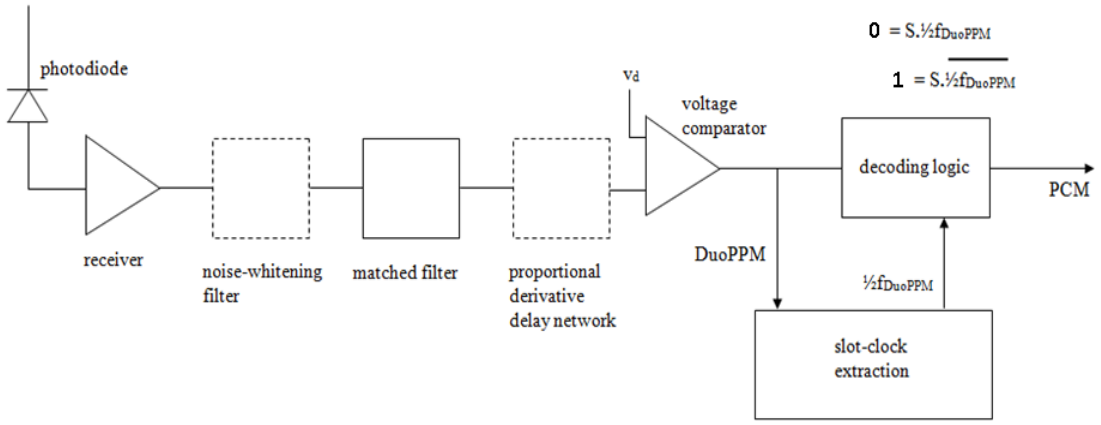


Fig. 3.2: Schematic of a DuoPPM receiver (The dashed boxes are optional).

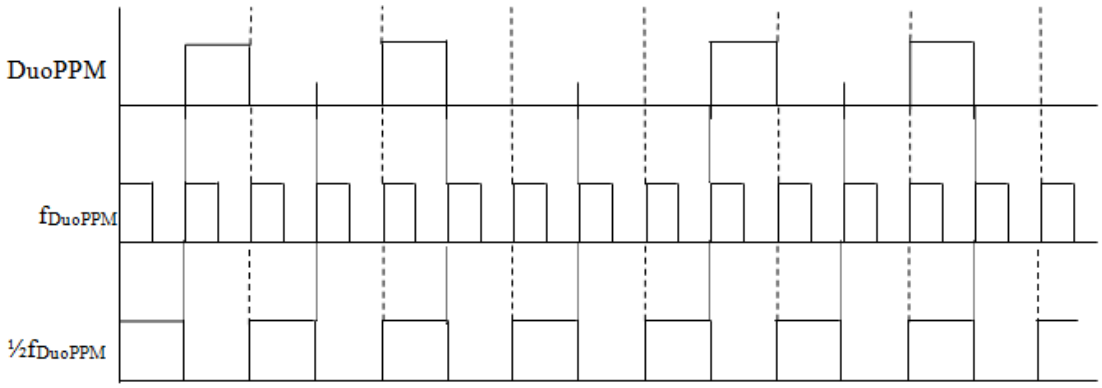


Fig. 3.3: Slot clock extraction timing diagram.

3.6 Conclusions

In conclusion, this chapter details the duobinary PPM coding scheme which is the main focus of the research that has been completed. The underlying theories of the coding scheme have been introduced in this section such as rules for conversion of PCM data into DuoPPM data, DuoPPM coding table and signal representations, errors and the probabilities of errors for wrong-slot, erasure and false-alarm errors. Mathematical representations of error probabilities of each type of errors have also been presented in this section. In addition, equivalent PCM data errors in DuoPPM coding system have been described and analysed in this section with the aid of tabulated examples of errors and how they can be detected and corrected using MLSD. This chapter also describes DuoPPM transceiver design and clock extraction methods briefly.

Chapter 4

Duobinary PPM Mathcad Simulation and Results

DuoPPM system has been theoretically modelled using Mathcad system simulation software[11] and results were gathered to make viable comparison of the performance between DuoPPM and other relevant coding scheme for feasibility study of the proposed coding scheme. Some of results and materials of this chapter have been published[12] thus some similarities may be noticed.

4.1 Mathematical Modelling of DuoPPM System

The optimum predetection filter for DuoPPM consists of a noise-whitened matched filter and a PDD network which can be removed if pulse dispersion is low [82]. In addition, if the receiver has a white noise spectrum over its bandwidth, the predetection filter becomes a classical matched filter and this system has been used for DuoPPM system modelling [2, 28 and 33].

Assuming the received pulse shape, $h_p(t)$, have the following property:

$$\int_{-\infty}^{\infty} h_p(t)dt = 1 \tag{4.1}$$

The impulse response of the channel (GI-POF) can be approximated to a Gaussian [81] and thus

$$h_p(t) = \frac{1}{\sqrt{2\pi\alpha^2}} \exp\left(-\frac{t^2}{2\alpha^2}\right) \tag{4.2}$$

[11] Please see appendix 2.1 for complete simulation file and appendix 2.2 for additional results.
[12] Please see appendix 1.1 for the publication.

The Fourier transform of the input pulse, $H_p(\omega)$, is given by

$$H_p(\omega) = \exp\left(-\frac{\alpha^2\omega^2}{2}\right) \tag{4.3}$$

The pulse variance, α, is linked to the fibre bandwidth by

$$\alpha = \frac{0.1874T_b}{f_n} \tag{4.4}$$

where T_b is the PCM bit time and f_n is the fibre bandwidth normalised to the PCM data rate, B, given by

$$f_n = \frac{f}{B} \tag{4.5}$$

The pulse shape of the classical matched filter presented to the threshold detector is

$$v_o(t) = \frac{b\eta q}{2\pi}\int_{-\infty}^{\infty} Z_{pre}(\omega)H_p(\omega)^2 \exp(j\omega t)\,d\omega \tag{4.6}$$

where b is the number of photons per pulse, η is the quantum efficiency of the detector, q is the electronic charge, $Z_{pre}(\omega)$ is the frequency dependent transimpedance of the preamplifier and $H_p(\omega)$ is the Fourier Transform of the input pulse. The solution to (4.6) is

$$\begin{aligned} v_o(t) = b\eta q R_T \frac{\omega_c}{2}\exp\left(\alpha^2{\omega_c}^2\right)\exp\left(-\omega_c t\right) \\ \text{x}\left[erfc\left(\alpha\omega_c - t/2\alpha\right)\right] \end{aligned} \tag{4.7}$$

where R_T is the mid-band transimpedance of the receiver and ω_c is the -3dB bandwidth of the receiver. The receiver noise appearing at the output of the matched filter is

$$< n_o{}^2 >= \frac{S_o}{2\pi}\int_{-\infty}^{\infty}\left|H_p(\omega)Z_{pre}(\omega)\right|^2 d\omega$$
$$= S_o\frac{\omega_c}{2}R_T{}^2\exp(\alpha^2\omega_c{}^2)\ erfc(\alpha\omega_c) \qquad (4.8)$$

where S_o is the double-sided, equivalent input noise current spectral density of the preamplifier, assumed white. It is also assumed that a PIN photodiode is used, and that its shot noise can be neglected. Equations (4.4), (4.5) and (4.7) have been used in the Mathcad simulations and calculations for Gaussian pulse shaping and approximating the variations of the received pulses. The code is provided in appendices 2.1 and 2.3. It can be seen from the aforementioned appendices that at the start of the model, the specifications for the simulations such as pre-amplifier bandwidth, noise at the preamplifier input, data rate, quantum energy, operational wavelength, pulse variation model, Gaussian pulse shaping, photon energy, timing and threshold detections, peak pulse amplitude are defined.

4.2 Evaluation of DuoPPM Performance

In common with Dicode PPM, a threshold level, v, was used as a system variable defined by

$$v = \frac{v_d}{v_{pk}} \qquad (4.9)$$

where v_{pk} is the peak voltage of an isolated pulse and v_d is the decision (threshold) voltage. The pulse shape and noise can be determined theoretically if the fibre bandwidth is known [2]. Simulations were performed to find the optimum value of v_d that gave the minimum number of photons per pulse, b, for a specified error rate of 1 in 10^9.

Since the simulation results are to be comparable to digital and Dicode PPM, identical system parameters were used to evaluate system performance. The original data was assumed to be

line-coded with a run length (n) of 10 and a data rate of 1 Gbit/s was used for the simulated system. A wavelength of 1.55 μm was chosen with a photodiode quantum efficiency of 100%. A receiver with a bandwidth of 10 GHz and white noise of 50×10^{-24} A^2/Hz was taken (see appendices 2.1 and 2.3).

The optical power for the digital PPM system, P_{DPPM}, can then be obtained from

$$P_{DPPM} = \frac{b}{M} h\upsilon B \tag{4.10}$$

where b is the number of photons in a single pulse, h is Planck's constant, υ is the optical frequency, B is the original bit rate and M is the level of coding (number of bits coded).

For the DuoPPM system, the average number of photons in a frame containing a pulse is b/2. As there are two frames containing pulses, each occurring with a probability of 1/4, the average number of photons is b/4. Thus the optical power required, $P_{DuoPPM,}$ is given by

$$P_{DuoPPM} = \frac{b}{4} h\upsilon B \tag{4.11}$$

Similarly, for Dicode PPM, $P_{DicodePPM,}$ is given by

$$P_{DicodePPM} = \frac{b}{4} h\upsilon B \tag{4.12}$$

For all aforementioned systems, sensitivity in dBm can be found by

$$\text{Sensitivity (dBm)} = 10 log_{10}(P * 10^3) \tag{4.13}$$

where P is the required optical power of the system.

The aforementioned equations for optical power calculations and sensitivity have been used in the Mathcad simulations to obtain the final sensitivities of the systems (see appendices 2.1 and 2.3).

4.3 Results and Discussion

Figure 4.1 (following page) shows the variation, with normalised fibre bandwidth, in the number of photons per pulse (b) required for an error rate of 1 in 10^9. These results were obtained by calculating the error probabilities obtained from the equations given in Chapter 3 and then applying the mathematical model in Mathcad to get the final error rate. The value of b was then adjusted to obtain the performance criterion of 1 error in 10^9 bits [26].

	Data rate 1Gbit/s	
	Sensitivity in dBm	
Normalised fibre bandwidth	$f_n = 1$	$f_n = 100$
DuoPPM	–34.6	-42.2
Digital PPM **7 level coding**	-25.9	-44.1
Dicode PPM	–33.4	–41.7

Table 4.1: Comparison of sensitivities for DuoPPM, Digital PPM and Dicode PPM at 1 Gbit/s PCM data rate.

As can be seen from table 4.1 above, all systems have similar performance, in terms of photons per pulse, at high bandwidths. However, as the bandwidth reduces (increasing dispersion) the digital PPM system requires significantly more photons per pulse to achieve the target error rate of 1 in 10^9. (In order to obtain the results for digital PPM, 7 level coding was used with a modulation index of 0.8.) This is due to high levels of dispersion causing the slope of the

received pulse to increase and this increases the error rate. The apparent resilience to dispersion presented by DuoPPM is, in part, due to the very nature of the code. In DuoPPM system, there exists a minimum of one no-pulse (C) signal between 1 and 0 signals, or vice-versa. This is fundamental to the code. Thus, in the low bandwidth region, the first pulse can spread into the adjacent C (no pulse and empty) slot so making the code more resilient to ISI.

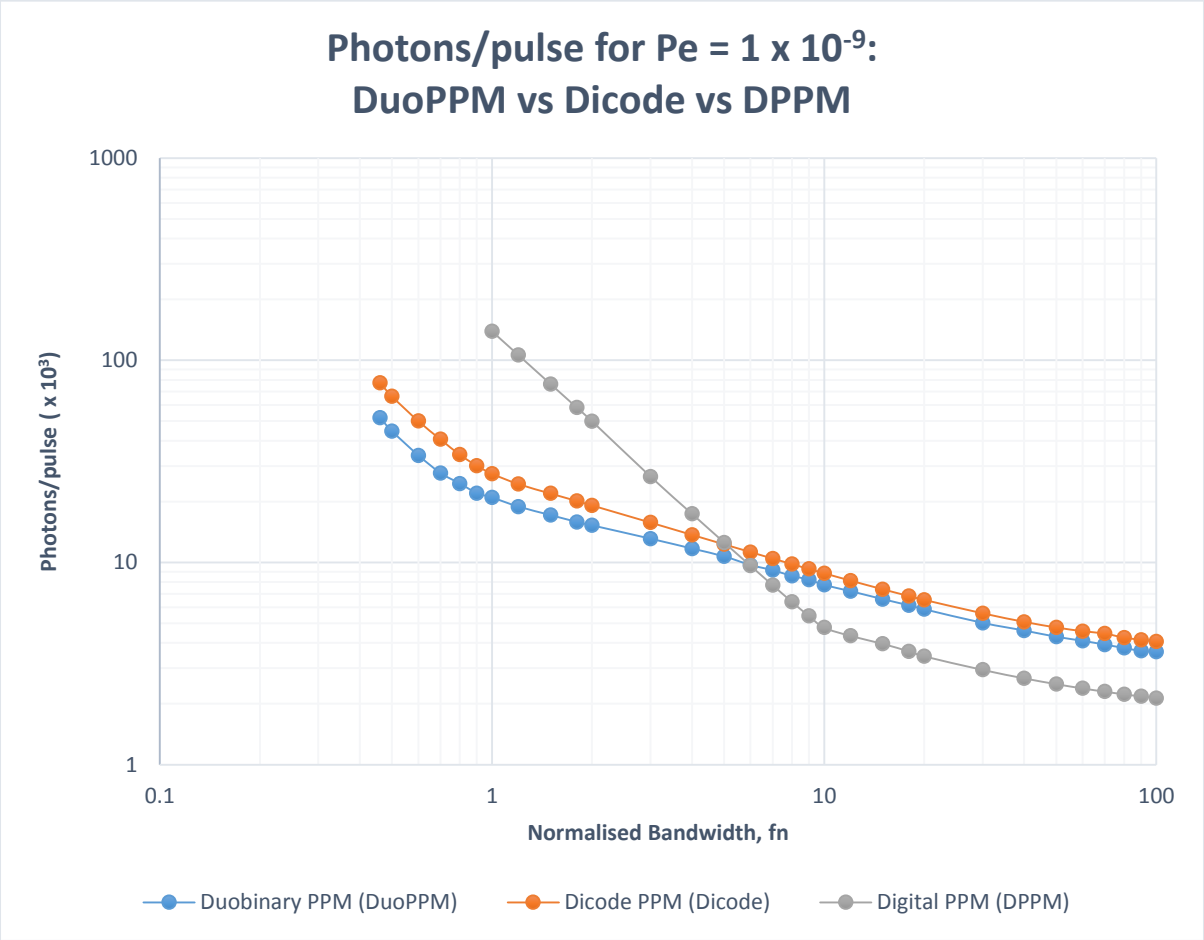


Fig. 4.1: Variation in photons per pulse with frequency normalised to bit rate, f_n, for Duobinary, Dicode and Digital PPM.

As previously mentioned, the sensitivity of digital PPM can be high due to the effects of a low mark:space ratio and figure 4.2 compares the sensitivities of DuoPPM, Digital PPM and Dicode PPM. Equations 4.11, 4.12 and 4.13 were used to obtain the average power.

Table 4.1, as shown earlier, summarises the results at high and low fibre bandwidths. As can be seen from figure 4.2 and table 4.1, Digital PPM out-performs DuoPPM by 1.9 dB at a normalised bandwidth of 100. However, as the bandwidth reduces, so does the advantage Digital PPM has over DuoPPM and Dicode PPM. Eventually, at a normalised bandwidth of 1, DuoPPM offers an advantage of 8.7 dB over Digital PPM. DuoPPM also offers an improvement of 1.2 dB over Dicode PPM. These results indicate that DuoPPM has an advantage over both Digital PPM and Dicode PPM when operating with a high level of dispersion (low bandwidth).

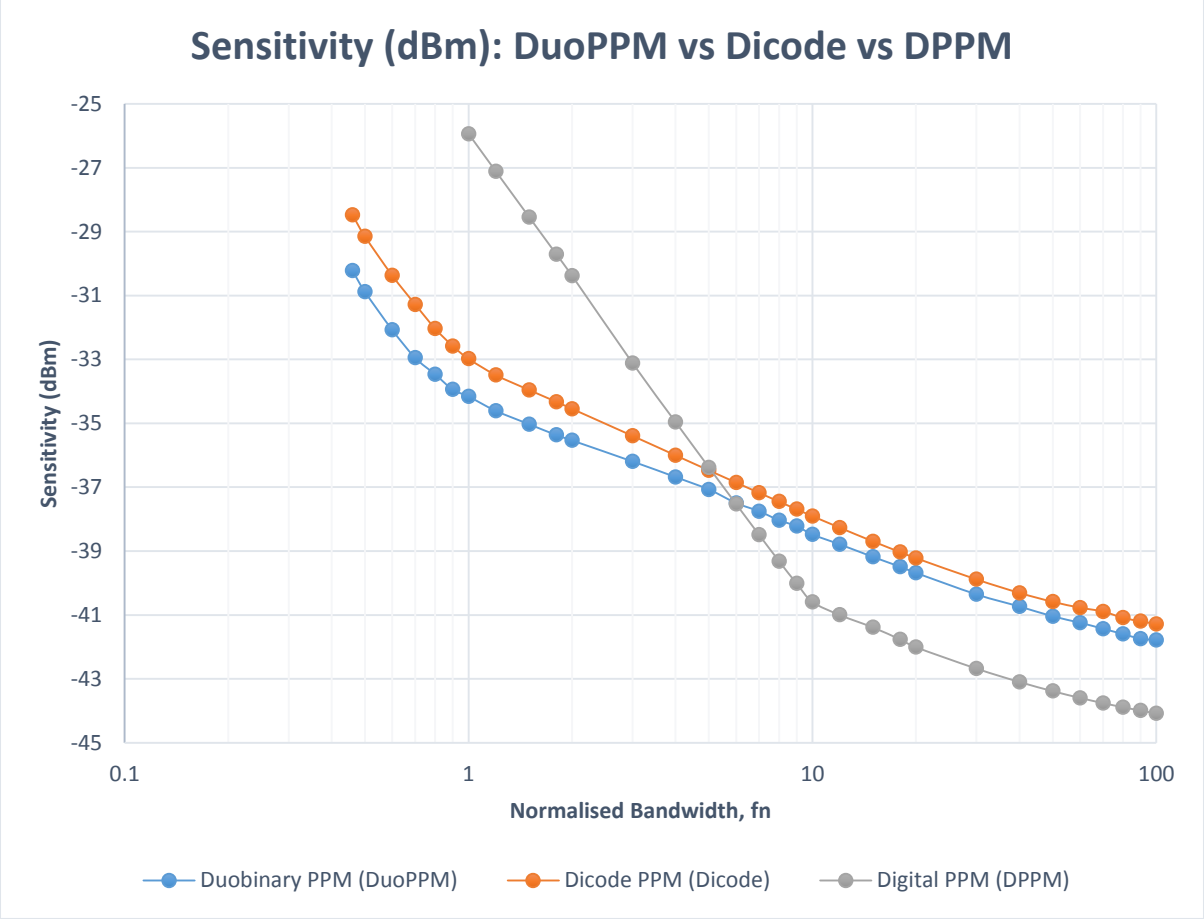


Fig. 4.2: Variation in sensitivity (dBm) with normalised fibre bandwidth for Duobinary, Dicode and Digital PPM.

4.4 Conclusions

Original theoretical results show that a simple, leading-edge, threshold-detection DuoPPM system gives comparable sensitivity to that of digital PPM at high fibre bandwidths and for low fibre bandwidths, the sensitivity is significantly greater. The results presented are for a data rate of 1 Gbit/s. The simulations carried out so far have considered a highly dispersive graded-index Plastic Optical Fibre (POF) channel as the primary focus of targeted improvement. Such fibre channels exhibit an impulse response that can be approximated to a Gaussian shape [81] and have a relatively poor bandwidth. The reason to deliberately choose this channel is to demonstrate the effects of dispersion on the coding technique. Although the simulations have been restricted to 1 Gbit/s the technique can be adapted to high-speed optical communications links potentially exceeding 10 Gbit/s without any significant compromise of improved sensitivity. Application of this coding scheme in free-space communications links and other detection schemes is also possible [37, 82].

Chapter 5

Duobinary PPM Maximum Likelihood Sequence Detection Theory

Original theory[13] of the Maximum Likelihood Sequence Detection (MLSD) has been modelled and simulated using Mathcad to compare and contrast between the systems performances with and without MLSD, and also to investigate how the DuoPPM system performs better for reduced bandwidth highly dispersive plastic optical fibre (POF) channels. A paper has been written [27] and submitted for publication from the excerpt of Chapter 5 and Chapter 6 of this thesis. This chapter describes the theory of the MLSD of DuoPPM and how an effective algorithm has been developed for the system from the theoretical work which has been implemented later in the project to work in the receiver system to improve sensitivity performance of DuoPPM.

The following chapter[14] describes how the mathematically represented system has been modelled in order to simulate the DuoPPM system operating with MLSD. Key results obtained from the simulations have been presented and analysed to establish the improvements that DuoPPM provides over the existing coding schemes for dispersive optical channels especially POFs.

[13] Originally developed by Dr Martin Sibley which has been analysed, modelled and simulated during the research project.
[14] Simulation files and more results available in Appendix 2.3 and Appendix 2.4.

5.1 DuoPPM MLSD Operations

For the verification and optimum operations of MLSD, main algorithms were developed and tested on all possible erroneous data sequences for verification. Using the devised algorithm, number of equivalent PCM errors in a given erroneous DuoPPM sequence can be calculated theoretically. Appendix 5 explains how the equations were developed for the MLSD and they are presented in table A5-5.1. All possible error sequences and equivalent PCM errors in each sequence have also been presented in appendix 5. Two key assumptions that have been made are: number of DuoPPM errors in any one data sequence is no more than 1 and maximum number of consecutive C (Change) symbols in any given sequence is 9. There was no need to devise equations for wrong-slot errors since all wrong-slot errors will be detected and corrected by the MLSD. Erasure error of 1 and 0 in a sequence of same characteristics will result in same number of equivalent PCM errors. However, false alarm of same symbol (0 in 0C1 and 1 in 1C0) and different symbol (0 in 1C0 and 1 in 0C1) will result in different numbers of equivalent PCM errors which have been explained and shown in appendix 5 as well as in this chapter. Equivalent PCM errors that have been found in the comprehensive MLSD tables in appendix 5 successfully verifies the algorithms developed, thus confirming the validity of the MLSD.

5.1.1 Wrong-slot Errors

The primary reason of wrong slot errors is intersymbol interference (ISI) when operating at low fibre bandwidths. It occurs when the noise on the slope of a pulse in a given time slot makes the edge of the pulse appear in adjacent time slot [26]. Duobinary PPM coding scheme has been developed to provide significant advantage when operating at low bandwidths and highly dispersive channels thus it is imperative that the wrong-slot errors are completely eliminated to be able gain any improvement in sensitivities.

Pulse Error	**Invalid Sequence**	**Method of Detection**
0 → 1	1/0 *x*C 1/0 *y*C 1/0	Same symbols at both ends after ODD number of Cs Opposite symbol at both ends after EVEN Cs
0 ← 1	1/0 *x*C 1/0 *y*C 1/0	Double Pulse
1 ← 0	1/0 1/0 0/1 yC 1/0	1 and 0 consecutively.
1→ 0	1/0 xC 1/0 0/1 0/1	1 and 0 consecutively.

Table 5.1: Wrong-slot pulse error and detection methods for duobinary PPM.

As it can be seen from the table[15] 5.1 that the invalid sequence for wrong slot of 0 forwarded to 1 can be easily detected by counting the number of C pulses that arrives consecutively. This is always corrected by changing the middle 1/0 pulse to the opposite pulsed symbol thus returning 0 errors. The key MLSD rules of the duobinary PPM is that when a number of consecutive Cs are received then if the number is ODD, this indicates that first and last symbol before and after the reception of Cs must be OPPOSITE, and if the number of Cs are EVEN then it indicates that first and last symbol of a the sequence[16] must be SAME. Furthermore, there will never be a 1 right after 0 and vice versa for a sequence to be valid and these rules are

[15] Please see appendix 5 for a complete set of error detection and correction table.
[16] The sequence here means 1/0 xC 1/0 NOT 1/0 xC 1/0 yC 1/0

applicable for all three types of errors for detection and correction algorithm. When 1 goes back to 0 as shown in the table 5.1 it will produce double pulse in the same frame which is easily detectable and after correction returns 0 PCM errors. However, there are exceptional circumstances when a 0 goes back to 1 and a 1 goes forward to 0 to cause wrong-slot errors. Although these are wrong-slot errors, they do appear to be false alarm errors when being detected. However, for the coding scheme to be operated over dispersive low bandwidth channel, these two errors must be eliminated in order to completely eliminate the wrong-slot errors which is the main types of errors of the aforementioned channel at low bandwidth. Therefore, whenever these two particular error occurs, they are treated as wrong-slot errors even though they may appear as false-alarm and corrected always by changing the middle symbol of three consecutive pulsed symbols to C.

For example, when 110xC1 is received as an invalid sequence it will always be corrected to 1C0xC1 and when 0xC100 is detected it will always be corrected as 0xC1C0 thus completely eliminating the wrong-slot errors in the process which will significantly improve the sensitivity of the coding scheme at low bandwidths.

5.1.2 Erasure Errors

Due to erasure errors the pulses in 1 or 0 from a sequence can be erased thus introducing errors in the sequence. Depending on the maximum permissible consecutive like symbols the number of errors at the PCM output could be severe for the longest sequence allowed. If not resolved by using MLSD this kind of errors can have negative impact on the sensitivity of the system. Table 5.2 shows an erasure of 1 in the transmitted sequence and when this error is detected by MLSD there are 5 possible valid sequence combinations that can be derived. The most possible valid combination is decided by determining all possible PCM sequences, finally averaging each bit to find the most likely sequence.

Transmitted Sequence								0	C	C	C	1	C	0		
Error Detected								0	C	C	C	***C***	C	0		
All Valid Combinations								**Decoded PCM**								
0	0	C	C	C	C	0		0	0	0	1	0	1	0	0	
0	C	1	C	C	C	0		0	0	1	1	0	1	0	0	
0	C	C	0	C	C	0		0	0	1	0	0	1	0	0	
0	C	C	C	1	C	0		**0**	**0**	**1**	**0**	**1**	**1**	**0**	**0**	
0	C	C	C	C	0	0		0	0	1	0	1	0	0	0	
								0	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1 ERROR**

Table 5.2: MLSD Detection and correction of a duobinary sequence where a 1 has been erased (highlighted in bold italic).

In case of the error shown in Table 5.2 above, the most likely valid sequence has a PCM error of 1 after using MLSD. Therefore, it is clear that there will still be a possible number of errors even with the use of the MLSD algorithm. However, without MLSD the number of PCM errors would be 3. An exception in the erasure error detection is that if 08C1 is received then it will immediately appear that an erasure error had occurred somewhere in the sequence. However,

if the next symbol after 1 is 0 then it will be detected a wrong-slot error of 0 back to 1, the sequence will be corrected by changing 1 to C thus the corrected sequence would be 09C1. In any disambiguation during the decision making process for correction, wrong-slot correction will always take priority.

5.1.3 False Alarm Errors

This occurs when the amplitude of the noise is greater than the threshold level and can result in false 0 or 1 in a C symbol slot [26]. Similar to the method shown in the previous section of erasure errors the detected invalid sequence is resolved by determining all valid PCM sequences and averaging each bit to get the final valid PCM sequence. Table 5.3 below shows a transmitted sequence been corrupted by a false-alarm of 1. After applying MLSD to the invalid sequence, the overall PCM error is 0.5. Without the MLSD use the error in the sequence would be 3. Number of final PCM errors after applying MLSD depends on where the error has occurred in the sequence. If it occurs early in the sequence and the sequence is particularly long then the number of PCM errors would increase. However, applying MLSD will still ensure significant improvement in sensitivity compared to when deployed without MLSD.

Transmitted Sequence								1	C	0	C	C	C	1
Error Detected								1	C	0	C	***1***	C	1
All Valid Combinations								**Decoded PCM**						
1	C	0	C	1	1	1		1	1	0	0	1	1	1	1		
1	C	0	C	C	C	1		**1**	**1**	**0**	**0**	**1**	**0**	**1**	**1**		
								1	**1**	**0**	**0**	**1**	**1/0**	**1**	**1**		**0.5 ERROR**

Table 5.3: MLSD Detection and correction of a duobinary sequence where a false 1 has been detected (highlighted in bold italic).

5.2 DuoPPM Algorithm of Error Probabilities

5.2.1 General Error Probabilities

The general error probabilities of duobinary PPM is same as dicode PPM [18]. Therefore, considering a general duobinary PPM sequence such as 1*x*C0*y*C1 where *x* and *y* represents odd numbers of C symbols, the average PCM error due to an error event is given by the following equation:

$$P_{e_{x.y}} = \sum_{y}^{n-1}\left(\sum_{x}^{n-1}\left(\left(\frac{1}{2}\right)^{x+2}\left(\frac{1}{2}\right)^{y+2} P_e Error_{x.y}\right) + \left(\frac{1}{2}\right)^{n+1}\left(\frac{1}{2}\right)^{y+2} P_e Error_{n.y}\right) + \sum_{x}^{n-1}\left(\left(\frac{1}{2}\right)^{x+2}\left(\frac{1}{2}\right)^{n+1} P_e Error_{x.n}\right) + \left(\frac{1}{2}\right)^{n+1}\left(\frac{1}{2}\right)^{n+1} P_e Error_{n.n} \quad (5.1)$$

Where P_e is the probability of an erasure or false-alarm pulse detection error and $Error_{x,y}$ is the number of PCM errors resulting from the pulse detection error. Sections 5.2.2 and 5.2.3 discuss the effects of erasure and false-alarm detection error on the PCM data stream so that the equivalent PCM error can be found using equation (5.1).

This equation has been used to calculate errors at the start of the calculation for each type of error which is then used in the equations 5.3 and 5.5 to obtain the total probability of error that has been done in Mathcad calculations. Use of this equation can be seen in appendix 2.1 and 2.3 (Mathcad calculations and simulations) highlighted in yellow and green.

5.2.2 Algorithm and Probabilities of Erasure Error

An erasure of a pulse occurs when a pulse is erased in between two like symbols which results in an invalid sequence of code containing two like symbols separated by any of the other two types of symbols. Equivalent PCM errors was derived from the following expression for a duobinary PPM sequence of **0xC1/0yC1/0**,

$$\text{Error}_{x,\,y} = \frac{|x-y|}{2} \tag{5.2}$$

Equation (2) applies to both erasure of pulse 1 and 0. If the invalid sequence shown previously in section 5.1.2, table 5.1 then equation (2) resolves the invalid sequence and provides with correct number of equivalent PCM errors that will be produced.

The probability of an erasure error, P_{er}, is

$$P_{er} = Errors * 0.5 erfc\left(\frac{Q_{er}}{\sqrt{2}}\right) \tag{5.3}$$

where

$$Q_{er} = \frac{v_{pk} - v_d}{\sqrt{< n_o{}^2 >}} \tag{5.4}$$

Where V_{pk} is the peak-signal voltage within the given time slot and the effect of ISI can be measured by determining the peak amplitude of the given pulse within the frame for certain combinations of x and y. At low normalised fibre bandwidths there is very high probability of the peak of the signal to appear in the following time slot, as shown in figure 6.4[17], largely due to pulse dispersion. Once the 'Errors' are calculated, this equation has been used to calculate the total probability of error that has been done in Mathcad calculations. Use of this equation can be seen in appendix 2.3 (Mathcad calculations and simulations) just after yellow and green highlighted sections.

[17] Figure 6.4 is available in the following Chapter (6).

5.2.3 Algorithm and Probabilities of False Alarm Error

The probability of a false alarm error is given by

$$P_f = Error * 0.5\, erfc\left(\frac{Q_f}{\sqrt{2}}\right) \qquad (5.5)$$

where

$$Q_f = \frac{v_d - v_{ISI}}{\sqrt{< n_o^{\,2} >}} \qquad (5.6)$$

Threshold level, *v*, was used as a system variable which is defined by

$$v = \frac{v_d}{v_{pk}} \qquad (5.7)$$

where v_d is the peak voltage of an isolated pulse and is the decision voltage. Pulse shape and noise can be determined theoretically if the fibre bandwidth is known. Once the 'Error' is calculated, this equation has been used to calculate the total probability of error that has been done in Mathcad calculations. Use of this equation can be seen in appendix 2.3 (Mathcad calculations and simulations) just after yellow and green highlighted sections of false-alarm errors.

Equivalent PCM errors was derived from the following expression

$$Error_{x,y} = \frac{|Combinations_{x,y} - 1|}{2} \qquad (5.8)$$

Number of valid combinations varies depending on type of false-alarm error, data sequence and the position of the error in the sequence. Therefore, for a false-alarm error of **0 in 1yC0** or **1 in 0yC1**, number of valid combinations are calculated using the following equations:

If position of error *(k)* is ODD, then

$$Combinations_{x,y} = k+1 \qquad (5.9)$$

If position of error *(k)* is EVEN, then

$$Combinations_{x,y} = y-k+1 \qquad (5.10)$$

For a false-alarm error of **0 in 0yC1** or **1 in 1yC0**, number of valid combinations are calculated using the following equations:

If position of error *(k)* is ODD, then

$$Combinations_{x,y} = y-k+1 \qquad (5.11)$$

If position of error *(k)* is EVEN, then

$$Combinations_{x,y} = k+1 \qquad (5.12)$$

5.3 Conclusions

In conclusion, the chapter presented the MLSD theory of DuoPPM and how this is used in Mathcad simulations and calculations. Derivations of the MLSD equations are given in detail in appendix 5 which are described both in this chapter and in appendix 5. Complete tables of error sequences along with equivalent PCM errors for each are provided in the aforementioned appendix. In addition, how MLSD applies to each of the three types of errors have been explained in this chapter with the aid of example sequences. Mathematical representations of estimating errors in a given sequence and how the probability of error is calculated are presented in this chapter.

Chapter 6

Duobinary PPM MLSD Mathcad Simulation and Results

As has been mentioned in the previous chapter, the code for Mathcad model and more results have been provided in Appendix 2.3 and 2.4 for further reading and understanding. In addition, all the possible theoretical error sequences, and MLSD detection and correction tables have been provided in Appendix 5. The tables have been completed assuming that the maximum number of consecutive Cs (Change Symbols) that are allowed to occur is 10 and for 1 bit PCM errors because if there is more errors than one in a sequence then it becomes very complex to resolve the sequence. Later in this document it is also shown that the practical FPGA implementation of MLSD has also been done using the maximum allowable same symbols of Cs to be 10.

6.1 Mathematical Modelling and Performance Evaluation

Mathematical simulation and representation of DuoPPM MLSD has been done in order to evaluate the performance of the system in Graded-Index (GI) POF channel. The reason for choosing this particular channel was that it is highly dispersive and as has been proposed by the previous publication [26] that DuoPPM will perform better in dispersive channel with MLSD compared to digital PPM and Dicode PPM [2, 11-12]. The impulse response of the GI-POF channels can be approximated to be a Gaussian distributed pulse shape [81]. The signal represented to the threshold detector of the system is similar to that of the Dicode PPM [2, 18]

as both systems have to be comparable for the purpose of analyses, due to their inherent coding mechanisms. The signal is given by the following expression

$$v_o(t) = \frac{b\eta q}{2\pi} \int_{-\infty}^{\infty} Z_{pre}(\omega) H_p(\omega)^2 \exp(j\omega t)\, d\omega \qquad (6.1)$$

This can be described as the pulse shape of a classical matched filter which is presented at the input of the threshold detector where b is the number of photons per pulse, η is the quantum efficiency of the detector, q is the electronic charge and $Z_{pre}(\omega)$ is the frequency dependent transimpedance of the preamplifier at the receiver. Variation of the received pulses is given by, α, which is directly linked to the fibre bandwidth [58] and given by

$$\alpha = \frac{0.1874 T_b}{f_n} \qquad (6.2)$$

where T_b is the PCM bit time and f_n is the fibre bandwidth normalised to the PCM data rate.

Equations (6.1) and (6.2) have been used in the Mathcad simulations and calculations for Gaussian pulse shaping and approximating the variations of the received pulses. The code is provided in appendix 2.3. It can be seen from the aforementioned appendix that the first four pages of the model defines the specifications for the simulations such as pre-amplifier bandwidth, noise at the preamplifier input, data rate, quantum energy, operational wavelength, pulse variation model, Gaussian pulse shaping, photon energy, timing and threshold detections, peak pulse amplitude.

A receiver system has been proposed in the previous publication [26] and the block diagram of the proposed receiver system is given in the figure 6.1 below.

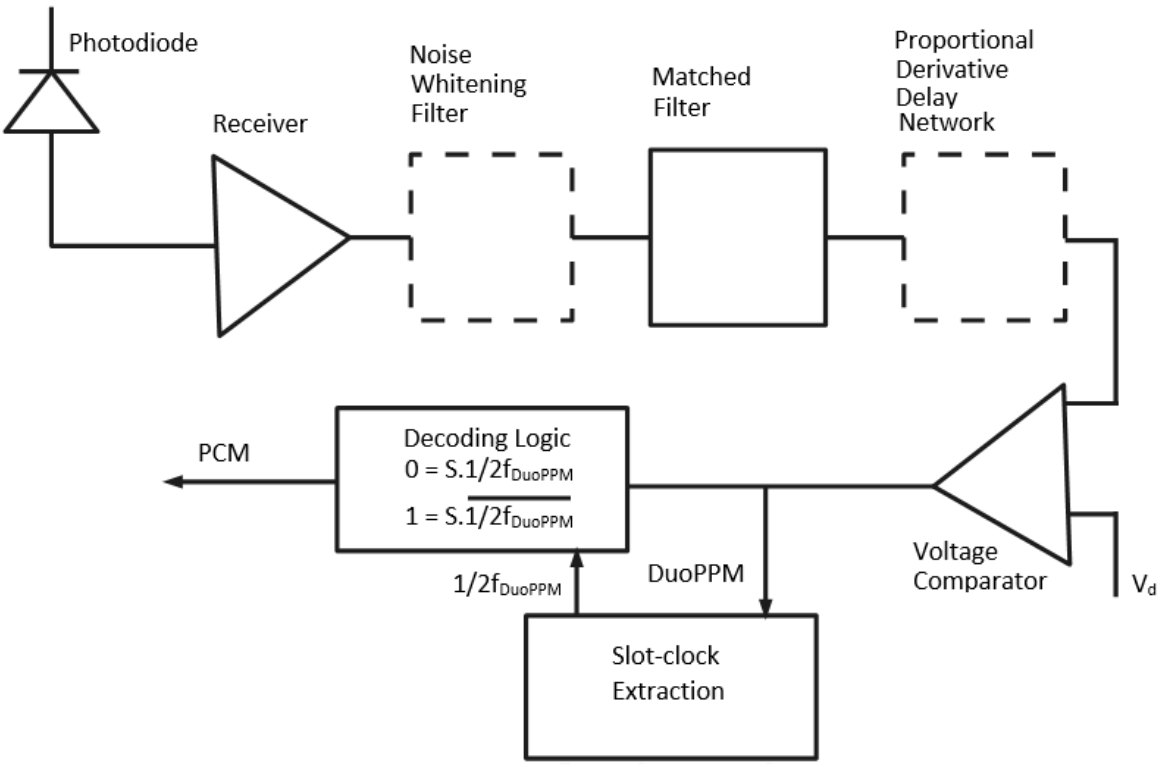


Fig. 6.1: Block diagram of the proposed DuoPPM receiver.

According to the proposed system given in figure 6.1, the mathematical system used for simulation implements an optical receiver with a limited-bandwidth which is given by, ω_c, and a white noise spectrum at the output (appendix 2.3). Since a PIN photodiode has been used its shot noise is negligible for the system modelling purpose. Matched filter has been used a pre-detection filter and proportional derivative delay (PDD) network is optional to the receiver system and it has not been used in the simulation model before the signal being presented at the threshold detector. Noise that appears on the signal is similar to that of Dicode PPM and Multiple PPM [2, 28-29] therefore has not been repeated here.

In common with Dicode PPM, a threshold level, v, was used as a system variable defined by

$$v = \frac{v_d}{v_{pk}} \tag{6.3}$$

where v_{pk} is the peak voltage of an isolated pulse and v_d is the decision (threshold) voltage. The pulse shape and noise can be determined theoretically if the fibre bandwidth is known [2]. Simulations were performed to find the optimum value of v_d that gave the minimum number of photons per pulse, b, for a specified error rate of 1 in 10^9.

A 1 Gbit/s PCM data-rate system, operating at a wavelength of 650 nm and a photodiode quantum efficiency of 100% was considered. The preamplifier had a bandwidth of 10 GHz and white noise of 50 x 10-24 A2/Hz when referred to the input. The aforementioned parameters were obtained from a commercial device. Line coded PCM data was used so that n=10 and simulations were conducted on DuoPPM system operating with an MLSD.

6.2 Results and Discussion

Results have been obtained and analysed to verify the performance of the modelled system operating with MLSD. Three key results have been presented in this section to make sufficient comparisons between DuoPPM and Dicode PPM. Figure 6.2 shows the required number of photons per pulse with fibre bandwidth normalised between 0.46 and 100 for DuoPPM and Dicode operating with MLSD. It can be seen from the overall graph that DuoPPM outperforms Dicode PPM for low fibre bandwidths. However, at high fibre bandwidths the performance of both coding scheme is very similar although DuoPPM still holds slightly better performance than Dicode.

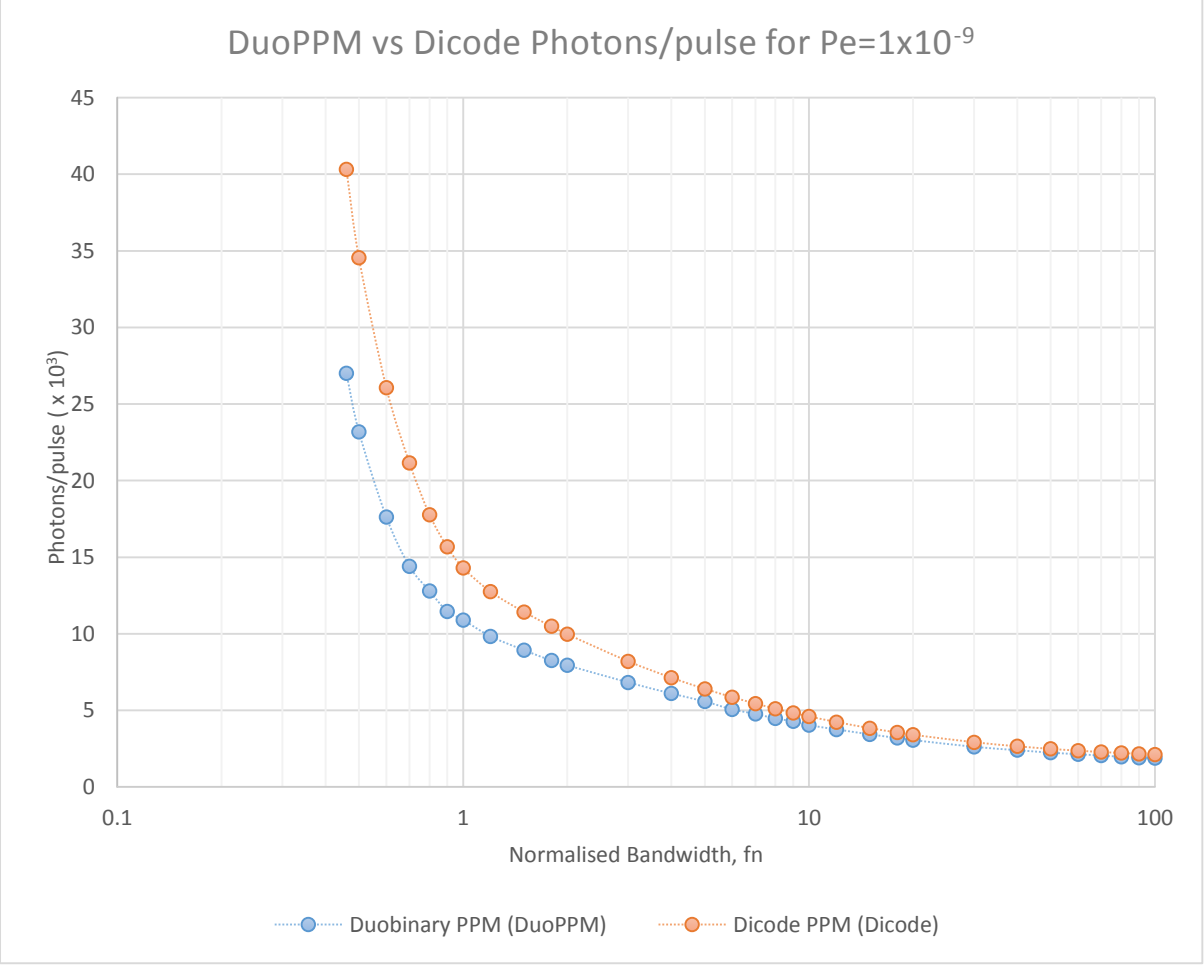


Fig. 6.2: Comparison between DuoPPM and Dicode required photons/pulse as a function of normalised bandwidth, f_n.

Both coding systems are functionally operational at normalised fibre bandwidth as low as 0.46, however, it is not possible to go below this point as the pulses become highly dispersed and the threshold voltage required for detection is very high as can be seen from figure 6.4 (in the following page) compared to less dispersed pulses as shown in figure 6.3. At high bandwidth, photons per pulse required for DuoPPM is 1902 compared to 2114 of Dicode. These numbers are very similar at high bandwidths because the intersymbol interference (ISI) is favourably low and errors are pattern independent. Therefore, there the difference in error probabilities between 100 and 10 normalised bandwidths is negligible.

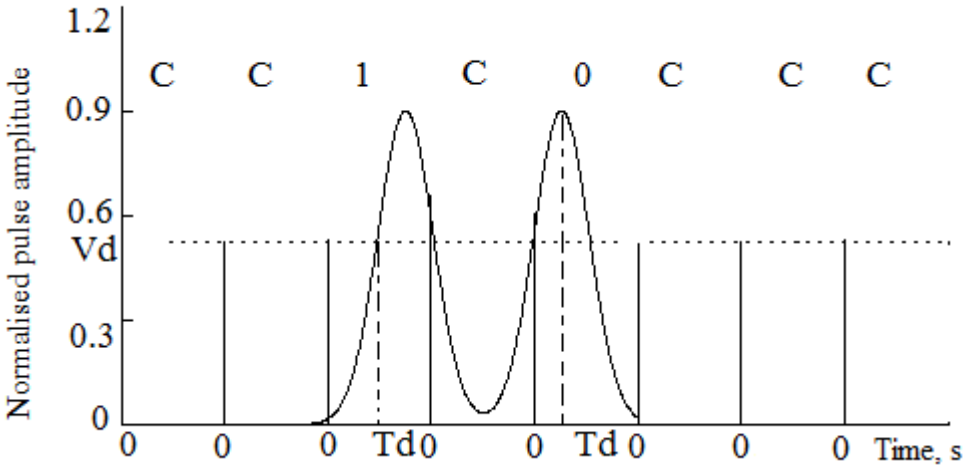


Fig. 6.3: Simulated pulse response at normalised bandwidth of 1 for the sequence 1C0 (amplitude normalised to a single isolated pulse).

As the normalised bandwidths gets low down to 1 and below, DuoPPM performance advantage is significant as it needs considerably less photons per pulse, with 10.9 x 10^3 photons required compared to 14.3 x 10^3 needed for Dicode which results in a sensitivity difference of 1.2 dB approximately. Below the normalised bandwidth of 1 the pulses become very dispersed which has direct effect on the performance of both systems as shown by figure 6.3 and 6.4. Pulse become dispersed so that the peaks spreads out in the adjacent slots and detection only possible

by the pulse remaining at the edge of the correct slots and the detection also requires very high threshold level. The lowest normalised bandwidth that the systems can be operable is down to 0.46 where DuoPPM requires 27 x 10^3 photons per pulse compared to 40.3 x 10^3 required by Dicode.

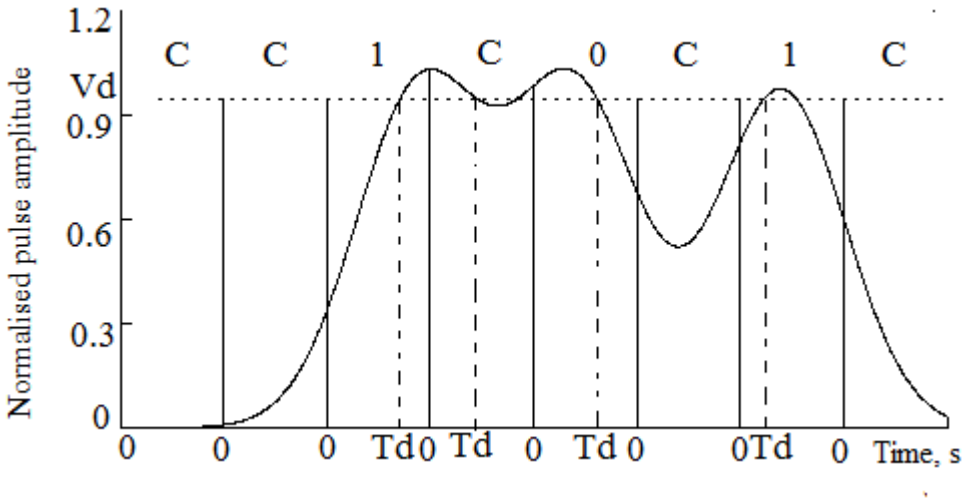


Fig. 6.4: Simulated pulse response at normalised bandwidth of 0.46 for the sequence 1C0C1 (amplitude normalised to a single isolated pulse).

Table 6.1 shows the required photons per pulse for DuoPPM system operating over specific normalised fibre bandwidths and the error probabilities in 1 x 10^{-10} for each type of error that has been discussed in chapter 5 previously. It has been shown that with the operation of MLSD wrong-slot errors can be eliminated thus the error probabilities and the overall sensitivity of the system is are dominated by the erasure and false-alarm errors. Probability of erasure for both 1 and 0 are same over the range of the bandwidths which is expected as has been discussed previously in chapter 5. However false-alarm of 1 is significantly higher as the bandwidth goes very low and contrastingly false-alarm of 0 becomes a non-occurring event. This is expected as well because at very low normalised fibre bandwidths the pulses are so dispersed that they spread out to the neighbouring frames and slots thus giving rise to the false-alarm error of 1

and for the same reasons the false-alarm error of 0 becomes non-existent. DuoPPM system has been able to operate down to 0.46 times the bit rate as shown in the table 6.1 and the system is inoperable below this due to very high threshold voltage as has been shown in figure 6.4. It is also noticeable that when DuoPPM is deployed for highly dispersive optical channels at very low normalised fibre bandwidths it must be operated with MLSD as non-MLSD system will be highly unsuitable.

Normalised link bandwidth (f_n)	**100**	**10**	**1**	**0.5**	**0.46**
Photons per pulse (10^3)	1.9	4.03	10.9	23.19	27
Threshold parameter, V	0.4	0.49	0.58	0.89	0.975
Error Probabilities (10^{-10})					
Erasure 1 => C	3.19	2.55	2.38	2.23	2.08
Erasure 0 => C	3.19	2.55	2.38	2.23	2.08
False Alarm C => 1	1.31	2.25	2.43	5.54	5.84
False Alarm C => 0	2.32	2.74	2.81	0	0

Table 6.1: Error probability results of DuoPPM system operating with MLSD at specific normalised link bandwidths.

6.3 Conclusions

In conclusion, this chapter has presented the mathematical calculations and simulations of maximum likelihood sequence detection system of DuoPPM using Mathcad in order to predict theoretical sensitivities that can be achieved. Mathcad simulations and calculations have been carried out with the specifications of a wide-band receiver, matched filter and highly dispersive graded-index POF channel operating at a data rate of 1 Gbp/s. The results that have been presented and analysed in this chapter demonstrate that at low fibre bandwidths DuoPPM sensitivity outperforms dicode PPM by 1.2 dB when operating with MLSD because it requires considerably less photons per pulse for pulse detection. In addition, it shows that at high fibre bandwidths photon counts for both DuoPPM and dicode PPM are very similar as was expected due to low intersymbol interference (ISI).

Chapter 7

VHDL and FPGA Implementation of Duobinary PPM Coding System

7.1 Introduction

This chapter describes the VHDL circuits that have been designed for the duobinary PPM coder and decoder system. A paper [91] has been published[18] presenting the functional and timing simulations of the coder and decoder thus some similarities may be found between this chapter and sections of the published paper. All the VHDL designs have been listed in Appendix 3. Duobinary PPM coder and decoder main section includes an FPGA PLL block for clock division and clock extraction, maximum length PRBS PCM input generator circuit, duobinary PPM coder system which has been implemented using schematic design technique, a two-bit serial-in-parallel-out (SIPO) register, finally the decoder for the system. The decoder has been designed using both schematic method using discrete logic gates in VHDL and HDL programming language. Altera © Quartus™ II design software has been used for all the VHDL design purposes.

Specifications and functionality of the designed systems have been verified by both functional and timing simulations. After completion of successful timing simulation every block of code has been implemented on to FPGA and verified experimentally using an oscilloscope. MLSD and bit error rate (BER) code described later in Chapter 8 has been experimentally verified using electrical back-to-back test for more accurate verification.

[18] Please see Appendix 1.3 for the paper in its entirety.

In order to practically implement the designed coder and decoder on an FPGA timing analysis on all logic circuits needed to be completed since functional simulation does not consider any timing delays. First of all, the delays were identified for both circuits and required measures had to be taken to either remove the delays or if they were not removable then measures had to be taken to compensate for the existing delays as the signals need to be synchronised with the clock signals to produce correct outputs. Main types of delays identified for the circuits were inertia delay which is inherent in FPGA, transport delay (propagation delay), gate delays, fan-out and clock skew [91]. Most of the delays were compensated by using DFFs that shift the signals to synchronise with required signals. The delays in coder circuit were compensated using additional logic elements of 3 DFFs, 1 OR gate and 1 NOR gate. For functional simulation, 120MHz clock was used which is the frequency for PCM. But for practical timing analysis it was determined that two different clock frequencies were required: one 240MHz clock for DuoPPM as it runs at the data rate two times that of PCM thus PCM requires a 120MHz clock. Phase-locked Loop (PLL) was used to process the external 240MHz clock signal and it produces two output clock signals of 120MHz and 240MHz; and both output clock signals were source synchronised as will be shown later in the chapter.

7.2 Phase-locked Loop (PLL) Clock

For all the clock requirements in the entire duobinary PPM system, integrated PLLs in the FPGA have been used. It is considerably easy to design and any latency is compensated by the FPGA thus less concern over delay and phase synchronisation issues. It is also used for clock extraction form the data signals later in the design. The schematic block diagram of the FPGA PLL used in the design is given in figure 7.1 below.

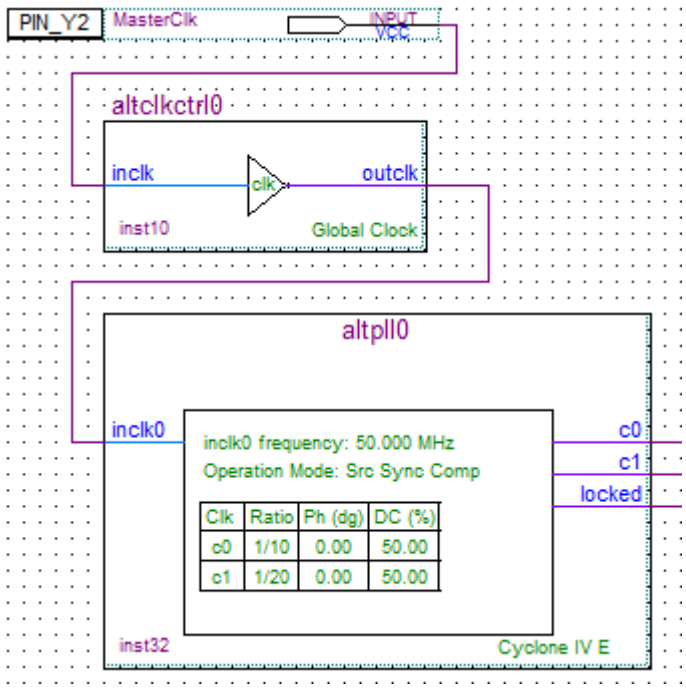


Fig. 7.1: Duobinary PPM PLL design for clocking requirements.

The PLL block shown in the above diagram has to be operated with manufacturer's clock control block for better optimisation for Cyclone © IV E series FPGAs as shown in the figure above and recommended by the manufacturer. It has many different ratios of clock division if required. The clock signals had to available throughout both circuits as dedicated clock signals to avoid any delays related to clock skew. Therefore, the clock signals were routed in the circuits as GLOBAL signals available approximately at the same time at different components minimising the effects of clock skew. If the clock signals are not routed as GLOBAL signals

then FPGA will consider them as general signals and this may cause, in synchronous circuits, the signals to arrive at different components at different times causing erroneous outputs from logic components. Figure 7.2 below shows the simulation results of the PLL clock generation.

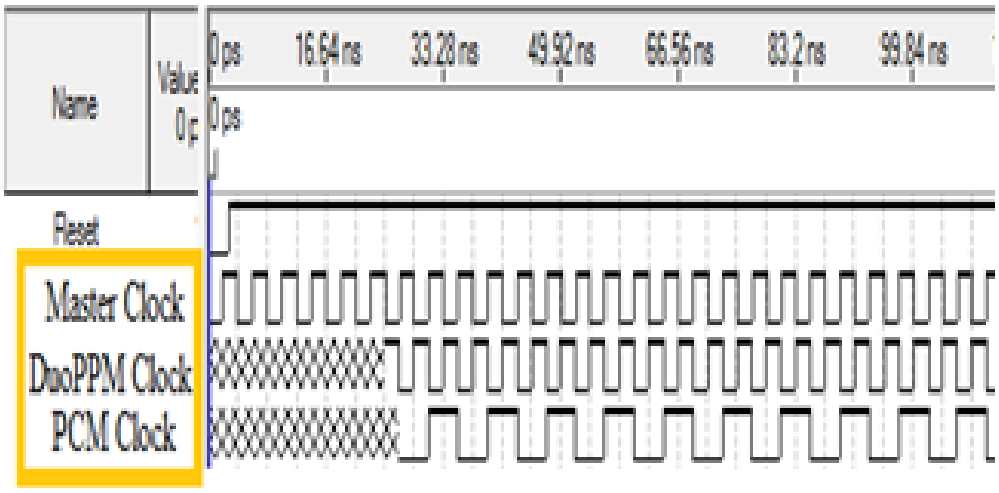


Fig. 7.2: PLL clock generation simulation result.

Key signals are marked in the coloured box. Master clock is the input clock to the PLL system either from inter 50 MHz source or from external SMA clock input. DuoPPM clock is the same as the master clock and the master clock is finally divided by a factor of 2 in order to produce the PCM clock. As has been mentioned in the earlier chapters, duobinary PPM only operates at twice the original PCM data rate.

7.3 Maximum Length PRBS PCM Data Generator

An 8-bit shift register has been implemented as a pseudo random binary sequence (PRBS) generator. This will simulate the OOK PCM input to the duobinary PPM coder system. In addition, the PRBS generator has been designed to maximum length random data available from the 8-bit shift register. This will be very useful as the sequences will be deterministic and will help analyse the system better. It will also help regenerate the PRBS sequences in-phase and properly for the BER test system. The circuit will produce 255 bits of random data before repeating the sequence. In order to make an 8-bit shift register operating at maximum length 4 separate data bits need to be tapped [92] as shown in the figure 7.3below.

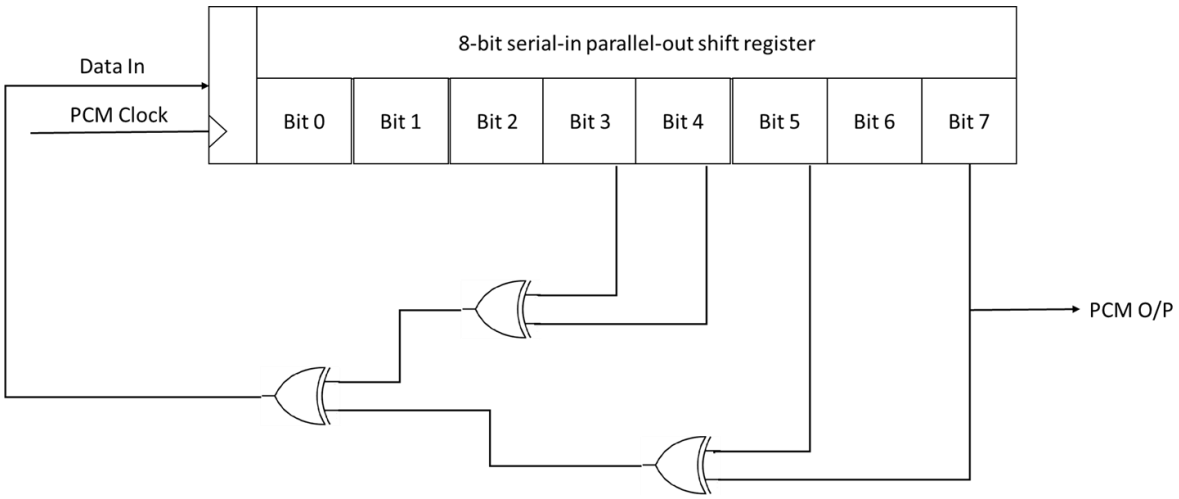


Fig. 7.3: Block diagram of the maximum length 8-bit PRBS generator.

As shown above, 4 outputs of the shift register needs to be tapped using XOR gates which was implemented for the system. PRBS generator designed using discrete components usually requires a self-starter circuit, however, this is easily implemented in the VHDL by pre-defining the initial values of the shift register.

The main section of the code that has been designed for the PRBS generator has been given in the listing 7.1 below[19].

```
SIGNAL Tmp     : std_logic_vector(0 TO 7):= "10000101";

VARIABLE first_tap  : std_logic;
VARIABLE second_tap : std_logic;
VARIABLE third_tap  : std_logic;

ELSE IF (Reset = '1') THEN
    first_tap   := Tmp (3) xor Tmp (4);
    second_tap  := Tmp (5) xor Tmp (7);
    third_tap   := first_tap xor second_tap;
    Tmp         <= third_tap & Tmp (0 TO 6);
END IF;
```

Listing 7.1: Main segments of the PRBS PCM generator code.

It can be seen from the listing 7.1 above that initially shift register has been loaded with a non-zero data stream (first box) and three variables (second box) have been used in order to implement the multiple tap (third box) of the maximum length PRBS generator.

Figure 7.4 below shows the simulation results of the PRBS PCM data generation for the duobinary system. Waveforms are annotated for ease of reading and understanding.

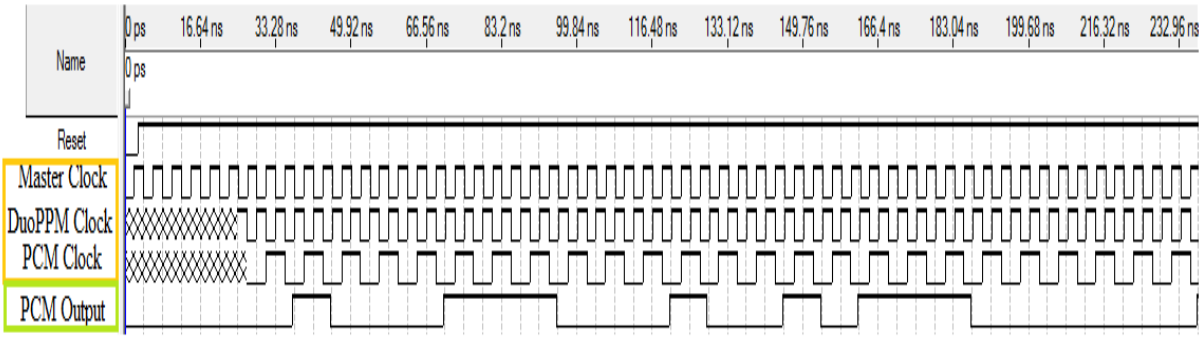


Fig. 7.4: PRBS data generation in VHDL.

[19] Listings of code do not include all the code, only the main parts from a design. For complete code please see Appendix 3. Boxes in the listing indicate that there are missing code between the lines.

Experimental verification of the PLL clock divider and PRBS PCM data generator is given in figure 7.5 below.

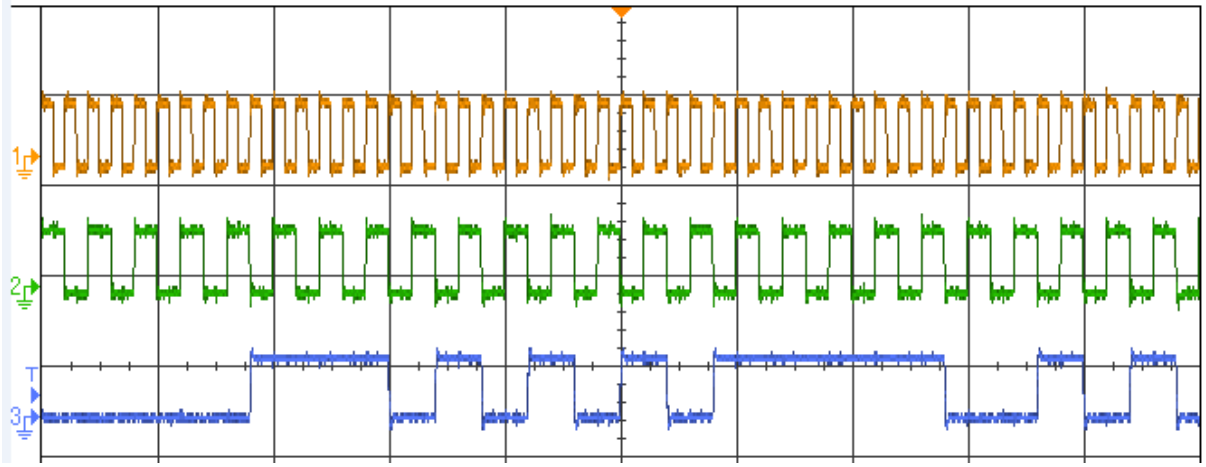


Fig. 7.5: Experimental verification of derived clock signals from master clock (DuoPPM clock top trace and PCM clock middle trace) and the generated PCM data (bottom trace).

7.4 Duobinary PPM Coder

Code of the duobinary PPM was designed to get the required theoretical output as has been discusses in section 3.2 (Table 3.1). The coder is the part of the duobinary PPM system that converts any PCM sequences into sequences that contain the DuoPPM symbols (Table 3.1). The PCM sequences were generated randomly by a Pseudo Random Binary Sequence (PRBS) generator discussed in the previous section. The output of this PRBS block was used as the input of DuoPPM coder. The logic components that have been used to complete this coder are four D-type Flip-Flop (DFF), three NOR gate, one OR gate, one NOT gate and three AND gates. DFF delays the PCM sequence by half the clock cycle, the output of which is used with original PCM sequence to produce pulses at slots 0 and 1. Both original and delayed PCM sequences are then used as inputs to an AND gate and NOR gate. The use of clock signal and

inverted clock signal are required to retime the DuoPPM pulse sequences for slot 0 and slot 1. The output of the AND gate then used as one of the two inputs of another AND gate along with the clock signal; and the output of the NOR gate is used as one of the two inputs of an AND gate along with inverted clock signal to produce pulses at slot 0 and slot 1. The outputs of the last two AND gates were then fed to the inputs of an OR gate that combines the signals to get the required duobinary PPM coded sequences which have been converted from original PCM sequences. Figure 7.6 below shows the schematic diagram of the design that has been implemented.

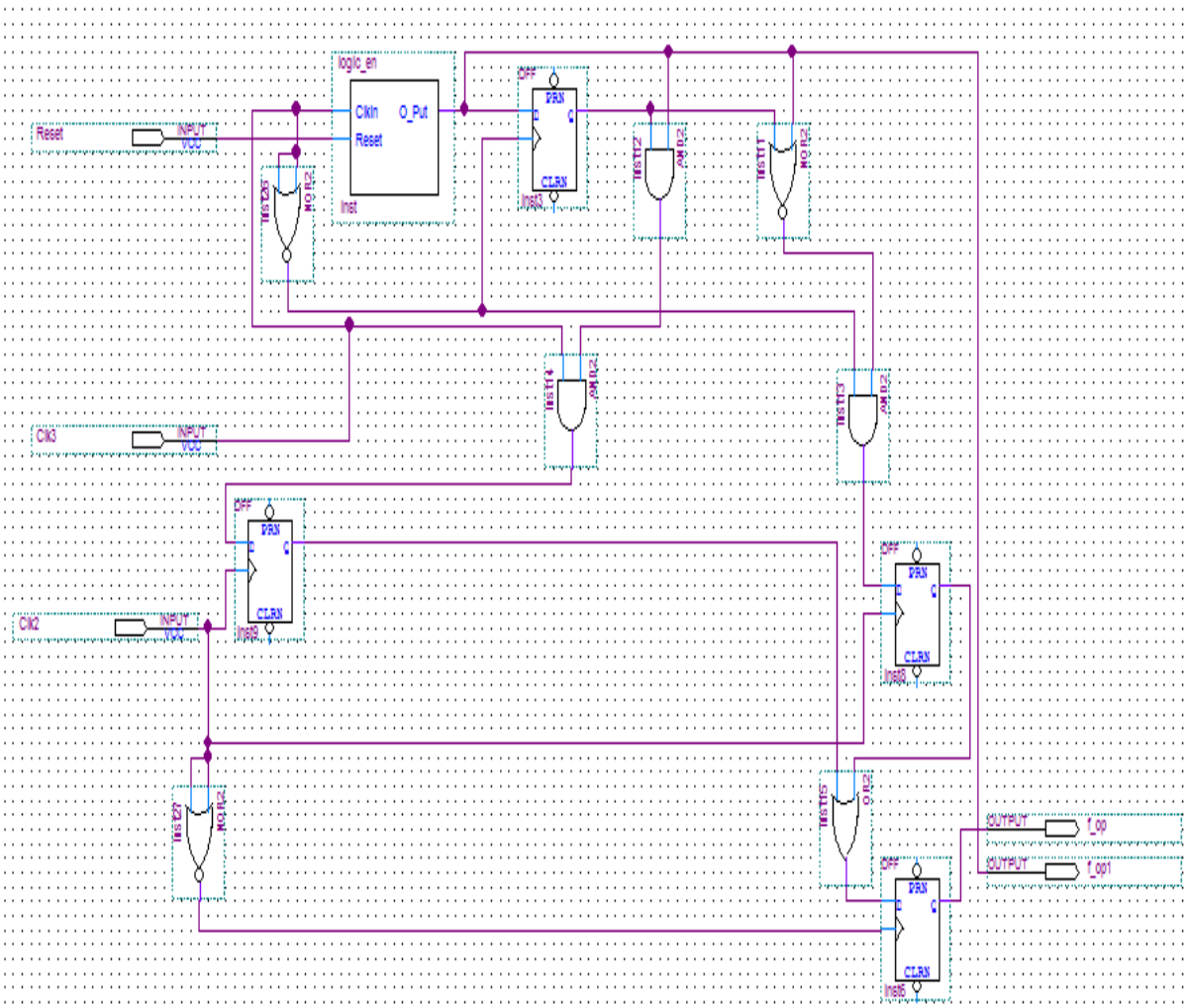


Fig. 7.6: Duobinary PPM encoder logic circuit schematic.

The simulation waveform of the duobinary PPM coder is given in the figure 7.7 below. The waveform is annotated and it is clearly noticeable that the PCM data has been successfully coded into duobinary PPM data according to the theoretical table given in chapter 3.2 (Table 3.1). Start positions of PCM input to valid DuoPPM encoded output are marked by purple boxes in the waveforms for both figures 7.7 and 7.8 (following page).

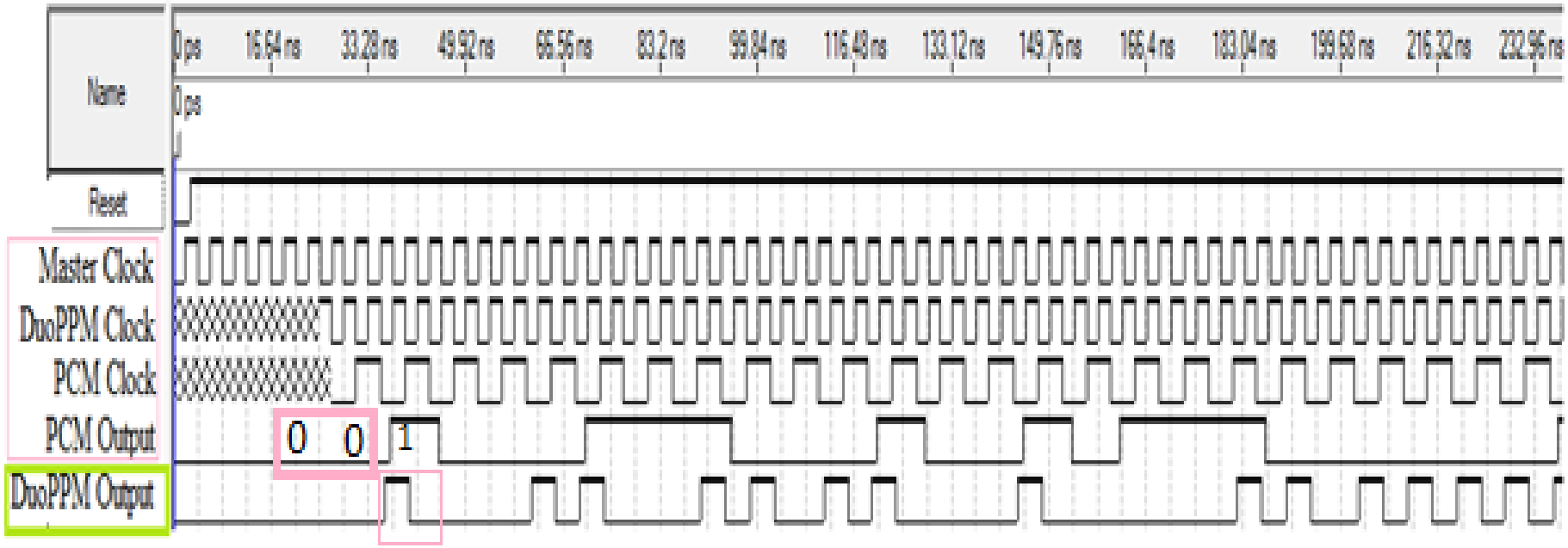
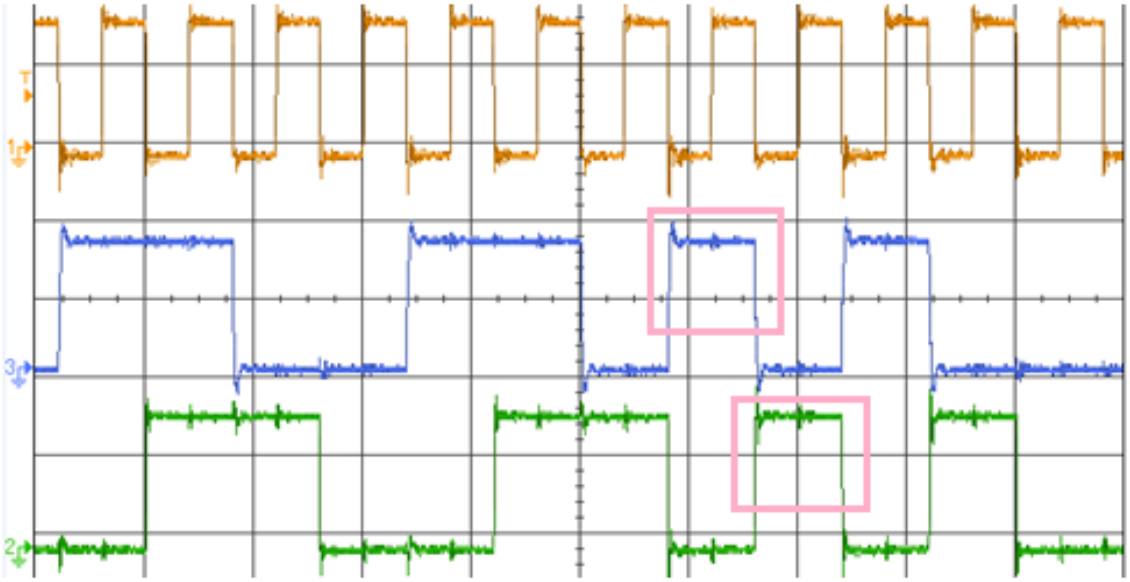
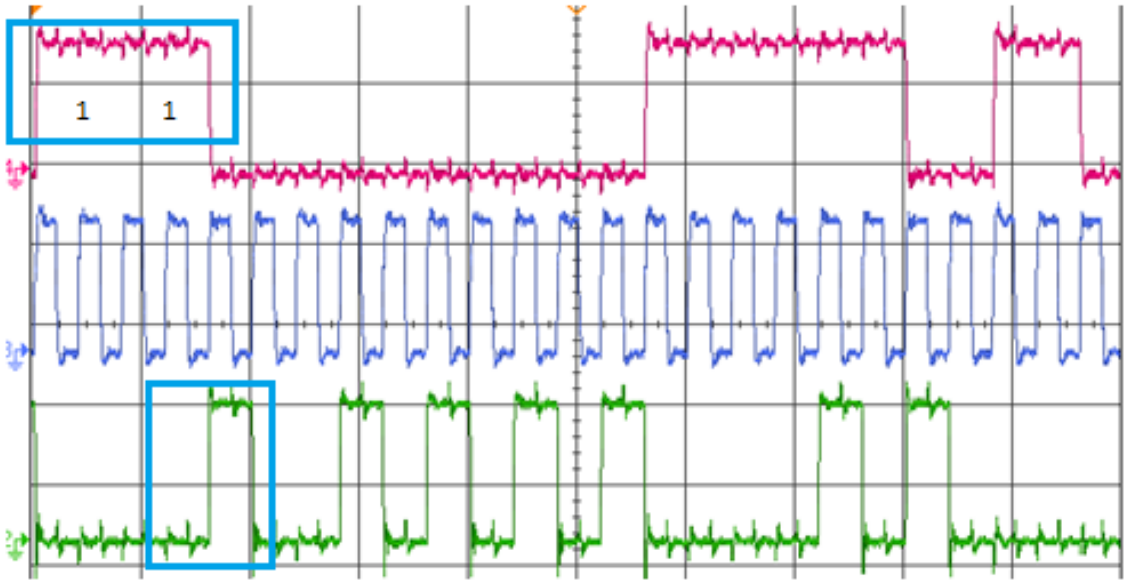


Fig. 7.7: Duobinary PPM encoder VHDL simulation results.

Experimental verification results of the duobinary PPM coder is given in figure 7.8 below.



(a)



(b)

Fig. 7.8 (a) and (b): Experimental results of duobinary PPM coder (a) top trace is the PCM clock and bottom trace is one clock cycle shifted PCM data (middle trace) and (b) bottom trace is the coded duobinary PPM data. PCM data (Top trace) and clock (middle trace)

7.5 Duobinary PPM Decoder

A PCM transitions of 1 to 0 and 0 to 1 no pulses were produced (Table 3.1). Therefore, decoding the parts of DuoPPM sequence when no pulses were available had to be carefully considered to decode the correct PCM sequence. There are two probable PCM sequences when no duobinary PPM pulses were received consecutively: PCM transition of 1 to 0 and PCM transition of 0 to 1. This decision can be made if the position of the most recently received pulse, before the sequence of no pulse (C), is known. If the most recently received pulse is in slot 0 then the PCM sequence will be 1, 0, 1, 0…and so on; and if it is in slot 1 then the PCM sequence will be 0, 1, 0, 1…and so on. Therefore, a temporary memory block had to be designed using D-Type Flip-flops (DFF) and logic gates to store the most recently received DuoPPM pulse position. The logic components that have been used to complete the duobinary PPM decoder are 12 DFFs, 6 XOR gates, 2 NOT gates, 1 XNOR gate, 2 NAND gates and 8 AND gates. The complexity of the decoder design increased due to be able to correctly decode PCM sequences when there were no pulses (C) received in DuoPPM sequence. Figure 7.9 in the following page shows the schematic diagram of the design that has been implemented.

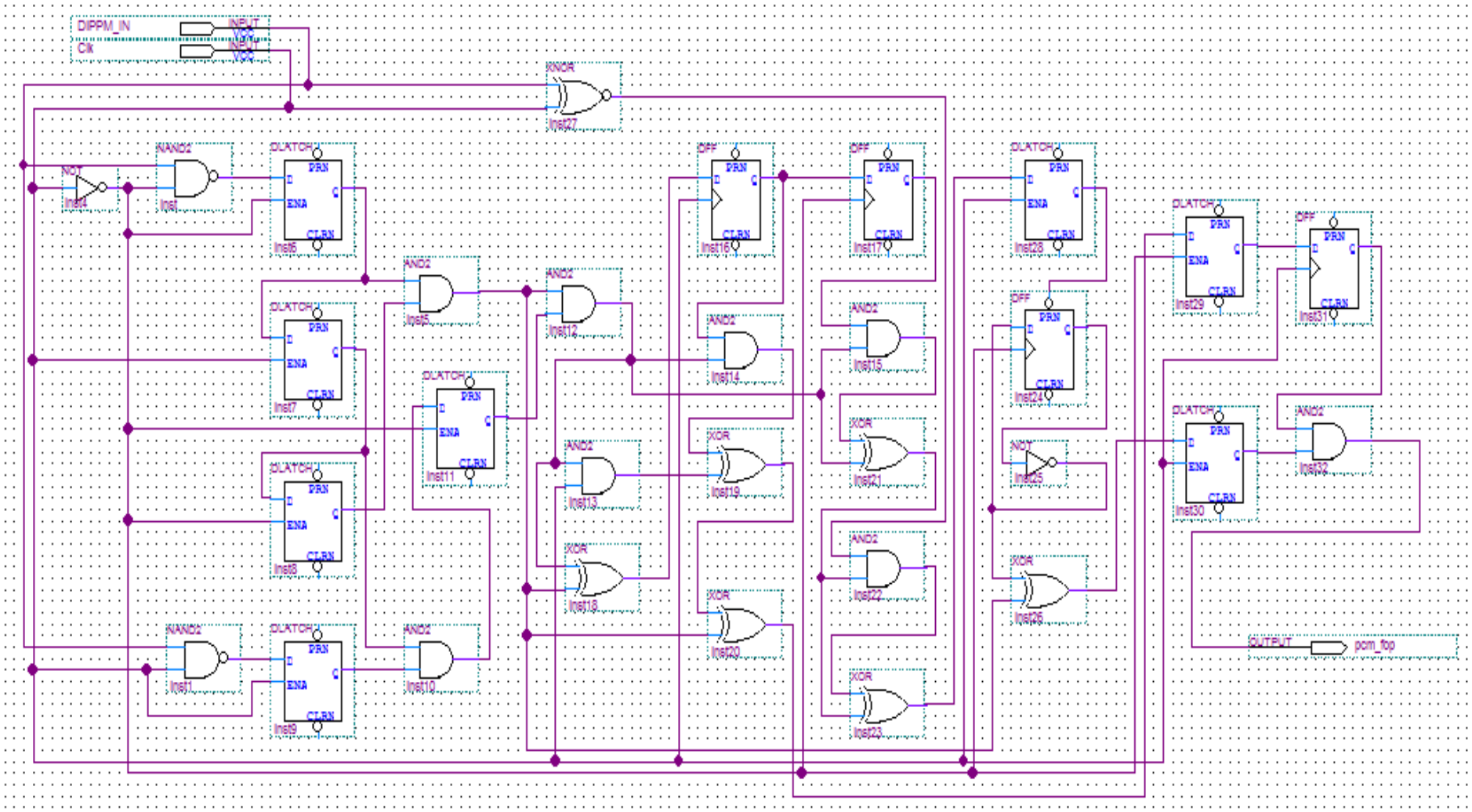


Fig. 7.9: Duobinary PPM decoder logic circuit schematic.

The simulation waveform of the duobinary PPM decoder is given in the figure 7.10 in the following page. The waveform is annotated and it is clearly noticeable that the duobinary PPM data has been successfully decoded into original PCM data according to the theoretical table given in chapter 3.2 (Table 3.1). There is a delay between the input PCM and the output PCM as shown by the pink boxes in the figure 7.10 below. This is due to MLSD coding blocks being in between coder and decoder. The signals from MLSD has been omitted for this section as they will be discussed in detail later in this chapter.

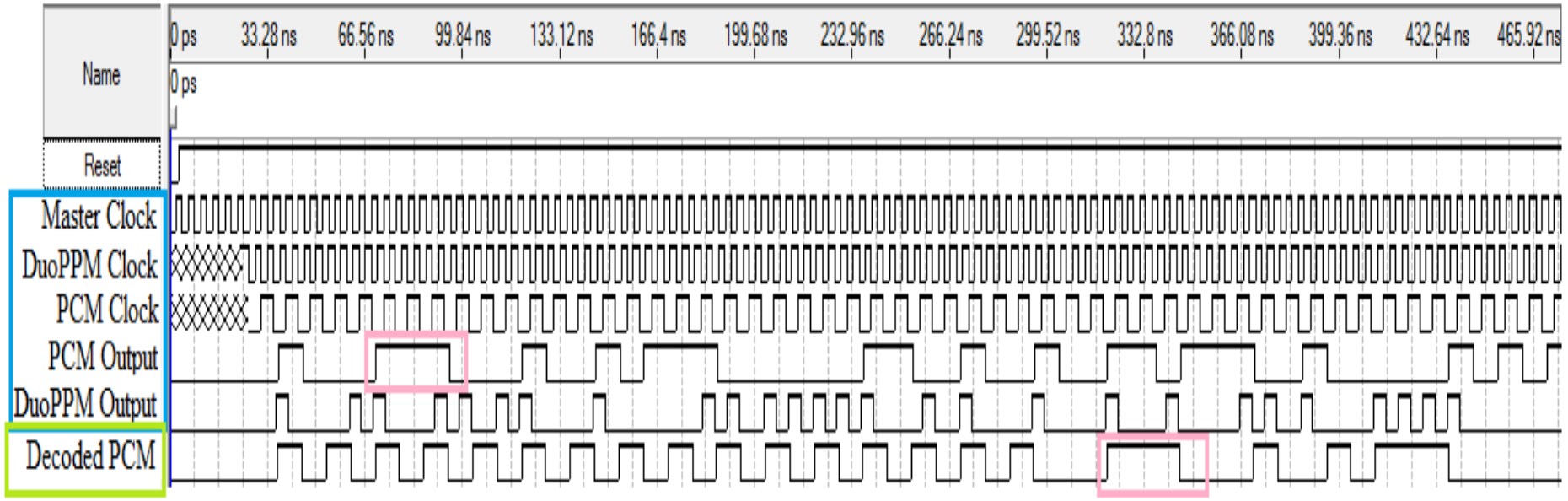


Fig. 7.10: Duobinary PPM decoder VHDL simulation results.

Experimental verification results of the duobinary PPM decoder is given in figure 7.11 below. There is a long delay between PCM output and Decoded PCM similar to figure 7.10 in the previous page, therefore first and second traces of the waveform have been shifted using DFFs to show all three waveforms clearly in the same screenshot.

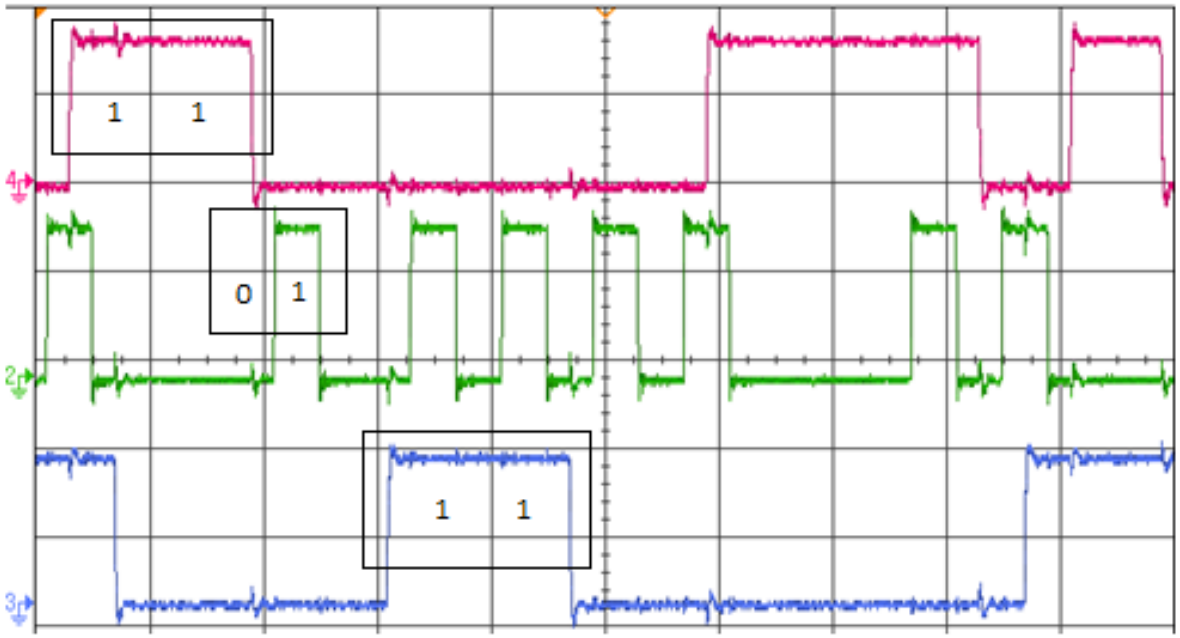


Fig. 7.11: Experimental verification of DuoPPM decoder: PCM input (top trace), DuoPPM (middle trace) and decoded PCM (bottom trace).

7.6 Bit Error Rate (BER) Test Circuit

The coder, decoder and MLSD of the duobinary PPM coding system has been implemented using VHDL and FPGA thus it was imperative to have a bit error rate test (BERT) system available integrated with this system in order to be able to monitor the errors and calculate the link sensitivity while the system is operational in real time. To implement BERT, first it was important to modify the PCM data generation system which has been discussed in section 7.3. The modification was to make the pseudo random binary sequence (PRBS) data generation maximum length theoretically possible for the given bits of shift register because in this way once this PRBS data is decoded at the receiver then known sequences will appear given the data has not been significantly corrupted with errors.

A design flow block diagram of the BERT system designed for duobinary PPM system is given in the figure 7.12 in the following page. In duobinary PPM coding system, an 8-bit PRBS generator has been used thus it is known that every random sequence of 255 bits PCM data will contain a sequence of 8 consecutive 1s (‘11111111’). Therefore, when the duobinary PPM data is decoded back to PCM it is sent to the BERT system where a sequence detector has been designed to detect the sequence of ‘11111111’ in the PCM data. Once this sequence has been detected, the circuit fills the 8-bit shift register of the PRBS generator with ‘01111111’ which will be the next shift of the register after ‘11111111’ therefore the regenerated PCM will be at the same point and phase as the original PCM data.

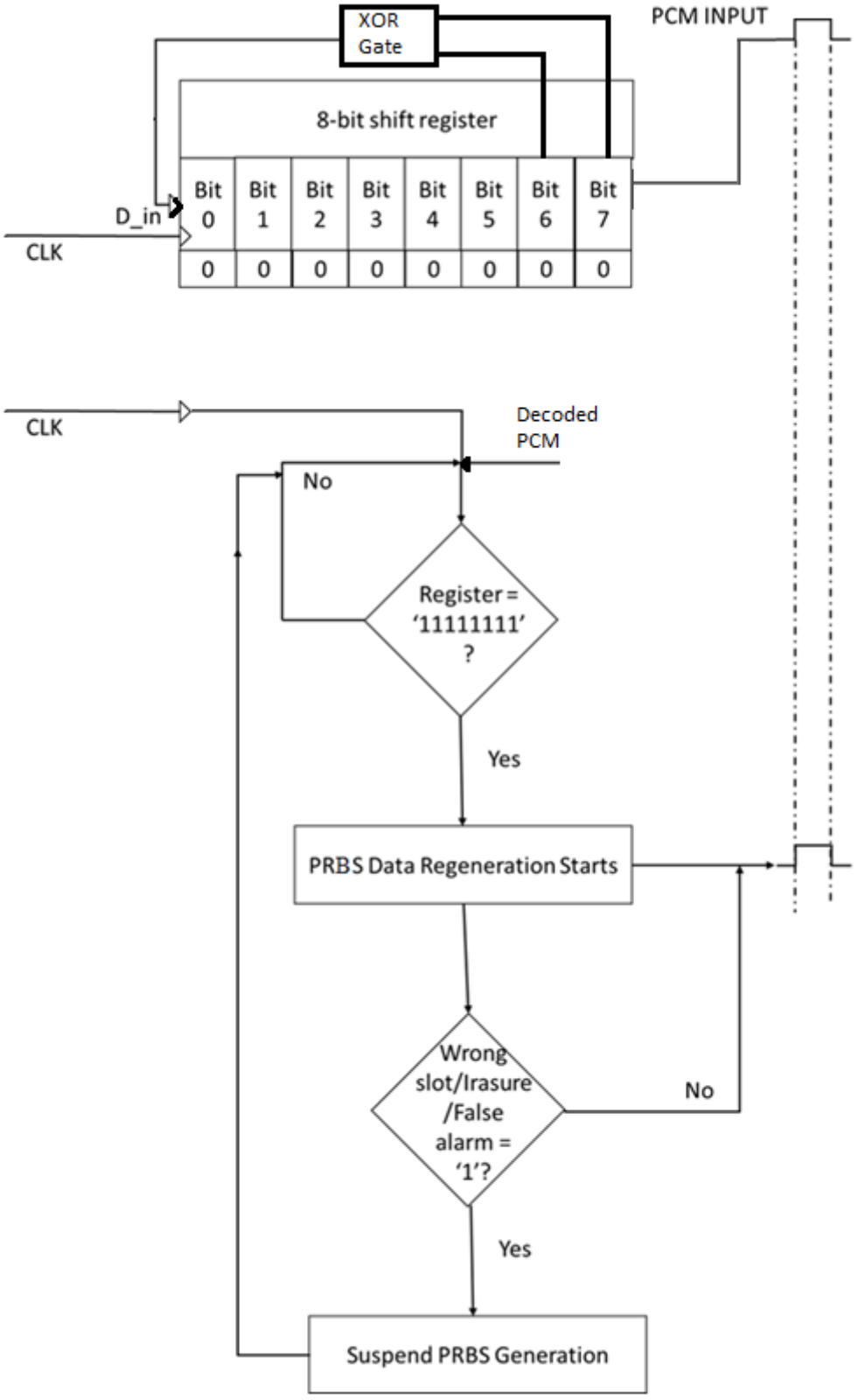


Fig. 7.12: Design flow block diagram of BER test circuit using VHDL.

The key section of the sequence detection code is given below in listing 7.2. The PRBS generator code has not been repeated since they are same as the code discussed previously in section 7.3.

```
SIGNAL internal_reg1    : std_logic_vector (0 TO 7) := "00000000";
SIGNAL Tmp              : std_logic_vector (0 TO 7)  := "01111111";
SIGNAL load             : std_logic := '1';

IF (Reset = '0') THEN
internal_reg1 <= "00000000";
Tmp           <= "01111111";
load          <= '1';

IF (internal_reg1 = "11111111") THEN

load        <= '0';
first_tap   := Tmp (3) xor Tmp (4);
second_tap  := Tmp (5) xor Tmp (7);
third_tap   := first_tap xor second_tap;
Tmp         <= third_tap & Tmp (0 TO 6);

PCM_Regen <= Tmp (0);

ELSIF (load = '1') THEN
internal_reg1 <= internal_reg1 (1 TO 7) & duoppm;
```

Listing 7.2: Key sections of the BERT sequence detector.

In listing 7.2, it can be seen that there are three key section of the code. In the top box (pink), an internal register is used to keep the incoming sequence of PCM data and a load signal which goes high at the start of every clock to load the incoming PCM data into the checking register. In the middle box (brown), the registers and the load signal is initially reset and in the bottom box (green), first the code checks if the required sequence has been received. If the required sequence has been received the PRBS data regeneration starts as shown in figure 7.13 in the following page and the load signal is set to active LOW. Finally, the program checks whether the load signal is active HIGH, if so then the circuit loads the input PCM data to the internal checking shift register to complete the operation of the BERT system. Experimental verification results of the BERT is also given in figures 7.14, 7.15 and 7.16 later in the section.

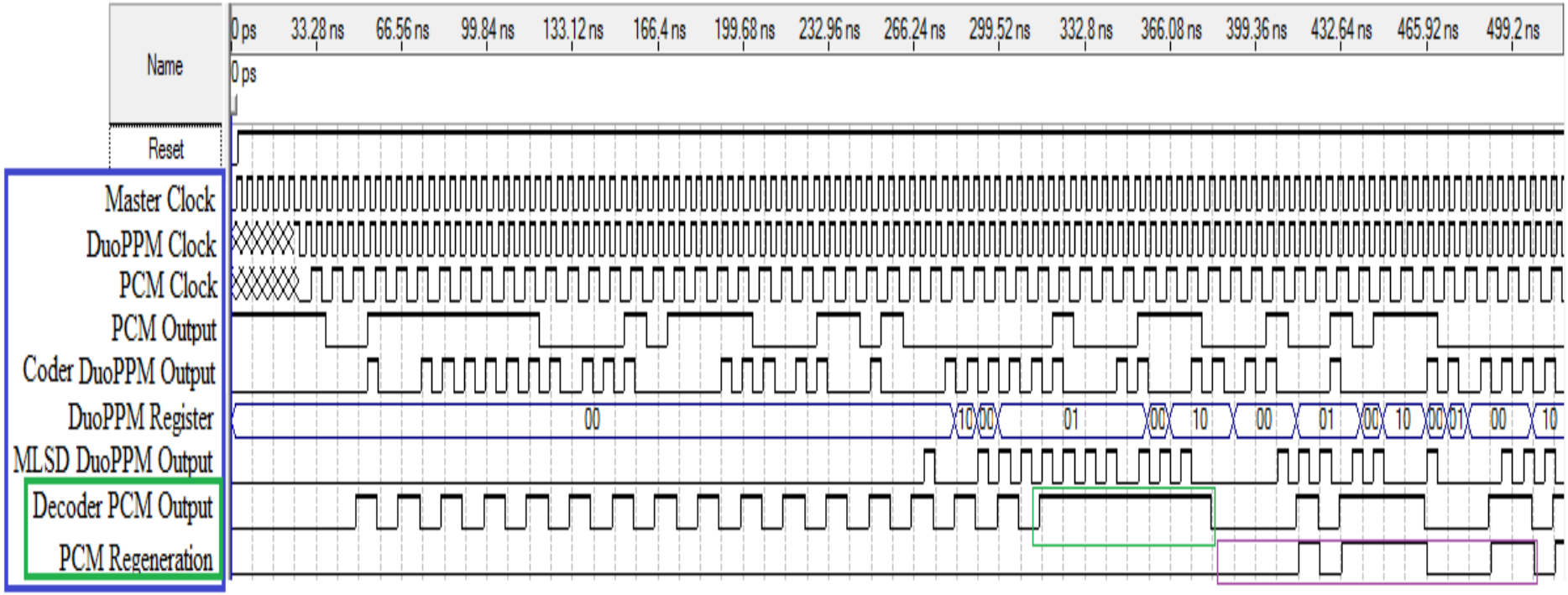


Fig. 7.13: VHDL simulation results of the duobinary PPM BERT system.

The last two (left hand side green box) signals in the output waveform in figure 7.13 shows the original decoded PCM output and the BERT regenerated PCM signal and as can be seen further down the waveform marked in coloured boxes that once the sequence ‘1111111’ is received by the BERT system it start regenerating in-phase identical PCM signal thus both can be compared to check for errors.

Experimental verification of the design using FPGA has been successfully completed as well and the results are given in the figures below.

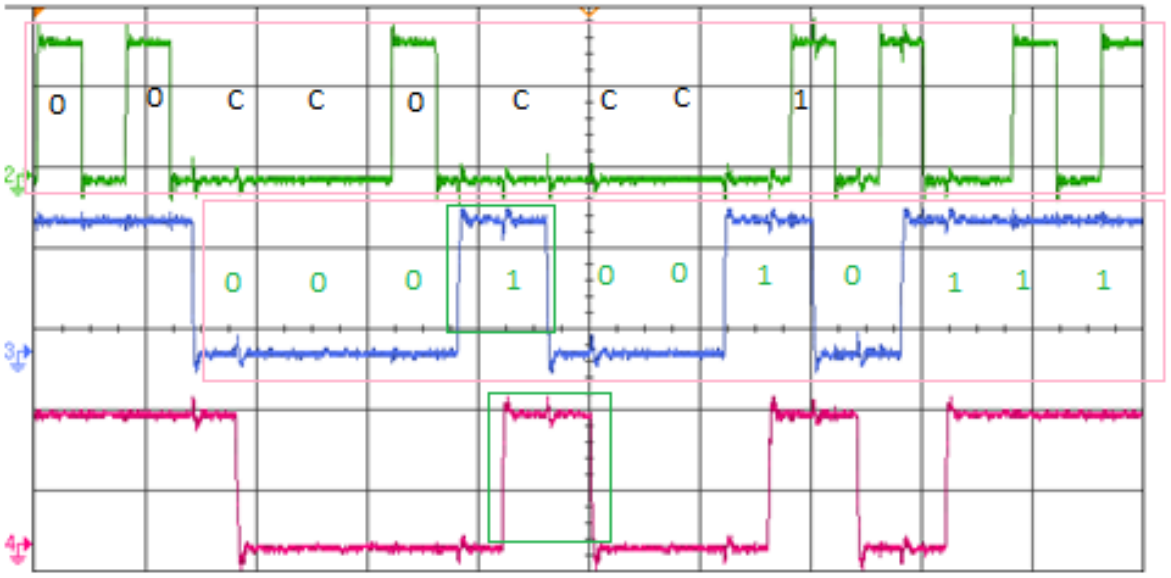


Fig. 7.14: Experimental verification of BERT system: duobinary PPM (top trace), decoded PCM (middle trace) and regenerated PCM (bottom trace).

It is evident from figure 7.14 that the BERT system has successfully regenerated the required PCM data, however, it is out of phase. Therefore, a delay was introduced to bring both PCM data streams as has been shown in figure 7.15 in the following page of this section.

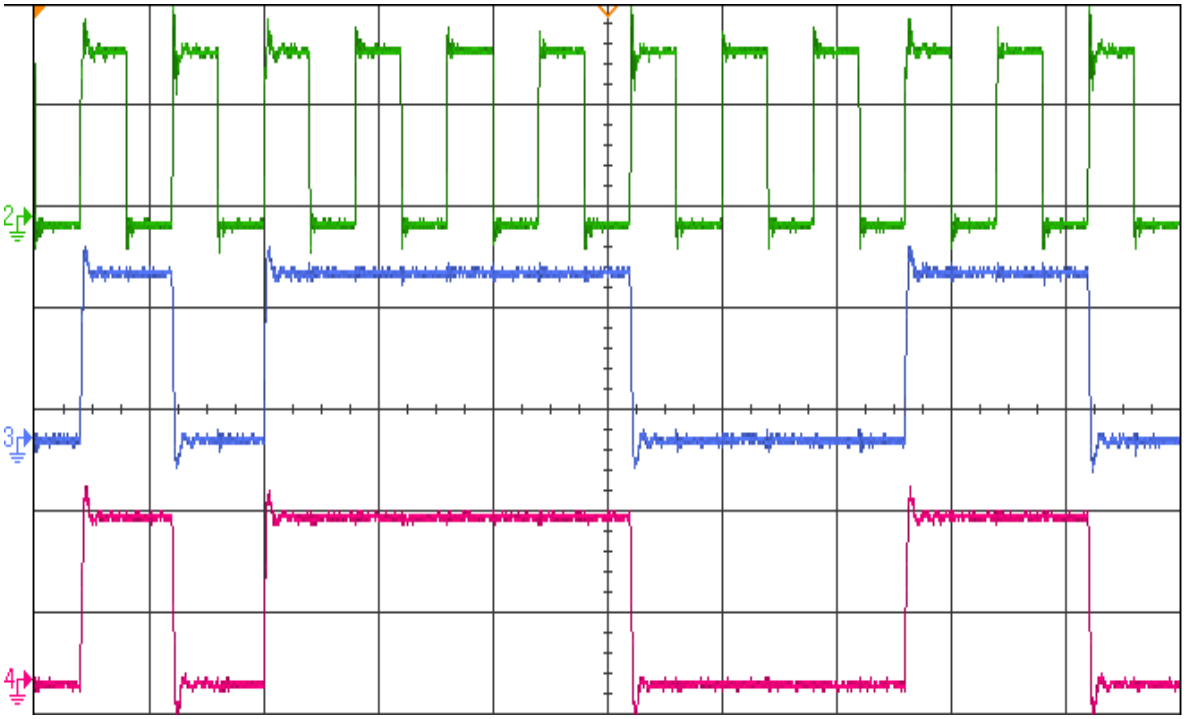


Fig. 7.15: Experimental phase synchronised PCM data for BERT: PCM clock (top trace), decoded PCM (middle trace) and regenerated PCM (bottom trace).

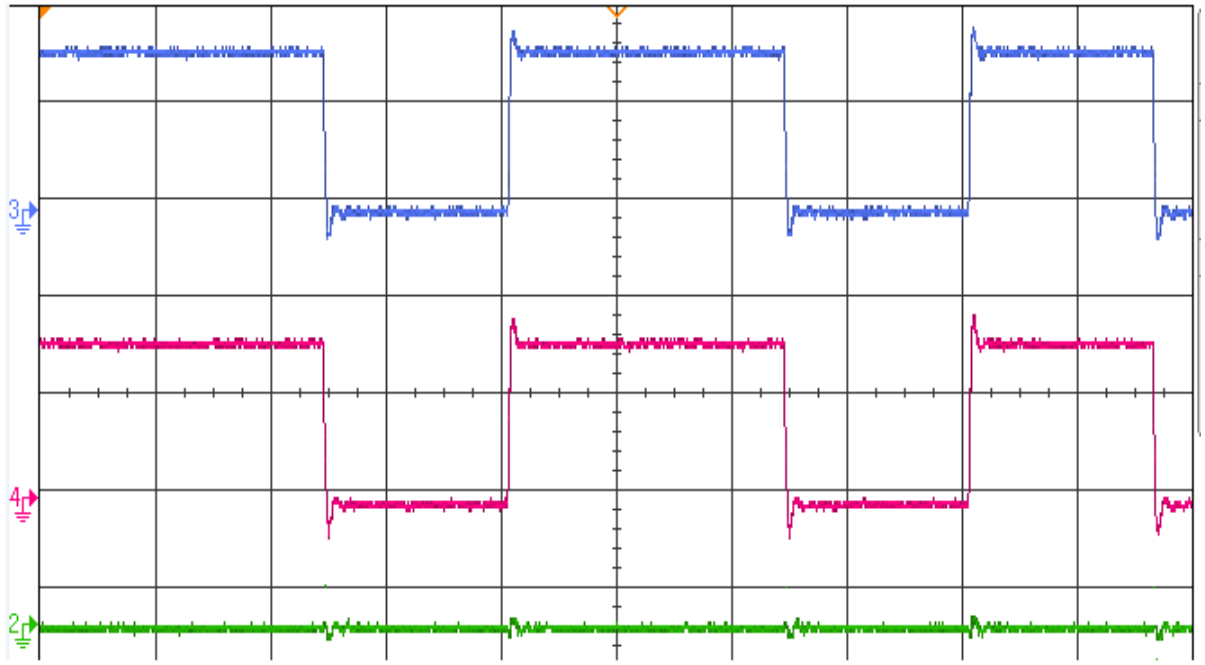


Fig. 7.16: Experimental error output for BERT system: decoded PCM (top trace), regenerated PCM (middle trace) and error output (bottom trace).

7.7 FPGA Implementation of Duobinary PPM MLSD

7.7.1 Duobinary PPM MLSD Design Description

The final stage of the design and implement the duobinary PPM coding system using VHSIC hardware description language (VHDL) and field programmable gate array (FPGA) is to complete an integrated system design. Previously attempts have been made [4] to implement MLSD schemes of other channel coding scheme using discrete logic. However, as the systems becomes more complex the device becomes bulky and compromises need to be made regarding reduction of inherent complexity. The modern FPGA processing power and VHDL design capability means that with expertise of programming and design any complex systems such as MLSD can be easily implemented without making any compromises. Figure 7.17 in the following page shows a proposed system for MLSD implementation of duobinary PPM [27].

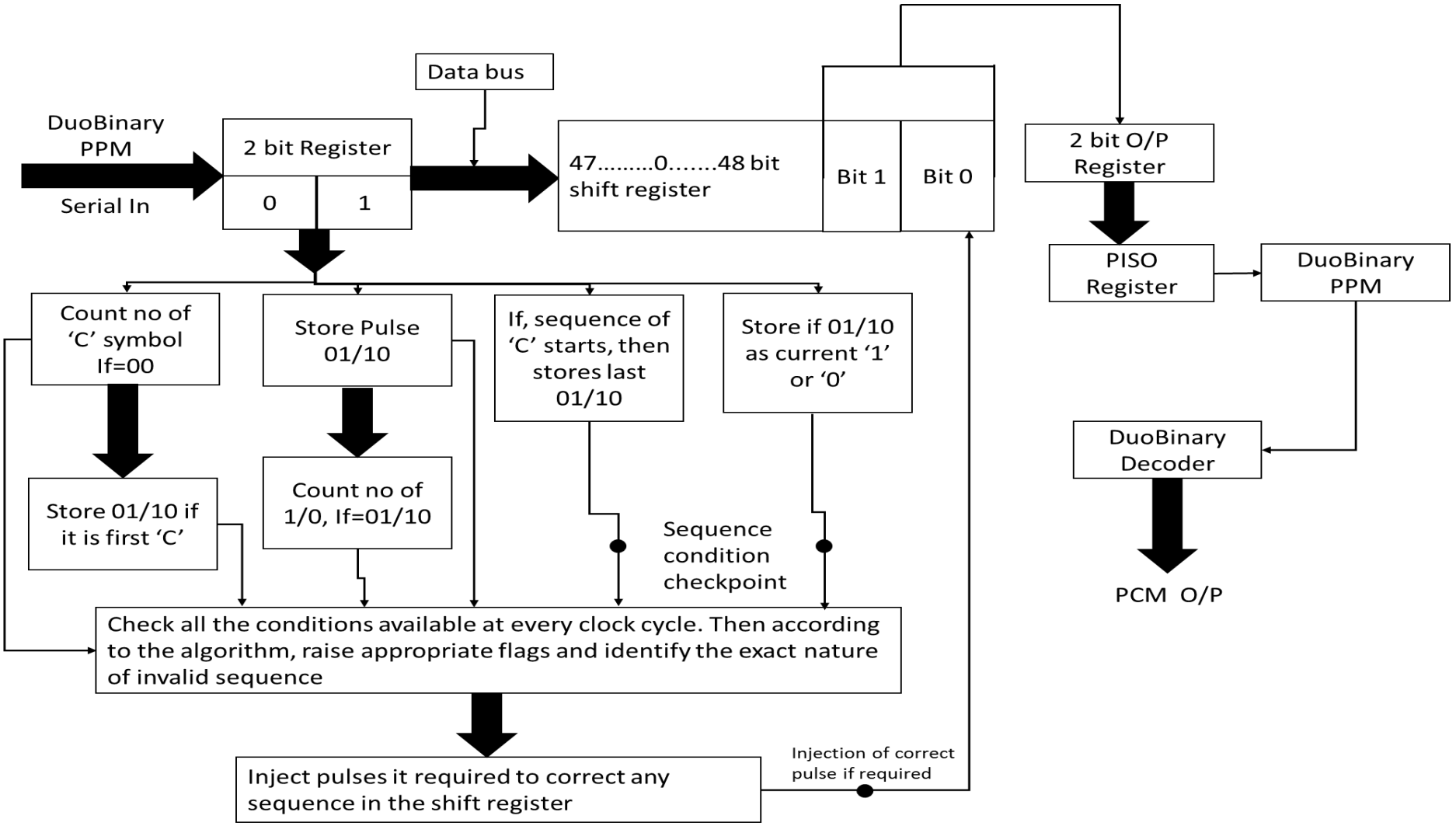


Fig. 7.17: Block diagram of proposed MLSD implementation using VHDL and FPGA.

In the design shown in the previous page, input duobinary PPM data will be stored in a two-bit register according to slot and frame synchronisation. Therefore, the two-bit register will hold a complete frame of the duobinary PPM. Another 48-bit internal register will hold 24 frames of duobinary PPM data at given time. Any two bit incoming data will be added in the 48-bit register as this acts as shift register where correction will take place and the last two-bits will be corrected output at every clock cycle. Maximum number of like symbols has been assumed to be 10 thus 24 frames in the shift register. However, any good VHDL design is easily scalable and higher number can be implemented easily. 24 frames of duobinary PPM include two complete sequences of maximum length for error detection and correction purpose.

An example would be, 1 10C 1 10C 11 where 24 frames complete that whole sequence. Every time as frame is received checks are made for variables such as counters to count number of Cs or number of 1s and 0s, first symbol of a sequence, middle pulse if there are two sequences, last symbol of the sequence. If there are errors, flags are raised for any of the three errors and exact location of the error is determined. If flag is raised the corrector will correct the required frames and output will be last two bits of the 48-bit shift register. Currently work is being carried out to implement the MLSD using VHDL and FPGA completed with bit error rate test system embedded in the device. Results of the practical implementation will be published soon upon successful completion.

A design flow block diagram of the frame count mechanism is given in the next page in figure 7.18. Main segments of the MLSD coding block will be discussed later in the section. MLSD coding block receives input as 2-bit register which contains a complete frame of duobinary data with two slots. This is delivered by a previous design of 2-bit SIPO shift register synchronised correctly with the clock.

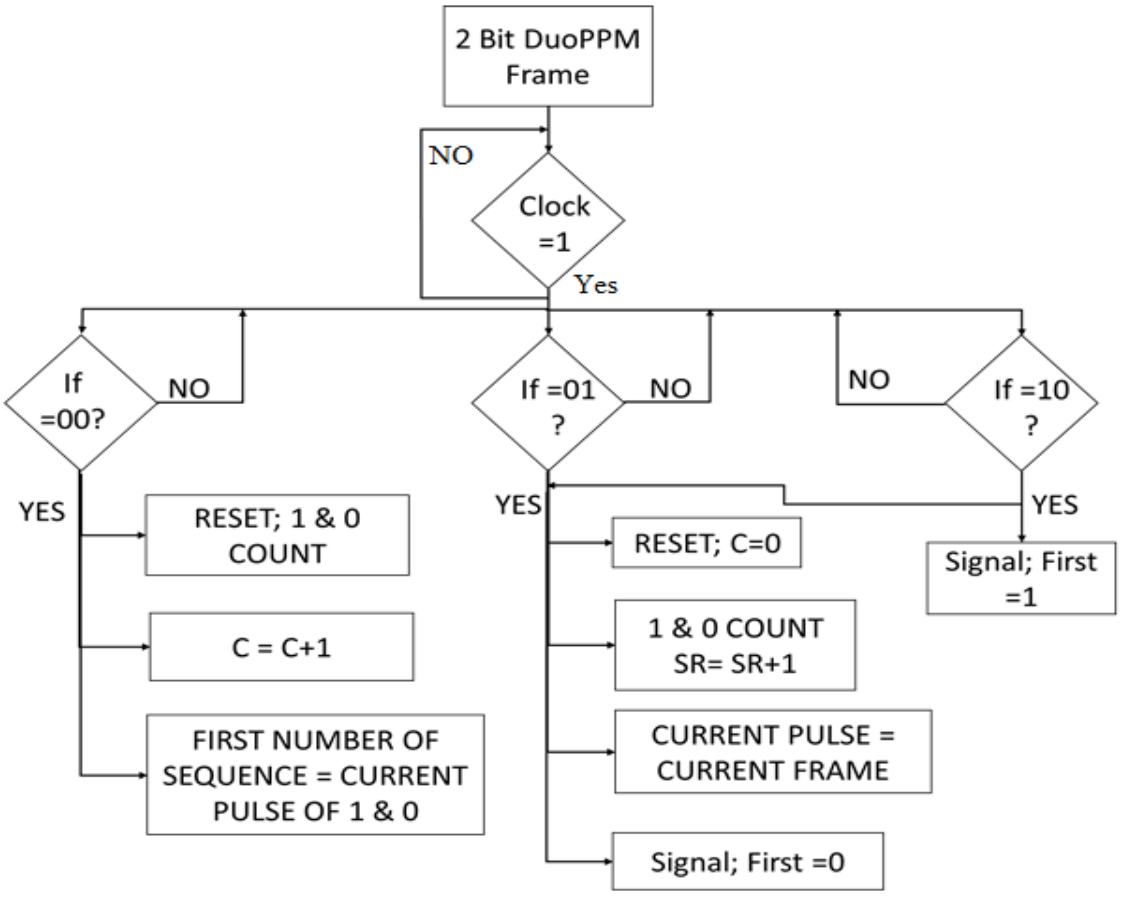


Fig. 7.18: Design flow diagram to register various information of received sequences from the duobinary PPM data frame.

The MLSD code in its entirety is given in Appendix 3. As discussed at the beginning of the section, a 48-bit SISO shift register has been used to store duobinary PPM data for detection and correction of error. The main reason a 48-bit serial in serial out (SISO) shift register was used in the design to hold minimum two complete data sequences (assuming, maximum number of consecutive Cs (no pulse) is 10, for simplification of design) as it was understood that, for some instances, an error in PRESENT data sequence can be detected due to an error in PREVIOUS data sequence and it can be corrected in the PRESENT data sequence. Otherwise both data sequences will be corrected thus possibly violating both data sequences and increasing the possibility of error. This is the main reason to use a 48-bit SISO shift register so that minimum two complete consecutive data sequences can be looked at during correction process.

Listing 7.3 below shows a segment of MLSD code that counts the number of Cs, 1s and 0s according to the incoming data frame and determines and stores the first and last symbols of data sequence and also stores the current symbol as can be seen from the code below. The signal 'regConCat' is the duobinary frame.

```
IF (regConCat = "00")THEN

                countSR <= "0000";
                countC <= countC + "0001";
                f_num  <= cc;
ELSIF (regConCat = "10")OR (regConCat = "01") THEN

                countC <= "0000";
                countSR <= countSR + "0001";
                cc <= regConCat;
                IF (regConCat = "10")THEN
                one <= '1';
                ELSE
                one <= '0';
                END IF;
END IF;
```

Listing 7.3: Duobinary PPM symbol counter for sequence characterisation in VHDL.

There were many internal registers and signals that were necessary to implement the MLSD. Listing 7.4 in the following page shows the internal registers and signals used to raise three different types of error flags and storing the types of errors as binary numbers as shown in the code.

```
SIGNAl w_slot            : std_logic;
SIGNAl w_slotR           : std_logic;
SIGNAl f_alrm            : std_logic;
SIGNAl wrongslot_det     : std_logic_vector (1 downto 0);
SIGNAl wrongslot_flg     : std_logic_vector (3 downto 0);
SIGNAl wrongslotR_flg    : std_logic_vector (4 downto 0);
SIGNAL false_alm         : std_logic_vector (5 downto 0);
```

Listing 7.4: Internal signals and registers for error flags and error type information storage for MLSD.

As the MLSD code will be storing two complete sequences, the data from the previous sequence need to be stored before start counting and characterising the current sequence and this done by the segments of the code given in the listing 7.5 below.

```
WAIT UNTIL (Clk' EVENT AND Clk = '0');
IF countC > "0000" THEN
dly_C <= countC;
ELSIF countC = "0000" THEN
dly_C <= dly_C;
    IF countSR >= "1111" THEN
        dly_C <= "0000";
    ELSE dly_C <= dly_C;
END IF;
```

Listing 7.5: Storing data of previous sequence C counts in MLSD.

The code above is for count of Cs from the previous sequence and the count of 1s and 0s are done similarly thus the code has not been shown[20]. Once the frame has been counted and sequence characterised, these data are them used in a nested IF-ELSE programming statements to consider all the possibilities that can give rise to an invalid sequence and for all possible invalid sequences.

[20] Available in Appendix 3.

```
IF (wrongslot_det = "01") AND (cc = "01") THEN  --err of 101

        wrongslot_flg   <= "0101";
        wrongslot_det   <= "00";
        w_slot          <= '1';


 ELSIF (countSR = "0001") AND (wrongslot_flg = "0000") AND (f_num = "01") AND (cc = "01")AND (dly_C = "0001") THEN   --1C1

       false_alm <= "000001";

 ELSIF (countSR = "0001") AND (wrongslot_flg = "0000") AND (f_num = "01") AND (cc = "10")AND (dly_C = "0010") THEN

       false_alm <= "000010";

ELSIF (wrongslot_flg    = "0010") AND (countSR = "0001") AND (dly_C = "0100") AND (cc = "01") THEN  --err of 10C 4 iCorrect

        wrongslot_flg   <= "0000";
        w_slotR         <= '1';
        wrongslotR_flg  <= "10110";
        false_alm <= "000000";
        f_alrm  <= '0';

ELSIF (wrongslot_flg    = "0010") AND (countSR = "0001") AND (dly_C = "0101") AND (cc = "10") THEN  --err of 10C 5 iCorrect

        wrongslot_flg   <= "0000";
        w_slotR         <= '1';
        wrongslotR_flg  <= "10111";
        false_alm <= "000000";
        f_alrm  <= '0';
```

Listing 7.6: Programming conditions to check for invalid sequences and raise appropriate flags.

The code listing above shows part of each type of conditional checking to raise flag and characterise exactly what the error is so that it can be corrected in the final stage. It gives examples of each type of error checking. Top box in green is for wrong-slot error check, middle box in blue is the check done for false-alarm errors by checking appropriate conditions and the bottom brown box is for erasure error check of the MLSD system. The code listed in listing 7.7 in the following page shows how the error types are corrected when any error flags are raised.

```
ELSIF Reset = '1' THEN
            regOP1  <= IP1 & regOP1 (47 downto 2);
            regOP2  <= IP1 & regOP2 (47 downto 2);

            IF (w_slot = '1') THEN

            CASE wrongslot_flg IS
            WHEN "0110" => regOP1  <= IP1 & regOP1  (n-1 downto 42) & "10" & regOP1  (39 downto 2);
            WHEN "0101" => regOP1  <= IP1 & regOP1  (n-1 downto 42) & "01" & regOP1  (39 downto 2);
```

```
ELSIF (w_slotR = '1') THEN


CASE wrongslotR_flg IS

WHEN "00100" => regOP1  <= IP1 & regOP1  (n-1 downto 42) & "00" & regOP1  (39 downto 2);
                regOP2  <= IP1 & regOP1 (n-1 downto 2);
WHEN "01010" => regOP1  <= IP1 & regOP2  (n-1 downto 40) & "10" & regOP2  (37 downto 2);
WHEN "01011" => regOP1  <= IP1 & regOP2  (n-1 downto 38) & "10" & regOP2  (35 downto 2);
WHEN "01100" => regOP1  <= IP1 & regOP2  (n-1 downto 36) & "10" & regOP2  (33 downto 2);
```

```
ELSIF (f_alrm = '1') THEN

regOP2  <= IP1 & regOP1 (n-1 downto 2);

CASE false_alm IS

WHEN "010011" =>   regOP1  <= IP1 & regOP1  (n-1 downto 42) & "01" & regOP1  (39 downto 2);
WHEN "010100" =>   regOP1  <= IP1 & regOP1  (n-1 downto 42) & "10" & regOP1  (39 downto 2);
WHEN "000001" =>   regOP1  <= IP1 & regOP1  (n-1 downto 40) & "01" & regOP1  (37 downto 2);
```

Listing 7.7: MLSD error correction mechanism using the raised flag and the detected types of errors: wrong-slot correction (top box), erasure correction (middle box) and false-alarm correction (bottom box).

Last two bits of the 48-bit shift register is always sent to the output of the MLSD as part of valid sequence.

7.7.2 Duobinary PPM MLSD Experimental Verification

It has been observed that the MLSD has been performing as required by the theory[21]. As it was tested both using simulation and experimental verification, the MLSD produced error free outputs which are shown in the waveforms in this section. BERT worked as intended with the system and shown in the waveforms as well. MLSD was simulated with deterministic errors in the code and found to be detecting and correcting errors as expected.

Deterministic error sequence and check was not possible for experimental verification due to lack of time available at the time as it requires erroneous sequences to be stored in the FPGA Memory module elements and access the transmission inputs from there. Further work is necessary and currently being carried out by the author to access and implement the FPGA memory functions to deterministic errors and correction procedure. A paper is also being written on the practical implementation and experimental verification of duobinary PPM MLSD and BERT. All the experimental verification produced correct results thus the reliability of the timing analysis simulation result means that it is fair to conclude that when the deterministic errors can be introduced in the system it will detect and correct the sequences as has been shown for the simulated results.

[21] Theoretical error sequences and correction table available in Appendix 5.

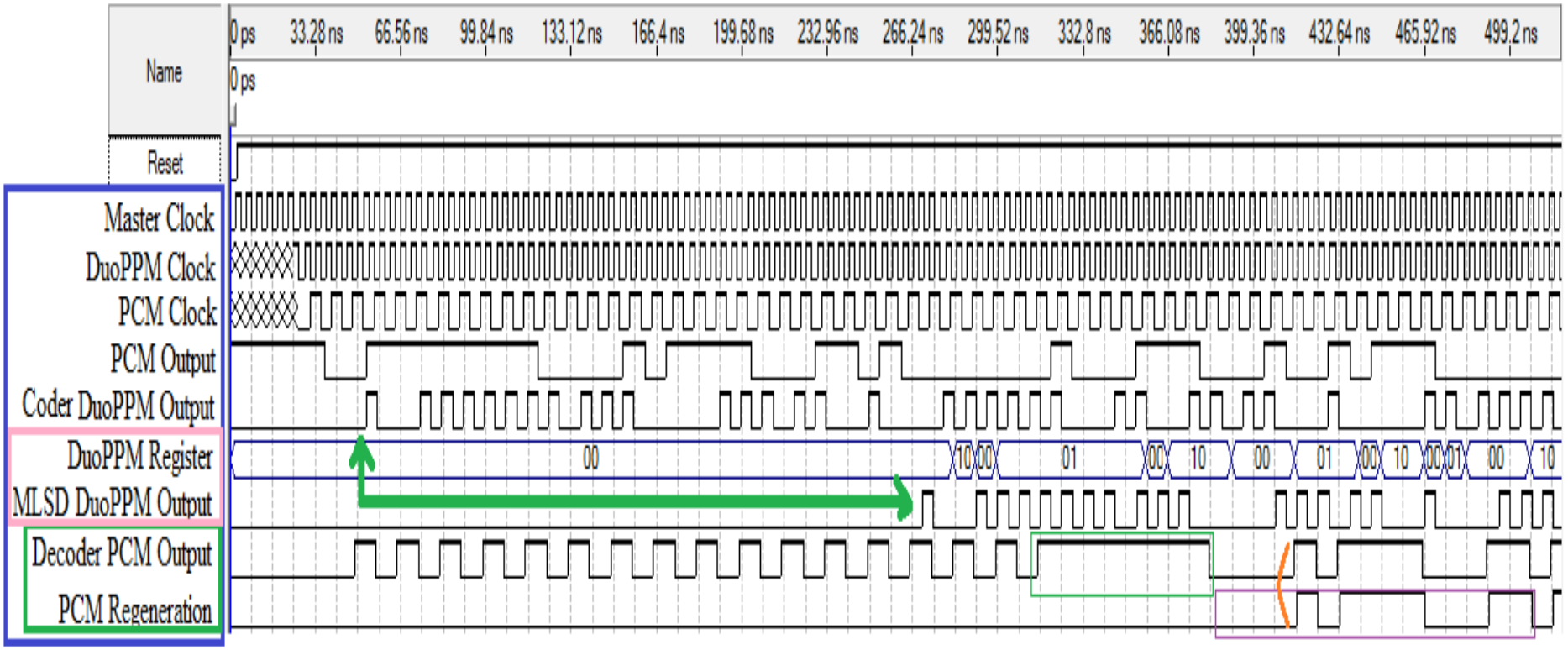


Fig. 7.19: Simulation of duobinary PPM operations when tested with deterministic PRBS PCM data of valid sequences.

As shown in the figure 7.19 above when tested with PRBS data no error was detected and corrected as was expected and BERT output shows that the input PCM data matches output PCM data therefore functionality is verified. Deterministic errors were inserted as duobinary PPM data stream and the errors flags and signal registers for error types have been observed at the output and they were all found to be performing as expected by the design.

Figures 7.20, 7.21 and 7.22 shows deterministic error detection and correction of wrong-slot, false-alarm and erasure errors respectively.

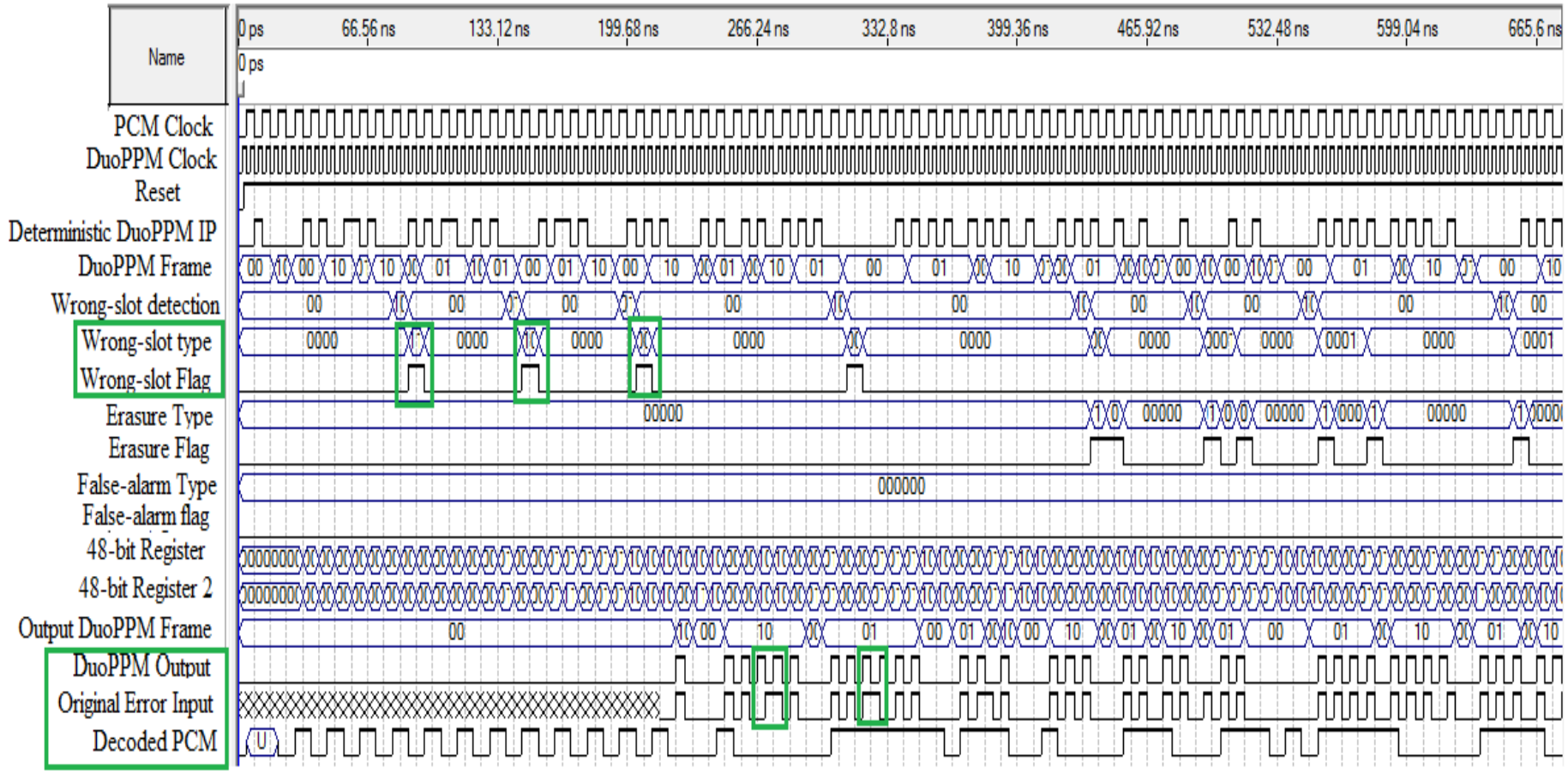


Fig. 7.20: Simulation of error detection and correction of wrong-slot errors.

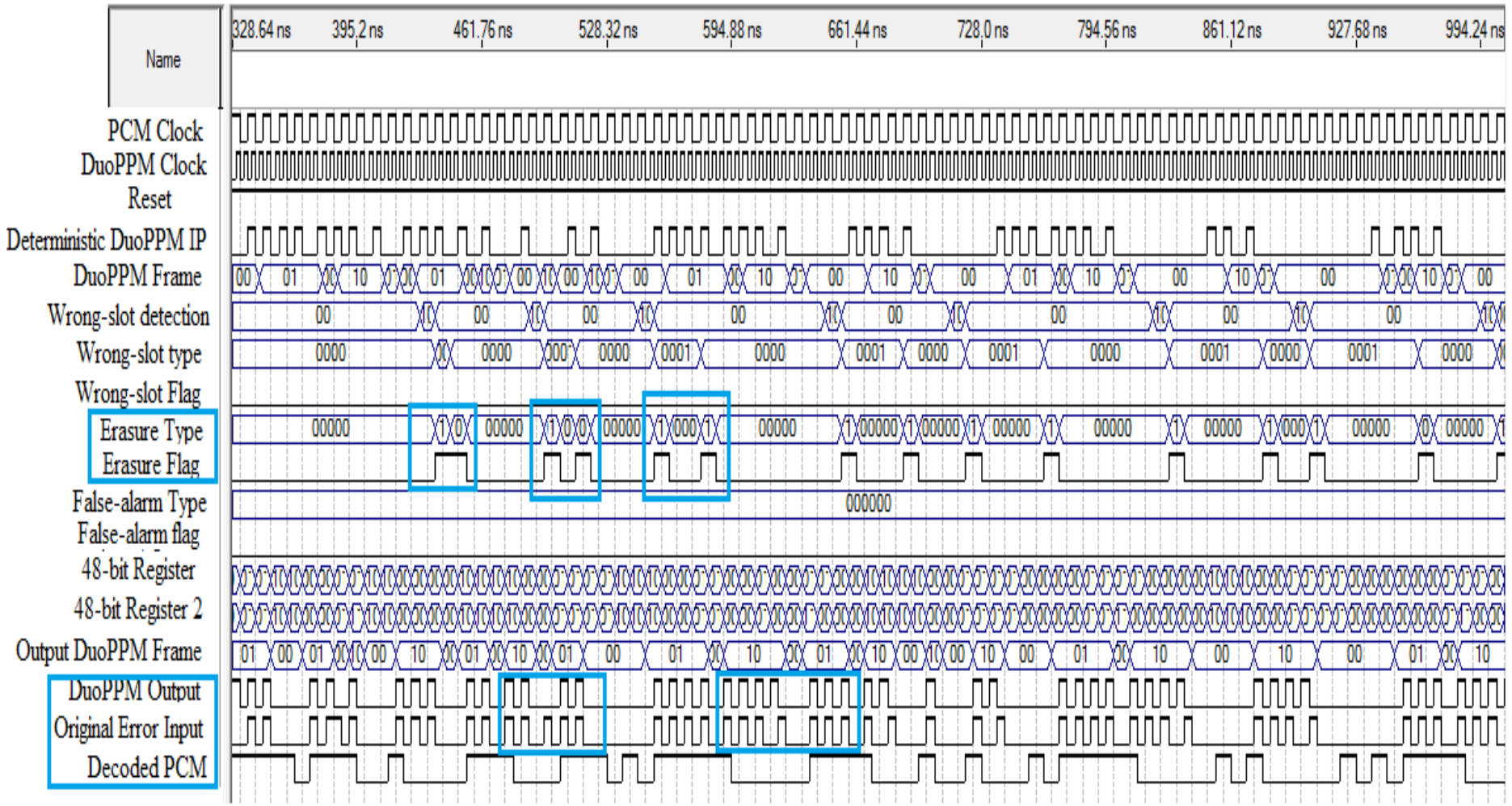


Fig. 7.21: Simulation of error detection and correction of erasure errors.

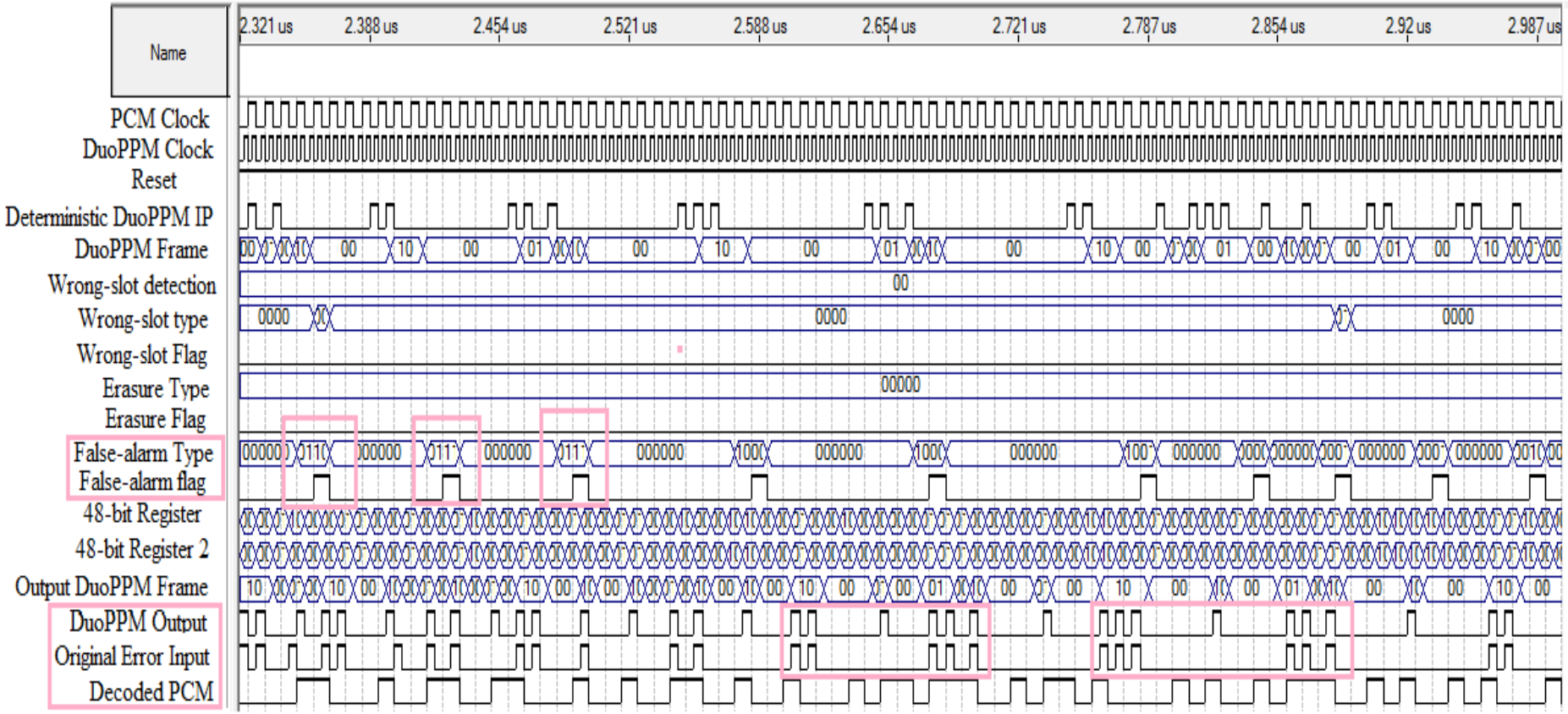


Fig. 7.22: Simulation of error detection and correction of false-alarm errors.

All types of errors detection and correction points are shown in coloured boxes. Given in the following page are the waveforms for experimental verification of the practical MLSD implementation.

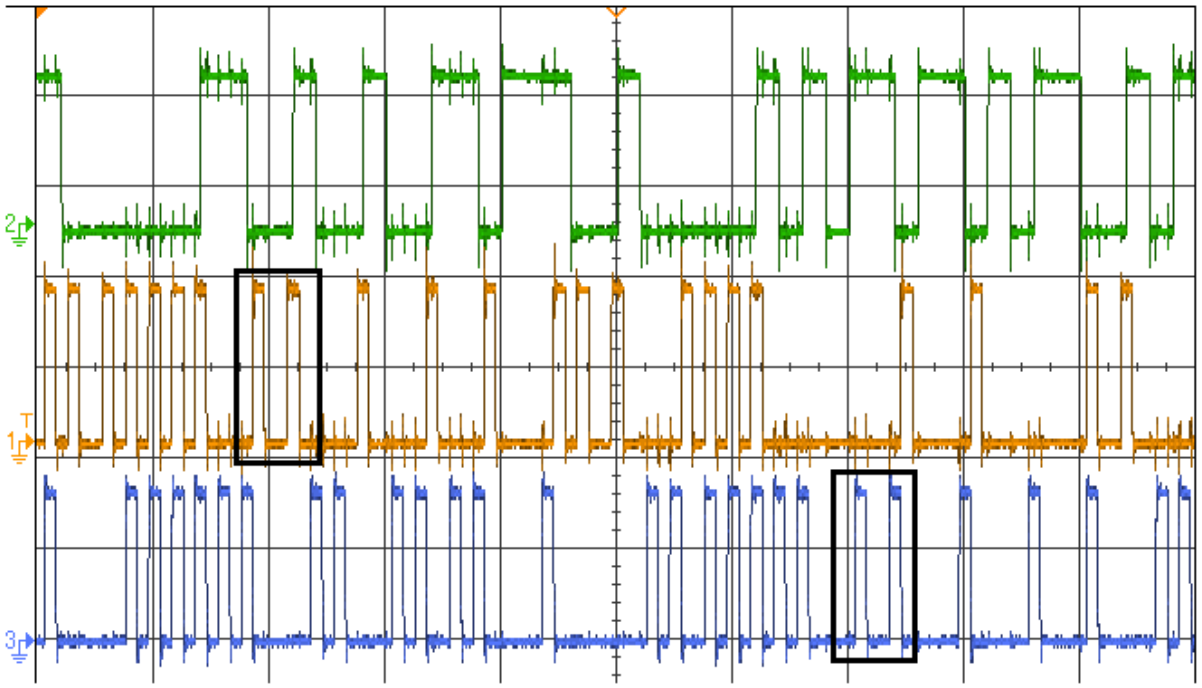


Fig. 7.23: MLSD module duobinary PPM output (bottom trace), PRBS PCM data (top trace) and input duobinary PPM data (middle trace): black box shows corresponding points.

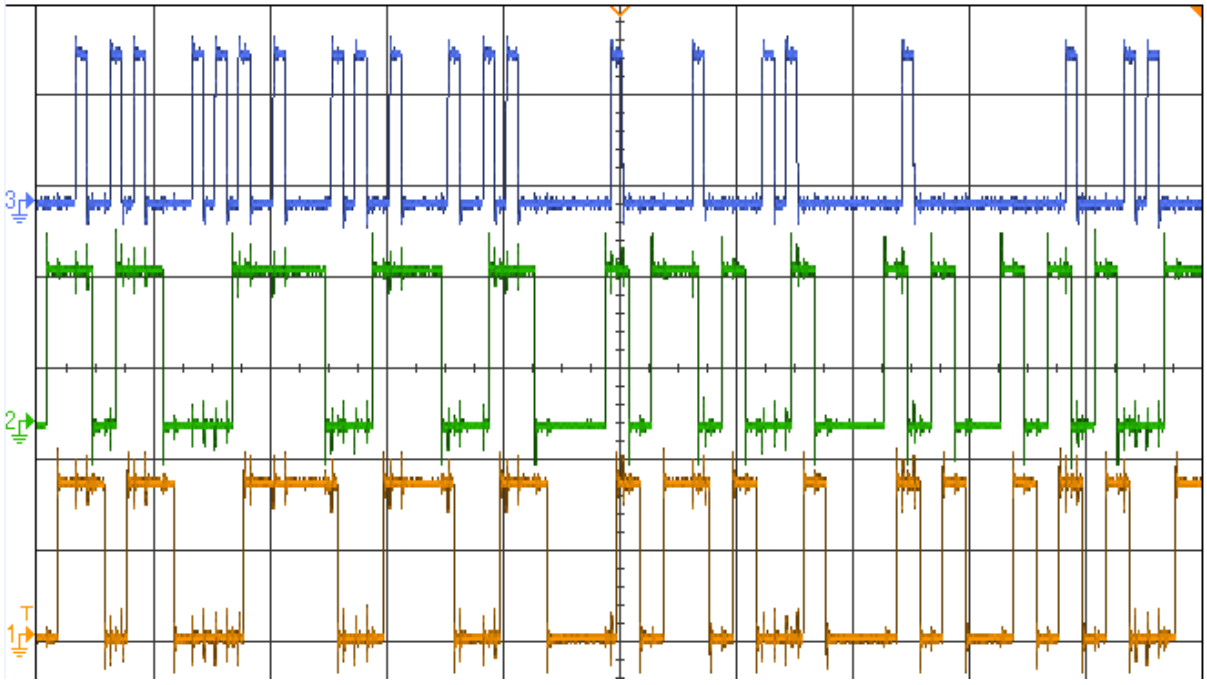


Fig. 7.24: Decoded PCM (middle trace) and regenerated PCM (bottom trace) with MLSD module checked duobinary PPM output (top trace).

7.8 Conclusions

In conclusion, this chapter has presented an introduction to the work that has been completed to successfully design and implement the complete duobinary PPM system on FPGA using VHDL hardware programming language. The main contents of the chapter showed how the phase-locked loop module has been used for clock recovery and clock division in the VHDL and design description of an 8-bit maximum length PRBS PCM data generator which is used for randomised input data sequences. The design and development of DuoPPM coder and decoder have been presented in this chapter. VHDL simulation waveforms and practical implementation results for both coder and decoder have been presented in this chapter. It also presented the bit error rate (BER) test circuit and the MLSD implementation of DuoPPM using VHDL and FPGA. Key sections of all the code and designs have been explained and the results in the forms of simulation waveforms and practical test results have been presented as well. BER test circuit has been implemented by regenerating the original PCM data from the PRBS generator and synchronising this regenerated data stream with the output PCM data to check for bit errors successfully. MLSD has been designed and implemented according to the theory and algorithms developed for the coding scheme and they have been discussed in more detail earlier in chapters 5 and 6. The error sequence tables and the algorithms have been implemented using the hardware description language and has been successfully integrated with other devices in the system such as clock divider, PRBS generator, coder, decoder, BER system. The complete system has worked as required which has been demonstrated by the output waveforms.

Chapter 8

Transceiver Design and Implementation of DuoPPM

8.1 VCSEL Transceiver and FPGA Interface

After the completion of VHDL and FPGA implementation of duobinary PPM coding system, a transceiver system[22] using VCSEL operating at 850nm wavelength and PIN photodiode receiver was designed for practical testing and verification of the link. An interface block diagram of the required system is given in the figure 8.1 below.

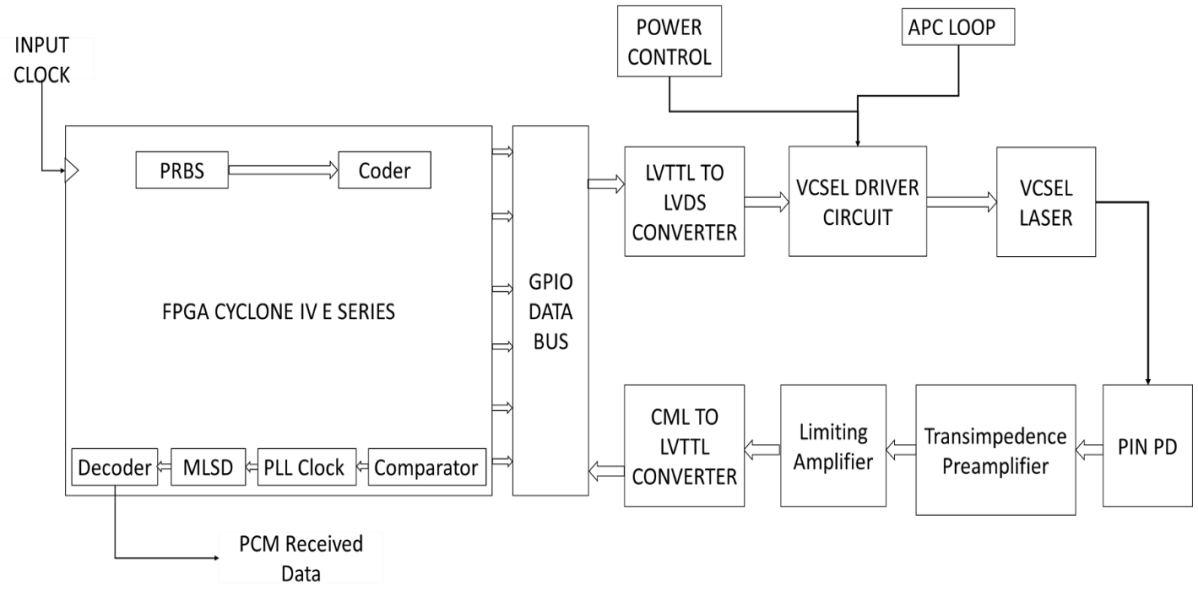


Fig. 8.1: Interface diagram of the FPGA and duobinary PPM transceiver.

Duobinary PPM outputs are received from the FPGA general-purpose input/output (GPIO) pin which is an LVTTL (Low-voltage transistor-transistor logic). Therefore, the input type and level conversion was required before it can be used as LVDS (Low-voltage differential signal) input to the MAX3735 IC [96] from Maxim Integrated © which is a multi-rate VCSEL driver that can be operated up to 3.2 Gbps data rate.

[22] Key information of all the datasheet are given at the end of the thesis in an organised manner.

For receiver module, the light is received by high sensitivity PIN photodiode and the output goes to the transimpedance preamplifier (TIA) and subsequently the output of the TIA is fed to the limiting amplifier (LA). The limiting amplifier output type is current-mode logic (CML) differential signal and the FPGA input is LVTTL single ended thus a voltage translator needs to be used for correct interface of the circuits. Once received by the FPGA, depending on the quality of the input signal analysed through characterisation process, a comparator can be used to further reconstruct the received signal.

In the FPGA module, the clock is extracted using one of the four embedded PLLs and the duobinary PPM data is used as the input of the MLSD module where algorithm is applied to check for detection and correction of any errors that may corrupt the original sequences. Once the data has been checked and given as output, the final stage is the decoder which decodes the duobinary PPM data back to original OOK PCM data. This PCM data finally is used to regenerate in-phase maximum length PRBS data to check for final errors in the output PCM data.

VCSEL has been custom connectorised by the manufacturer with ST receptacle in order to minimise coupling loss. The key properties of the 850nm VCSEL that has been used for the transceiver which has been procured from Lasermate Group Inc. © [93] are given below:

- Pre-aligned for multimode fibre communication.
- With monitor photodiode (PD).
- Power: >1 mW @ 6 mA.
- Maximum Rise/Fall time: 0.15 ns ≅6.67GHz.
- Monitor Current:$I_m = 50\ \mu A$.
- Breakdown voltage: V_BD = 14 V (typ.).

- This has to run at typically 2mA I_{TH} (Threshold current).
- Maximum forward current: I_F = 20 mA.

The key features such as average power, power control loop, current monitor, modulation current, bias current, and monitor PD current have been calculated and designed according to these specifications. All the circuits have been built[23] using SMDs (surface-mount device) for optimum performance except few components such as connector and VCSEL. The laser operates up to 1.25 Gbps data rate.

PIN-PD was used at the receiver [94]. Some of the key features of the PD receiver are given below:

- Customised with ST receptacle.
- Tuned for detection of 850nm wavelength.
- Pre-aligned for 62.5µm/125µm MM fibres.
- Maximum operating speed of up to 1.25 Gbps.

FPGA GPIO bus connectors are not designed for direct connection to the transceiver circuits thus an interface board which converts GPIO inputs to SMAs for ease of connectorisation with the transceiver module.

[23] PCB layouts are given in Appendix 4

8.2 Duobinary PPM Transmitter Design

8.2.1 LVTTL to LVDS Voltage Translator

The schematic diagram of the designed circuit for LVTTL to LVDS voltage translator is given in the figure 8.2 below.

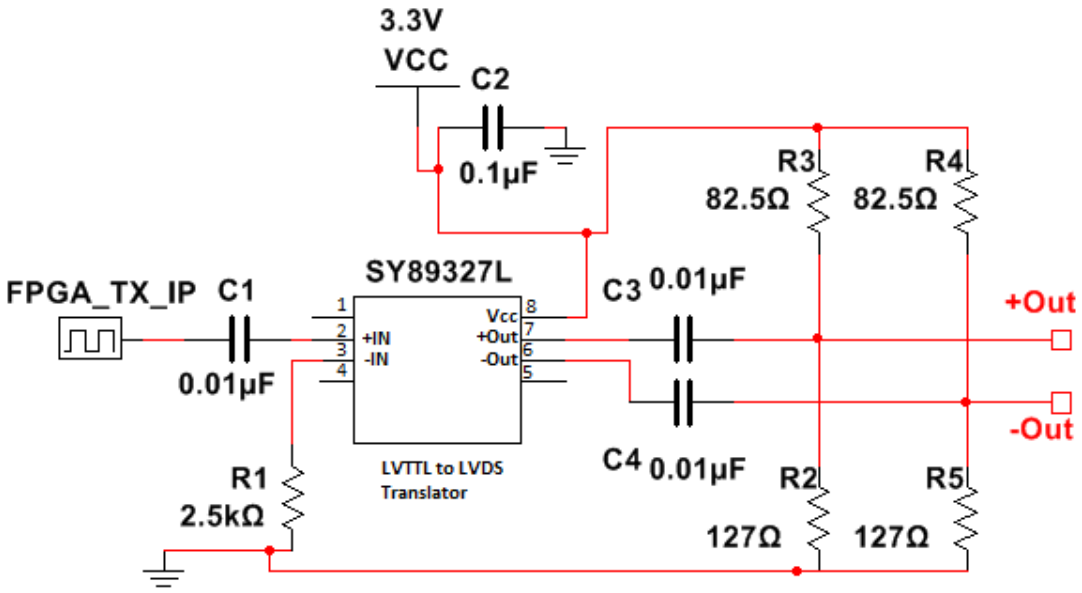


Fig. 8.2: LVTTL to LVDS voltage translator circuit schematic diagram.

Precision Edge © SY89327L IC has been used for this circuit [95]. This circuit connects to the inputs of the VCSEL driver to form a single transmitter module. All the AC coupling capacitors used in this circuit and the rest of the circuits in the following section are of the value of 0.01µF. Due to the single ended input to positive input pin[24] (2) the other input of negative pin (3) has been externally terminated to ground using a 2.5kΩ resistor. Both normal and inverted output have been terminated with 50Ω to V_{cc} – 2V. This impedance matching is required for the interface with the following VCSEL driver stage.

[24] Pin numbers are followed immediately in the parenthesis.

8.2.2 VCSEL Driver Circuit

The schematic diagram of the designed circuit for VCSEL driver is given in the figure 8.3 below.

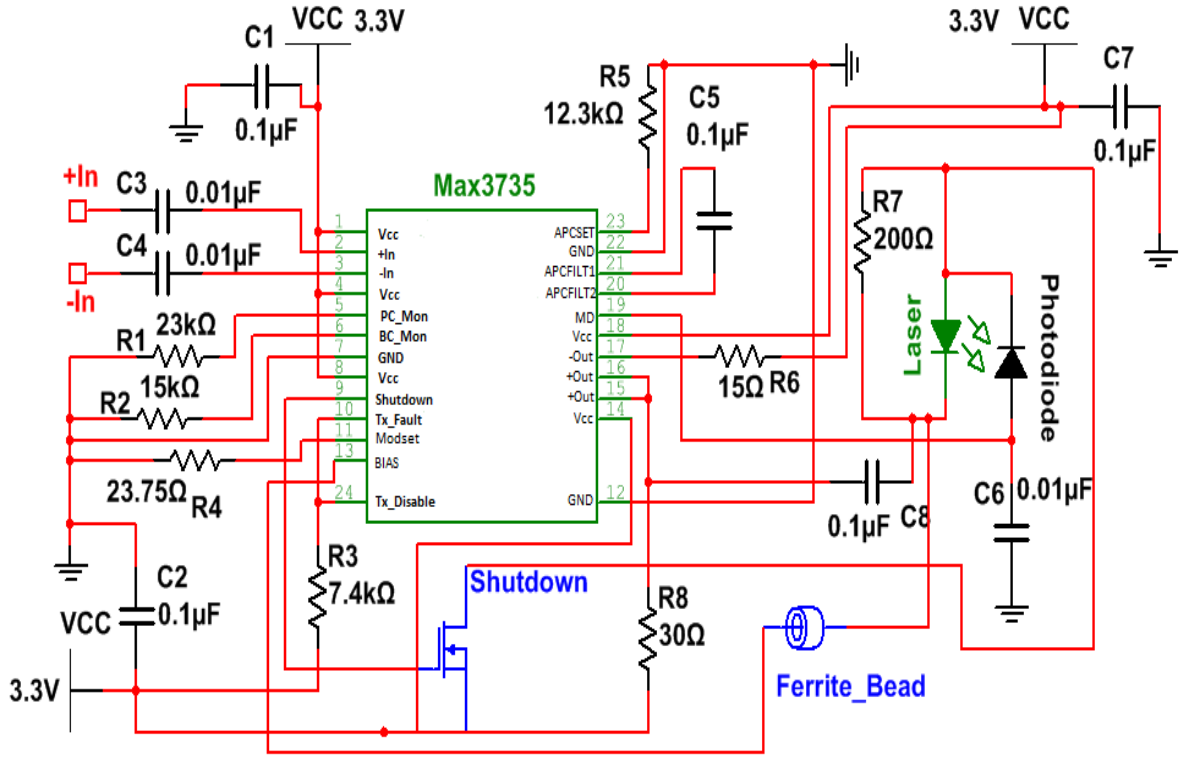


Fig. 8.3: VCSEL driver circuit schematic diagram.

MAX3735 VCSEL driver IC [96] has been used for the laser driver circuit. On-chip 100Ω differential impedance is provided for optimal termination. In case of any slight mismatch of impedance, the IC is highly resilient to a certain degree of mismatch. Some of the key set-up and safety feature calculations are given in this section.

'MODSET' pin is used to set up modulation current of the circuit. A resistor value need to be chosen which is connected to the ground (figure 8.4) according to the calculation to get desired modulation current. Some of the other important features such as average power, photo-current monitor and bias-current monitor are set up similarly as well.

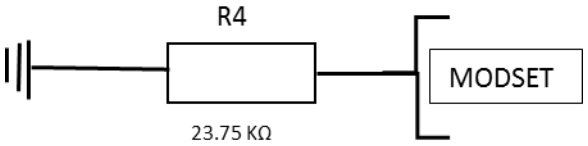


Fig. 8.4: Modulation current set-up diagram.

$$I_{MOD} = 14\ mA$$

$$I_{MOD} = 1.23/(0.0037 \times R_{MODSET}) \qquad (8.1)$$

$$R_{MODSET} = \frac{1.23}{0.0037\ \times\ I_{MOD}} = 23.75\ K\Omega$$

Maximum value of modulation current was chosen to be 14 *m*A and the value of the R_{MODSET} was calculated to be 23.75kΩ which was found by using the equation (8.1). Similarly, calculations for average power, photo-current monitor and bias-current monitor are given below.

Resistor value for Average Optical Power:

$$I_{MD} = 50\ \mu A$$

$$Where, \quad I_{MD} = P_{AVG}\ \times \rho^{mon} = 50\ \mu A$$

$$I_{MD} = 1.23/(2 \times R_{APCSET}) \qquad (8.2)$$

$$R_{APCSET} = 12.3\ K\Omega$$

Resistor value for photo current monitor:

$R = \frac{1.38}{50\ \mu A} = 27.6\ K\Omega$, Resistor value for photo current monitor.

$V_{PC\_MON} = 50\ \mu A \times 23\ K\Omega$

$V_{PC\_MON} = (\frac{I_{BIAS}}{76}) \times R$ (8.3)

Voltage greater than 1.38V at both photo current and bias current monitor result in a fault state. Therefore, the resistor values is chosen to give just below that voltage so that if the limit exceeds it will trigger the fault state.

Resistor value for bias current monitor:

$\frac{1.38}{\frac{7\ mA}{76}} = 15\ K\Omega$ = Resistor value for bias current monitor.

$V_{BC\_MON} = \left(\frac{I_{BIAS}}{76}\right) \times R$

Average Optical Power loop filter control capacitor:

$C_{APC} = 0.1\ \mu F$

$C_{MD} = 0.01 \mu F$

$0.02 = \frac{50\ \mu A}{I_{BIAS} - 2\ mA}$

$I_{BIAS} - 2\ mA = \frac{50\ \mu A}{0.02} = 2.5\ mA$

$I_{BIAS} = 2\ mA + 2.5\ mA = 4.5\ mA$

Capacitor for MD (Monitor Diode) was also chosen to be 0.01µF.

'TX_Disable' and 'TX_Fault' were connected together using a pull-up resistor to the Vcc as the output of the fault pin is open collector output. Pull-up resistor of the value of 7.4kΩ was used for this. When the fault pin goes high it disables the transmission by disabling the laser output. In order to re-enable the transmission, Vcc or 'TX_Disable' needs to be toggled.

There is an additional safety feature of 'Shutdown' that has been implemented using an external transistor connected to the Vcc and the 'Shutdown' pin. The supply to the laser is through this transistor and this arrangement works as an additional safety feature of the circuit as shown previously in figure 8.3.

Output stage circuits are very important for bias current set up (I_{BIAS}). Figure 8.5 and 8.6 below shows simple equivalent modulation and bias current models respectively from the circuit designed.

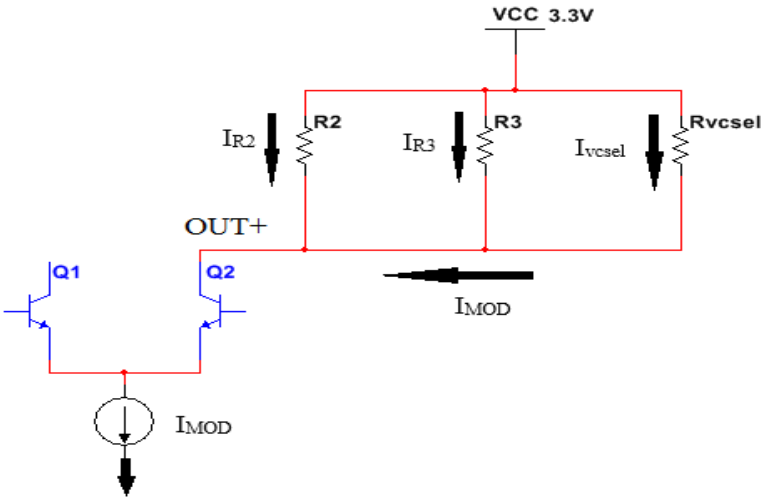


Fig. 8.5: Simplified model of modulation current circuit.

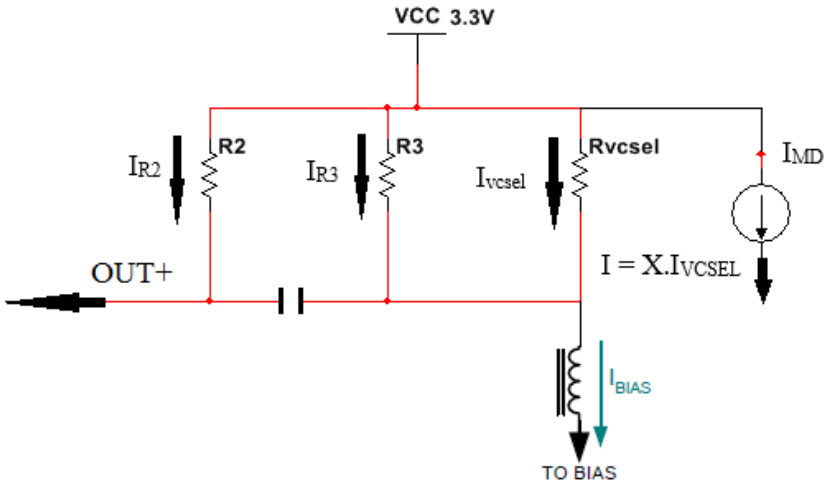


Fig. 8.6: Simplified model of bias current circuit.

The relevant calculations are given below.

$I_{MOD} = 14\,mA$

$R_2 = 30\ \Omega$

$R_3 = 200\ \Omega$

$R_{VCSEL} = 45\ \Omega$

$R_{LOAD} = R_2 // R_3\ // R_{VCSEL}$ (8.4)

$R_{LOAD} = 16.5\ \Omega$

Using current divider rules:

$I_{VCSEL} = I_{MOD} \times \left(\frac{R_F // R_S}{R_F // R_S + R_{VCSEL}}\right) = 5.138\,mA$ (8.5)

$I_{R_2} = I_{MOD} \times \left(\frac{R_S // R_{VCSEL}}{R_S // R_{VCSEL} + R_F}\right) = 7.706\,mA$

$I_{R_3} = I_{MOD} \times \left(\frac{R_F // R_{VCSEL}}{R_F // R_{VCSEL} + R_S}\right) = 1.156\,mA$

$\equiv 14\,mA$

$I_{BIAS} = I_{VCSEL} + I_{R_S} = 6.294\,mA$

$Gain = \left(\frac{I_{MD}}{(I_{VCSEL} + I_{R3} - I_{THRESHOLD})}\right)$ (8.6)

8.3 Duobinary PPM Receiver Design and Results

8.3.1 PIN-PD and Transimpedance Preamplifier

After the transmitter design, receiver was designed using PIN photodiode and transimpedance preamplifier (TIA). The output of this circuit goes to the limiting amplifier circuit as will be shown in the following section. Figure 8.7 below shows the TIA circuit schematic diagram.

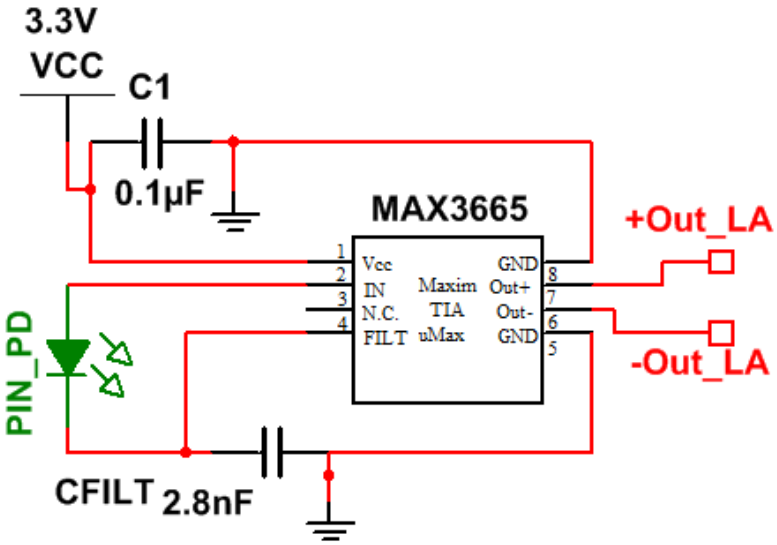


Fig. 8.7: Transimpedance preamplifier circuit schematic diagram.

MAX3665 TIA packaged IC [97] has been used for the TIA circuit. The key calculation for this circuit was to choose the capacitor filter (C_{FILT}) to be used with the PIN-PD. The required parameters for calculation are as follows:

$$V_{noise} = 50\ mV\ pk - pk$$

$$C_{PHOTO} = 0.5\ pF$$

$$R_{FILT} = 1.5\ k\Omega$$

$$I_{noise} = 6\ nA\ (\frac{1}{10}\ of\ the\ RMS\ noise)$$

$$C_{FILT} = \left(\frac{V_{noise}\ x\ C_{PHOTO}}{R_{FILT}\ x\ I_{noise}}\right) \qquad (8.7)$$

$$C_{FILT} = 2.77\ nF$$

8.3.2 Limiting Amplifier

After the TIA design, limiting amplifier (LA) was designed. PIN-PD, TIA and LA together to make the receiver circuit. The output of this circuit goes to CML LVDS to LVTTL voltage translator circuit as will be shown in the following section. Figure 8.8 below shows the LA circuit schematic diagram.

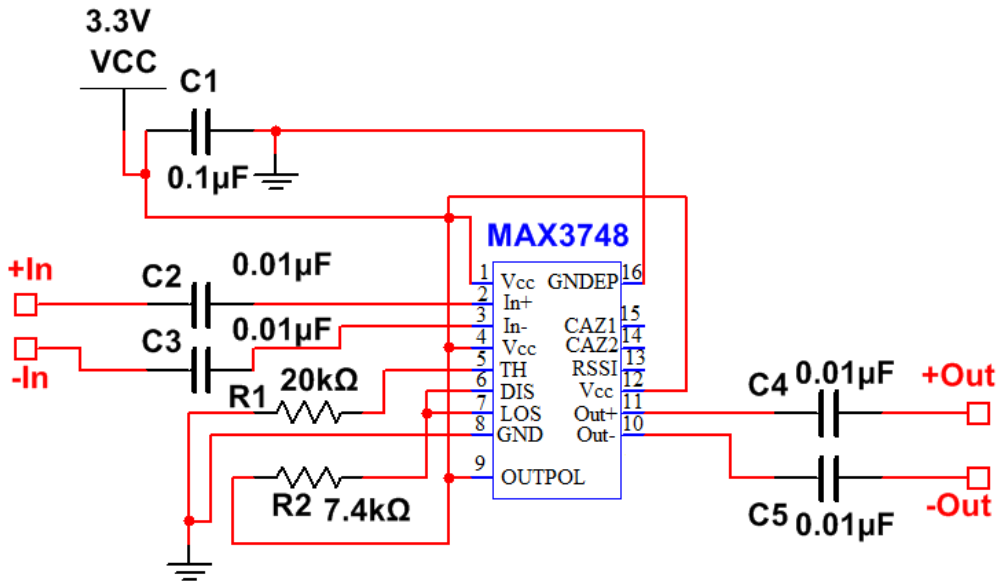


Fig. 8.8: Limiting amplifier circuit schematic diagram.

MAX3748 packaged IC [98] has been used for the LA circuit. The key for this circuit was to choose the value of threshold resistor which is a datasheet parameter according to the operating data rate and channel characteristics. For example, low LOS (Loss of Signal) characteristics of the channel operating at 155 Mbps the recommended resistor value is 20 kΩ. 'Disable' and 'LOS' pins were connected together using a pull-up resistor to the Vcc as the output of the loss of signal indicator pin is open collector output. Pull-up resistor of the value of 7.4kΩ was used for this. When the LOS pin goes high it disables output. Once LOS is asserted, it is not deasserted until the input amplitude rises to the required level ($V_{DEASSERT}$).

8.3.3 CML LVDS to LVTTL Voltage Translator

After the receiver circuit, the output goes to CML LVDS to LVTTL voltage translator circuit as is shown in the figure 8.9 below.

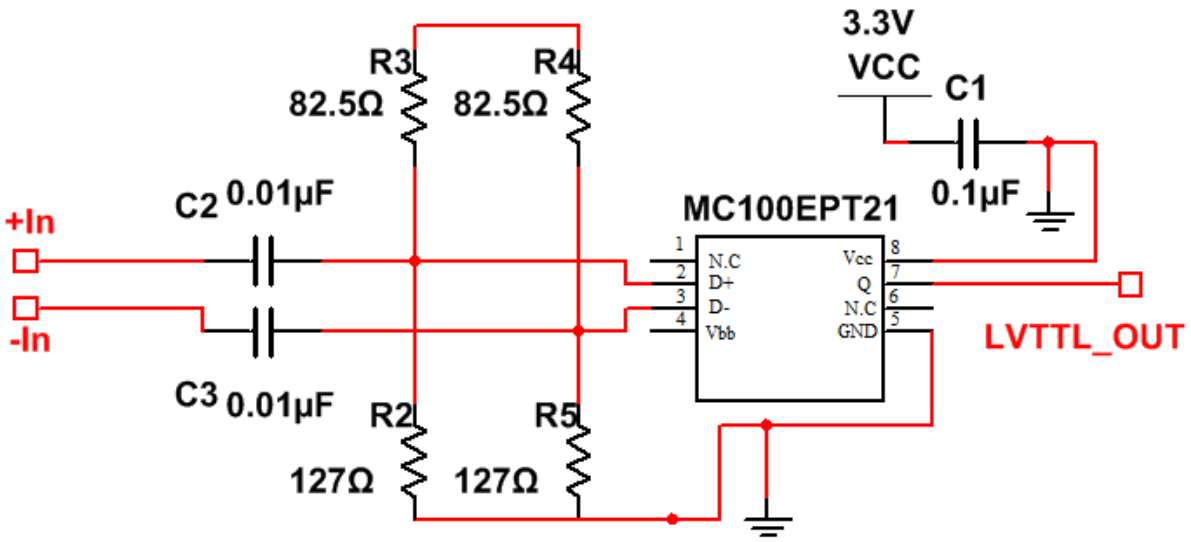


Fig. 8.9: CML LVDS to LVTTL voltage translator circuit schematic diagram.

MC100EPT21 [99] IC has been used for this circuit. This circuit takes the CML differential outputs as inputs to this circuit. The key consideration for this circuit is to ensure that previous stage outputs and the inputs of this stage match. This has been done by terminating both normal and inverted inputs from the previous stage with 50Ω to V_{cc} – 2V as has been shown in figure 8.9 above.

8.3.4 FPGA Results of Transceiver Design

The transceiver has been designed very late during the project, therefore, time has been limited to do comprehensive tests on the designed circuit such as receiver characterisation and deterministic error sequence verification. However, tests have been carried out with the FPGA coder, decoder and MLSD system for the correct functionality of the transceiver system. Figure 8.10 below shows the results from the FPGA MLSD and decoder output after data was received from the receiver module. It shows that the data has been received, checked and corrected as per theory. Tests were done on a 10m length GI-POF link of 1mm/2.2mm. Green boxes in figure 8.10 shows the in-phase check points of the PCM data sequence as there is a system latency mainly due to the initial output delay in the MLSD system.

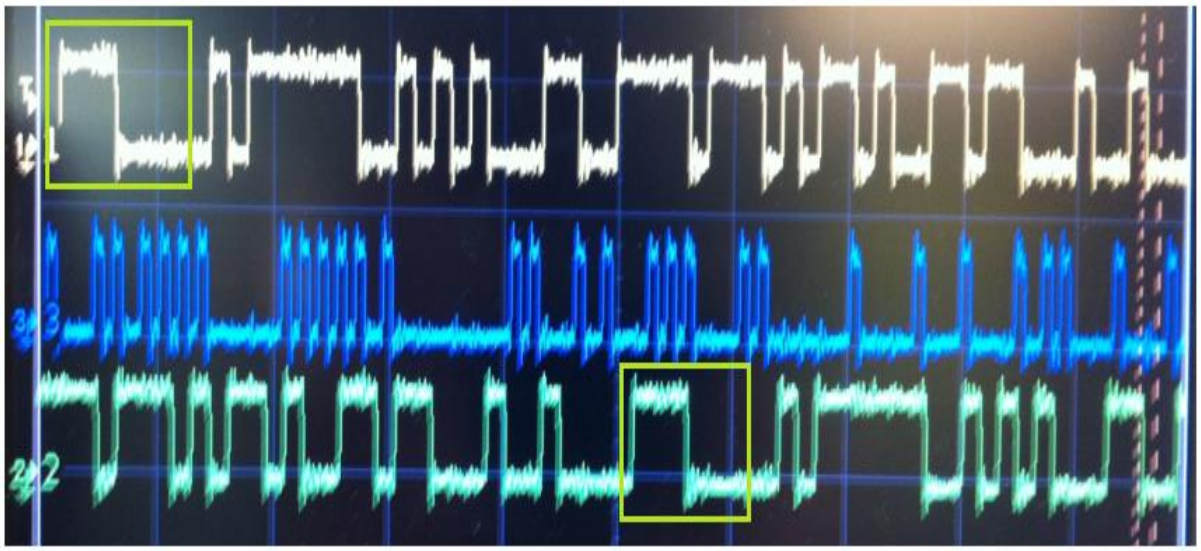


Fig. 8.10: Experimental verification of FPGA decoded PCM data after received from the receiver module of the transceiver: PCM input to the coder (top trace), duobinary PPM MLSD output (middle trace) and decoder output (bottom trace).

Figure 8.11 below shows the flags raised by FPGA MLSD when erroneous data sequences have been received. Deterministic error sequence and check was not possible due to lack of time as it requires erroneous sequences to be stored in the FPGA Memory module elements and access the transmission inputs from there. Further work is necessary and currently being carried out by the author to access and implement the FPGA memory functions to deterministic errors and correction procedure. A paper is also being written on the transceiver design and verification of duobinary PPM. The error flags shown in figure 8.11 was implemented by detecting start of every frame in the wrong slot by changing pulse detection edge of the clock in the code and PLL which means that using this code all the data received will be erroneous as shown below. All types of error flags have been raised which means that MLSD is working perfectly with the transceiver system and since the flag are being raised it can be said with confidence that the errors will be corrected as well given the operations of the MLSD discussed in Chapter 7.

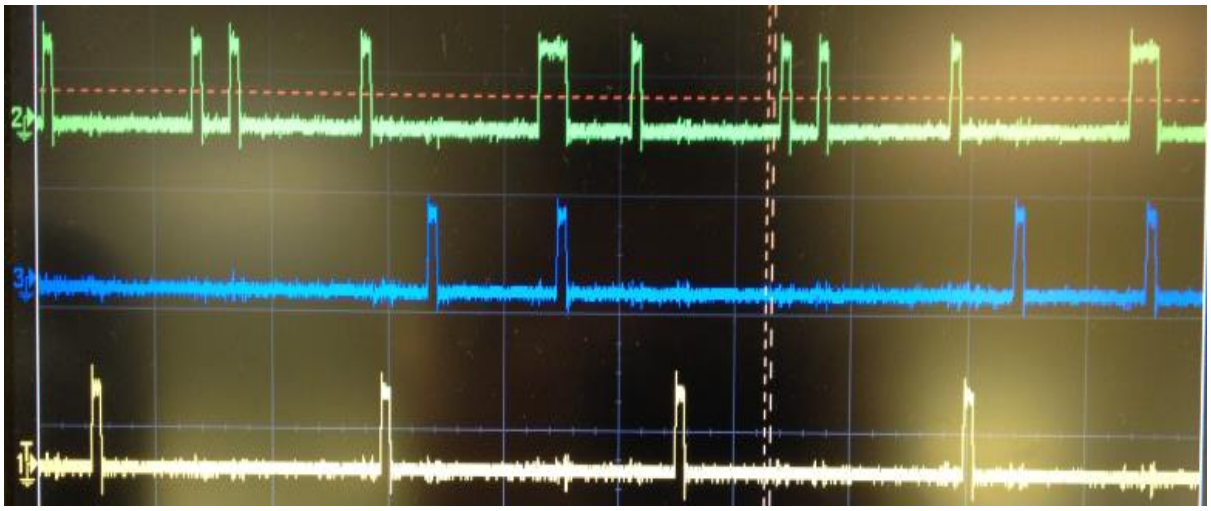


Fig. 8.11: Experimental verification of all three error flags for invalid sequences: wrong-slot flag (top trace), erasure flag (middle trace) and false-alarm flag (bottom trace).

8.4 Conclusions

In conclusion, a purpose-built transceiver design and implementation for DuoPPM coding scheme has been presented in this chapter. Designed transceiver is based on VCSEL Laser and PIN-PD receiver. This transceiver is interfaced with the FPGA and the test results have also been presented on a 10m length of POF to demonstrate correct functionality. For the receiver, an LVTTL to LVDS voltage translator was designed to interface the VCSEL laser driver with the FPGA output pins. A PIN-PD detector has been used for the receiver along with a transimpedance amplifier (TIA). Packaged ICs have been used for each circuit design for better performance. A limiting amplifier after TIA was required as well as a CML LVDS to LVTTL voltage translator to interface with the FPGA input pins.

Chapter 9

Discussions

Duobinary PPM [26-27, 91] has been proposed as novel coding scheme for bandwidth limited highly dispersive optical channels such as GI-POFs. Theories of the coding scheme have been presented and described appropriately in chapters 3 to 6. Results of theoretical simulations that have been carried out using mathematical modelling of the duobinary PPM system in Mathcad have been clearly laid out and analysed in chapters 4 and 6 where comparisons have been made with relevant existing coding schemes as well as analysing the significance of the results obtained for the duobinary PPM system. Power spectral density (PSD) analysis of the duobinary PPM is the same as that of dicode PPM [21-22] thus it has not been repeated for this research project.

Results proved the theoretical proposal by showing that with MLSD at 1 Gbps on OOK data duobinary PPM significantly outperforms optimised digital PPM at low fibre bandwidths by 8.7 dB while only operating at twice the original PCM data rate. It has also been shown at high fibre bandwidth that duobinary PPM gives a sensitivity of -42.2 dBm which is favourably comparable to digital PPM seven-level coding sensitivity of -44.1 dBm. Results presented in the thesis also demonstrates that at very low normalised fibre bandwidths (below 1 and down to 0.43) duobinary PPM outperforms dicode PPM by 1.2 dB requiring 27×10^3 photons per pulse compared to 40.3×10^3 required by Dicode PPM.

VHDL and FPGA implementations for the next stage of the research and design have also been successfully completed. The main blocks of VHDL design include PLL clock generation, 8-bit maximum length PRBS PCM generator, duobinary PPM coder, two bit SIPO module, a control pulse generation module, MLSD implementation, two bit serialiser, duobinary decoder, bit error rate (BER) test circuit by regenerating PRBS data synchronised with the decoded output to check for errors using an XOR logic gate. The results of functional and timing analyses completed in software and FPGA implementation results from the oscilloscope are given in chapter 7. All the codes and schematics have been fully listed in Appendix 3 for further reading.

Transceiver design using a VCSEL operating at 850nm wavelength has been completed. The maximum operating frequency of the VCSEL driver is 3.2 Gbps, however, the maximum operating frequency of the receiver unit is 622 MHz. Therefore, the transceiver could only operate at 622 MHz. This has been done mainly due to the lack of resources for testing of circuits that operate above 500 MHz at the moment of design development. In addition, maximum operating frequency of the FPGA used for testing was limited to 588 MHz thus it was not ideal to design a transceiver to operate at higher frequencies which cannot be tested for functionality. However, given the available resources research shows that a link can be designed and implemented for up to 10 Gbps [46, 66].

Previous research [23, 70-79] have suggested various methods of timing extraction, and slot and frame synchronisation for several coding schemes based on digital PPM. However, they all have faced problems in different ways such as bandwidth expansion, slot and frame synchronisation problems etc. More have been discussed in Chapter 2 regarding this topic but the key understanding from the literature is that timing extraction is a self-extracting mechanism for digital PPM schemes thus no additional data needs to be sent for this particular

purpose. Most of schemes use line coded PCM data to limit the maximum allowable run length of like symbols to an extent where timing extraction is possible. This is classically done by using PLL once the output is received from the decoder and for duobinary PPM this is done using one of the 4 dedicated PLLs available on the FPGA which has been programmed using VHDL making the implementation very simple. In addition, in the event of any change in specifications or test method, VHDL designs can be modified more easily than conventional logic based circuits.

The main problem is encountered when it comes to synchronising the recovered clock with the slot and frame of the data because it will take a phase difference of 180^0 to render all the detection wrong as start of the frame will be considered either half a clock cycle early or late depending on whether the phase difference is negative or positive. Elmirghani and Cryan et al. [76-79] have shown that in order to maintain frame and slot synchronisation, a scheme can be developed to generate phase bearing events. In general terms, it relies upon the presence of a pulse in the last slot of one frame followed by a pulse in the first slot of the next frame. This is a relatively simple method which can be achieved by adding two additional guard slots for extra pulses or modify the coding scheme to accommodate for two pulses. However, if no guard slots are used, it is not possible to implement for Duobinary PPM because DuoPPM only consists of two slots in a frame and both are used for data pulses. In addition, DuoPPM intends to operate without any guard slots in order to maximise the bandwidth efficiency. Therefore, other forms of solution must be sought for the coding scheme. Although, dicode PPM shows the clock recovery but effective frame synchronisation of clock remains open for further development.

It is clear that for most of these coding schemes, clock extraction has not been of any major concern for designers, and however, synchronisation with frames has been a significant issue, especially when no additional clock data has been sent. Although clock has been very easily extracted from the data using FPGA PLL for duobinary PPM coding scheme, frame and slot synchronisation remains a problem that needs further attention. A solution has been proposed in the following section[25] for slot and frame synchronisation of duobinary PPM.

[25] Section 10.2

Chapter 10

Conclusions and Further Work

10.1 Conclusions

To conclude the thesis, the key points are given as follows:

- Original theory of the duobinary PPM has been presented and described.
- Relevant literature has been reviewed, studied and presented in the thesis along with key aim and objectives of the research project.
- It has been shown theoretically that the proposed duobinary PPM coding scheme gives better bandwidth efficiency and sensitivity over existing coding schemes such as digital PPM, dicode PPM, multiple PPM and offset PPM while operating over slightly or highly dispersive GI-POF channels of limited bandwidth.
- Mathematical simulations of the theory have been carried out using Mathcad software and results have been presented in a clear manner to show that with MLSD at 1 Gbps on OOK data, duobinary PPM significantly outperforms optimised digital PPM at low fibre bandwidths by 8.7 dB while only operating at twice the original PCM data rate. It has been shown that at high fibre bandwidth, duobinary PPM operates with a sensitivity of -42.2 dBm which is favourably comparable to digital PPM seven-level coding sensitivity of -44.1 dBm. Results presented in the thesis also demonstrate that at very low normalised fibre bandwidths (below 1 and down to 0.43) duobinary PPM outperforms dicode PPM by 1.2 dB requiring 27×10^3 photons per pulse compared to 40.3×10^3 required by Dicode PPM.

- It has also been shown that duobinary MLSD completely eliminates wrong-slot errors and significantly reduces the effect of erasure and false-alarm errors.

- Successful VHDL and FPGA implementation of duobinary PPM coder, decoder and MLSD as a single system has been presented in the thesis. An FPGA embedded bit error rate (BER) test device has also been implemented for sensitivity measurement purpose and all the designs have been tested successfully.

- Designs and results of a VCSEL 850 nm wavelength based transceiver system built specifically for the duobinary PPM have been presented which has a current design specification of 622 Mbps data rate to match the maximum operating frequency of the FPGA. It also has the capability of operating up to 3.2 Gbps with design modifications.

- Further work on receiver characterisation and slot and frame synchronisation of duobinary PPM has been discussed in the thesis.

All the results and analyses indicate that duobinary PPM is an ideal alternative to be considered for highly dispersive optical channels, and performance evaluation for higher bandwidths also favourably compares to existing coding schemes with only twice the expansion of original PCM data rate.

10.2 Further Work

During the course of the research work all the key objectives that were set out in section 1.3 have been completed to a satisfactory extent. However, further improvements can be made in order to modify and optimise some of the objectives that have been completed. In addition, further investigations and testing need to be carried out for greater optimisation. This section discusses some of the main suggestions that have been made to improve the proposed coding scheme further.

Duobinary PPM has been successfully implemented with MLSD and bit error rate (BER) test circuits using VHDL and FPGA. However, further modifications can be made in order to improve design-for-test (DFT) functionality of the complete system. A digital counter can be implemented within VHDL in order to count the number of errors detected by BER and displayed on the LCD screen and real time calculations can be carried out to show live sensitivity data on a display screen which can be in turn be monitored for diagnostics and performance evaluation on the practically implemented system.

As has been discussed in the previous chapter[26], there are two viable options that can be implemented for slot and frame synchronisation. First option is to use extra slots in the frame in order to indicate the start and end of the data frames. However, it is not suitable as it carries the disadvantage of bandwidth expansion with it. Therefore, other methods of synchronisation such as a specifically designed header frame can be sent in order to indicate the start of incoming data sequences. Furthermore, predefined frames of data sequences can be sent when the data transmission has ceased. This will just add some very minor initial and end data

[26] Chapter 9 - Discussions

sequences during extraction without any bandwidth expansion. This method has another very useful application within the coding scheme, such as recognising when the system is idle. According to duobinary PPM data coding, when there are no PCM pulses present at the input to the coder, they will be coded as 0 which is not an ideal scenario from the perspective of power efficiency and the life-cycle of the laser.

Therefore, the header to indicate the start and stop of data sequence can be used to implement an 'Enable' signal to the coder therefore no output will be produced when there are no PCM data present at the input of the coder. The VCSEL transceiver that has been designed to test the coding scheme should be modified, given resources available for testing, to operate at the maximum data rate possible, which is 3.27 Gbps. Current maximum operating frequency is 622 Mbps. This is mainly due to the resources that were available for testing at the time of design which were limited by the maximum operating frequency of the FPGA, oscilloscope and testing facilities and equipment. The receiver of the duobinary PPM is yet to be characterised and it must be done in order to modify the current design and achieve further optimisations.

For test purposes, some of the key features of the VCSEL driver can be connected and monitored by external programmable embedded devices which requires attention for better driver performance. The main features that can be controlled and monitored real-time using external device are: adjustable average power, constant power range adjustment, photo current monitor, bias current monitor, adjustable modulation current setting, enable and disable the transmitter in the event of any safety feature failure. Finally, the system must be tested over various lengths of POF of up to 100 m to evaluate performance over distance in real-time so that comparisons and further optimisations can be implemented.

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Appendices

Appendix 1

Publications

Appendix 1.1: Published journal in IET

Optoelectronics.

Duobinary Pulse Position Modulation - A Novel Coding Scheme for the Dispersive Optical Channel

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Abstract

Pulse Position Modulation (PPM) coding schemes have been proposed and investigated widely as a technique of utilising the very high bandwidth available in optical fibres, with a significant improvement in sensitivity of 5 - 11 dB being achieved compared to an equivalent Non-Return to Zero (NRZ) On-Off Keying (OOK) scheme. However, this improvement has some trade-offs. When using 8 level digital PPM, the final data rate can be as high as 32 times that of the original data thus implementation becomes extremely difficult to the point where commercial viability becomes doubtful.

In this paper, the authors describe a novel coding scheme that combines the duobinary scheme with Pulse Position Modulation to form DuoPPM. It is shown that DuoPPM gives a sensitivity greater than digital PPM while operating at two times the original data rate. Original results presented in this paper predict that a high fibre bandwidth DuoPPM system can give a sensitivity of -42.2 dBm when operating with 1 Gbit/s PCM data and a fibre bandwidth of 100 GHz. In addition, it is shown that DuoPPM outperforms optimised digital PPM at low fibre bandwidths (1 GHz) by 8.7 dB.

1. Introduction

Recent developments in Pulse Position Modulation (PPM) have seen various coding schemes based on PPM being proposed by a number of authors for both free-space and optical fibre communications links. Digital PPM is one of the earliest coding schemes to be put forward. Garrett [1, 2] analysed this coding scheme and showed that there was a 5-11 dB theoretical improvement in sensitivity compared to standard Non-Return to Zero (NRZ) On-Off Keying (OOK) data. In digital PPM [3, 4], M bits of information are transmitted using a single pulse by positioning it in one of 2^M time slots, figure 1.

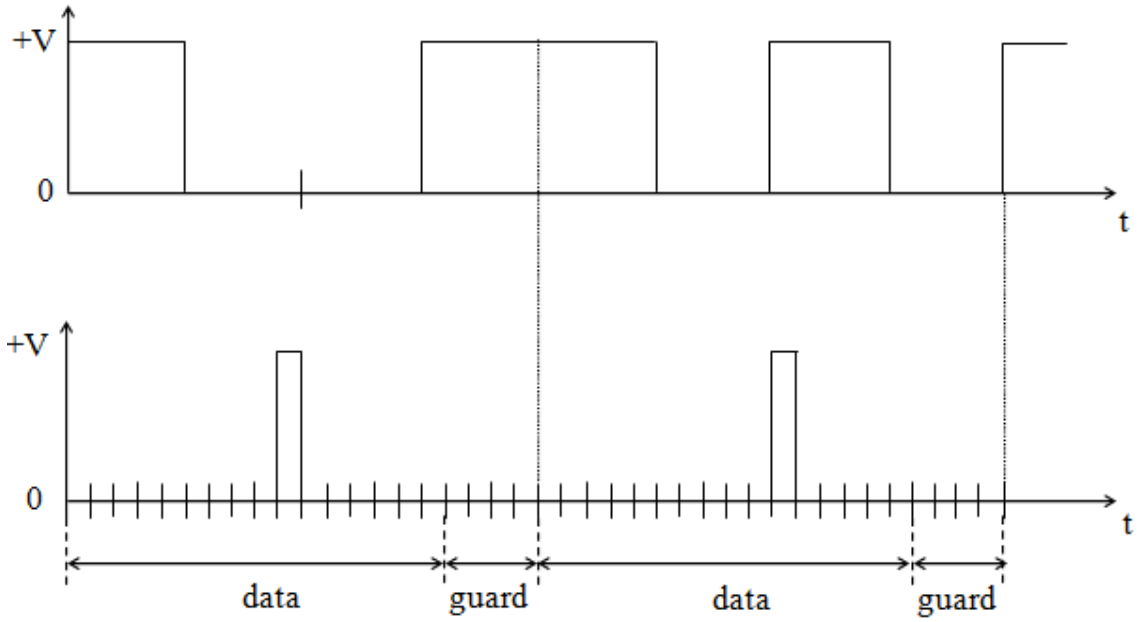

Fig. 1: Conversion of 4 bits of PCM (top trace) to digital PPM (bottom trace).

There is a significant improvement in sensitivity over NRZ OOK because a single pulse is used to transmit M bits of information. Therefore, by virtue of the lower mark:space ratio, increasing M means improving the sensitivity. However, in order to synchronise equivalent data throughput with NRZ OOK, the same amount of data must be transmitted within the same time frame. Therefore, for a data time frame of MT_b, where T_b is the bit period, there must be 2^M

PPM time slots which means that the PPM slot rate is $2^M/M$ faster than the PCM bit rate in order to maintain the same information throughput. This large bandwidth expansion can make the final line rate prohibitively high.

It is this bandwidth expansion that led to many alternative PPM schemes such as Multiple PPM [5-7], Dicode PPM [8, 9], Offset PPM [10, 11] and Differential PPM [12, 13] to name but a few. Multiple PPM and Dicode PPM are the two most bandwidth efficient of these coding schemes and both offer better sensitivities without large bandwidth expansion of the other schemes.

In Multiple PPM, the position of two or more pulses in a frame is governed by the original data word. Sugiyama and Nosu [5] analysed the error performance and introduced the Maximum Likelihood Sequence Detection (MLSD) technique which was later further investigated by Sibley and Nikolaidis [6, 7]. It was concluded that Multiple PPM is more power and bandwidth efficient than digital PPM.

MLSD has been applied to other coding schemes such as Dicode PPM [9] with significant success as results showed an improvement in sensitivity. Sequence detection and equalisation [14] and decision-feedback equalisation [15] have been proposed as alternatives to MLSD.

In Offset PPM, the offset from a datum, either 0000 or 1000 is coded by the position of a single pulse. Theoretical work has shown that this technique has a sensitivity comparable to digital PPM but at a line rate of half that of digital PPM.

In Differential PPM [12], the empty slots following a pulse are suppressed and this leads to a reduction in the line rate. Unfortunately coding and decoding are complicated by the fact that the frame time is variable and depends on the data being transmitted.

Duobinary Pulse Position Modulation (DuoPPM), the subject of this paper, is a novel coding scheme that combines the duobinary technique and digital PPM to form DuoPPM. In this signalling format, a signal is only transmitted when the data is constant at either logic one or logic zero and no signal is transmitted for data transitions from logic one to logic zero or logic zero to logic one – the change condition. As will be shown later, the use of a novel MLSD technique allows for the elimination of wrong-slot errors and a reduction in the effects of erasure and false-alarm errors. In addition, DuoPPM achieves this performance with only a twofold increase in speed. Thus the increased sensitivity of digital PPM is made available without the adverse effects and added complications of excessive bandwidth expansion.

Original theoretical results show that a simple, leading-edge, threshold-detection DuoPPM system gives comparable sensitivity to that of digital PPM at high fibre bandwidths and for low fibre bandwidths, the sensitivity is significantly greater. The results presented are for a data rate of 1 Gbit/s. The simulations carried out so far have considered a highly dispersive graded-index Plastic Optical Fibre (POF) channel as the primary focus of targeted improvement. Such fibre channels exhibit an impulse response that can be approximated to a Gaussian shape [16] and have a relatively poor bandwidth. The reason to deliberately choose this channel is to demonstrate the effects of dispersion on the coding technique. Although the simulations have been restricted to 1 Gbit/s the technique can be adapted to high-speed optical communications links potentially exceeding 10 Gbit/s without any significant compromise of improved sensitivity. Application of this coding scheme in free-space communications links and other detection schemes is also possible [17, 18].

2. Duobinary Pulse Position Modulation (DuoPPM)

In the DuoPPM signalling technique, data transitions are coded into DuoPPM pulse positions as follows: a constant stream of data of logic zero produces a pulse in slot zero of the DuoPPM frame and a constant stream of data of logic one produces a pulse in slot one of the DuoPPM frame. No pulses are transmitted in the frame when the data is in transition from logic one to zero and logic zero to one (figure 2).

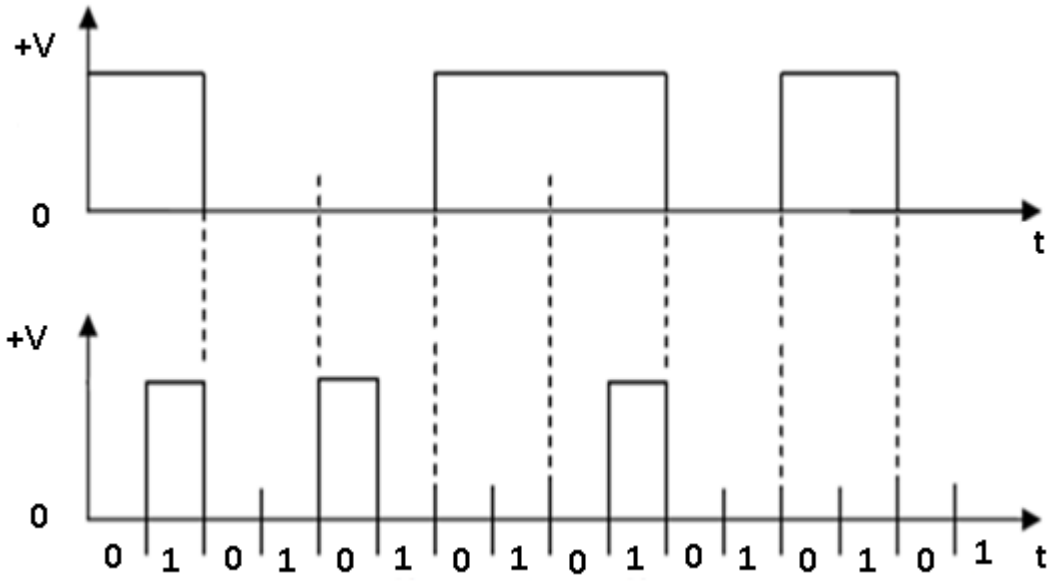

Fig. 2: Conversion of PCM data (top trace) into DuoPPM (bottom trace).

No guard slots are required for this coding scheme as the Inter-symbol Interference (ISI) will be significantly reduced by virtue of the inherent properties of the coding scheme. In addition, a novel MLSD and correction technique ensures that a particular error type can be completely eliminated. As can be seen from figure 2, the line rate is twice that of the original NRZ OOK data which is a considerable reduction in bandwidth expansion compared to digital PPM.

Table 1 shows the DuoPPM signal representation and, for comparison, the Dicode PPM code.

Data	Probability	DuoPPM	Symbol		Dicode PPM	Symbol
00	1/4	Pulse in slot 0	0		No pulse	NC – No change
01	1/4	No pulse	C – change		Pulse in slot SET	S
10	1/4	No pulse	C – change		Pulse in slot RESET	R
11	1/4	Pulse in slot 1	1		No pulse	NC – No change

Table 1: Duobinary and Dicode PPM signal representations.

It can be seen from Table 1 that each symbol has a probability of 1/4. However, the DuoPPM no-pulse signal (C) occurs for both 01 and 10 sequences and therefore has a total probability of 1/2. Thus, the probability of a 1 occurring in the first instance is 1/4 and the probability of a subsequent C or 1 immediately following it is 1/2 (given that a 1 has occurred and the current coder state is one). Likewise, the probability of a 0 occurring initially is 1/4 and the probability of a C or 0 immediately following it is 1/2. If it can be assumed that the original PCM data is line coded so that the run of no-pulse signals (C) is limited to n, the maximum DuoPPM run would be 1, nC, 0/1. With this condition, the final pulse will be a 0 if n is an odd number or, if n is an even number, the final pulse will be a 1. This is because the coding technique dictates that a sequence will end with the same symbol as the first one if n is an even number, otherwise

it will end with the opposite symbol (considering 0 is the opposite of 1 and vice versa). Some typical examples of valid DuoPPM sequences are 1C0, 0C1, 1CC1, 0CC0, 11, 00 etc.

In common with digital PPM, the optimum filter for a DuoPPM receiver consists of a noise-whitened matched filter and a PDD network, as shown in Fig. 3. Following the PDD network, a voltage comparator is used to slice the data and the resulting pulses are applied to a decoding logic circuit which is programmed according to appropriate decoding rules. To maintain frame synchronisation, a slot clock can be extracted from the data received and used to decode the DuoPPM signals, Fig. 4.

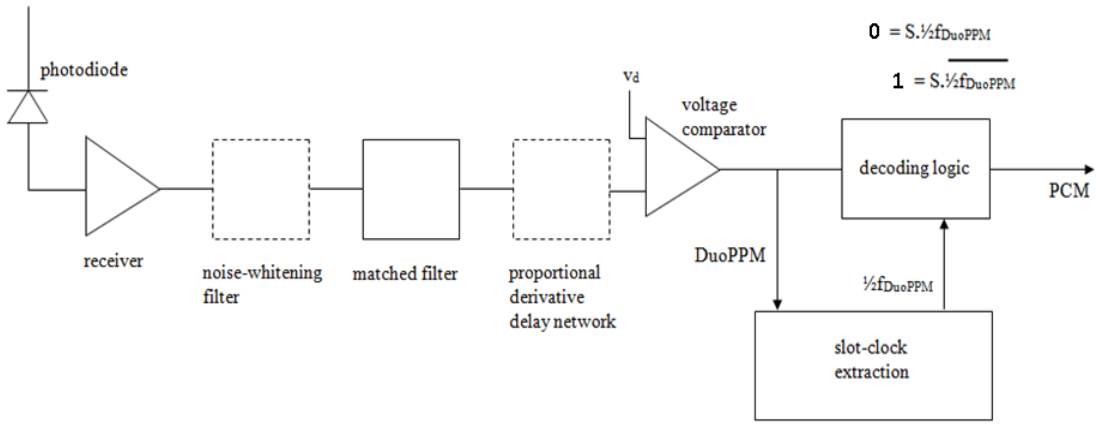

Fig. 3: Schematic of a DuoPPM receiver (The dashed boxes are optional - see Section 4).

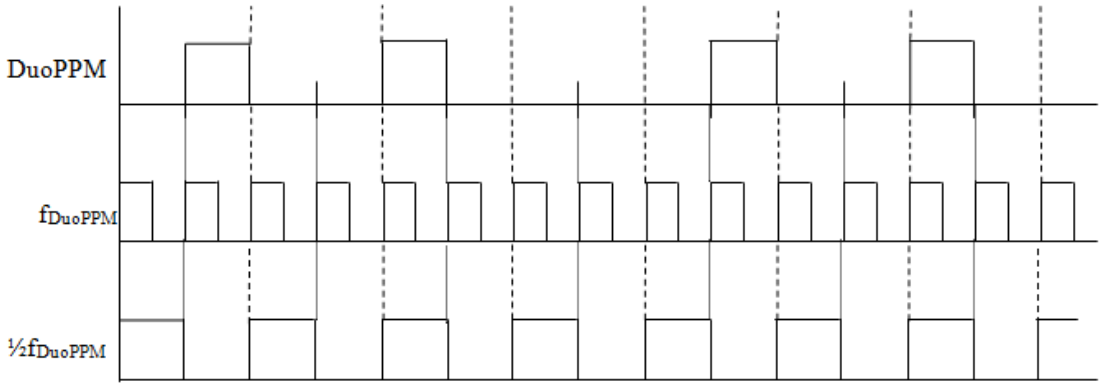

Fig. 4: Slot clock extraction timing diagram.

3. Equivalent Data Errors in DuoPPM

Three pulse detection errors affect PPM systems: wrong-slot, erasure and false alarm [2]. The expressions developed for the Dicode PPM [8] system for the probability of these detection errors are applicable to the DuoPPM scheme and so are not repeated here. Instead we concern ourselves with the equivalent data errors and discuss the operation of the MLSD.

In DuoPPM, a wrong-slot event will cause a pulse detection error. Noise on a pulse in the 0 slot, can cause the pulse edge to appear in the preceding 1 slot (previous frame) or in the following 1 slot (present frame). Similarly if the pulse is in the 1 slot, noise could cause the edge to appear in the preceding 0 slot (present frame) or the following 0 slot (next frame). Due to the action of the MLSD, these errors can be detected and corrected for as shown in Table 2.

$1 \leftarrow 0$	Transmitted	1	C	0	C	C	0	
	Received	1	**1**	0	C	C	0	Invalid sequence
	MLSD	1	C	0	C	C	0	error corrected
$0 \leftarrow 1$	Transmitted	0	C	1	C	C	1	
	Received	0	C	**0**	C	C	1	Invalid sequence
	MLSD	0	C	1	C	C	1	error corrected
$1 \rightarrow 0$	Transmitted	0	C	1	C	C	1	
	Received	0	C	1	**0**	C	1	Invalid sequence
	MLSD	0	C	1	C	C	1	error corrected
$0 \rightarrow 1$	Transmitted	1	C	0	C	C	0	

	Received	1	C	**1**	C	C	1	Invalid sequence
	MLSD	1	C	0	C	C	0	error corrected

Table 2: Showing the operation of the MLSD with wrong-slot errors. The symbol in error is shown in bold.

In a DuoPPM system, erasure of a 0 or a 1 pulse results in the change symbol C. This has the effect of generating an invalid DuoPPM sequence and so the MLSD acts to minimise the data error as in Table 3. The MLSD inserts a pulse of the correct polarity such that the sequences preceding and following the erasure event are valid. So, in the first entry in Table 3 – erasure of a 0 – the faulty sequence has eight C symbols between the 1 and 0. This is clearly at fault since the start and final pulses should be the same given an even number of C symbols. The MLSD detects the faulty sequence and inserts a 1 pulse as close to the centre of the run of Cs as possible. (As the MLSD has no information as to where the erasure has occurred, the mid-point in a run of Cs will yield the lowest error.) A similar mechanism occurs in the second example in Table 3 in which a 1 pulse is erased.

Erasure of 0	Transmitted	1	C	C	C	0	C	C	C	C	0
	Received	1	C	C	C	**C**	C	C	C	C	0
	Corrected	1	C	C	C	C	1	C	C	C	0
Erasure of 1	Transmitted	1	C	C	1	1	C	C	C	0	-
	Received	1	C	C	**C**	1	C	C	C	0	-
	Corrected	1	C	0	C	1	C	C	C	0	-

Table 3: Transmitted and received sequences with an erasure error.

In the case of false-alarm (FA) errors, a decoding error will occur if a false alarm happens in the following string of C signals. The severity of the error depends on the position of the false alarm occurrence in a given sequence, as Table 4 shows.

	Transmitted	0	C	C	C	C	C	C	C	C	0
FA of 0	Received	0	C	C	C	**0**	C	C	C	C	0
	Corrected	0	C	**1**	C	0	C	C	C	C	0
FA of 1	Received	0	C	C	C	C	C	C	**1**	C	0
	Corrected	0	C	C	C	1	C	C	1	C	0

Table 4 Transmitted and received sequences with a false-alarm error

The expressions for the pulse detection errors are the same as for Dicode PPM and can be found in reference [8].

4. System Modelling

The signal analysis for a DuoPPM system is the same as for the Dicode PPM system [8] and so the majority of the derivation will not be repeated here. Of importance are the equations relating to the fibre bandwidth and these are reproduced here.

The impulse response of the channel (GI-POF) can be approximated to a Gaussian [19] and thus

$$h_p(t) = \frac{1}{\sqrt{2\pi\alpha^2}} \exp\left(-\frac{t^2}{2\alpha^2}\right) \quad (1)$$

The Fourier transform of the input pulse, $H_p(\omega)$, is given by

$$H_p(\omega) = \exp\left(-\frac{\alpha^2\omega^2}{2}\right) \quad (2)$$

The pulse variance, α, is linked to the fibre bandwidth by

$$\alpha = \frac{0.1874T_b}{f_n} \quad (3)$$

where T_b is the PCM bit time and f_n is the dimensionless fibre bandwidth normalised to the PCM data rate, B in bit/s, given by

$$f_n = \frac{f}{B} \quad (4)$$

where f is the fibre bandwidth in Hz.

5. Performance Evaluation

In common with Dicode PPM, a threshold level, v, was used as a system variable defined by

$$v = \frac{v_d}{v_{pk}} \tag{5}$$

where v_{pk} is the peak voltage of an isolated pulse and v_d is the decision (threshold) voltage. The pulse shape and noise can be determined theoretically if the fibre bandwidth is known [8]. Simulations were performed to find the optimum value of v_d that gave the minimum number of photons per pulse, b, for a specified error rate of 1 in 10^9.

Since the simulation results are to be comparable to digital and Dicode PPM, identical system parameters were used to evaluate system performance. The original data was assumed to be line-coded with a run length (*n*) of 10 and a data rate of 1 Gbit/s was used for the simulated system. A wavelength of 1.55 μm was chosen with a photodiode quantum efficiency of 100%. A receiver with a bandwidth of 10 GHz and white noise of 50×10^{-24} A^2/Hz was taken.

The optical power for the digital PPM system, P_{DPPM}, can then be obtained from,

$$P_{DPPM} = \frac{b}{M} h\upsilon B \tag{6}$$

where b is the number of photons in a single pulse, h is Planck's constant, υ is the optical frequency, B is the original bit rate and M is the level of coding (number of bits coded). For the DuoPPM system, the average number of photons in a frame containing a pulse is b/2. As there are two frames containing pulses, each occurring with a probability of -1/4, the average number of photons is b/4.

Thus the optical power required, $P_{DuoPPM,}$ is given by

$$P_{DuoPPM} = \frac{b}{4} h\upsilon B \quad (7)$$

Similarly, for Dicode PPM, $P_{Dicode\ PPM,}$ is given by

$$P_{DuoPPM} = \frac{b}{4} h\upsilon B \quad (8)$$

6. Results and Discussion

Figure 5 shows the variation, with normalised fibre bandwidth, in the number of photons per pulse (b) required for an error rate of 1 in 10^9. These results were obtained by calculating the error probabilities obtained from the equations given in Appendix A and then applying the MLSD to get the final error rate. The value of b was then adjusted to obtain the performance criterion of 1 error in 10^9 bits.

As can be seen, all systems have similar performance, in terms of photons per pulse, at high bandwidths. However, as the bandwidth reduces (increasing dispersion) the digital PPM system requires significantly more photons per pulse to achieve the target error rate of 1 in 10^9. (In order to obtain the results for digital PPM, 7 level coding was used with a modulation index of 0.8.) This is due to high levels of dispersion causing the slope of the received pulse to increase and this increases the error rate. The apparent resilience to dispersion presented by DuoPPM is, in part, due to the very nature of the code. In DuoPPM system, there exists a minimum of one no-pulse (C) signal between 1 and 0 signals, or vice-versa. This is fundamental to the code. Thus, in the low bandwidth region, the first pulse can spread into the adjacent C (no pulse and empty) slot so making the code more resilient to ISI.

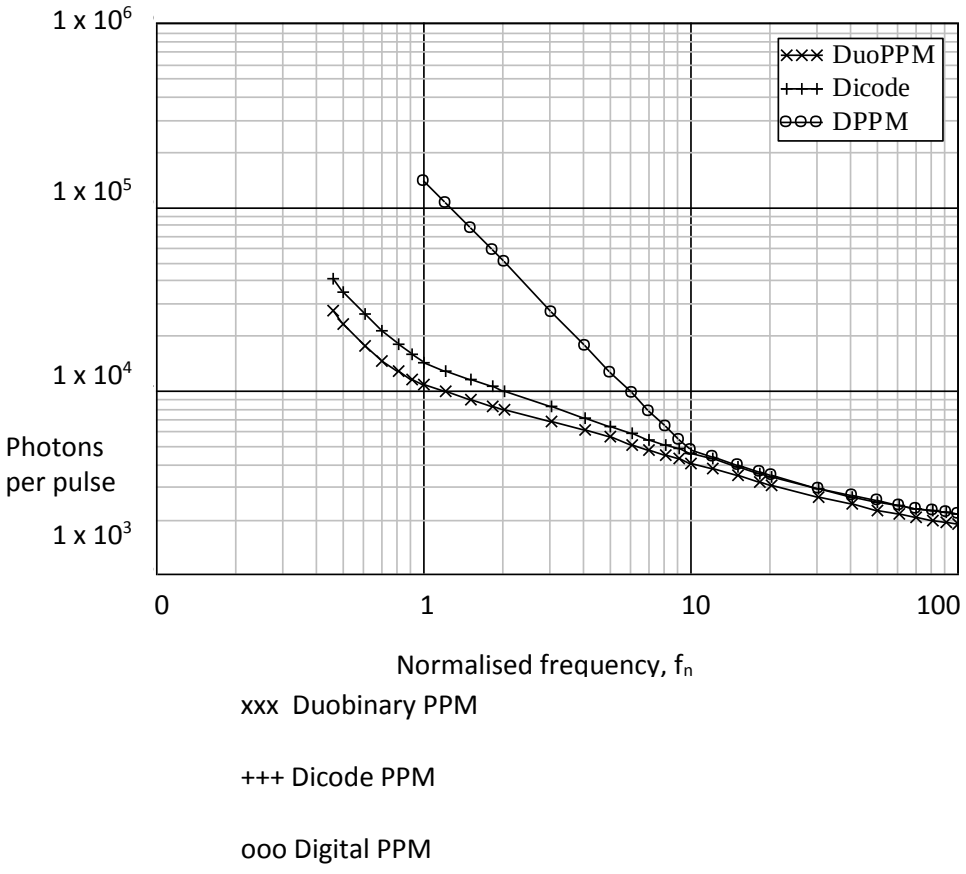

Fig. 5: Variation in photons per pulse with frequency normalised to bit rate, f_n, for Duobinary, Dicode and Digital PPM.

As previously mentioned, the sensitivity of digital PPM can be high due to the effects of a low mark:space ratio and figure 6 compares the sensitivities of DuoPPM, Digital PPM and Dicode PPM. Equations 6, 7 and 8 were used to obtain the average power. Table 5 summarises the results at high and low fibre bandwidths. As can be seen from figure 6 and table 5, Digital PPM out-performs DuoPPM by 1.9 dB at a normalised bandwidth of 100. However, as the bandwidth reduces, so does the advantage Digital PPM has over DuoPPM and Dicode PPM. Eventually, at a normalised bandwidth of 1, DuoPPM offers an advantage of 8.7 dB over Digital PPM. DuoPPM also offers an improvement of 1.2 dB over Dicode PPM. These results indicate that

DuoPPM has an advantage over both Digital PPM and Dicode PPM when operating with a high level of dispersion (low bandwidth).

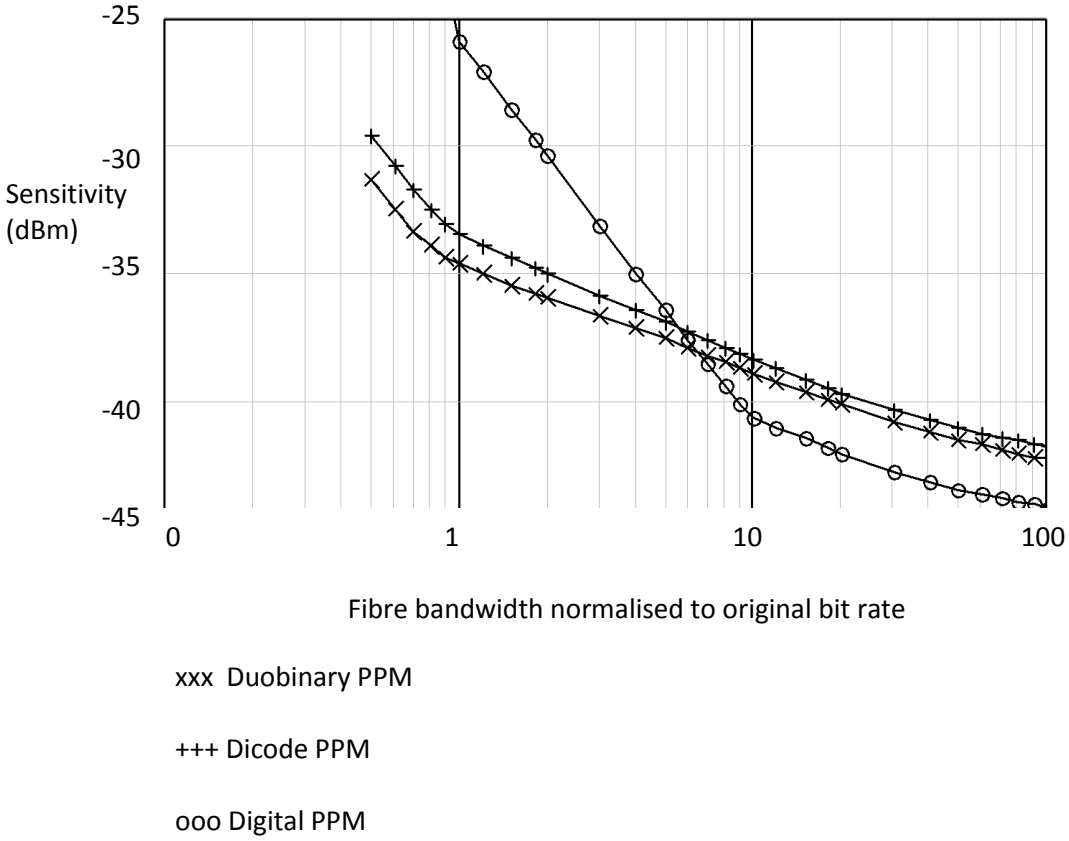

Fig. 6: Variation in sensitivity (dBm) with normalised fibre bandwidth for Duobinary, Dicode and Digital PPM.

	Data rate 1Gbit/s	
	Sensitivity in dBm	
Normalised fibre bandwidth	$f_n = 1$	$f_n = 100$
DuoPPM	–34.6	-42.2
Digital PPM 7 level coding	-25.9	-44.1
Dicode PPM	–33.4	–41.7

Table 5: Comparison of sensitivities for DuoPPM, Digital PPM and Dicode PPM at 1 Gbit/s PCM data rate.

7. Conclusions

A novel coding technique for applications in optical fibre links, particularly for highly dispersive and bandwidth limited optical links, has been presented and described in this paper. This coding scheme combines the duobinary technique with digital PPM to form DuoPPM. Theoretical simulation models have been developed in order to obtain performance characteristics of the new technique. The results were analysed and compared to that of digital PPM and Dicode PPM.

Results from sensitivity calculations have shown that digital PPM offers a better sensitivity than DuoPPM and Dicode PPM at high bandwidths when the dispersion is low. This is by virtue of the low mark:space ratio giving a low average power in the digital PPM frame.

However, as the bandwidth reduces, the advantage of digital PPM is reduced until DuoPPM offers the best sensitivity. This is due to dispersion on the link being higher, and this affects digital PPM more than DuoPPM. This is due to the very nature of the code and also due to the fact DuoPPM uses a Maximum Likelihood Sequence Detector (MLSD) to decode the data word in the presence of errors.

From all relevant properties and performance characteristics discussed in the paper with appropriate results, it can be concluded that this novel code can be a viable alternative to NRZ OOK, digital PPM and Dicode PPM systems.

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Appendix A – Error probabilities

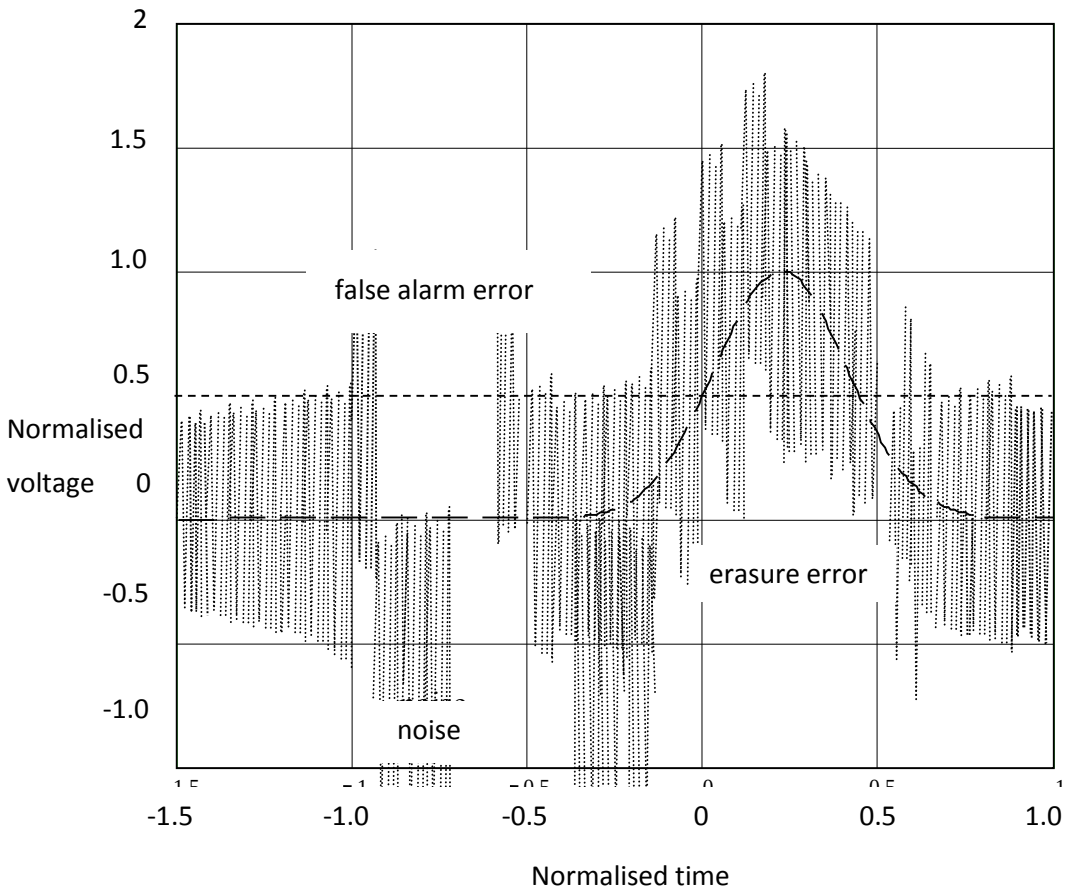

Figure A-1: A Gaussian shaped pulse in the presence of noise showing false alarm and erasure errors. The threshold voltage is shown as the horizontal dotted line at 0.5. The decision time is 0.

A.1 Wrong slot errors

Wrong slot errors are produced by noise on the leading edge of a pulse causing a threshold crossing in the time-slot immediately before or immediately after the current slot. The probability of this error occurring is given by

$$P_s = 0.5erfc\left(\frac{Q_s}{\sqrt{2}}\right) \quad \text{(A-1)}$$

where $$Q_s = \frac{T_s}{2}\frac{slope(t_d)}{\sqrt{\langle n_o^2 \rangle}} \quad \text{(A-2)}$$

in which T_s is the slot time; $slope(t_d)$ is the slope of the received pulse at the decision time t_d and $<n_o^2>$ is the mean squared noise presented to the threshold detector. The threshold time is dependent on where the decision level is set on the received pulses.

A.2 Erasure errors

Erasure errors occur when noise corrupts the pulse amplitude such that the voltage level drops below the decision voltage, v_d. The probability of this occurring is:

$$P_{er} = 0.5erfc\left(\frac{Q_{er}}{\sqrt{2}}\right) \quad \text{(A-3)}$$

where $$Q_{er} = \frac{v_{pk} - v_d}{\sqrt{\langle n_o^2 \rangle}} \quad \text{(A-4)}$$

with v_{pk} being the peak signal voltage within the time slot.

A.3 False alarm errors

A false alarm error is caused by noise in an empty slot generating a threshold crossing and hence a false pulse. The probability of this is:

$$P_f = \frac{T_s}{\tau_R} 0.5 erfc\left(\frac{Q_t}{\sqrt{2}}\right) \quad \text{(A-5)}$$

where the term T_s/τ_R is the number of uncorrelated noise samples per time slot, τ_R is the time at which the autocorrelation time has become small, and Q_t is given by

$$Q_t = \frac{v_d - v_{ISI}}{\sqrt{\langle n_o^{\,2} \rangle}} \quad \text{(A-6)}$$

where v_{ISI} is any signal voltage that is present in a particular time slot.

Appendix 1.2: Submitted for publication

Performance Analysis of Duobinary Pulse Position Modulation for Graded-Index Plastic Optical Fibre Channel Using Maximum Likelihood Sequence Detection

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Abstract

Similar to pulse-position modulation (PPM), Duobinay PPM (DuoPPM) suffers from three types of pulse detection errors: wrong-slot, erasure and false-alarm. Due to naturally occurring sequences and inherent properties of DuoPPM, a maximum likelihood sequence detection (MLSD) technique can be found and algorithm has been developed for DuoPPM MLSD to detect and correct the pulse detection errors. This paper presents a performance analysis of DuoPPM MLSD over a highly dispersive optical channel operating at 1 Gbps pulse code modulation (PCM) data rate with a wide-band receiver and a matched filter.

The results show that at low fibre bandwidths DuoPPM outperforms Dicode PPM by 1.2 dB when operating with MLSD required considerably less photons per pulse. At high fibre bandwidths photon counts for both DuoPPM and Dicode PPM are very similar as expected due to low inter-symbol interference (ISI). DuoPPM can operate down to 0.46 times the bit rate at which it requires 27×10^3 photons per pulse compared to 40.3×10^3 required by Dicode PPM, and this indicates significant improvement in performance. All the results presented indicate that DuoPPM coding scheme with MLSD is an ideal alternative to be used for highly dispersive optical channels.

1. Introduction

In digital pulse-position modulation (PPM) based channel coding schemes, pulse detection errors that can occur are same [1-2]: wrong-slot, erasure and false-alarm errors. Recent coding schemes such as dicode PPM [3-4], multiple PPM [5-6], offset PPM [7] and duobinary PPM [8] have been considered and maximum likelihood sequence detection (MLSD) have been successfully applied to these schemes mainly operating over highly dispersive fibre optic channels. Other recent works have also been reported of applying MLSD for non-directed and free-space optical channels [9-11] with varying degrees of success.

Forney [12] first proposed maximum likelihood sequence estimation to resolve errors in digital sequences in the presence of intersymbol interference (ISI) which has been adopted as MLSD for the modern digital channel coding schemes. ISI is introduced by the channel and the degree of this depends on the channel dispersion and bandwidth characteristics. Channels such as glass fibre with higher bandwidth and low dispersion has very low ISI. On the other hand, graded-index plastic fibre optic channels (GI-POF) has very high ISI at low bandwidth and high dispersion characteristics. Therefore, application of MLSD for coding schemes used by such channels will significantly improve sensitivity [2-3, 5].

Digital PPM has greater resilience to ISI [1, 13] thus it is preferred for non-directed free-space optical channels [14]. However, digital PPM is not very efficient for its prohibitively high bandwidth expansion for low bandwidth channels such as GI-POF [15]. Therefore, alternative schemes have been proposed for dispersive channels [3-7].

Duobinary pulse-position modulation (PPM) has been previously proposed as a novel coding scheme to improve sensitivity and bandwidth efficiency operating over highly dispersive graded-index plastic optical fibre channel [1]. When used with MLSD multiple PPM [5-6] offers the same sensitivity as digital PPM without significantly comparable bandwidth expansion. These alternative coding schemes has inherent valid sequences that can be checked and determined at the receiver using MLSD algorithm if the data is corrupted due to ISI of the channel, and in the event of any error in the sequence, the MLSD algorithm designed with the decoder will suggest the most likely correct sequence for the given error and the data will be decoded after it is checked. Sibley [4] showed that by using MLSD algorithm for dicode PPM the effect of all three types of errors can be remarkably reduced to give comparable sensitivity of digital PPM with only twice the data rate of the original pulse code modulation (PCM) signal.

MLSD has also been considered and applied to other modulation systems operating over free-space channels, such as differential PPM [16], Pulse-Interval Modulation (PIM) [17-18] and Dual-Header PIM (DH-PIM) [19]. Simple alternatives to MLSD such as decision-feedback equalisation [20] and Trellis-coded modulation [21] have also been proposed but MLSD is very simple to implement thus simplifying decoder design.

Duobinary PPM [8], is an alternative coding scheme to digital PPM and other coding schemes for dispersive channels which combines the duobinary technique and digital PPM to form DuoPPM as shown in Fig. 1.

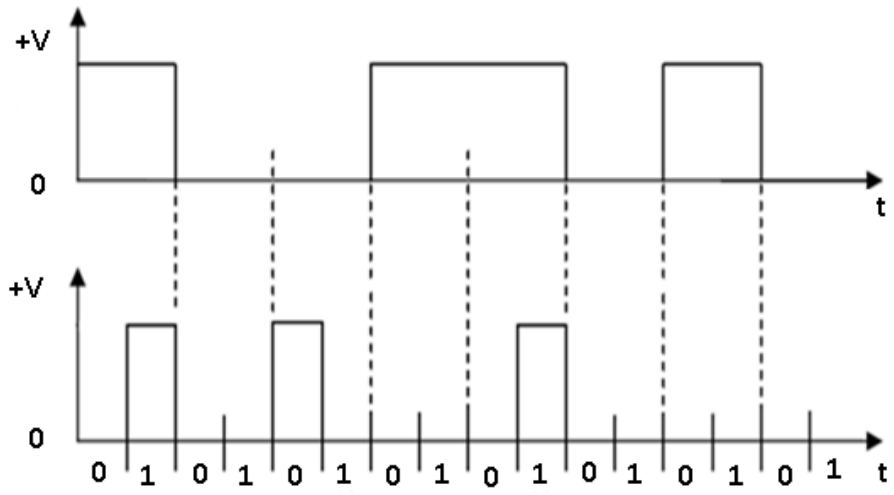

Fig. 1: Conversion of PCM data (top trace) into DuoPPM (bottom trace).

In this signalling format, a signal is only transmitted when the data are constant at either logic 1 or logic 0, and no signal is transmitted for data transitions from logic 1 to logic 0 or from logic 0 to logic 1 – the change condition. As will be described and analysed later, the use of a novel MLSD algorithm allows for the elimination of wrong-slot errors and significantly reduces the effects of false alarm and erasure errors. Original PCM data is line coded thus the maximum number of like symbols is limited to facilitate timing extraction [4].

An original method of implementing the duobinary PPM MLSD algorithm has been presented in the paper. Due to the predetection errors mentioned earlier which is caused by the ISI of the channel, valid sequences become invalid – such as a 1 is received immediately after a 0 and further complex form of invalid sequences. MLSD detects these errors and applies algorithm to suggest most reliable valid sequence in case of errors. Mathematically modelled theoretical

simulation results presented in this paper show that duobinary PPM has a sensitivity advantage of 1.2 dB over dicode PPM for highly dispersive optical channels at very low fibre bandwidths where ISI is very high. Theoretical system operates at 1 Gbps with a classical matched filter.

2. MLSD Operation of Duobinary PPM

2.1 Wrong-slot Errors

The primary reason of wrong slot errors is intersymbol interference (ISI) when operating at low fibre bandwidths. It occurs when the noise on the slope of a pulse in a given time slot makes the edge of the pulse appear in adjacent time slot [8]. Duobinary PPM coding scheme has been developed to provide significant advantage when operating at low bandwidths and highly dispersive channels thus it is imperative that the wrong-slot errors are completely eliminated to be able gain any improvement in sensitivities.

Pulse Error	**Invalid Sequence**	**Method of Detection**
0 → 1	1/0 *x*C 1/0 *y*C 1/0	Same symbols at both ends after ODD number of Cs Opposite symbol at both ends after EVEN Cs
0 ← 1	1/0 *x*C 1/0 *y*C 1/0	Double Pulse
1 ← 0	1/0 1/0 0/1 yC 1/0	1 and 0 consecutively.
1→ 0	1/0 xC 1/0 0/1 0/1	1 and 0 consecutively.

Table 1: Wrong-slot pulse error and detection methods for duobinary PPM.

As it can be seen from the Table 1 that the invalid sequence for wrong slot of 0 forwarded to 1 can be easily detected by counting the number of C pulses that arrives consecutively. This is always corrected by changing the middle 1/0 pulse to the opposite pulsed symbol thus returning

0 errors. The key MLSD rules of the duobinary PPM is that when a number of consecutive Cs are received then if the number is ODD, this indicates that first and last symbol before and after the reception of Cs must be OPPOSITE, and if the number of Cs are EVEN then it indicates that first and last symbol of a the sequence must be SAME. Furthermore, there will never be a 1 right after 0 and vice versa for a sequence to be valid and these rules are applicable for all three types of errors for detection and correction algorithm. When 1 goes back to 0 as shown in the Table 1 it will produce double pulse in the same frame which is easily detectable and after correction returns 0 PCM errors. However, there are exceptional circumstances when a 0 goes back to 1 and a 1 goes forward to 0 to cause wrong-slot errors. Although these are wrong-slot errors, they do appear to be false alarm errors when being detected. However, for the coding scheme to be operated over dispersive low bandwidth channel, these two errors must be eliminated in order to completely eliminate the wrong-slot errors which is the main types of errors of the aforementioned channel at low bandwidth. Therefore, whenever these two particular error occurs, they are treated as wrong-slot errors even though they may appear as false-alarm and corrected always by changing the middle symbol of three consecutive pulsed symbols to C.

For example, when 110xC1 is received as an invalid sequence it will always be corrected to 1C0xC1 and when 0xC100 is detected it will always be corrected as 0xC1C0 thus completely eliminating the wrong-slot errors in the process which will significantly improve the sensitivity of the coding scheme at low bandwidths.

2.2 Erasure Errors

Due to erasure errors the pulses in 1 or 0 from a sequence cane be erased thus introducing errors in the sequence. Depending on the maximum permissible consecutive like symbols the number of errors at the PCM output could be severe for the longest sequence allowed. If not resolved by using MLSD this kind of errors can have negative impact on the sensitivity of the system. Table 2 shows an erasure of 1 in the transmitted sequence and when this error is detected by MLSD there are 5 possible valid sequence combinations that can be derived. Most possible valid combination is decided by determining all possible PCM sequences, finally averaging each bit to find the most likely sequence.

Transmitted Sequence								0		C		C		C		1		C		0	
Error Detected								0		C		C		C		***C***		C		0	
All Valid Combinations								**Decoded PCM**													
0	0	C	C	C	C	0		0	0	0	1	0	1	0	0						
0	C	1	C	C	C	0		0	0	1	1	0	1	0	0						
0	C	C	0	C	C	0		0	0	1	0	0	1	0	0						
0	C	C	C	1	C	0		**0**	**0**	**1**	**0**	**1**	**1**	**0**	**0**						
0	C	C	C	C	0	0		0	0	1	0	1	0	0	0						
								0	**0**	**1**	**0**	**0**	**1**	**0**	**0**		**1 ERROR**				

Table 2: MLSD Detection and correction of a duobinary sequence where a 1 has been erased (highlighted in bold italic).

In case of the error shown in Table 2 above, the most likely valid sequence has a PCM error of 1 after using MLSD. Therefore, it is clear that there will still be a possible number of errors even with the use of the MLSD algorithm. However, without MLSD the number of PCM errors would be 3. An exception in the erasure error detection is that if 08C1 is received then it will immediately appear that an erasure error had occurred somewhere in the sequence. However,

if the next symbol after 1 is 0 then it will be detected a wrong-slot error of 0 back to 1, the sequence will be corrected by changing 1 to C thus the corrected sequence would be 09C1. In any disambiguation during the decision making process for correction, wrong-slot correction will always take priority.

2.3 False-alarm Errors

This occurs when the amplitude of the noise is greater than the threshold level and can result in false 0 or 1 in a C symbol slot [8]. Similar to the method shown in the previous section of erasure errors the detected invalid sequence is resolved by determining all valid PCM sequences and averaging each bit to get the final valid PCM sequence. Table 3 below shows a transmitted sequence been corrupted by a false-alarm of 1. After applying MLSD to the invalid sequence, the overall PCM error is 0.5. Without the MLSD use the error in the sequence would be 3. Number of final PCM errors after applying MLSD depends on where the error has occurred in the sequence. If it occurs early in the sequence and the sequence is particularly long then the number of PCM errors would increase. However, applying MLSD will still ensure significant improvement in sensitivity compared to when deployed without MLSD.

Transmitted Sequence								1	C	0	C	C	C	1
Error Detected								1	C	0	C	***1***	C	1
All Valid Combinations								**Decoded PCM**						
1	C	0	C	1	1	1		1	1	0	0	1	1	1	1		
1	C	0	C	C	C	1		**1**	**1**	**0**	**0**	**1**	**0**	**1**	**1**		
								1	**1**	**0**	**0**	**1**	**1/0**	**1**	**1**		**0.5 ERROR**

Table 3: MLSD Detection and correction of a duobinary sequence where a false 1 has been detected (highlighted in bold italic).

2.4 Proposed MLSD Implementation on FPGA

The next stage of the research is to design and implement the duobinary PPM coding system using VHSIC hardware description language (VHDL) and field programmable gate array (FPGA) to complete an integrated system design. Previously attempts have been made [4] to implement MLSD schemes of other channel coding scheme using discrete logic. However, as the systems becomes more complex the device becomes bulky and compromises need to be made regarding reduction of inherent complexity. The modern FPGA processing power and VHDL design capability means that with expertise of programming and design any complex systems such as MLSD can be easily implemented without making any compromises. Fig. 2 in the following page low shows a proposed system for MLSD implementation of duobinary PPM.

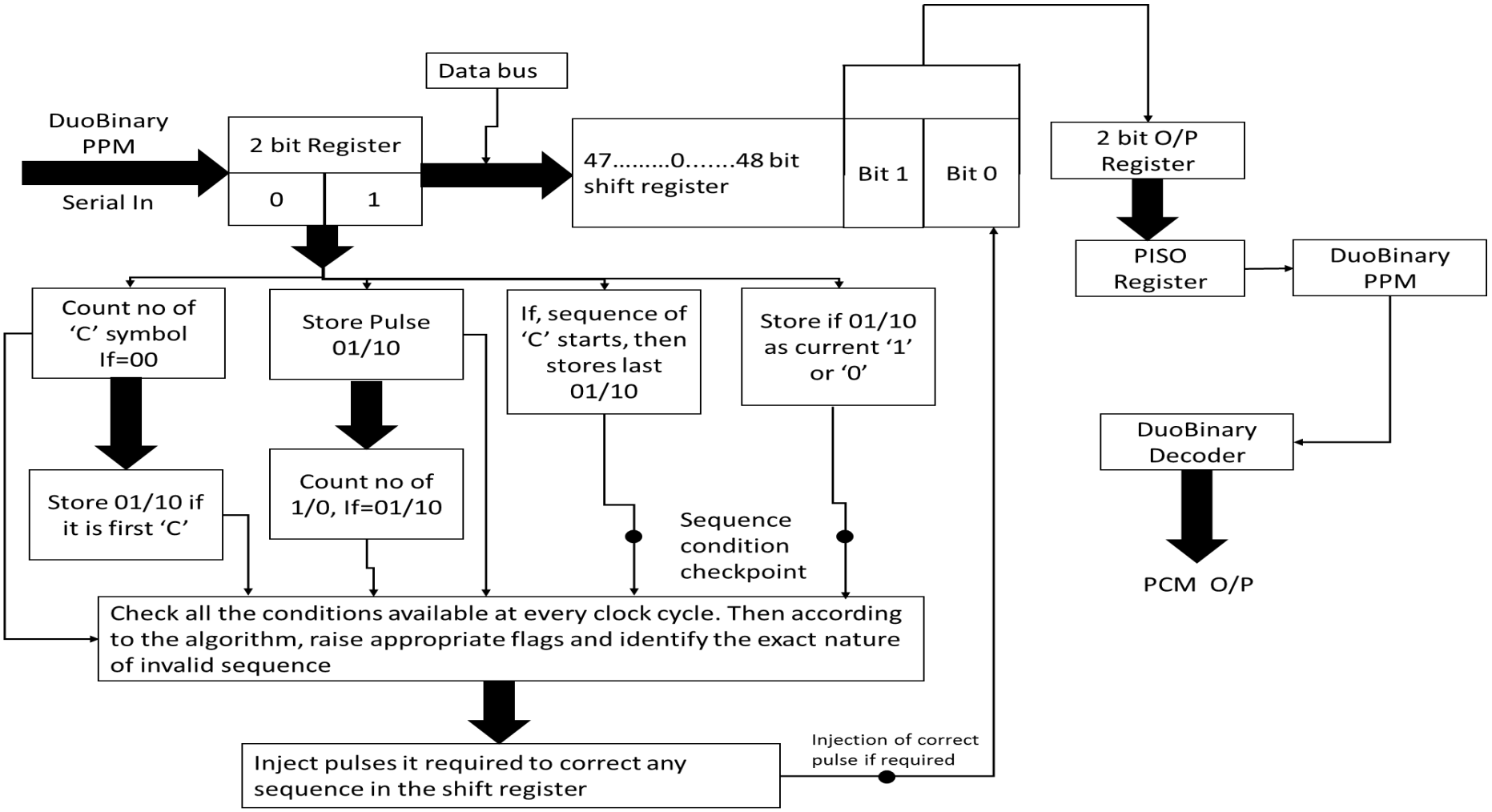

Fig. 2: Block diagram of proposed MLSD implementation using VHDL and FPGA.

In this design (shown in previous page), input duobinary PPM data will be stored in a two-bit register according to slot and frame synchronisation. Therefore, two-bit register will hold a complete frame of the duobinary PPM. Another 48-bit internal register will hold 24 frames of duobinary PPM data at given time. Any two bit incoming data will be added in the 48-bit register as this acts as shift register where correction will take place and the last two-bits will be corrected output at every clock cycle. Maximum number of like symbols has been assumed to be 10 thus 24 frames in the sift register. However, any good VHDL design is easily scalable and higher number can be implemented easily. 24 frames of duobinary PPM include two complete sequences of maximum length for error detection and correction purpose.

An example would be, 1 10C 1 10C 11 where 24 frames complete that whole sequence. Every time as frame is received checks are made for variables such as counters to count number of Cs or number of 1s and 0s, first symbol of a sequence, middle pulse if there are two sequences, last symbol of the sequence. If there are errors, flags are raised for any of the three errors and exact location of the error is determined. If flag is raised the corrector will correct the required frames and output will be last two bits of the 48-bit shift register. Currently work being carried out to implement the MLSD using VHDL and FPGA completed with bit error rate test system embedded in the device. Results of the practical implementation will be published soon upon successful completion.

3. Duobinary PPM Error Probabilities Algorithm

General error probabilities of duobinary PPM is same as dicode PPM [18]. Therefore, it is not necessary to repeat the equation for the general probability.

3.1 Erasure Algorithm

An erasure of a pulse occurs when a pulse is erased in between two like symbols which results in an invalid sequence of code containing two like symbols separated by any of the other two types of symbols. Equivalent PCM errors was derived from the following expression for a duobinary PPM sequence of **0xC1/0yC1/0**,

$$\text{Error}_{x,y} = \frac{|x-y|}{2} \quad (1)$$

Equation (1) applies to both erasure of pulse 1 and 0. If the invalid sequence shown previously in section 2.2, table 2 then equation (1) resolves the invalid sequence and provides with correct number of equivalent PCM errors that will be produced.

The probability of an erasure error, P_{er}, is

$$P_{er} = Errors * 0.5 erfc\left(\frac{Q_{er}}{\sqrt{2}}\right) \quad (2)$$

where

$$Q_{er} = \frac{v_{pk} - v_d}{\sqrt{< n_o^{\,2} >}} \quad (3)$$

Where V_{pk} is the peak-signal voltage within the given time slot and the effect of ISI can be measured by determining the peak amplitude of the given pulse within the frame for certain

combinations of x and y. At low normalised fibre bandwidths there is very high probability of the peak of the signal to appear in the following time slot, as shown in Fig. 6, largely due to pulse dispersion.

3.2 False Alarm Algorithm

The probability of a false alarm error is given by

$$P_f = Error * 0.5\, erfc\left(\frac{Q_f}{\sqrt{2}}\right) \tag{4}$$

where

$$Q_f = \frac{v_d - v_{ISI}}{\sqrt{< n_o^{\,2} >}} \tag{5}$$

Threshold level, *v*, was used as a system variable which is defined by

$$v = \frac{v_d}{v_{pk}} \tag{6}$$

where v_d is the peak voltage of an isolated pulse and is the decision voltage. Pulse shape and noise can be determined theoretically if the fibre bandwidth is known.

Equivalent PCM errors was derived from the following expression

$$Error_{x,y} = \frac{|Combinations_{x,y} - 1|}{2} \tag{7}$$

Number of valid combinations varies depending on type of false-alarm error, data sequence and the position of the error in the sequence. Therefore, for a false-alarm error of **0 in 1yC0** or **1 in 0yC1**, number of valid combinations are calculated using the following equations:

If position of error *(k)* is ODD, then

$$Combinations_{x,y} = k+1 \quad (8)$$

If position of error *(k)* is EVEN, then

$$Combinations_{x,y} = y-k+1 \quad (9)$$

For a false-alarm error of **0 in 0yC1** or **1 in 1yC0**, number of valid combinations are calculated using the following equations:

If position of error *(k)* is ODD, then

$$Combinations_{x,y} = y-k+1 \quad (10)$$

If position of error *(k)* is EVEN, then

$$Combinations_{x,y} = k+1 \quad (11)$$

4. Mathematical Modelling and Performance Evaluation

Mathematical simulation and representation of DuoPPM MLSD has been done in order to evaluate the performance of the system in Graded-Index (GI) POF channel. The reason for choosing this particular channel was that it is highly dispersive, and as has been proposed by the previous publication [8] that DuoPPM will perform better in dispersive channel with MLSD compared to digital PPM and Dicode PPM [1-4]. The impulse response of the GI-POF channels can be approximated to be a Gaussian distributed pulse shape [22]. The signal represented to the threshold detector of the system is similar to that of the Dicode PPM [3-4] as both systems have to be comparable for the purpose of analyses, due to their inherent coding mechanisms.

The signal is given by the following expression:

$$v_o(t) = \frac{b\eta q}{2\pi} \int_{-\infty}^{\infty} Z_{pre}(\omega) H_p(\omega)^2 \exp(j\omega t)\, d\omega \qquad (12)$$

This can be described as the pulse shape of a classical matched filter which is presented at the input of the threshold detector where b is the number of photons per pulse, η is the quantum efficiency of the detector, q is the electronic charge and $Z_{pre}(\omega)$ is the frequency dependent transimpedance of the preamplifier at the receiver. Variation of the received pulses is given by, α, which is directly linked to the fibre bandwidth [23] and given by

$$\alpha = \frac{0.1874 T_b}{f_n} \qquad (13)$$

where T_b is the PCM bit time and f_n is the fibre bandwidth normalised to the PCM data rate. A receiver system has been proposed in the previous publication [8] and the block diagram of the proposed receiver system is given in the Fig. 3 below.

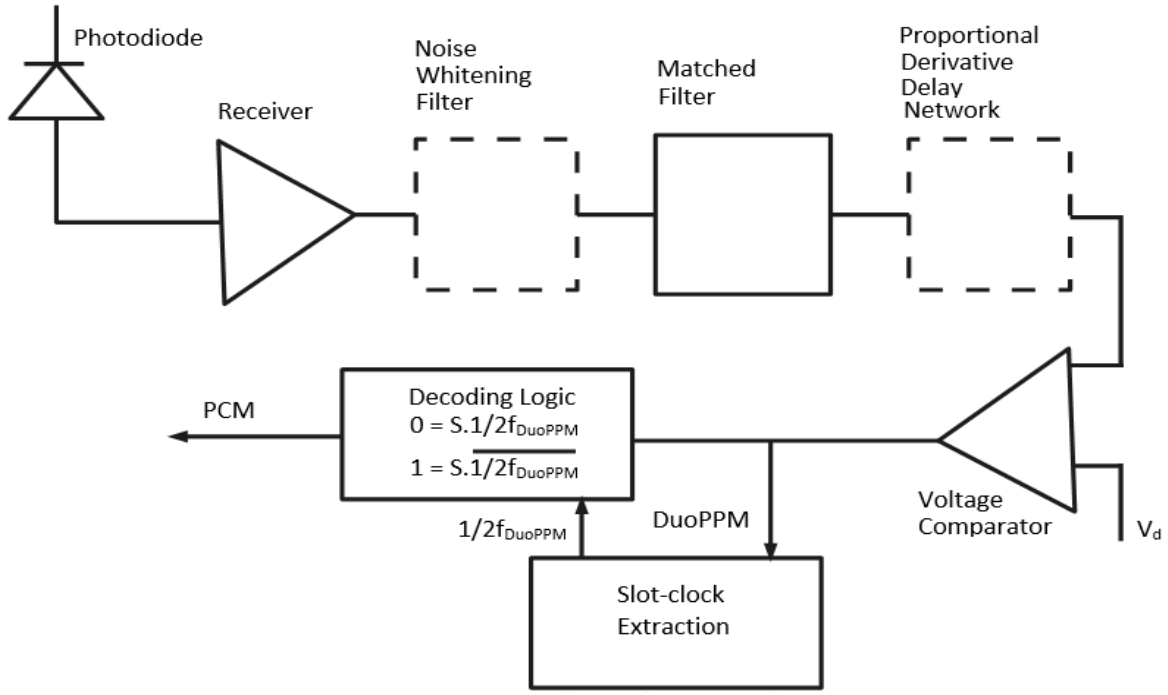

Fig. 3: Block diagram of the proposed DuoPPM receiver.

According to the proposed system given in Fig. 3, the mathematical system used for simulation implements an optical receiver with a limited-bandwidth which is given by, ω_c, and a white noise spectrum at the output. Since a PIN photodiode has been used its shot noise is negligible for the system modelling purpose. Matched filter has been used a pre-detection filter and proportional derivative delay (PDD) network is optional to the receiver system and it has not been used in the simulation model before the signal being presented at the threshold detector. Noise that appears on the signal is similar to that of Dicode PPM and Multiple PPM [3-6] therefore has not been repeated here.

In common with Dicode PPM, a threshold level, v, was used as a system variable defined by

$$v = \frac{v_d}{v_{pk}} \qquad (14)$$

where v_{pk} is the peak voltage of an isolated pulse and v_d is the decision (threshold) voltage. The pulse shape and noise can be determined theoretically if the fibre bandwidth is known [3]. Simulations were performed to find the optimum value of v_d that gave the minimum number of photons per pulse, b, for a specified error rate of 1 in 10^9.

A 1 Gbit/s PCM data-rate system, operating at a wavelength of 650 nm and a photodiode quantum efficiency of 100% was considered. The preamplifier had a bandwidth of 10 GHz and white noise of 50 x 10-24 A2/Hz when referred to the input. The aforementioned parameters were obtained from a commercial device. Line coded PCM data was used so that n=10 and simulations were conducted on DuoPPM system operating with an MLSD.

5. Results and Discussion

Results have been obtained and analysed to verify the performance of the modelled system operating with MLSD. Three key results have been presented in this section to make sufficient comparisons between DuoPPM and Dicode PPM. Fig. 4 shows the required number of photons per pulse with fibre bandwidth normalised between 0.46 and 100 for DuoPPM and Dicode operating with MLSD. It can be seen from the overall graph that DuoPPM outperforms Dicode PPM for low fibre bandwidths. However, at high fibre bandwidths the performance of both coding scheme is very similar although DuoPPM still holds slightly better performance than Dicode.

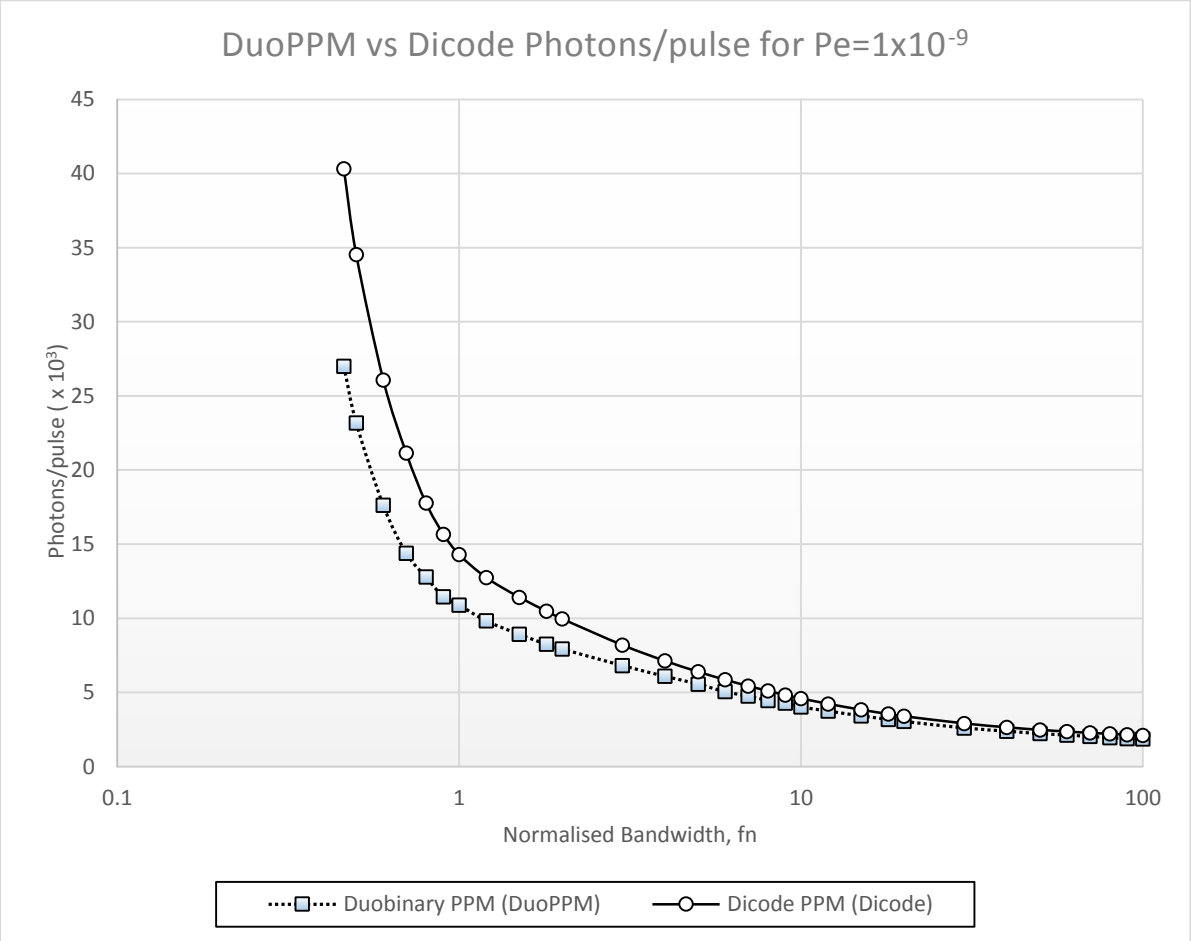

Fig. 4: Comparison between DuoPPM and Dicode required photons/pulse as a function of normalised bandwidth, f_n.

Both coding systems are functionally operational at normalised fibre bandwidth as low as 0.46, however, it is not possible to go below this point as the pulses become highly dispersed and the threshold voltage required for detection is very high as can be seen from Fig. 6 compared to less dispersed pulses as shown in Fig. 5. At high bandwidth, photons per pulse required for DuoPPM is 1902 compared to 2114 of Dicode. These numbers are very similar at high bandwidths because the intersymbol interference (ISI) is favourably low and errors are pattern independent. Therefore, there the difference in error probabilities between 100 and 10 normalised bandwidths is negligible.

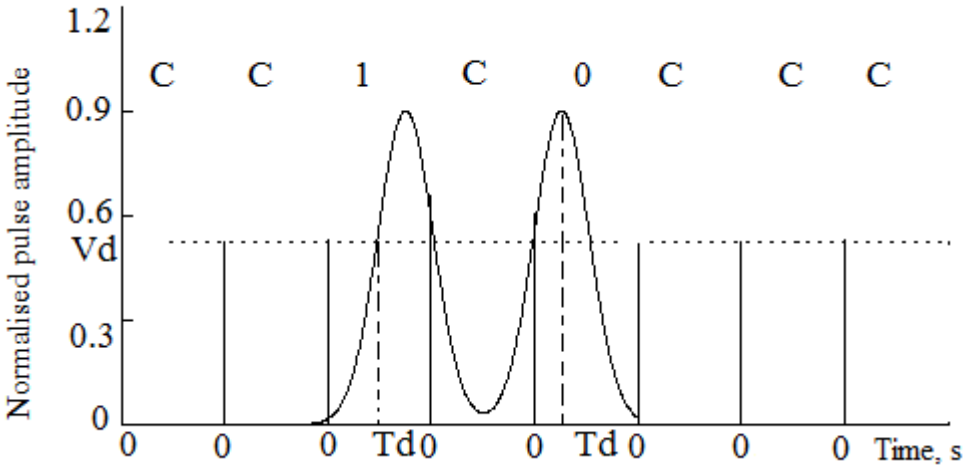

Fig. 5: Simulated pulse response at normalised bandwidth of 1 for the sequence 1C0 (amplitude normalised to a single isolated pulse).

As the normalised bandwidths gets low down to 1 and below, DuoPPM performance advantage is significant as it needs considerably less photons per pulse, with 10.9 x 10^3 photons required compared to 14.3 x 10^3 needed for Dicode which results in a difference of 1.2 dB approximately. Below the normalised bandwidth of 1 the pulses become very dispersed which has direct effect on the performance of both systems as shown by figure 6.3 and 6.4. Pulse become dispersed so that the peaks spreads out in the adjacent slots and detection only possible

by the pulse remaining at the edge of the correct slots and the detection also requires very high threshold level. The lowest normalised bandwidth that the systems can be operable is down to 0.46 where DuoPPM requires 27 x 10^3 photons per pulse compared to 40.3 x 10^3 required by Dicode.

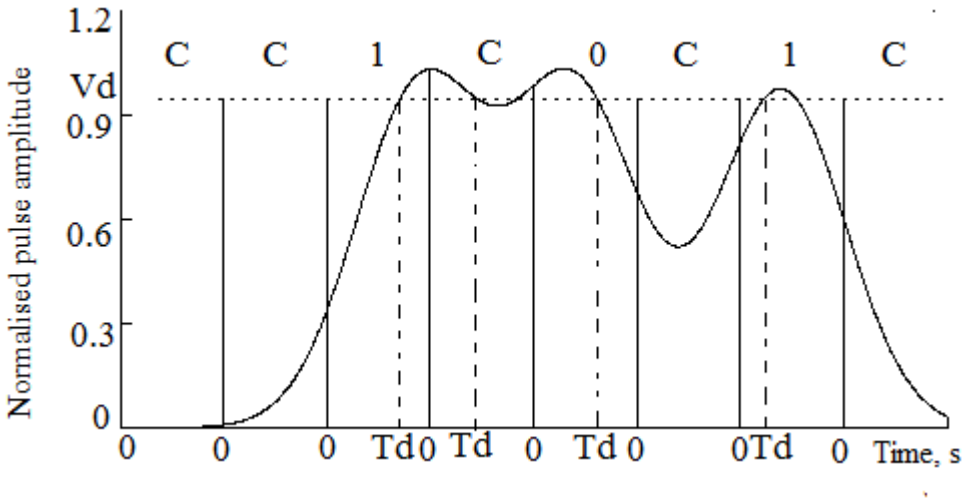

Fig. 6: Simulated pulse response at normalised bandwidth of 0.46 for the sequence 1C0C1 (amplitude normalised to a single isolated pulse).

Table 4 shows the required photons per pulse for DuoPPM system operating over specific normalised fibre bandwidths and the error probabilities in 1 x 10^{-10} for each type of error that has been discussed in section 2 and 3 previously. It has been shown that with the operation of MLSD wrong-slot errors can be eliminated thus the error probabilities and the overall sensitivity of the system is are dominated by the erasure and false-alarm errors. Probability of erasure for both 1 and 0 are same over the range of the bandwidths which is expected as has been discussed previously in section 2. However false-alarm of 1 is significantly higher as the bandwidth goes very low and contrastingly false-alarm of 0 becomes a non-occurring event. This is expected as well because at very low normalised fibre bandwidths the pulses are so dispersed that they spread out to the neighbouring frames and slots thus giving rise to the false-

alarm error of 1 and for the same reasons the false-alarm error of 0 becomes non-existent. DuoPPM system has been able to operate down to 0.46 times the bit rate as shown in the Table 4 and the system is inoperable below this due to very high threshold voltage as has been shown in Fig. 6. It is also noticeable that when DuoPPM is deployed for highly dispersive optical channels at very low normalised fibre bandwidths it must be operated with MLSD as non-MLSD system will be highly unsuitable.

Normalised link bandwidth (f_n)	**100**	**10**	**1**	**0.5**	**0.46**
Photons per pulse (10^3)	1.9	4.03	10.9	23.19	27
Threshold parameter, V	0.4	0.49	0.58	0.89	0.975
Error Probabilities (10^{-10})					
Erasure 1 => C	3.19	2.55	2.38	2.23	2.08
Erasure 0 => C	3.19	2.55	2.38	2.23	2.08
False Alarm C => 1	1.31	2.25	2.43	5.54	5.84
False Alarm C => 0	2.32	2.74	2.81	0	0

Table 4: Error probability results of DuoPPM system operating with MLSD at specific normalised link bandwidths.

6. Conclusions

This paper has presented the maximum likelihood sequence detection system and algorithm that has been developed and implemented for the Duobinary PPM coding system. There are inherent properties of the coding scheme that dictate the correct and incorrect sequences of pulses that should be received and any deviation from these rules will result in detection of errors in the sequence. These properties of the coding scheme have been discussed both in general terms and mathematically in sections 2 and 3. From these naturally occurring correct sequences, algorithm has been developed for ease of understanding and practical implementation which is the next stage of the research. Using the MLSD for DuoPPM, wrong-slot errors can be completely eliminated and the effect of erasure and false-alarm errors can be significantly reduced especially when operating at very low normalised fibre bandwidths.

Mathematical modelling and simulations have been carried out with a wide-band receiver, matched filter and highly dispersive graded-index POF channel operating at a data rate of 1 Gbps. The results have been presented and analysed in the previous section which shows that at low fibre bandwidths Duobinary PPM sensitivity outperforms Dicode PPM by 1.2 dB when operating with MLSD because it requires considerably less photons per pulse for pulse detection. At high fibre bandwidths photon counts for both DuoPPM and Dicode PPM are very similar as expected due to low ISI.

Duobinary PPM can operate down to 0.46 times the bit rate at which it requires 27×10^3 photons per pulse compared to 40.3×10^3 required by Dicode PPM, and this indicates significant improvement in performance. Considering the results presented in this paper it can be concluded that Duobinary PPM coding scheme with MLSD is an alternative that needs significant attention for further research to be used for highly dispersive optical channels.

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Appendix 1.3: This paper has been published in the Computing and Engineering Researcher's Conference, University of Huddersfield, December 2013.

SIMULATION AND TIMING ANALYSES OF VHDL MODELS OF CODER AND DECODER OF DUOBINARY PULSE POSITION MODULATION

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Abstract

Duobinary Pulse Position Modulation (DuoPPM) has been proposed as an alternative novel coding scheme which manifests many advantages over currently existing PPM formats according to the preliminary results obtained from theory and simulations run by one of the authors, Sibley. It combines the bandwidth reduction of the three-level duobinary code with the dispersion characteristics of conventional PPM. This coding is intended to be implemented using VHDL (VHSIC hardware description language) and an FPGA (Field-programmable gate array) over Plastic Optical Fibre (POF). Nevertheless if the preliminary promises of this new coding scheme are fulfilled upon successful implementation, it may be adapted to high-speed optical communications links. For the first time, the original VHDL designs, simulation results and timing analyses of DuoPPM coder and decoder are presented in this paper. These design developments are the fundamental circuits required for further investigation of this proposed coding scheme.

Keywords: Duobinary, DuoPPM, Coder, Decoder, VHDL, FPGA, Plastic optical fibre (POF)

1. Introduction

Pulse Position Modulation (PPM) schemes has been established as a leading method of utilising bandwidth available in the optical fibres, with significant improvement in sensitivity compared to equivalent Pulse Code Modulation (PCM) [1-3]. Various schemes of PPM have been proposed and investigated in the past for use in optical communications links [1-9]. Some of these PPM schemes can be attractive and suitable to implement for use in glass fibre or direct line of sight networks where bandwidth is not a concern, but unfortunately these optical communications links are expensive and not suitable for everyday use such as home networks, industrial networks and many other potentially direct consumer applications.

The authors introduce a novel coding technique that combines dibit, an alternative form of a tertiary code sometimes used in magnetic recording, and digital PPM to form DuoPPM. DuoPPM operates at only two times faster than that of the original PCM data rate, thus reducing the bandwidth, making it a potentially attractive coding scheme for Plastic Optical Fibre (POF) which suffers from low bandwidth; and high dispersion and attenuation because of the material [10-12]. Siemens AG (2007) [13] claimed to successfully achieve 1 Gbit/s data rate over POF for 100 meter long distance using Quadrature Amplitude Modulation (QAM). This claim may prove to be significant as it proves that with the rapid development in POF material and related technologies, it can achieve sufficiently high bandwidth to cater for increasingly high speed consumer demands.

PCM data coded by DuoPPM scheme is as follows: a PCM data transition from zero to zero produces a pulse in slot 0 and a one to one transition produces a pulse in slot 1 (fig 1.1). No pulses are transmitted during PCM data transitions of one to zero and zero to one and these frames are denoted as C (change). Table 1 shows the DuoPPM symbol alphabet. As there are four symbols, each symbol has a probability of $1/4$. However, the probability of a change sequence (C) is $1/2$ as it occurs with both one to zero and zero to one transitions of PCM sequence. A typical DuoPPM sequence would be 0, xC, 1 with probability of $1/4$, $(1/2)^x$ and $1/2$ respectively.

As only two slots are used to transmit one bit of PCM data, the data rate is two times that of the original PCM, thus the speed has been significantly reduced compared to digital PPM. For the first time, original VHDL hardware designs of DuoPPM coder and decoder will be presented and analysed in this paper.

2. DuoPPM Coder and Decoder

As this is a novel coding scheme, no previous references of coder or decoder construction of such types have been found. Therefore, these circuits had to be designed, developed and implemented using VHDL and FPGA in order to carry out further investigation of the DuoPPM scheme. First of all, the circuits were designed and simulated for functional verification and functional verification does not consider FPGA delays (fan-out, inertial delay, propagation delay, gate delay etc.). All delays were considered and compensated for FPGA implementation after the functional simulations were successfully completed for both circuits. As the bit rate of the data to be coded was at a high frequency (120 Mbit/s), Altera Cyclone® II FPGA was

the targeted device for the experimental implementation of the design; and timing analyses were successfully completed for the targeted device.

2.1 DuoPPM Coder

The DuoPPM coder is the part of a DuoPPM system that converts any PCM sequences into sequences that contain the DuoPPM symbols (Table 1). The PCM sequences were generated randomly by a Pseudo Random Binary Sequence (PRBS) generator. The PRBS generator was designed and implemented using VHDL language (Fig. 2.1) and the output of this PRBS block was used as the input of DuoPPM coder. The logic components that have been used to complete this DuoPPM coder are one D-type Flip-Flop (DFF), one NOR gate, 1 OR gate, one NOT gate and three AND gates. DFF delays the PCM sequence by half the clock cycle, the output of which is used with original PCM sequence to produce pulses at slots 0 and 1. Both original and delayed PCM sequences are then used as inputs to an AND gate and NOR gate. The use of clock signal and inverted clock signal are required to retime the DuoPPM pulse sequences for slot 0 and slot 1.The output of the AND gate then used as one of the two inputs of another AND gate along with the clock signal; and the output of the NOR gate is used as one of the two inputs of an AND gate along with inverted clock signal to produce pulses at slot 0 and slot 1. The outputs of the last two AND gates were then fed to the inputs of an OR gate that combines the signals to get the required DuoPPM coded sequences which have been converted from original PCM sequences.

2.2 DuoPPM Decoder

Theoretically, it is understood by engineers that a decoder could be constructed by using reverse design procedure of the coder. Nevertheless, in this case using the reverse design method produced incorrectly decoded PCM sequences because during PCM transitions of 1 to 0 and 0 to 1 no pulses were produced (Table 1). Therefore, decoding the parts of DuoPPM sequence when no pulses were available had to be carefully considered to decode the correct PCM sequence. There are two probable PCM sequences when no DuoPPM pulses were received consecutively: PCM transition of 1 to 0 and PCM transition of 0 to 1. This decision can be made if the position of the most recently received pulse, before the sequence of no pulse (C), is known. If the most recently received pulse is in slot 0 then the PCM sequence will be 1, 0, 1, 0…and so on; and if it is in slot 1 then the PCM sequence will be 0, 1, 0, 1…and so on. Therefore, a temporary memory block had to be designed using D-Type Flip-flops (DFF) and logic gates to store the most recently received DuoPPM pulse position. The logic components that have been used to complete the DuoPPM decoder are 12 DFFs, 6 XOR gates, 2 NOT gates, 1 XNOR gate, 2 NAND gates and 8 AND gates. The complexity of the decoder design increased due to be able to correctly decode PCM sequences when there were no pulses (C) received in DuoPPM sequence.

3. Simulation Results of Coder and Decoder

3.1 Simulation Results of DuoPPM Coder

Running the system with PRBS sequences as PCM input sequence is shown in figure 3.1 operating at 120MHz clock frequency. As it can be observed (fig 3.1) that the coded DuoPPM sequence for the input PCM sequence (PRBS) was as expected (table 1) according to the theory

of this coding scheme. Figure 3.1 clearly demonstrates that consecutive PCM bits of 1 produce pulses at slot 1 of the DuoPPM frame at the beginning of the second half of a clock period and consecutive PCM bits of 0 produce pulses at slot 0 of the DuoPPM frame at the beginning of a clock period for half a clock cycle.

3.2 Simulation Results of DuoPPM Decoder

Designed decoder of the system was tested by operating at the same frequency as the coder, 120MHz. Input DuoPPM sequences were taken from the output of the coder and the final decoded PCM sequence was compared with the input PCM (PRBS) sequence of the coder for functional verification of the decoder. Simulation result of the decoded output waveform is shown in figure 3.2. As expected the start edge of every decoded PCM pulse starts when the clock period starts. Figure 3.3 shows the simulation result of the complete system (coder and decoder) where coded DuoPPM is used as input of the decoder and the decoded PCM sequence can be observed. From the comparison of the PCM input sequence of the coder and the decoded PCM output sequence of the decoder it can be seen that the DuoPPM sequence has been correctly decoded back to PCM sequence. The short delay that appears between these two sequences is a result of the DFF delay in the decoder. Further checks were carried out to confirm the validity of the decoder output by using an XOR gate as Bit Error Rate Test (BERT) device. Both coder input PCM sequence and decoder PCM output sequence were synchronised and used as inputs of the XOR gate and no errors were registered.

4. Timing Analyses of Coder and Decoder

4.1 Timing Analyses of DuoPPM Coder and Decoder

In order to practically implement the designed coder and decoder on an FPGA timing analysis on all logic circuits needed to be completed since functional simulation does not consider any timing delays. First of all, the delays were identified for both circuits and required measures had to be taken to either remove the delays or if they were not removable then measures had to be taken to compensate for the existing delays as the signals need to be synchronised with the clock signals to produce correct outputs. Main types of delays identified for the circuits were inertia delay which is inherent in FPGA, transport delay (propagation delay), gate delays, fan-out and clock skew. Most of the delays were compensated by using DFFs that produce more delay to make the signals synchronised with required signals. The delays in coder circuit were compensated using additional logic elements of 3 DFFs, 1 OR gate and 1 NOR gate. Existing delays in the decoder circuit were compensated with the use of 19 additional DFFs. For functional simulation, 120MHz clock was used which is the frequency for PCM. But for practical timing analysis it was determined that two different clock frequencies were required: one 240MHz clock for DuoPPM as it runs at the data rate two times that of PCM thus PCM requires a 120MHz clock. Phase-locked Loop (PLL) was used to process the external 240MHz clock signal and it produces two output clock signals of 120MHz and 240MHz; and both output clock signals were source synchronised. The clock signals had to available throughout both circuits as dedicated clock signals to avoid any delays related to clock skew. Therefore, the clock signals were routed in the circuits as GLOBAL signals available approximately at the same time at different components minimising the effects of clock skew. If the clock signals are not routed as GLOBAL signals then FPGA will consider them as general signals and this

may cause, in synchronous circuits, the signals to arrive at different components at different times causing erroneous outputs from logic components.

4.2 Timing Analyses Measurements of DuoPPM Coder and Decoder

Figure 4.1 shows the complete circuit block schematic after design analyses were completed and input/output pins were assigned which will be implemented on FPGA. As it can be seen, a PLL circuit block was added for clock division and source synchronisation of the clock signals. This PLL can also be used during further investigation of slot and frame synchronisation and clock extraction for the received DuoPPM sequence. An MLSD error detector and corrector was also constructed using an original algorithm for this coding scheme which can also be seen from figure 4.1. As it can be observed from the timing analysis output waveform in figure 4.2 that the PLL, coder, decoder and MLSD error detector and corrector produces correct results at each stage of the circuit by compensating or removing all types of delays. It is also noticeable from figure 4.1 that there is delay of approximately 217ns from received DuoPPM sequence to the decoded PCM sequence. Most of this delay is due to MLSD error detector and corrector's register buffer and the rest is due to the delay compensation in the decoder.

5. Conclusions

The design and development of DuoPPM coder and decoder have been presented in this paper for the first time. Theoretical representations of DuoPPM coder and decoder waveforms and VHDL design simulation outputs haven shown. Two fundamental and essential parts of the system, coder and decoder, have been developed and further investigation on DuoPPM scheme can be carried out using these circuits.

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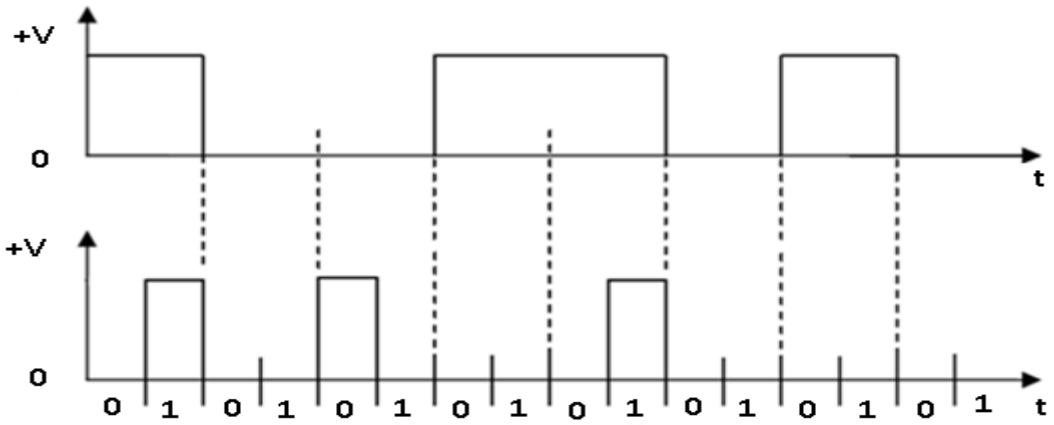


Fig. 1.1: Conversion of PCM data (top trace) to DuoPPM (bottom trace).

PCM	Probability	DuoPPM	Symbol
00	1/4	Pulse in slot 0	0
01	1/4	No pulse	C
10	1/4	No pulse	C
11	1/4	Pulse in slot 1	1

Table 1: DuoPPM symbol alphabet.

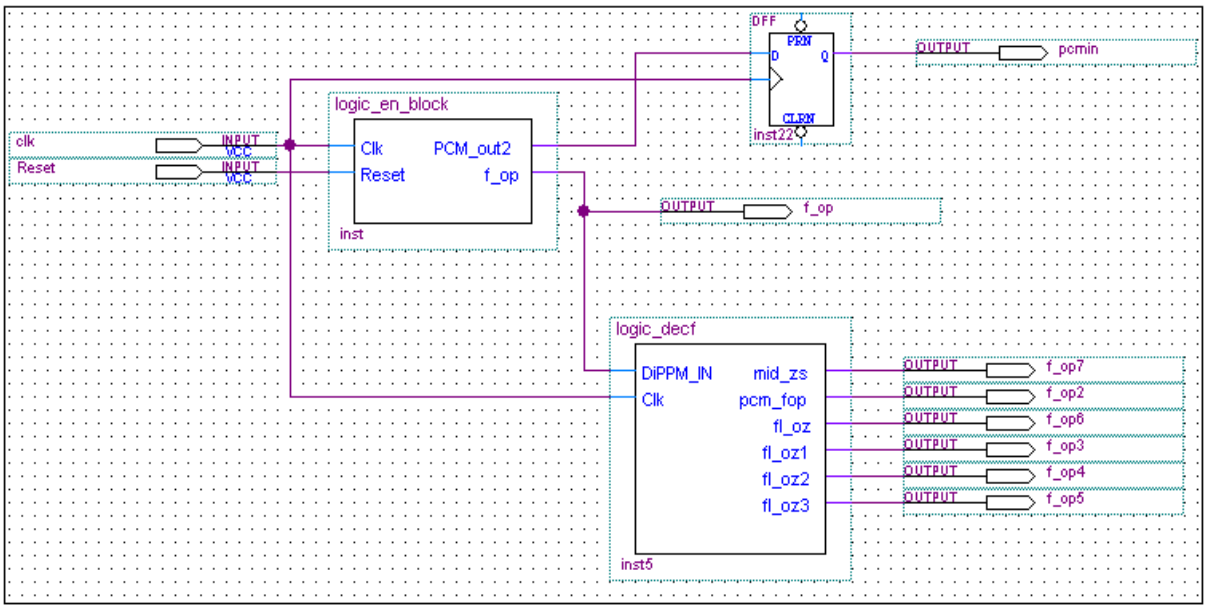


Fig. 2.1: VHDL coder and decoder block diagram schematic of DuoPPM decoder circuit.

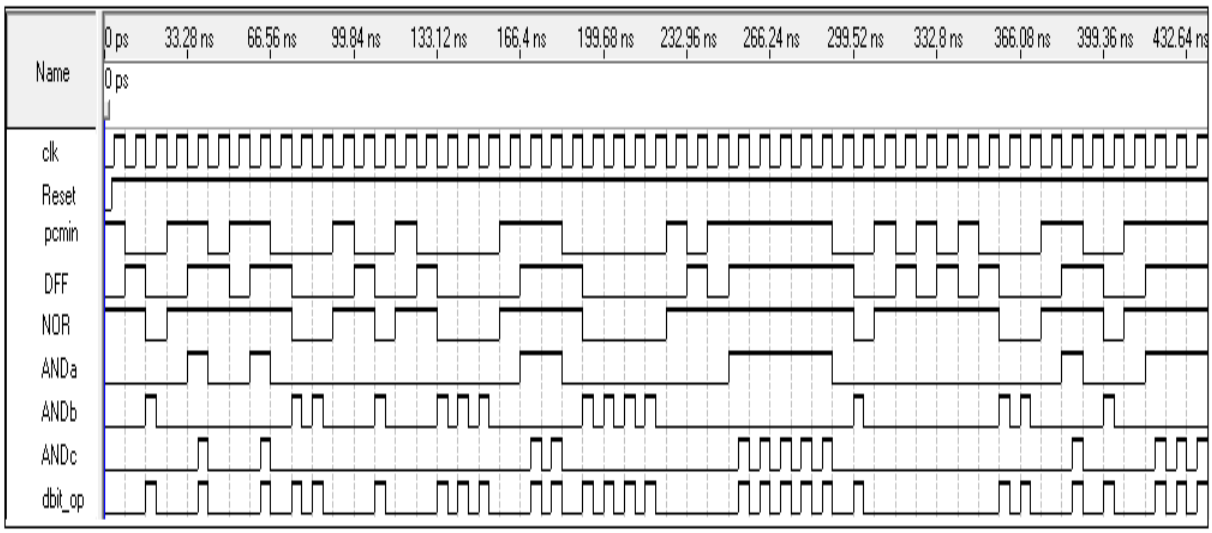


Fig. 3.1: VHDL coder simulation output waveform.

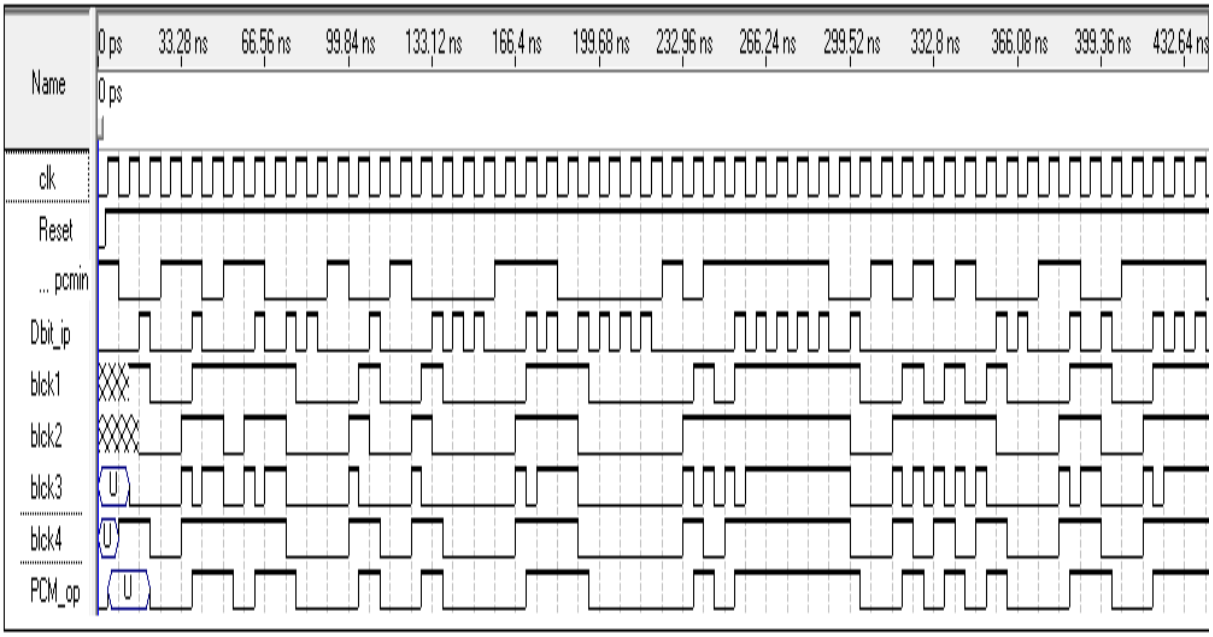


Fig. 3.2: VHDL decoder simulation output waveform.

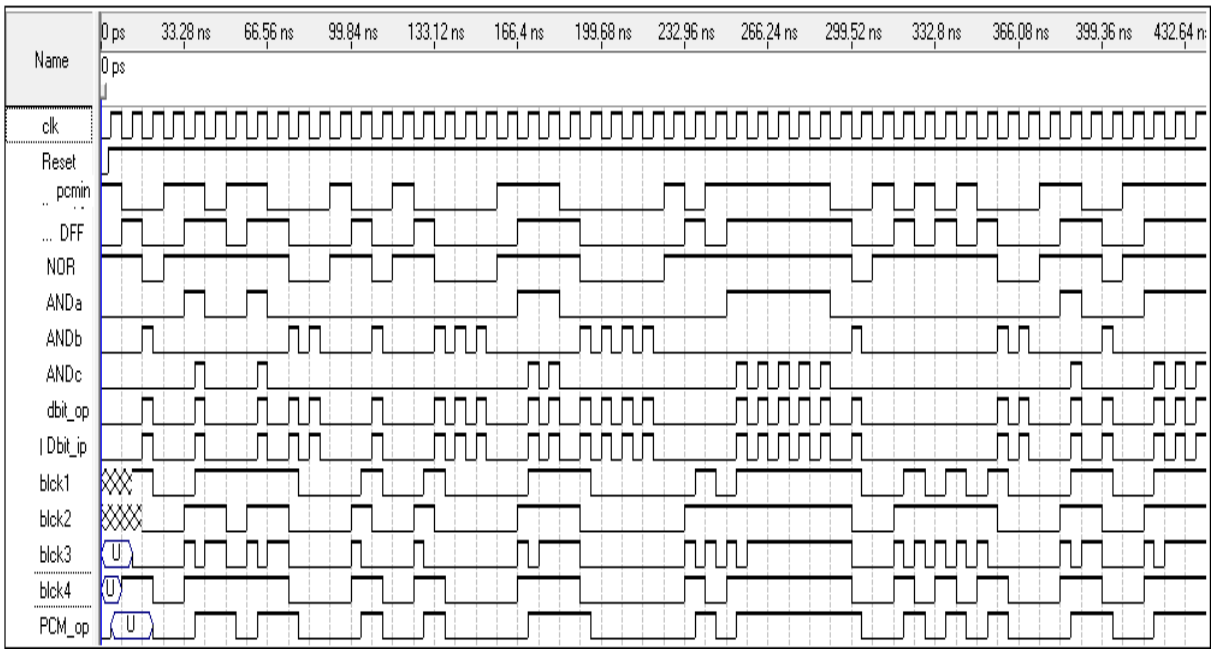


Fig. 3.3: VHDL coder and decoder simulation output waveform.

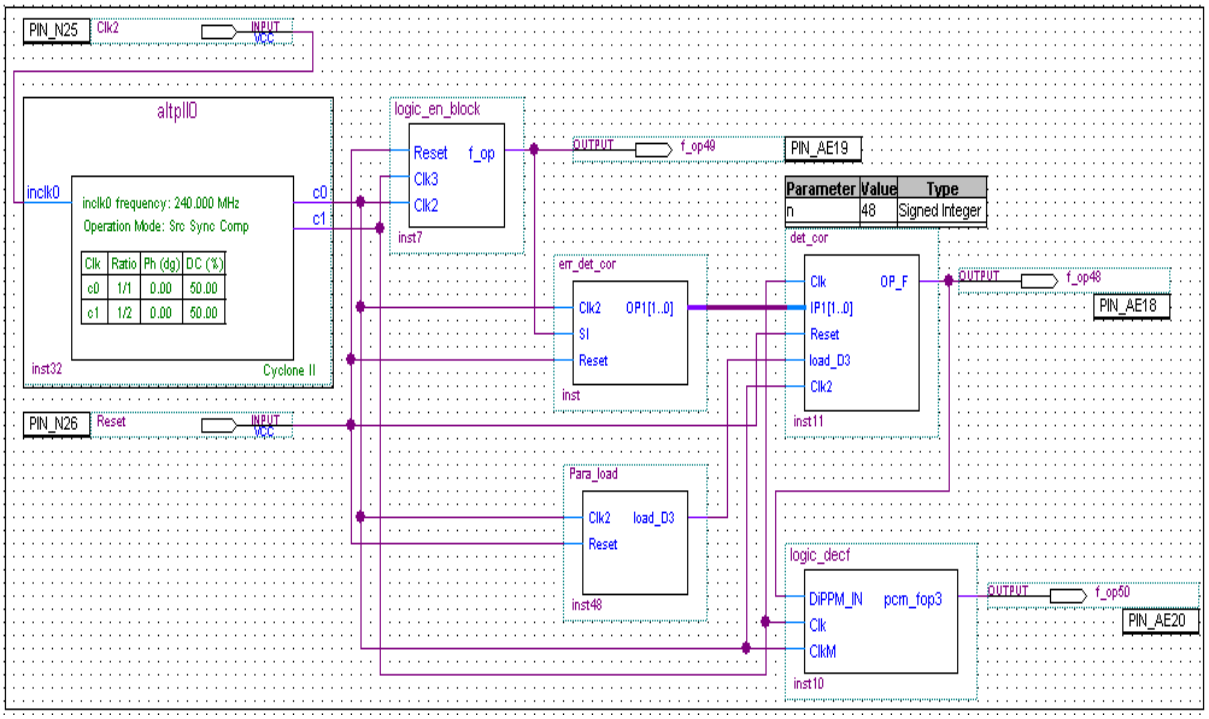


Fig. 4.1: Complete DuoPPM system after timing analysis (coder, decoder and MLSD error detector).

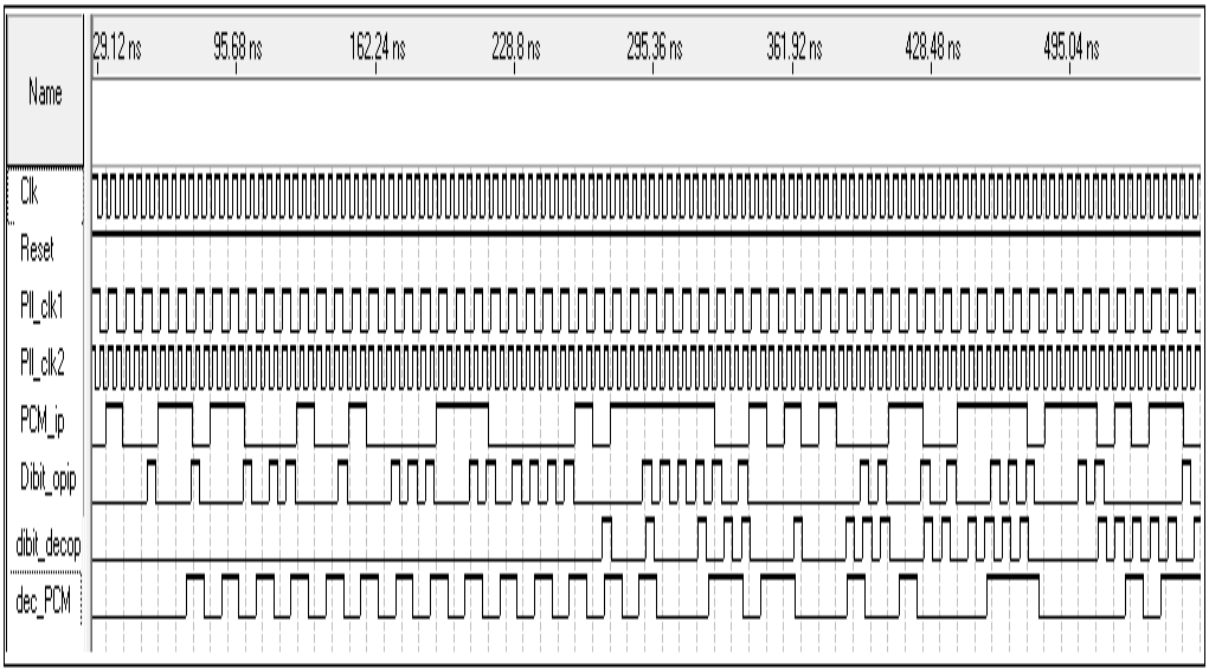


Fig. 4.2: Complete DuoPPM system timing analysis output waveform (coder and decoder).

Appendix 2

Appendix 2.1: DuoPPM Mathcad Simulation Model (Non-MLSD)

Complete Mathcad simulation file for the DuoPPM system (non-MLSD) is presented in this appendix. The key features are characterised by Gaussian shaped pulses, noise-whitening matched filter and central decision detection without the aid of MLSD.

DuoPPM using Gaussian shaped pulses, matched filter and central decision detection without MLSD

$i := 0, 1 .. 20$ $\quad n := 10$ Set up the scan limits

$v_i := v_{off} + \frac{i}{range}$

$x := 0..n$ This gives the row of the matrix

$y := 0..n$ This gives the column of the matrix

Preamplifier terms

$f_p := 10 \cdot 10^{9}$ Preamp bandwidth

$S_o := 50 \cdot 10^{-24}$ Preamp noise at input - double sided Philips CGY2110CU

$B := 1 \cdot 10^{9}$ Bit rate

$T_b := \frac{1}{B}$ PCM bit time

$T_s := \frac{T_b}{2}$ Slot time

$\eta q := 1.6 10^{-19}$ Quantum energy

$\lambda := 1.55 10^{-6}$ This is the wavelength of operation

$photon\_energy := \frac{6.63 10^{-34} \cdot 3 \cdot 10^{8}}{\lambda}$

Pulse shape terms

$$R_o := \frac{\eta q}{photon\_energy} \qquad R_o = 1.247$$

$$\alpha := \frac{0.1874 T_b}{f_n}$$

$$\alpha_n := \frac{0.1874 T_b}{f_n \cdot T_s}$$

$$\omega_p := 2\cdot\pi\cdot f_p \qquad \omega_{pn} := 2\cdot\pi\cdot f_p \cdot T_s$$

$$\tau_R := \alpha \qquad \tau_{Rn} := \frac{\alpha}{T_s}$$

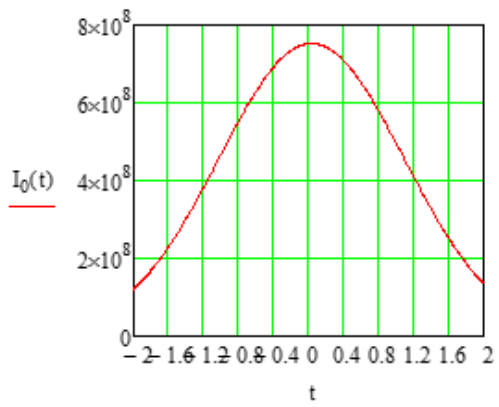
$$Pulse(t) := \frac{1}{\sqrt{2\cdot\pi}\cdot\alpha_n\cdot T_s}\cdot\exp\left(\frac{-t^2}{2\cdot\alpha_n{}^2}\right)$$

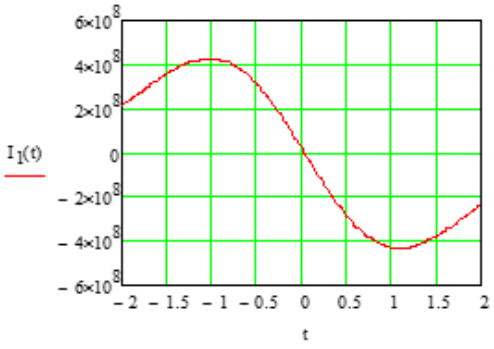
Pulse shape
Matched filter only

$$I_0(t) := \frac{\omega_{pn}}{2\cdot T_s}\cdot\exp\left[\left(\alpha_n\cdot\omega_{pn}\right)^2\right]\cdot\exp\left(-\omega_{pn}\cdot t\right)\cdot\operatorname{erfc}\left(\alpha_n\cdot\omega_{pn} - \frac{t}{2\cdot\alpha_n}\right)$$

$$I_1(t) := \frac{\omega_{pn}{}^2}{2\cdot T_s}\cdot\exp\left[\left(\alpha_n\cdot\omega_{pn}\right)^2\right]\cdot\exp\left(-\omega_{pn}\cdot t\right)\cdot\left[\frac{\exp\left[-\left(\alpha_n\cdot\omega_{pn} - \frac{t}{2\cdot\alpha_n}\right)^2\right]}{\alpha_n\cdot\omega_{pn}\cdot\sqrt{\pi}} - \operatorname{erfc}\left(\alpha_n\cdot\omega_{pn} - \frac{t}{2\cdot\alpha_n}\right)\right]$$

$t := -2, -1.99 .. 2$





$$noise := \frac{\omega_{pn}}{2 \cdot T_s} \cdot \exp\left[\left(\alpha_n \cdot \omega_{pn}\right)^2\right] \cdot \operatorname{erfc}\left(\alpha_n \cdot \omega_{pn}\right)$$

$$noise = 7.52 \times 10^{8}$$

Determine the peak pulse amplitude - ISOLATED PULSE

$t_{g1} := 0.00$

$$t_{poo} := \operatorname{root}\left(I_1\left(t_{g1}\right) \cdot T_s^{\,2}, t_{g1}\right)$$

This is the peak time for pulse in slot 0 as a function of x and y

$$t_{poo} = 9.009 \times 10^{-3}$$

$$t_{poo} = 9.009 \times 10^{-3}$$

Determine the decision time

$t_{g2} := -0.7$

$$t_{tho_i} := \operatorname{root}\left[\left(I_0\left(t_{g2}\right) - v_i \cdot I_0\left(t_{poo}\right)\right) \cdot T_s^{\,2}, t_{g2}\right]$$

$$t_{tho_7} = -0.437$$

$$v_{th_i} := I_0\left(t_{tho_i}\right)$$

This is the decision level voltage

Modify peak of single pulse

$$t_{poo} = 9.009 \times 10^{-3}$$

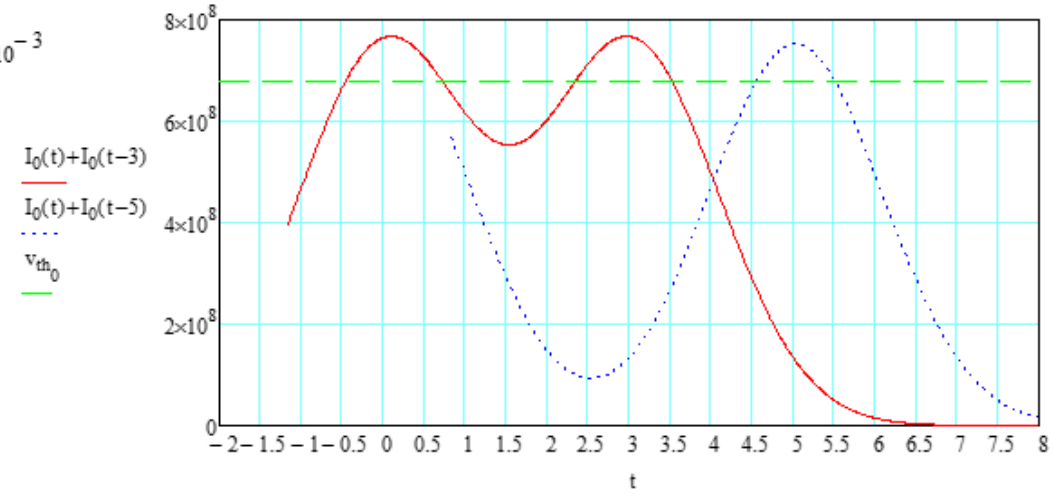
$$t_p := \text{if}\left[\left(t_{poo} - t_{tho_0} + 0.5 \geq 1\right), \left(t_{tho_0} + 0.5\right), t_{poo}\right]$$

$$t_p = 9.009 \times 10^{-3}$$

$t_{po} := t_p$

$$t_{po} = 9.009 \times 10^{-3}$$

$t := -2, -1.99 .. 8$



Error sources

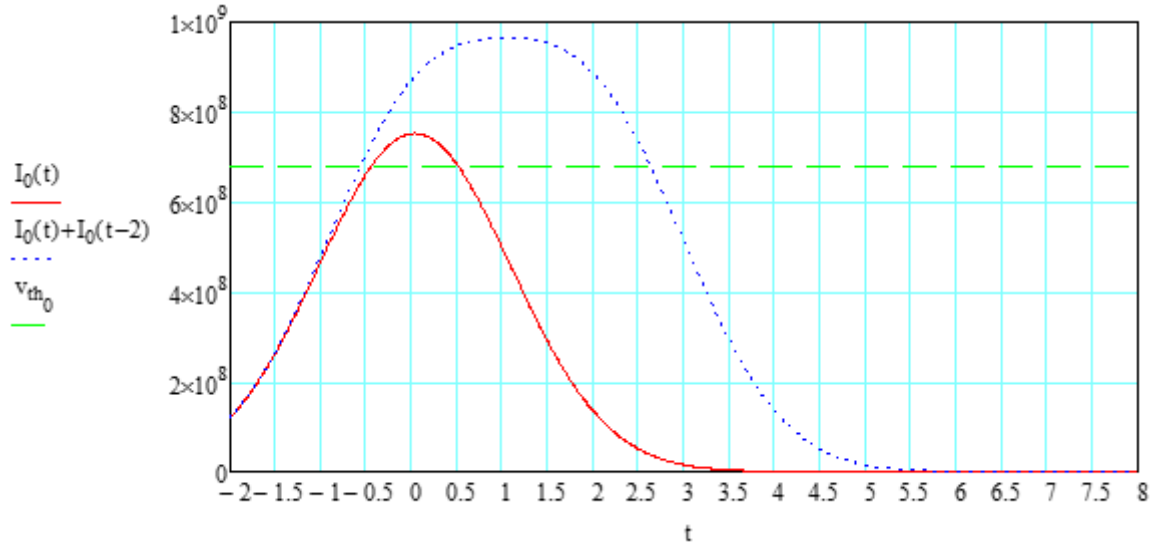
Erasure

Erasure - Erasure of middle symbol in 0 xC 1/0 yC 1/0

$$Err(x,y) := \left|\frac{x-y}{2}\right|$$ Clearly x=0 and y=0 gives 0 errors

x=0 and y>=1 is a special case for ISI Find the amplitude of the zero pulse in 00yCI

$t := -2, -1.99..8$



$$Q_i := \eta q \cdot \frac{\left(I_0(t_{po}) + I_0(t_{po}-2) - v_{th_i}\right)}{\sqrt{S_o \cdot noise}}$$ $Q_7 = 1.584 \times 10^{-4}$

$$Errors := \left[\sum_{y=0}^{n-1}\left[\frac{1}{4}\cdot\left(\frac{1}{2}\right)^0\cdot\left(\frac{1}{2}\right)\cdot\left(\frac{1}{2}\right)^y\cdot\frac{1}{2}\cdot Err(0,y)\right]\ldots + \frac{1}{4}\cdot\left(\frac{1}{2}\right)^0\cdot\left(\frac{1}{2}\right)\cdot\left(\frac{1}{2}\right)^n\cdot 1\cdot Err(0,n)\right]$$

$Errors = 0.062$

$$erfc\left(\frac{b\cdot Q_5}{\sqrt{2}}\right) = 0.425$$

$$P_{er00yC}(b,i) := Errors\cdot\left(\frac{1}{2}\cdot erfc\left(\frac{b\cdot Q_i}{\sqrt{2}}\right)\right)$$ $P_{er00yC}(b,0) = 0.013$

Erasure of middle symbol in 0 xC 1/0 yC 1/0 with x=1 to n & y=0 to n

$$Q_i := \eta q \cdot \frac{I_0(t_{po}) - \left(v_i \cdot I_0(t_{po})\right)}{\sqrt{S_o \cdot noise}}$$

$$Errors := \left[\sum_{x=1}^{n-1}\left[\sum_{y=0}^{n-1}\left[\frac{1}{4}\cdot\left(\frac{1}{2}\right)^x \cdot\frac{1}{2}\cdot\left(\frac{1}{2}\right)^y \cdot\frac{1}{2}\cdot Err(x,y)\right] + \frac{1}{4}\cdot\left(\frac{1}{2}\right)^x \cdot\frac{1}{2}\cdot\left(\frac{1}{2}\right)^n \cdot 1\cdot Err(x,n)\right]\ldots\right.$$
$$\left.+\left[\sum_{y=0}^{n-1}\left[\frac{1}{4}\cdot\left(\frac{1}{2}\right)^n \cdot 1\cdot\left(\frac{1}{2}\right)^y \cdot\frac{1}{2}\cdot Err(n,y)\right] + \frac{1}{4}\cdot\left(\frac{1}{2}\right)^n \cdot 1\cdot\left(\frac{1}{2}\right)^n \cdot 1\cdot Err(n,n)\right]\right]$$

$Errors = 0.104$

$$P_{er0xSyS}(b,i) := Errors\cdot\left(\frac{1}{2}\cdot erfc\left(\frac{b\cdot Q_i}{\sqrt{2}}\right)\right) \qquad P_{er0xSyS}(b,0) = 0.039$$

$$P_{er0}(b,i) := P_{er00yC}(b,i) + P_{er0xSyS}(b,i) \qquad P_{er0}(b,0) = 0.052$$

Erasure of middle symbol in 1 xC 0 yC 1 for both instances are identical to what has already been calculated

$$P_{ee1}(b,i) := 2\cdot P_{er0}(b,i) \qquad P_{ee1}(b,0) = 0.105$$

False Alarm

False 0 following a 1 at some time

k = ODD combinations = k+1
K = EVEN combinations = x-k+1

Errors = (combs-1)/2

$$odd(k) := \frac{k}{2} - trunc\left(\frac{k}{2}\right) = 0.5$$

$$Errodd(x,y,k) := \frac{k+1-1}{2}$$

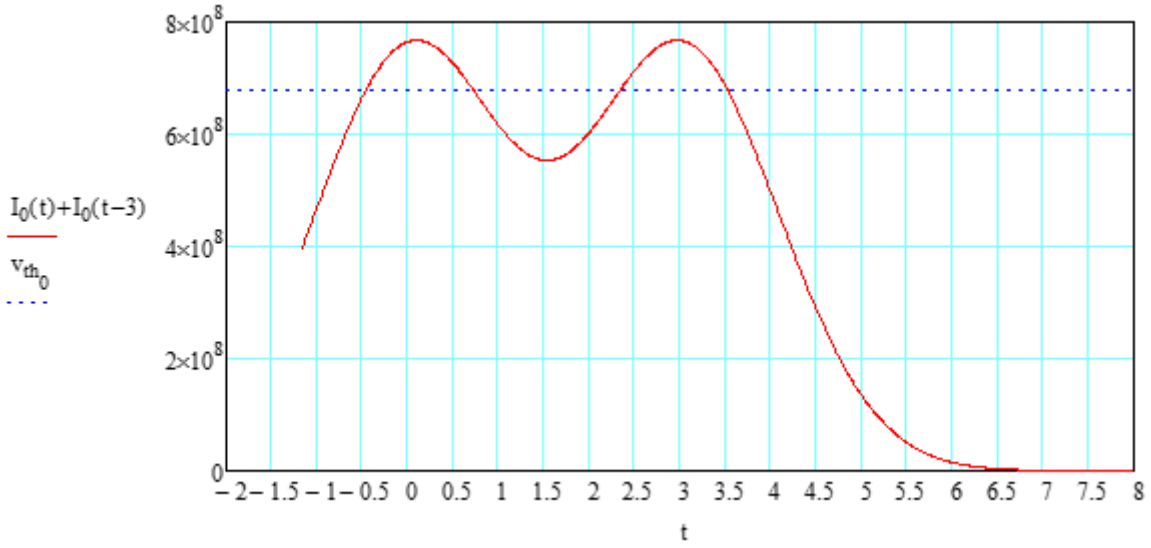
$$even(k) := \frac{k}{2} - trunc\left(\frac{k}{2}\right) = 0$$

$$Erreven(x,y,k) := \frac{x-k+1-1}{2}$$

$$Err(x,y,k) := Erreven(x,y,k)\cdot even(k) + Errodd(x,y,k)\cdot odd(k)$$

0 yC 1 xC 0: x=1, k=1 condition is special - ISI from pulse 1 spilling into the slot 0 of C

$t := -2, -1.99 .. 8$



$$Q_i := \eta q \cdot \frac{v_{th_i} - \left(I_0(1 + t_{po}) + I_0(1 + t_{po} - 3)\right)}{\sqrt{S_o \cdot noise}}$$

$$Errors := \left[\sum_{y=1}^{n-1} \left[\left(\frac{1}{2}\right)^{1+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(1, y, 1) \right] \ldots + \left(\frac{1}{2}\right)^{1+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(1, n, 1) \right]$$

$Errors = 0.016$

$$P_{false0\,in\,1C0}(b, i) := Errors \cdot \left(\frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}} \right) \right)$$

$P_{false0\,in\,1C0}(b, 0) = 6.215 \times 10^{-3}$

x=2..n, k=1 condition is special - ISI from pulse 1 spilling into the slot 0 of C

$$Errors := \left[\sum_{x=2}^{n-1} \left[\sum_{y=1}^{n-1} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(x, y, 1) \right] + \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(x, n, 1) \right] \right] \ldots + \sum_{y=1}^{n-1} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(n, y, 1) \right] + \left[\left(\frac{1}{2}\right)^{n} \cdot \left(\frac{1}{4}\right) \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(n, n, 1) \right] \right]$$

$Errors = 0.016$

$$Q_i := \eta q \cdot \frac{v_{th_i} - \left(I_0\left(1 + t_{po}\right)\right)}{\sqrt{S_o \cdot noise}}$$

$$P_{false0in1xC0}(b, i) := Errors \cdot \left(\frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}}\right)\right)$$

$$P_{false0in1xC0}(b, 0) = 3.482 \times 10^{-3}$$

x=2..n, k=2..x condition

$$Errors := \left[\sum_{y=1}^{n-1}\left[\sum_{x=2}^{n-1}\sum_{k=2}^{x}\left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(x,y,k)\right] + \sum_{k=2}^{n}\left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(n,y,k)\right]\right] \ldots\right.$$
$$\left. + \sum_{x=2}^{n-1}\sum_{k=2}^{x}\left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(x,n,k)\right] + \sum_{k=2}^{n}\left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(n,n,k)\right]\right]$$

$Errors = 0.058$

$$Q_i := \eta q \cdot \frac{v_{th_i}}{\sqrt{S_o \cdot noise}}$$

$$P_{false0post1}(b, i) := Errors \cdot \frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}}\right)$$

$$P_{false0post1}(b, 0) = 1.521 \times 10^{-4}$$

$$P_{ef0post1}(b, i) := P_{false0in1C0}(b, i) + P_{false0in1xC0}(b, i) + P_{false0post1}(b, i)$$

$$P_{ef0post1}(b, 0) = 9.85 \times 10^{-3}$$

False 1 following a 0 at some time

k = ODD combinations = k+1
K = EVEN combinations = y-k+1

Errors = (combs-1)/2 in x+y+4 PCM bits

$$odd(k) := \frac{k}{2} - trunc\left(\frac{k}{2}\right) = 0.5$$

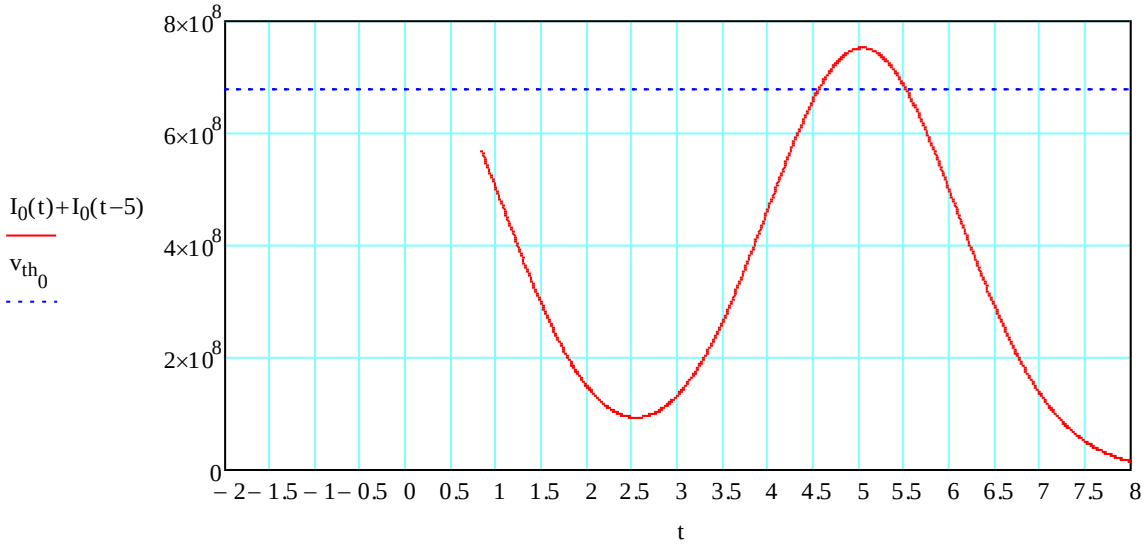
$$Errodd(x, y, k) := \frac{k + 1 - 1}{2}$$

$$even(k) := \frac{k}{2} - trunc\left(\frac{k}{2}\right) = 0$$

$$Erreven(x,y,k) := \frac{y - k + 1 - 1}{2}$$

$$Err(x,y,k) := Erreven(x,y,k)\cdot even(k) + Errodd(x,y,k)\cdot odd(k)$$

$t := -2, -1.99 .. 8$



0C1: y=1 - ISI from pulse 0 spilling into the slot 1 of the same frame, no violation occurs as due to central decision detection the pulse will be first detected in slot 0 (as it is still present in slot 0) and decoder will stop once a pulse has been received thus no effect of the spilled pulse in slot 1

However, y=1, k=1 condition is special - noise can cause a threshold crossing event in C

$$Errors := \left[\sum_{x=1}^{n-1}\left[\left(\frac{1}{2}\right)^{x+1}\cdot\frac{1}{4}\cdot\left(\frac{1}{2}\right)^{1+1}\cdot Err(x,1,1)\right]\ldots + \left(\frac{1}{2}\right)^{n}\cdot\frac{1}{4}\cdot\left(\frac{1}{2}\right)^{1+1}\cdot Err(n,1,1)\right]$$

$$Errors = 0.016$$

$$Q_i := \eta q\cdot\frac{v_{th_i} - \left(I_0(3 + t_{po}) + I_0(3 + t_{po} - 5)\right)}{\sqrt{S_o\cdot noise}}$$

$$P_{false1in0C1}(b,i) := Errors\cdot\left(\frac{1}{2}\cdot erfc\left(\frac{b\cdot Q_i}{\sqrt{2}}\right)\right) \qquad P_{false1in0C1}(b,0) = 2.017\times 10^{-4}$$

0yC1: y=2..n - ISI from pulse 0 spilling into the slot 1 of the same frame will be detected the same way mentioned above thus no effect of the spilled pulse in slot 1

However, y=2..n, k=1 condition is special - noise can cause a threshold crossing event in the first C immediately after 0

$$Errors := \left[\sum_{x=1}^{n-1} \left[\sum_{y=2}^{n-1} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(x,y,1) \right] + \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(x,n,1) \right] \right] \ldots \right.$$
$$\left. + \sum_{y=2}^{n-1} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(n,y,1) \right] + \left[\left(\frac{1}{2}\right)^{n} \cdot \left(\frac{1}{4}\right) \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(n,n,1) \right] \right]$$

$Errors = 0.016$

$$Q_i := \eta q \cdot \frac{v_{th_i} - \left(I_0\left(3 + t_{po}\right)\right)}{\sqrt{S_o \cdot noise}}$$

$$P_{false1in0yC1}(b,i) := Errors \cdot \left(\frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}} \right) \right)$$

$P_{false1in0yC1}(b,0) = 4.911 \times 10^{-5}$

y=2..n, k=2..x condition

$$Errors := \left[\sum_{y=2}^{n-1} \left[\sum_{x=2}^{n-1} \sum_{k=2}^{x} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(x,y,k) \right] + \sum_{k=2}^{n} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(n,y,k) \right] \right] \ldots \right.$$
$$\left. + \sum_{x=2}^{n-1} \sum_{k=2}^{x} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(x,n,k) \right] + \sum_{k=2}^{n} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(n,n,k) \right] \right]$$

$Errors = 0.022$

$$Q_i := \eta q \cdot \frac{v_{th_i}}{\sqrt{S_o \cdot noise}}$$

$$P_{false1post0}(b,i) := Errors \cdot \frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}} \right)$$

$P_{false1post0}(b,0) = 5.849 \times 10^{-5}$

$P_{ef1post0}(b,i) := P_{false1in0C1}(b,i) + P_{false1in0yC1}(b,i) + P_{false1post0}(b,i)$

$P_{ef1post0}(b,0) = 3.093 \times 10^{-4}$

$P_{efdiff}(b,i) := P_{ef0post1}(b,i) + P_{ef1post0}(b,i)$

$P_{efdiff}(b,0) = 0.01$

False 0 following a 0 at some time

k = ODD combinations = x-k+1
K = EVEN combinations = k+1

Errors = (combs-1)/2

$$odd(k) := \frac{k}{2} - trunc\left(\frac{k}{2}\right) = 0.5$$

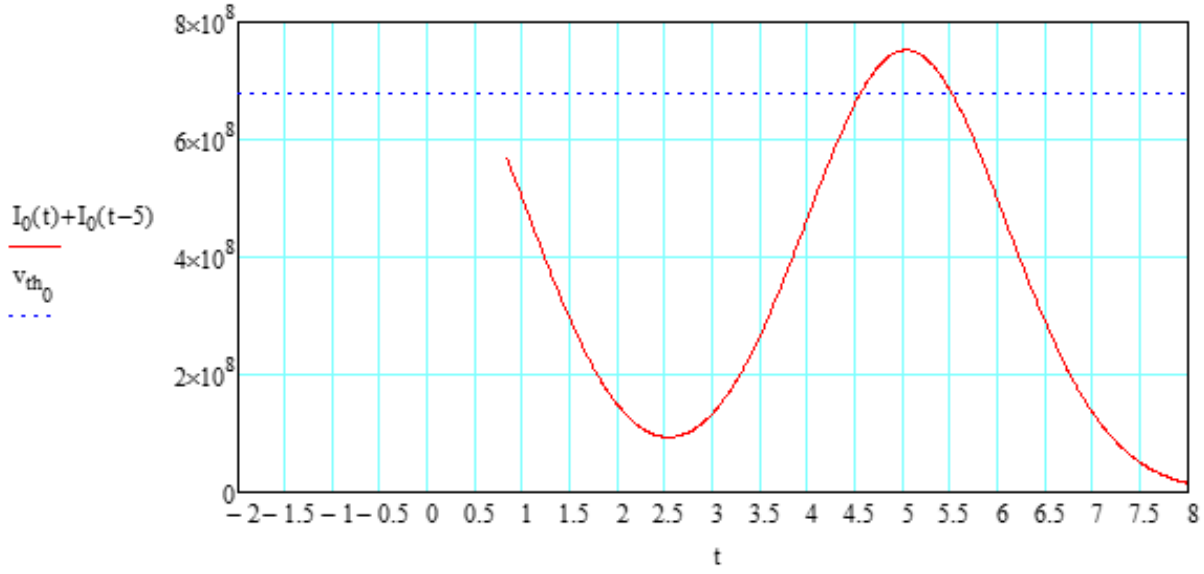
$$Errodd(x,y,k) := \frac{x-k+1-1}{2}$$

$$even(k) := \frac{k}{2} - trunc\left(\frac{k}{2}\right) = 0$$

$$Erreven(x,y,k) := \frac{k+1-1}{2}$$

$$Err(x,y,k) := Erreven(x,y,k)\cdot even(k) + Errodd(x,y,k)\cdot odd(k)$$

$t := -2, -1.99 .. 8$



00 yC 1: y=1, k=1 - if ther is false alarm of 0 in C slot following 0 (1xC001) then there will be zero errors as there's only one possible correct combination of the aforementioned error which will be corrected by MLSD.

1 xC 0 yC 1: if y=2..n then K>=2 thus this condition can be covered by the following condition of y=2..n, k=2..x

y=2..n, k=2..x condition

$$\text{Errors} := \left[\sum_{y=2}^{n-1} \left[\sum_{x=2}^{n-1} \sum_{k=2}^{x} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot \text{Err}(x,y,k) \right] + \sum_{k=2}^{n} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot \text{Err}(n,y,k) \right] \right] \ldots \right.$$
$$\left. + \sum_{x=2}^{n-1} \sum_{k=2}^{x} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot \text{Err}(x,n,k) \right] + \sum_{k=2}^{n} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot \text{Err}(n,n,k) \right] \right]$$

$\text{Errors} = 0.033$

$$Q_i := \eta q \cdot \frac{v_{th_i}}{\sqrt{S_o \cdot \text{noise}}}$$

$$P_{false0post0}(b,i) := \text{Errors} \cdot \frac{1}{2} \cdot \text{erfc}\left(\frac{b \cdot Q_i}{\sqrt{2}}\right)$$

$P_{false0post0}(b,0) = 8.547 \times 10^{-5}$

$P_{ef0post0}(b,i) := P_{false0post0}(b,i)$

$P_{ef0post0}(b,0) = 8.547 \times 10^{-5}$

False 1 following a 1 at some time

k = ODD combinations = y-k+1
K = EVEN combinations = k+1

Errors = (combs-1)/2 in x+y+4 PCM bits

$$\text{odd}(k) := \frac{k}{2} - \text{trunc}\left(\frac{k}{2}\right) = 0.5$$

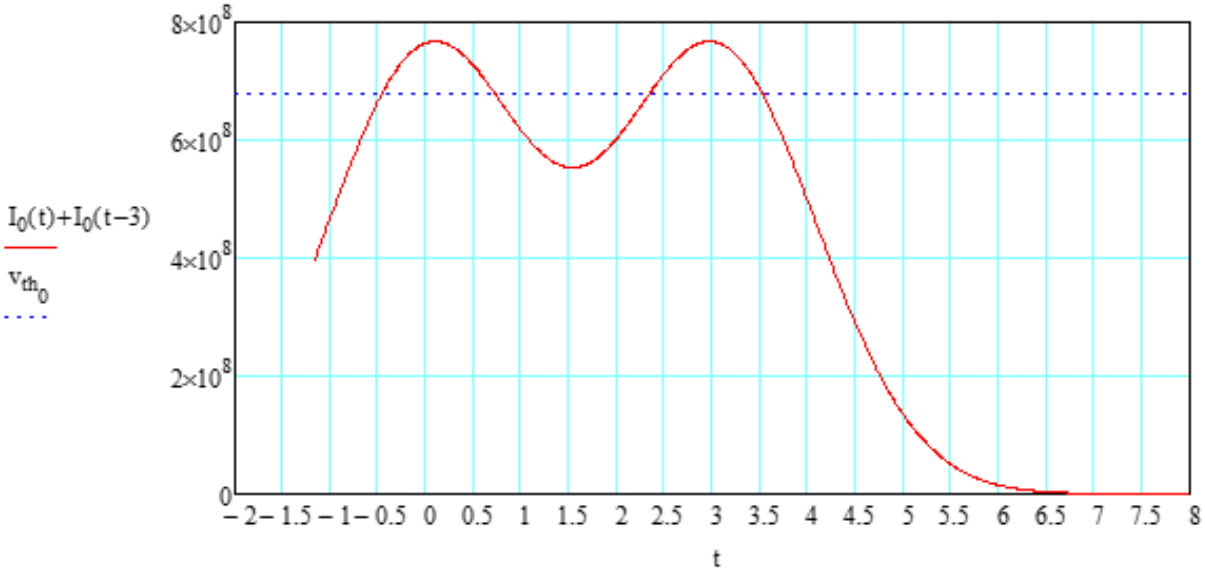
$$\text{Errodd}(x,y,k) := \frac{y-k+1-1}{2}$$

$$\text{even}(k) := \frac{k}{2} - \text{trunc}\left(\frac{k}{2}\right) = 0$$

$$\text{Erreven}(x,y,k) := \frac{k+1-1}{2}$$

$$\text{Err}(x,y,k) := \text{Erreven}(x,y,k) \cdot \text{even}(k) + \text{Errodd}(x,y,k) \cdot \text{odd}(k)$$

$t := -2, -1.99 .. 8$



x=2..n, k=2..x condition

1C0: x=1, k=1 - in this condition ISI from 1 pulse spilling into the C frame - this will be detected as a false 0 and will generate zero errors as there's only one possible correct combination of the aforementioned error which will be corrected by MLSD.

if x=2..n then K>=2 thus this condition can be covered by the following condition of x=2..n, k=2..x

$$\text{Errors} := \left[\sum_{y=1}^{n-1} \left[\sum_{x=2}^{n-1} \sum_{k=2}^{x} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot \text{Err}(x,y,k) \right] + \sum_{k=2}^{n} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot \text{Err}(n,y,k) \right] \right] \ldots \right.$$
$$\left. + \sum_{x=2}^{n-1} \sum_{k=2}^{x} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot \text{Err}(x,n,k) \right] + \sum_{k=2}^{n} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot \text{Err}(n,n,k) \right] \right]$$

$$Q_i := \eta q \cdot \frac{v_{th_i}}{\sqrt{S_o \cdot \text{noise}}}$$

$Errors = 0.038$

$$P_{false1post1}(b,i) := Errors \cdot \frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}}\right)$$

$P_{false1post1}(b,0) = 1.001 \times 10^{-4}$

$P_{ef1post1}(b,i) := P_{false1post1}(b,i)$

$P_{ef1post1}(b,0) = 1.001 \times 10^{-4}$

$P_{efsame}(b,i) := P_{ef0post0}(b,i) + P_{ef1post1}(b,i)$

$P_{efsame}(b,0) = 1.855 \times 10^{-4}$

$P_{ef}(b,i) := P_{efdiff}(b,i) + P_{efsame}(b,i)$

$P_{ef}(b,i) =$

0.01
0.01
0.01
0.01
0.01
0.01
0.01
0.01
0.01
$9.997 \cdot 10^{-3}$
$9.959 \cdot 10^{-3}$
$9.921 \cdot 10^{-3}$
$9.883 \cdot 10^{-3}$
$9.845 \cdot 10^{-3}$
$9.807 \cdot 10^{-3}$
...

$P_{eer}(b,i) =$

0.105
0.105
0.105
0.106
0.106
0.106
0.107
0.107
0.107
0.108
0.108
0.109
0.109
0.109
0.11
...

$P_{eb}(b,i) := P_{eer}(b,i) + P_{ef}(b,i)$

$pc(b,i) := \left(\log\left(P_{eb}(b,i) \cdot 10^3\right) + 6\right)$ Set for 1 in 10^9 errors

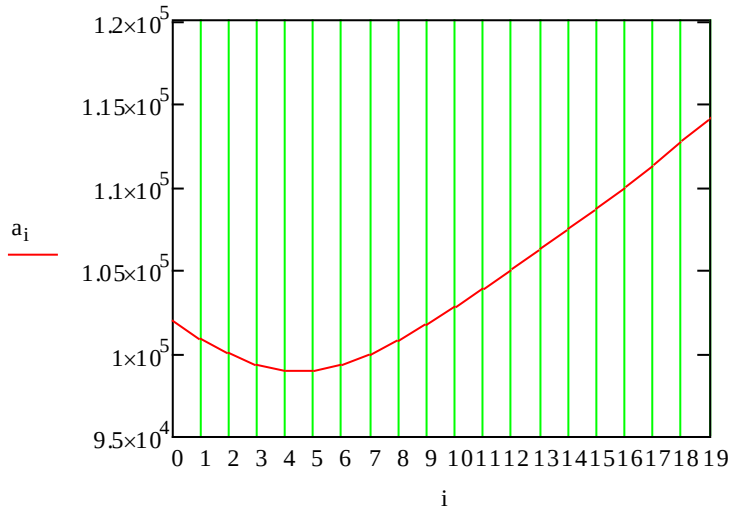
$a_i := root(pc(b,i), b)$ Find the root to give 1 in 10^9

minimum := min(a)

minimum = 9.892 × 10^4

a_i =

$1.02 \cdot 10^5$
$1.009 \cdot 10^5$
$9.999 \cdot 10^4$
$9.93 \cdot 10^4$
$9.893 \cdot 10^4$
$9.892 \cdot 10^4$
$9.927 \cdot 10^4$
$9.99 \cdot 10^4$
$1.007 \cdot 10^5$
$1.017 \cdot 10^5$
$1.028 \cdot 10^5$
$1.039 \cdot 10^5$
$1.051 \cdot 10^5$
$1.063 \cdot 10^5$
$1.075 \cdot 10^5$
...



$b \equiv 5 \cdot 10^3$

$v_{off} \equiv 0.9$ range ≡ 100

$f_n \equiv 0.5$

b := minimum

$$dBm := 10 \cdot \log\left[b \cdot \frac{photon\_energy}{10^{-3}} \cdot \left[\frac{n+1}{2 \cdot (2) \cdot n}\right] \cdot B\right]$$

dBm = −24.571

$$dBm_{guardslots} := 10 \cdot \log\left[b \cdot \frac{photon\_energy}{10^{-3}} \cdot \left[\frac{n+1}{4 \cdot (2) \cdot n}\right] \cdot B\right]$$

$dBm_{guardslots}$ = −27.581

i := 7

v_i = 0.907

minimum 10^{-3} = 98.924

$P_{eef}(b, i) \cdot 10^9 = 1.176$ $P_{ef}(b, i) \cdot 10^9 = 0.216$

$P_{er0}(b, i) \cdot 10^{10} = 5.882$ $\left(P_{ef0post1}(b, i) + P_{ef0post0}(b, i)\right) \cdot 10^{10} = 2.156$

$\left(P_{ef1post1}(b, i) + P_{ef1post0}(b, i)\right) \cdot 10^{10} = 0$

$$PCM_{155M} := 10 \cdot \log\left(\frac{6}{1 \cdot 10^{-3}} \cdot \sqrt{2 \cdot 6.8 \cdot 10^{-24} \cdot 0.564155 \cdot 10^{6}} \right)$$

SA5212A - Phillips
140MHz b/w
155Mbit/s data

$$PCM_{155M} = -36.843$$

$$PCM_{1G} := 10 \cdot \log\left(\frac{6}{1 \cdot 10^{-3}} \cdot \sqrt{2 \cdot 16 \cdot 10^{-24} \cdot 0.5641 \cdot 10^{9}} \right)$$

TZA 3043 - Phillips
1.2GHz b/w
1Gbit/s data

$$PCM_{1G} = -30.936$$

Appendix 2.2

DuoPPM Non-MLSD Mathcad Results

DuoPPM, dicode PPM (DiPPM), digital PPM (DPPM) and optimised PPM (opt) results.

$$freq := \begin{pmatrix} 100 \\ 90 \\ 80 \\ 70 \\ 60 \\ 50 \\ 40 \\ 30 \\ 20 \\ 10 \\ 9 \\ 8 \\ 7 \\ 6 \\ 5 \\ 4 \\ 3 \\ 2 \\ 1.5 \\ 1 \end{pmatrix} \quad DuoPPM155 := \begin{pmatrix} -50.468 \\ -50.403 \\ -50.215 \\ -50.203 \\ -49.975 \\ -49.873 \\ -49.611 \\ -49.228 \\ -48.602 \\ -47.327 \\ -47.116 \\ -46.876 \\ -46.6 \\ -46.277 \\ -45.89 \\ -45.412 \\ -44.791 \\ -43.911 \\ -43.264 \\ -41.502 \end{pmatrix} \quad DiPPM155 := \begin{pmatrix} -50.067 \\ -49.993 \\ -49.904 \\ -49.793 \\ -49.653 \\ -49.469 \\ -49.216 \\ -48.846 \\ -48.245 \\ -47.005 \\ -46.799 \\ -46.564 \\ -46.293 \\ -45.975 \\ -45.599 \\ -45.136 \\ -44.533 \\ -43.475 \\ -42.327 \\ -39.753 \end{pmatrix} \quad DPPM155 := \begin{pmatrix} -50.248 \\ -50.174 \\ -50.085 \\ -49.975 \\ -49.836 \\ -49.653 \\ -49.4 \\ -49.029 \\ -48.42 \\ -47.017 \\ -46.437 \\ -45.744 \\ -44.931 \\ -43.981 \\ -42.846 \\ -41.442 \\ -39.615 \\ -37.014 \\ -35.035 \\ -32.44 \end{pmatrix} \quad opt155 := \begin{pmatrix} -50.248 \\ -50.174 \\ -50.085 \\ -49.975 \\ -49.836 \\ -49.653 \\ -49.4 \\ -49.029 \\ -48.419 \\ -47.017 \\ -46.437 \\ -46.088 \\ -45.812 \\ -45.456 \\ -44.693 \\ -43.865 \\ -42.678 \\ -41.107 \\ -39.533 \\ -37.106 \end{pmatrix}$$

$$opt_{155M} := \begin{pmatrix} 20 & -48.419 & 7 & 0.8 \\ 10 & -47.017 & 7 & 0.8 \\ 9 & -46.437 & 7 & 0.8 \\ 8 & -46.088 & 6 & 0.7 \\ 7 & -45.812 & 6 & 0.8 \\ 6 & -45.456 & 6 & 0.8 \\ 5 & -44.493 & 6 & 0.8 \\ 4 & -43.865 & 5 & 0.8 \\ 3 & -42.678 & 5 & 0.8 \\ 2 & -41.107 & 4 & 0.8 \\ 1.5 & -39.533 & 3 & 0.8 \\ 1 & -37.106 & 3 & 0.8 \end{pmatrix}$$

The above results are for 155 Mbps data rate.

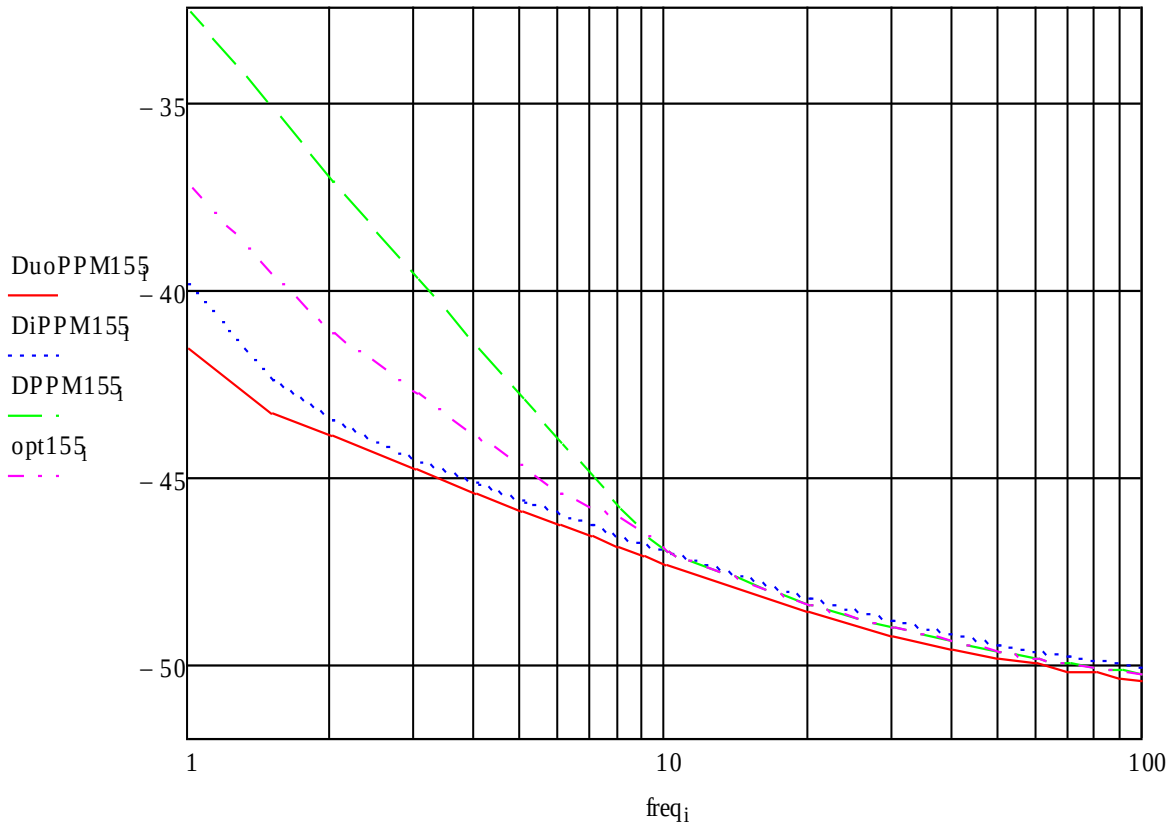


Fig. A2 - 2.1: Comparison of DuoPPM, dicode PPM (DiPPM), digital PPM (DPPM) and optimised PPM (opt) sensitivities at 155 Mbps data rate.

$$DuoPPM1G := \begin{pmatrix} -44.367 \\ -44.299 \\ -44.103 \\ -44.005 \\ -43.879 \\ -43.603 \\ -43.306 \\ -42.878 \\ -42.192 \\ -40.842 \\ -40.623 \\ -40.377 \\ -40.094 \\ -39.766 \\ -39.374 \\ -38.893 \\ -38.27 \\ -37.389 \\ -36.743 \\ -34.987 \end{pmatrix} \quad DiPPM1G := \begin{pmatrix} -43.898 \\ -43.811 \\ -43.705 \\ -43.575 \\ -43.412 \\ -43.2 \\ -42.911 \\ -42.495 \\ -41.834 \\ -40.52 \\ -40.306 \\ -40.064 \\ -39.787 \\ -39.464 \\ -39.084 \\ -38.617 \\ -38.011 \\ -37.058 \\ -35.831 \\ -33.252 \end{pmatrix} \quad DPPM1G := \begin{pmatrix} -44.079 \\ -43.991 \\ -43.886 \\ -43.757 \\ -43.595 \\ -43.383 \\ -43.096 \\ -42.678 \\ -42.009 \\ -40.589 \\ -40.016 \\ -39.318 \\ -38.493 \\ -37.529 \\ -36.38 \\ -34.962 \\ -33.12 \\ -30.382 \\ -28.543 \\ -25.939 \end{pmatrix} \quad opt1G := \begin{pmatrix} -44.079 \\ -43.991 \\ -43.886 \\ -43.757 \\ -43.595 \\ -43.383 \\ -43.096 \\ -42.678 \\ -42.009 \\ -40.589 \\ -40.016 \\ -39.583 \\ -39.306 \\ -38.959 \\ -38.021 \\ -37.346 \\ -36.18 \\ -34.5 \\ -33.019 \\ -30.606 \end{pmatrix}$$

$$opt_{1G} := \begin{pmatrix} 20 & -42.009 & 7 & 0.8 \\ 10 & -40.589 & 7 & 0.8 \\ 9 & -40.016 & 7 & 0.8 \\ 8 & -39.583 & 6 & 0.7 \\ 7 & -39.306 & 6 & 0.8 \\ 6 & -38.959 & 6 & 0.8 \\ 5 & -38.021 & 6 & 0.8 \\ 4 & -37.346 & 5 & 0.8 \\ 3 & -36.18 & 5 & 0.8 \\ 2 & -34.5 & 4 & 0.8 \\ 1.5 & -33.019 & 3 & 0.8 \\ 1 & -30.606 & 3 & 0.8 \end{pmatrix}$$

The above results are for 1 Gbps data rate.

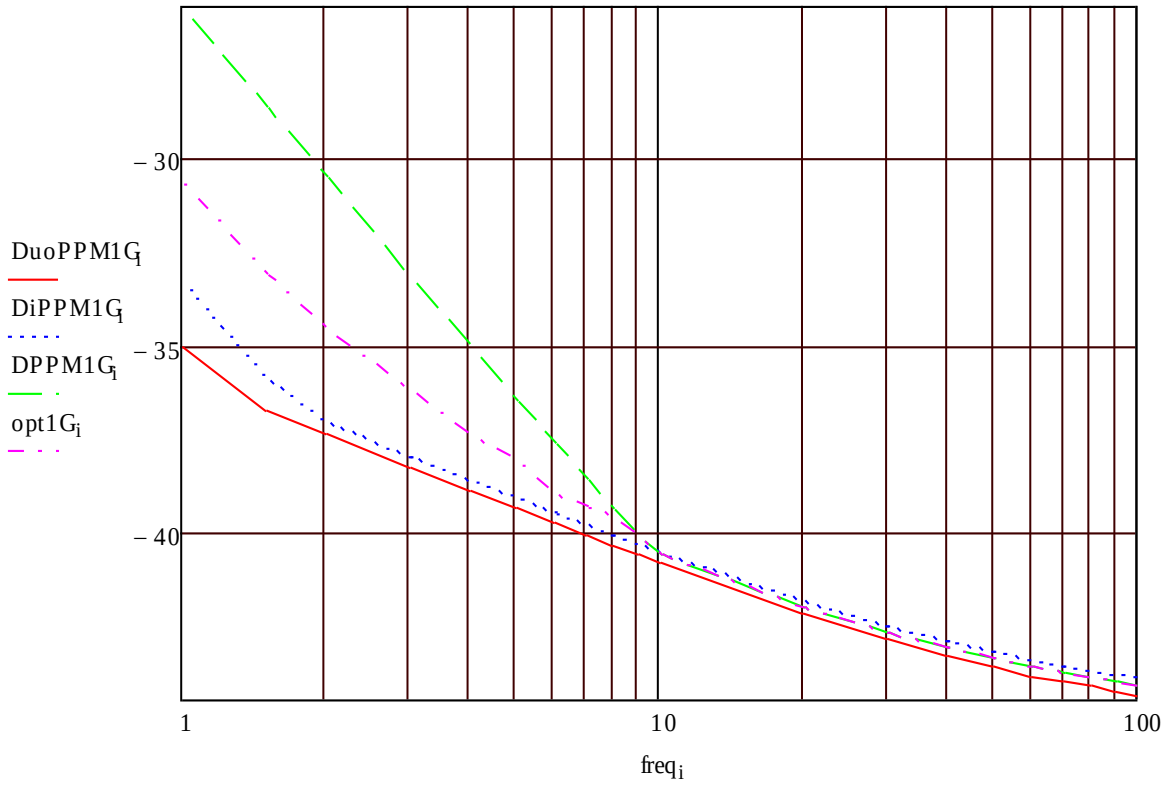


Fig. A2 - 2.2: Comparison of DuoPPM, dicode PPM (DiPPM), digital PPM (DPPM) and optimised PPM (opt) sensitivities at 1 Gbps data rate.

Appendix 2.3

DuoPPM MLSD Simulation Model

Complete Mathcad simulation file for the DuoPPM system MLSD is presented in this appendix. The key features are characterised by Gaussian shaped pulses, noise-whitening matched filter and central decision detection with the aid of MLSD.

DuoPPM Standard MLSD Central Decision Detection: Matched Filter and APD FN=0.43

$i := 0,1..20$ $n := 10$ Set up the scan limits

$v_i := v_{off} + \frac{i}{range}$

$x := 0..n$ This gives the row of the matrix

$y := 0..n$ This gives the column of the matrix

Preamplifier terms

$f_p := 10 \cdot 10^9$ Preamp bandwidth

$S_o := 50 \cdot 10^{-24}$ Preamp noise at input - double sided

$B := 1 \cdot 10^9$ Bit rate

$T_b := \frac{1}{B}$ PCM bit time

$T_s := \frac{T_b}{2}$ Slot time

$\eta q := 1.6\,10^{-19}$ Quantum energy

$\lambda := 1.55\,10^{-6}$ This is the wavelength of operation

$photon\_energy := \frac{6.63\,10^{-34} \cdot 3 \cdot 10^8}{\lambda}$

Pulse shape terms

$$R_o := \frac{\eta q}{photon\_energy} \qquad R_o = 1.247$$

$$\alpha := \frac{0.1874 T_b}{f_n}$$

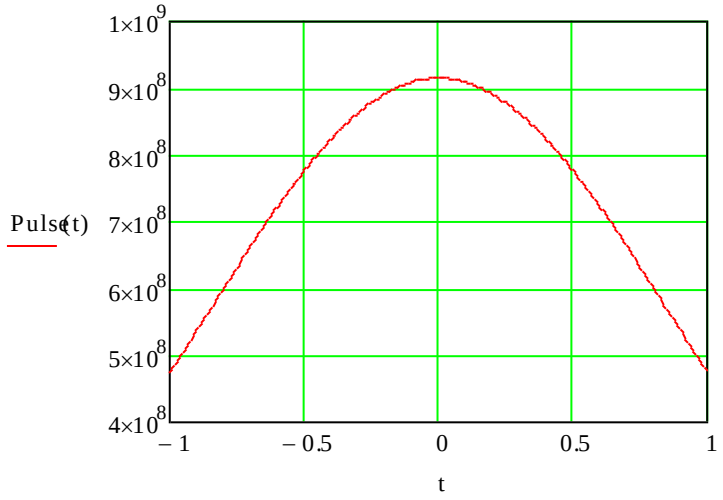
$$\alpha_n := \frac{0.1874 T_b}{f_n \cdot T_s}$$

$$\omega_c := 2 \cdot \pi \cdot f_p \qquad \omega_{cn} := 2 \cdot \pi \cdot f_p \cdot T_s$$

$$\tau_R := \alpha \qquad \tau_{Rn} := \frac{\alpha}{T_s}$$

$$Pulse(t) := \frac{1}{\sqrt{2 \cdot \pi} \cdot \alpha_n \cdot T_s} \cdot \exp\left(\frac{-t^2}{2 \cdot \alpha_n^{\,2}}\right)$$

$t := -1, -0.99 .. 1$



Pulse shape
Matched filter only

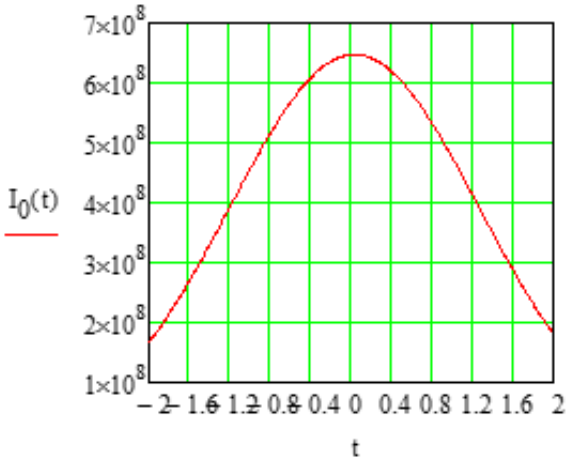
$$I_0(t) := \frac{\omega_{cn}}{2 \cdot T_s} \cdot \exp\left[\left(\alpha_n \cdot \omega_{cn}\right)^2\right] \cdot \exp\left(-\omega_{cn} \cdot t\right) \cdot \operatorname{erfc}\left(\alpha_n \cdot \omega_{cn} - \frac{t}{2 \cdot \alpha_n}\right)$$

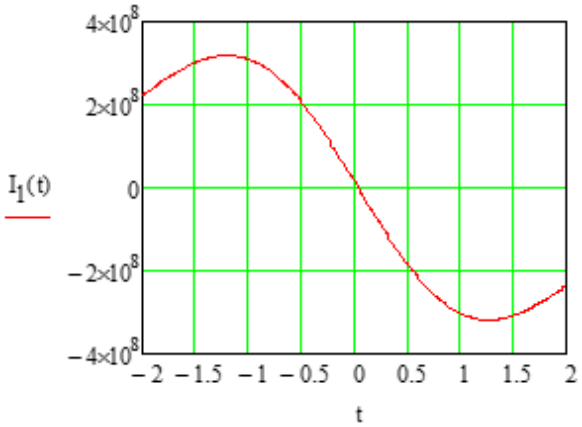
$$I_1(t) := \frac{-1}{2} \cdot \frac{\omega_{cn}^{\,2}}{T_s} \cdot \exp\left(\alpha_n^{\,2} \cdot \omega_{cn}^{\,2}\right) \cdot \exp\left(-\omega_{cn} \cdot t\right) \cdot \left(1 + \operatorname{erf}\left(-\alpha_n \cdot \omega_{cn} + \frac{1}{2} \cdot \frac{t}{\alpha_n}\right)\right) \ldots$$
$$+ \frac{1}{2} \cdot \frac{\omega_{cn}}{T_s} \cdot \exp\left(\alpha_n^{\,2} \cdot \omega_{cn}^{\,2}\right) \cdot \frac{\exp\left(-\omega_{cn} \cdot t\right)}{\pi^{\left(\frac{1}{2}\right)}} \cdot \frac{\exp\left[-\left(-\alpha_n \cdot \omega_{cn} + \frac{1}{2} \cdot \frac{t}{\alpha_n}\right)^2\right]}{\alpha_n}$$

$$I_0(t) := -.112837916709551257389 \cdot \omega_{cn} \cdot \frac{\left(20. \cdot \alpha_n^{\,4} \cdot \omega_{cn}^{\,2} - 20. \cdot \alpha_n^{\,2} \cdot \omega_{cn} \cdot t + 5. \cdot t^2 - 7. \cdot \alpha_n^{\,2}\right)}{\left[\left(-2. \cdot \alpha_n^{\,2} \cdot \omega_{cn} + t\right)^3 \cdot T_s\right]} \cdot \exp\left(-.250000000000000000000 \frac{t^2}{\alpha_n^{\,2}}\right)$$

$$I_1(t) := 5.641895835477562869480 \cdot 10^{-2} \cdot \left[\begin{array}{l} 40 \cdot \alpha_n^{\,6} \cdot \omega_{cn}^{\,2} \cdot \left(1 - \omega_{cn} \cdot t\right) + \alpha_n^{\,4} \cdot \omega_{cn} \cdot t \cdot \left(60 \cdot \omega_{cn} \cdot t - 26\right) \ldots \\ + 3. \cdot \alpha_n^{\,2} \cdot t^2 - 30 \cdot \alpha_n^{\,2} \cdot \omega_{cn} \cdot t^3 + 5 \cdot t^4 - 42 \cdot \alpha_n^{\,4} \end{array}\right] \cdot \exp\left[-\left(\frac{t}{2 \cdot \alpha_n}\right)^2\right] \cdot \frac{\omega_{cn}}{\left(-2 \cdot \alpha_n^{\,2} \cdot \omega_{cn} + t\right)^4 \cdot \alpha_n \cdot T_s}$$

$t := -2, -1.99 .. 2$





$noise := I_0(0)$ $\quad noise = 6.47 \times 10^8$

Determine the peak pulse amplitude - ISOLATED PULSE

Peak pulse amplitude - isolated pulse

$t_{poo} := \left| \begin{array}{l} t \leftarrow t_{pmin} \\ t_p \leftarrow \text{root}\left(I_1(t) \cdot T_s^{\,2}, t\right) \\ t_p \end{array} \right.$

$t_{pmin} := 0.032$

This is the peak time for pulse in slot 0 as a function of x and y

$t_{poo} = 0.032$

Determine the decision time

Threshold level - isolated pulse

$t_g := -0.477$

$t_{tho_i} := \left| \begin{array}{l} t \leftarrow t_g \\ t \leftarrow \text{root}\left[\left(I_0(t) - v_i \cdot I_0\left(t_{poo}\right)\right), t\right] \\ t \end{array} \right.$

$t_{tho_0} = -0.246$

$v_{th_i} := I_0\left(t_{tho_i}\right)$ This is the decision level voltage

$t_{d0_i} := t_{tho_i}$

Modify peak of single pulse

$t_p := \text{if}\left[\left(t_{poo} - t_{tho_0} + 0.5 \geq 1\right), \left(t_{tho_0} + 0.5\right), t_{poo}\right]$

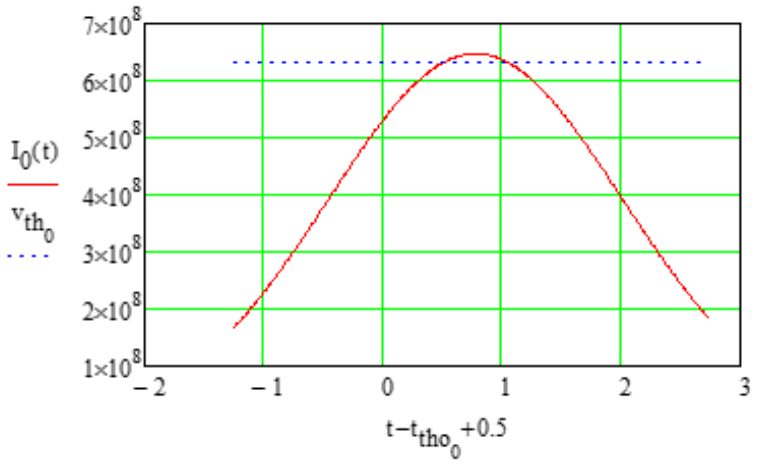
$t_p = 0.032$

$t_{po} := t_p$

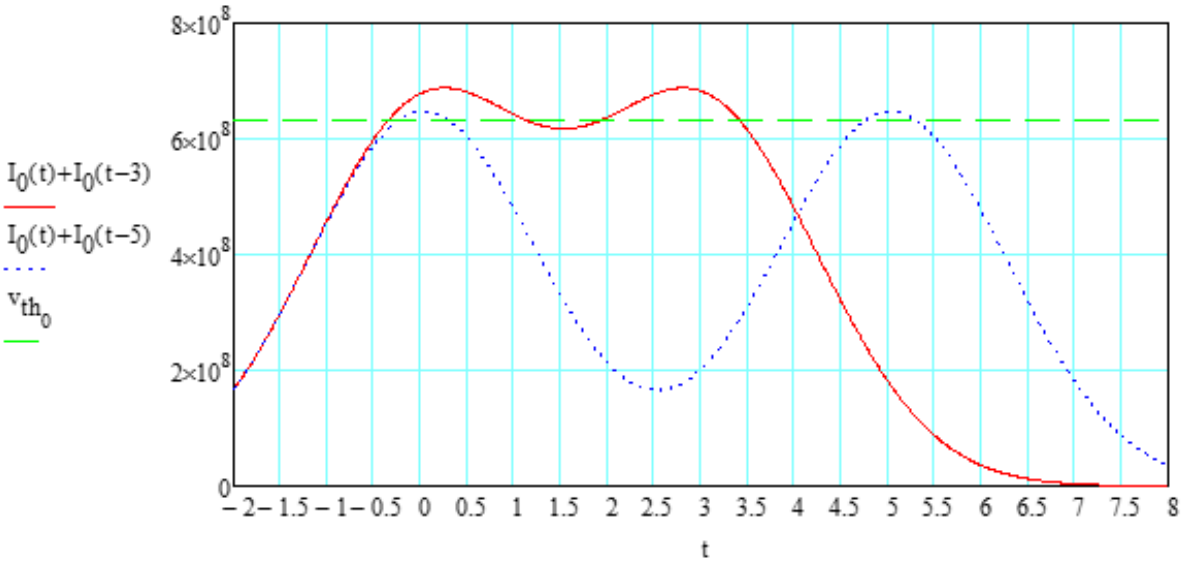
$t_{po} = 0.032$

$t_{po} - t_{tho_0} + 0.5 = 0.777$

$t := -2, -1.99 .. 2$



$t := -2, -1.99 .. 8$



Pulse definitions

$v_{o3}(a,b,c,t) := I_0(t + a) + I_0(t + b) + I_0(t + c)$

$v_{o2}(a,b,t) := I_0(t + a) + I_0(t + b)$

$v_{one3}(a,b,c,t) := I_1(t + a) + I_1(t + b) + I_1(t + c)$

$v_{one2}(a,b,t) := I_1(t + a) + I_1(t + b)$

$v_{o1C0CC0}(t) := v_{o3}(3,0,-7,t)$

$v_{o1C0C1}(t) := v_{o3}(3,0,-4,t)$

$v_{o11CC1}(t) := v_{o3}(2,0,-6,t)$

$v_{o1C00}(t) := v_{o3}(3,0,-2,t)$

$v_{o11C0}(t) := v_{o3}(2,0,-3,t)$

$v_{o111}(t) := v_{o3}(2,0,-2,t)$

$v_{o1CC1}(t) := v_{o2}(0,-6,t)$

$v_{o1C0}(t) := v_{o2}(0,-3,t)$

$v_{o11}(t) := v_{o2}(2,0,t)$

$v_{o0C1CC1}(t) := v_{o3}(5,0,-6,t)$

$v_{o0C1C0}(t) := v_{o3}(5,0,-3,t)$

$v_{o00CC0}(t) := v_{o3}(2,0,-6,t)$

$v_{o0C11}(t) := v_{o3}(5,0,-2,t)$

$v_{o00C1}(t) := v_{o3}(2,0,-5,t)$

$v_{o000}(t) := v_{o3}(2,0,-2,t)$

$v_{o0CC0}(t) := v_{o2}(6,0,t)$

$v_{o0C1}(t) := v_{o2}(5,0,t)$

$v_{o00}(t) := v_{o2}(0,-2,t)$

$v_{one1C0CC0}(t) := v_{one3}(3,0,-7,t)$

$v_{one1C0C1}(t) := v_{one3}(3,0,-4,t)$

$v_{one11CC1}(t) := v_{one3}(2,0,-6,t)$

$v_{one1C00}(t) := v_{one3}(3,0,-2,t)$

$v_{one11C0}(t) := v_{one3}(2,0,-3,t)$

$v_{one111}(t) := v_{one3}(2,0,-2,t)$

$v_{one1CC1}(t) := v_{one2}(0,-6,t)$

$v_{one1C0}(t) := v_{one2}(0,-3,t)$

$v_{one11}(t) := v_{one2}(2,0,t)$

$v_{one0C1CC1}(t) := v_{one3}(5,0,-6,t)$

$v_{one0C1C0}(t) := v_{one3}(5,0,-3,t)$

$v_{one00CC0}(t) := v_{one3}(2,0,-6,t)$

$v_{one0C11}(t) := v_{one3}(5,0,-2,t)$

$v_{one00C1}(t) := v_{one3}(2,0,-5,t)$

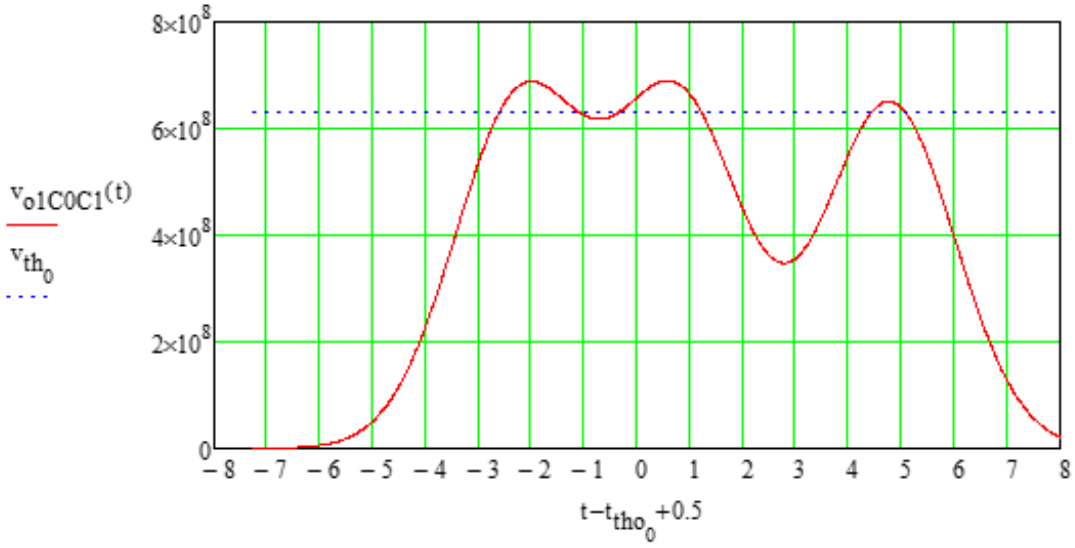
$v_{one000}(t) := v_{one3}(2,0,-2,t)$

$v_{one0CC0}(t) := v_{one2}(6,0,t)$

$v_{one0C1}(t) := v_{one2}(5,0,t)$

$v_{one00}(t) := v_{one2}(0,-2,t)$

$t := -8, -7.99 .. 8$



Peak value times

$$t_{p3}(a,b,c,t_{pmin}) := \left| \begin{array}{l} t \leftarrow t_{pmin} \\ t_{peak} \leftarrow \text{root}\left[\frac{d}{dt}\left(v_{o3}(a,b,c,t)\cdot T_s^{\,3}\right), t\right] \\ t_p \leftarrow \text{if}\left[\left(t_{peak} - t_{tho_0} + 0.5 \geq 1\right), \left(t_{tho_0} + 0.5\right), t_{peak}\right] \\ t_p \end{array} \right.$$

$$t_{p2}(a,b,t_{pmin}) := \left| \begin{array}{l} t \leftarrow t_{pmin} \\ t_{peak} \leftarrow \text{root}\left[\frac{d}{dt}\left(v_{o2}(a,b,t)\cdot T_s^{\,3}\right), t\right] \\ t_p \leftarrow \text{if}\left[\left(t_{peak} - t_{tho_0} + 0.5 \geq 1\right), \left(t_{tho_0} + 0.5\right), t_{peak}\right] \\ t_p \end{array} \right.$$

$t_{g2} := 0.007$ $t_{g3} := 0.0125$

$T_{p1C0CC0} := t_{p3}(3, 0, -7, t_{g3})$

$T_{p1C0CC0} - t_{tho_0} + 0.5 = 0.554$

$T_{p1C0C1} := t_{p3}(3, 0, -4, t_{g3})$

$T_{p1C0C1} - t_{tho_0} + 0.5 = 0.573$

$T_{p11CC1} := t_{p3}(2, 0, -6, t_{g3})$

$T_{p11CC1} - t_{tho_0} + 0.5 = -0.222$

$T_{p1C00} := t_{p3}(3, 0, -2, t_{g3})$

$T_{p1C00} - t_{tho_0} + 0.5 = 1$

$T_{p11C0} := t_{p3}(2, 0, -3, t_{g3})$

$T_{p11C0} - t_{tho_0} + 0.5 = -0.175$

$T_{p111} := t_{p3}(2, 0, -2, t_{g3})$

$T_{p111} - t_{tho_0} + 0.5 = 0.778$

$T_{p1CC1} := t_{p2}(0, -6, t_{g3})$

$T_{p1CC1} - t_{tho_0} + 0.5 = 0.778$

$T_{p1C0} := t_{p2}(0, -3, t_{g3})$

$T_{p1C0} - t_{tho_0} + 0.5 = 1$

$T_{p11} := t_{p2}(2, 0, t_{g2})$

$T_{p11} - t_{tho_0} + 0.5 = 0.753$

$T_{p0C1CC1} := t_{p3}(5, 0, -6, t_{g3})$

$T_{p0C1CC1} - t_{tho_0} + 0.5 = 0.776$ $\quad T_{p0C1CC1} = 0.031$

$T_{p0C1C0} := t_{p3}(5, 0, -3, t_{g3})$

$T_{p0C1C0} - t_{tho_0} + 0.5 = 1$

$T_{p00CC0} := t_{p3}(2, 0, -6, t_{g3})$

$T_{p00CC0} - t_{tho_0} + 0.5 = -0.222$ $\quad T_{p00CC0} = -0.968$

$T_{p0C11} := t_{p3}(5, 0, -2, t_{g3})$

$T_{p0C11} - t_{tho_0} + 0.5 = 1$ $\quad T_{p0C11} = 0.254$

$T_{p00C1} := t_{p3}(2, 0, -5, t_{g3})$

$T_{p00C1} - t_{tho_0} + 0.5 = -0.222$

$T_{p000} := t_{p3}(2, 0, -2, t_{g3})$

$T_{p000} - t_{tho_0} + 0.5 = 0.778$

$T_{p0CC0} := t_{p2}(6, 0, t_{g2})$

$T_{p0CC0} - t_{tho_0} + 0.5 = 0.753$ $\quad T_{p0CC0} = 7.007 \times 10^{-3}$

$T_{p0C1} := t_{p2}(5, 0, t_{g2})$

$T_{p0C1} - t_{tho_0} + 0.5 = 0.753$

$T_{p00} := t_{p2}(0, -2, t_{g3})$

$T_{p00} - t_{tho_0} + 0.5 = 1$ $\quad T_{p00} = 0.254$

Error sources

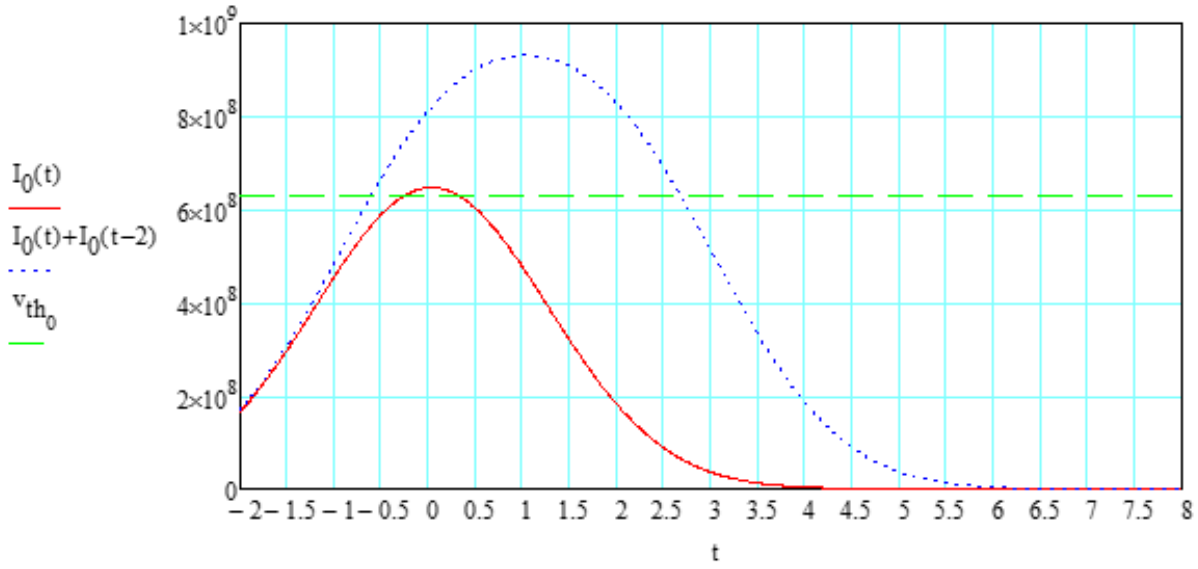
Erasure

Erasure - Erasure of middle symbol in 0 xC 1/0 yC 1/0

$$Err(x,y) := \left| \frac{x-y}{2} \right|$$ Clearly x=0 and y=0 gives 0 errors

x=0 and y>=1 is a special case for ISI

$t := -2, -1.99 .. 8$



$$Q_i := \eta q \cdot \frac{v_{o00C1}(T_{p00C1}) - v_{th_i}}{\sqrt{S_o \cdot noise}}$$

OK

$$Errors := \left[\sum_{y=0}^{n-1} \left[\frac{1}{4} \cdot \left(\frac{1}{2}\right)^0 \cdot \left(\frac{1}{2}\right) \cdot \left(\frac{1}{2}\right)^y \cdot \frac{1}{2} \cdot Err(0,y) \right] \ldots \right.$$
$$\left. + \frac{1}{4} \cdot \left(\frac{1}{2}\right)^0 \cdot \left(\frac{1}{2}\right) \cdot \left(\frac{1}{2}\right)^n \cdot 1 \cdot Err(0,n) \right]$$

$Errors = 0.062$

$$P_{er00yC}(b,i) := Errors \cdot \left(\frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}} \right) \right) \qquad P_{er00yC}(b,0) = 5.656 \times 10^{-3}$$

Erasure of middle symbol in 0 xC 1/0 yC 1/0 with x=1 to n & y=0 to n

$$Q_i := \eta q \cdot \frac{I_0(t_{po}) - (v_i \cdot I_0(t_{po}))}{\sqrt{S_o \cdot noise}}$$

$$Errors := \left[\sum_{x=1}^{n-1} \left[\sum_{y=0}^{n-1} \left[\frac{1}{4} \cdot \left(\frac{1}{2}\right)^x \cdot \frac{1}{2} \cdot \left(\frac{1}{2}\right)^y \cdot \frac{1}{2} \cdot Err(x,y) \right] + \frac{1}{4} \cdot \left(\frac{1}{2}\right)^x \cdot \frac{1}{2} \cdot \left(\frac{1}{2}\right)^n \cdot 1 \cdot Err(x,n) \right] \ldots \right.$$
$$\left. + \left[\sum_{y=0}^{n-1} \left[\frac{1}{4} \cdot \left(\frac{1}{2}\right)^n \cdot 1 \cdot \left(\frac{1}{2}\right)^y \cdot \frac{1}{2} \cdot Err(n,y) \right] + \frac{1}{4} \cdot \left(\frac{1}{2}\right)^n \cdot 1 \cdot \left(\frac{1}{2}\right)^n \cdot 1 \cdot Err(n,n) \right] \right]$$

$Errors = 0.104$

$$P_{er0xSyS}(b,i) := Errors \cdot \left(\frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}} \right) \right) \qquad P_{er0xSyS}(b,0) = 0.049$$

$$P_{er0}(b,i) := P_{er00yC}(b,i) + P_{er0xSyS}(b,i) \qquad P_{er0}(b,0) = 0.055$$

Erasure of middle symbol in 1 xC 0 yC 1 for both instances are identical to what has already been calculated

$$P_{eer}(b,i) := 2 \cdot P_{er0}(b,i) \qquad P_{eer}(b,0) = 0.109$$

False Alarm

False 0 following a 1 at some time

k = ODD combinations = k+1
K = EVEN combinations = x-k+1

Errors = (combs-1)/2

$$odd(k) := \frac{k}{2} - trunc\left(\frac{k}{2}\right) = 0.5$$

$$Errodd(x,y,k) := \frac{k+1-1}{2}$$

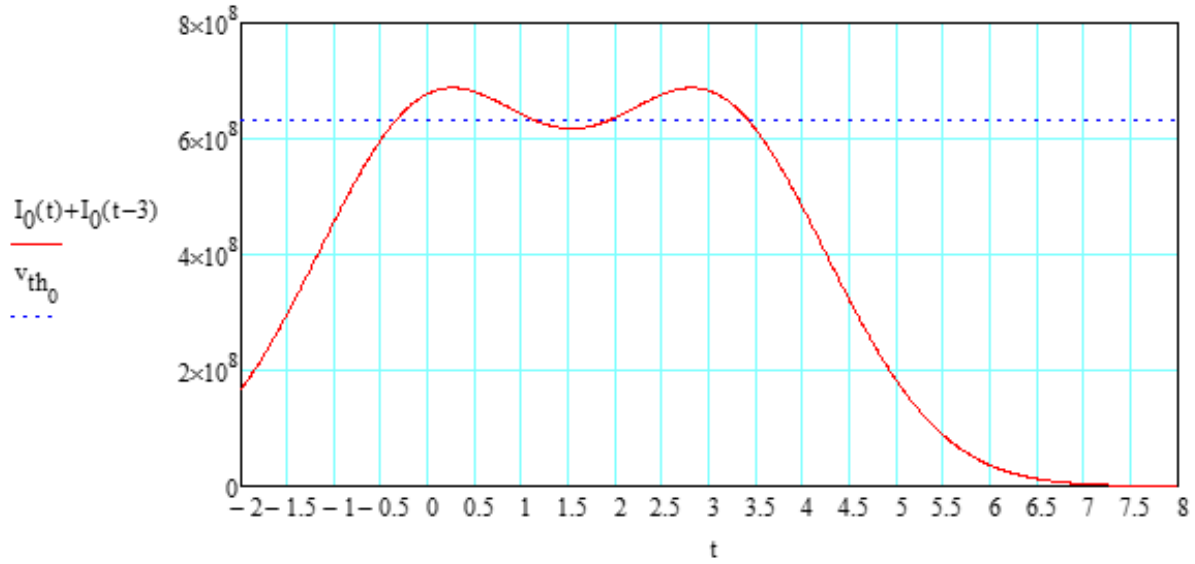
$$even(k) := \frac{k}{2} - trunc\left(\frac{k}{2}\right) = 0$$

$$Erreven(x,y,k) := \frac{x-k+1-1}{2}$$

$$Err(x,y,k) := Erreven(x,y,k)\cdot even(k) + Errodd(x,y,k)\cdot odd(k)$$

0 yC 1 xC 0: x=1, k=1 condition is special - ISI from pulse 1 spilling into the slot 0 of C

$t := -2, -1.99..8$



$$Q_i := \eta q \cdot \frac{v_{o0C1C0}(T_{p0C1C0}) - v_{th_i}}{\sqrt{S_o \cdot noise}}$$

$$Errors := \left[\sum_{y=1}^{n-1} \left[\left(\frac{1}{2}\right)^{1+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(1,y,1) \right] \ldots + \left(\frac{1}{2}\right)^{1+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(1,n,1) \right]$$

$Errors = 0.016$

$$P_{false0in1C0}(b,i) := Errors \cdot \left(\frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}} \right) \right)$$

$P_{false0in1C0}(b,0) = 6.249 \times 10^{-3}$

x=2..n, k=1 condition is special - ISI from pulse 1 spilling into the slot 0 of C

$$Errors := \left[\sum_{x=2}^{n-1} \left[\sum_{y=1}^{n-1} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(x,y,1) \right] + \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(x,n,1) \right] \right] \ldots + \sum_{y=1}^{n-1} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(n,y,1) \right] + \left[\left(\frac{1}{2}\right)^{n} \cdot \left(\frac{1}{4}\right) \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(n,n,1) \right] \right]$$

$Errors = 0.016$

$$Q_i := \eta q \cdot \frac{v_{th_i} - v_{o1C0}(T_{p1C0} + 1)}{\sqrt{S_o \cdot noise}}$$

$$P_{false0in1xC0}(b,i) := Errors \cdot \left(\frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}} \right) \right)$$

$P_{false0in1xC0}(b,0) = 7.643 \times 10^{-3}$

x=2..n, k=2..x condition

$$Errors := \left[\sum_{y=1}^{n-1} \left[\sum_{x=2}^{n-1} \sum_{k=2}^{x} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(x,y,k) \right] + \sum_{k=2}^{n} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(n,y,k) \right] \right] \ldots + \sum_{x=2}^{n-1} \sum_{k=2}^{x} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(x,n,k) \right] + \sum_{k=2}^{n} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(n,n,k) \right] \right]$$

$Errors = 0.058$

$$Q_i := \eta q \cdot \frac{v_{th_i}}{\sqrt{S_o \cdot noise}}$$

$$P_{false0post1}(b,i) := Errors \cdot \frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}}\right)$$

$$P_{false0post1}(b,0) = 1.457 \times 10^{-4}$$

$$P_{ef0post1}(b,i) := P_{false0in1C0}(b,i) + P_{false0in1xC0}(b,i) + P_{false0post1}(b,i)$$

$$P_{ef0post1}(b,0) = 0.014$$

False 1 following a 0 at some time

k = ODD combinations = k+1
K = EVEN combinations = y-k+1

Errors = (combs-1)/2 in x+y+4 PCM bits

$$odd(k) := \frac{k}{2} - trunc\left(\frac{k}{2}\right) = 0.5$$

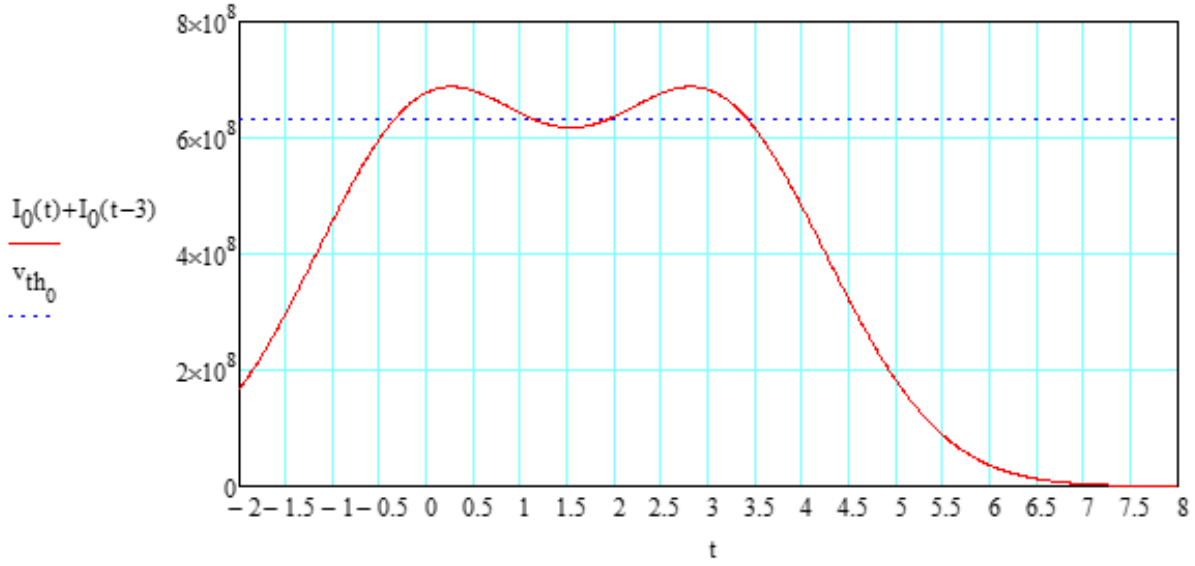
$$Errodd(x,y,k) := \frac{k+1-1}{2}$$

$$even(k) := \frac{k}{2} - trunc\left(\frac{k}{2}\right) = 0$$

$$Erreven(x,y,k) := \frac{y-k+1-1}{2}$$

$$Err(x,y,k) := Erreven(x,y,k) \cdot even(k) + Errodd(x,y,k) \cdot odd(k)$$

$t := -2, -1.99 .. 8$



0C1: y=1 - ISI from pulse 0 spilling into the slot 1 of the same frame, no violation occurs as due to central decision detection the pulse will be first detected in slot 0 (as it is still present in slot 0) and decoder will stop once a pulse has been received thus no effect of the spilled pulse in slot 1

However, y=1, k=1 condition is special - noise can cause a threshold crossing event in C

$$Errors := \left[\sum_{x=1}^{n-1} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{1+1} \cdot Err(x,1,1) \right] \ldots \right.$$
$$\left. + \left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{1+1} \cdot Err(n,1,1) \right]$$

$$Errors = 0.016$$

$$Q_i := \eta q \cdot \frac{v_{th_i} - v_{o0C1}\left(T_{p0C1} + 1\right)}{\sqrt{S_o \cdot noise}}$$

$$P_{false1in0C1}(b,i) := Errors \cdot \left(\frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}} \right) \right)$$

$$P_{false1in0C1}(b,0) = 3.775 \times 10^{-3}$$

0yC1: y=2..n - ISI from pulse 0 spilling into the slot 1 of the same frame will be detected the same way mentioned above thus no effect of the spilled pulse in slot 1

However, y=2..n, k=1 condition is special - noise can cause a threshold crossing event in the first C immediately after 0

$$Errors := \left[\sum_{x=1}^{n-1} \left[\sum_{y=2}^{n-1} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(x,y,1) \right] + \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(x,n,1) \right] \right] \ldots \right.$$
$$\left. + \sum_{y=2}^{n-1} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(n,y,1) \right] + \left[\left(\frac{1}{2}\right)^{n} \cdot \left(\frac{1}{4}\right) \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(n,n,1) \right] \right]$$

$$Errors = 0.016$$

$$Q_i := \eta q \cdot \frac{v_{th_i} - \left(I_0\left(3 + t_{po}\right)\right)}{\sqrt{S_o \cdot noise}}$$

$$P_{false1in0yC1}(b,i) := Errors \cdot \left(\frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}} \right) \right)$$

$$P_{false1in0yC1}(b,0) = 6.151 \times 10^{-5}$$

y=2..n, k=2..x condition

$$\text{Errors} := \left[\sum_{y=2}^{n-1} \left[\sum_{x=2}^{n-1} \sum_{k=2}^{x} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot \text{Err}(x,y,k) \right] + \sum_{k=2}^{n} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot \text{Err}(n,y,k) \right] \right] \ldots \right.$$
$$\left. + \sum_{x=2}^{n-1} \sum_{k=2}^{x} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot \text{Err}(x,n,k) \right] + \sum_{k=2}^{n} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot \text{Err}(n,n,k) \right] \right]$$

$$\text{Errors} = 0.022$$

$$Q_i := \eta q \cdot \frac{v_{th_i}}{\sqrt{S_0 \cdot noise}}$$

$$P_{false1post0}(b,i) := \text{Errors} \cdot \frac{1}{2} \cdot \text{erfc}\left(\frac{b \cdot Q_i}{\sqrt{2}}\right)$$

$$P_{false1post0}(b,0) = 5.603 \times 10^{-5}$$

$$P_{ef1post0}(b,i) := P_{false1in0C1}(b,i) + P_{false1in0yC1}(b,i) + P_{false1post0}(b,i)$$

$$P_{ef1post0}(b,0) = 3.893 \times 10^{-3}$$

$$P_{efdiff}(b,i) := P_{ef0post1}(b,i) + P_{ef1post0}(b,i)$$

$$P_{efdiff}(b,0) = 0.018$$

False 0 following a 0 at some time

k = ODD combinations = x-k+1
K = EVEN combinations = k+1

Errors = (combs-1)/2

$$\text{odd}(k) := \frac{k}{2} - \text{trunc}\left(\frac{k}{2}\right) = 0.5$$

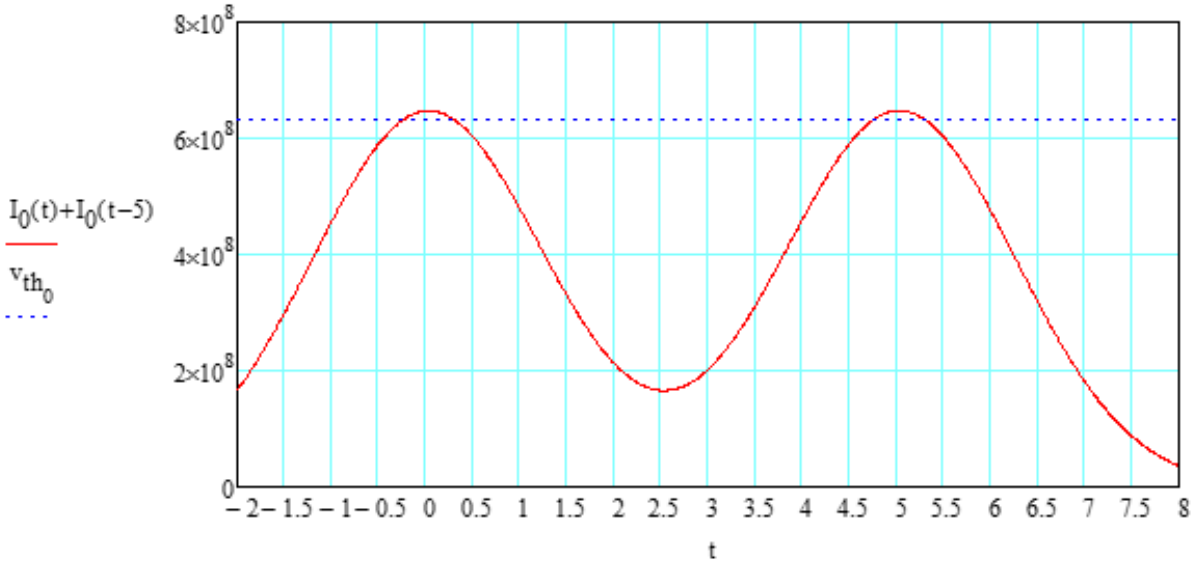
$$\text{Errodd}(x,y,k) := \frac{x-k+1-1}{2}$$

$$\text{even}(k) := \frac{k}{2} - \text{trunc}\left(\frac{k}{2}\right) = 0$$

$$\text{Erreven}(x,y,k) := \frac{k+1-1}{2}$$

$$\text{Err}(x,y,k) := \text{Erreven}(x,y,k) \cdot \text{even}(k) + \text{Errodd}(x,y,k) \cdot \text{odd}(k)$$

$t := -2, -1.99..8$



00 yC 1: y=1, k=1 - if there is false alarm of 0 in C slot following 0 (1xC001) then there will be zero errors as there's only one possible correct combination of the aforementioned error which will be corrected by MLSD.

1 xC 0 yC 1: if y=2..n then K>=2 thus this condition can be covered by the following condition of y=2..n, k=2..x

y=2..n, k=2..x condition

$$Errors := \left[\sum_{y=2}^{n-1} \left[\sum_{x=2}^{n-1} \sum_{k=2}^{x} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(x,y,k) \right] + \sum_{k=2}^{n} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(n,y,k) \right] \right] \ldots \right.$$
$$\left. + \sum_{x=2}^{n-1} \sum_{k=2}^{x} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(x,n,k) \right] + \sum_{k=2}^{n} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(n,n,k) \right] \right]$$

$$Q_i := \eta q \cdot \frac{v_{th_i}}{\sqrt{S_0 \cdot noise}}$$

$$P_{false0post0}(b,i) := Errors \cdot \frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}}\right)$$

$$P_{false0post0}(b,0) = 8.187 \times 10^{-5}$$

$$P_{ef0post0}(b,i) := P_{false0post0}(b,i)$$

$$P_{ef0post0}(b,0) = 8.187 \times 10^{-5}$$

False 1 following a 1 at some time

k = ODD combinations = y-k+1
K = EVEN combinations = k+1

Errors = (combs-1)/2 in x+y+4 PCM bits

$$odd(k) := \frac{k}{2} - trunc\left(\frac{k}{2}\right) = 0.5$$

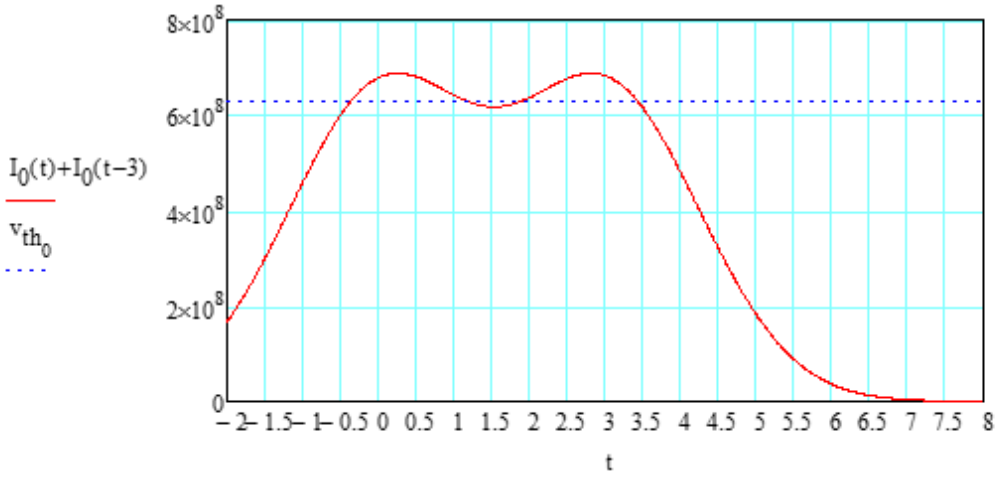
$$Errodd(x,y,k) := \frac{y-k+1-1}{2}$$

$$even(k) := \frac{k}{2} - trunc\left(\frac{k}{2}\right) = 0$$

$$Erreven(x,y,k) := \frac{k+1-1}{2}$$

$$Err(x,y,k) := Erreven(x,y,k)\cdot even(k) + Errodd(x,y,k)\cdot odd(k)$$

$$t := -2, -1.99..8$$



1C0: x=1, k=1 - in this condition ISI from 1 pulse spilling into the C frame - this will be detected as a false 0 and will generate zero errors as there's only one possible correct combination of the aforementioned error which will be corrected by MLSD.

If x=2..n then K>=2 thus this condition can be covered by the following condition of x=2..n, k=2..x
x=2..n, k=2..x condition

$$Errors := \left[\sum_{y=1}^{n-1} \left[\sum_{x=2}^{n-1} \sum_{k=2}^{x} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(x,y,k) \right] + \sum_{k=2}^{n} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{y+1} \cdot Err(n,y,k) \right] \right] \ldots \right.$$
$$\left. + \sum_{x=2}^{n-1} \sum_{k=2}^{x} \left[\left(\frac{1}{2}\right)^{x+1} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(x,n,k) \right] + \sum_{k=2}^{n} \left[\left(\frac{1}{2}\right)^{n} \cdot \frac{1}{4} \cdot \left(\frac{1}{2}\right)^{n} \cdot Err(n,n,k) \right] \right]$$

$$Q_i := \eta q \cdot \frac{v_{th_i}}{\sqrt{S_o \cdot noise}}$$

$$P_{false1post1}(b,i) := Errors \cdot \frac{1}{2} \cdot erfc\left(\frac{b \cdot Q_i}{\sqrt{2}}\right)$$

$$P_{false1post1}(b,0) = 9.587 \times 10^{-5}$$

$$P_{ef1post1}(b,i) := P_{false1post1}(b,i)$$

$$P_{ef1post1}(b,0) = 9.587 \times 10^{-5}$$

$$P_{efsame}(b,i) := P_{ef0post0}(b,i) + P_{ef1post1}(b,i)$$

$$P_{efsame}(b,0) = 1.777 \times 10^{-4}$$

$$P_{ef}(b,i) := P_{efdiff}(b,i) + P_{efsame}(b,i)$$

$P_{ef}(b,i) =$	$P_{eer}(b,i) =$
0.018	0.109
0.018	0.11
0.018	0.11
0.018	0.11
0.018	0.111
0.018	0.111
0.018	0.111
0.018	0.111
0.018	0.112
0.018	0.112
0.018	0.112
0.018	0.113
0.018	0.113
0.018	0.113
0.018	0.114
...	...

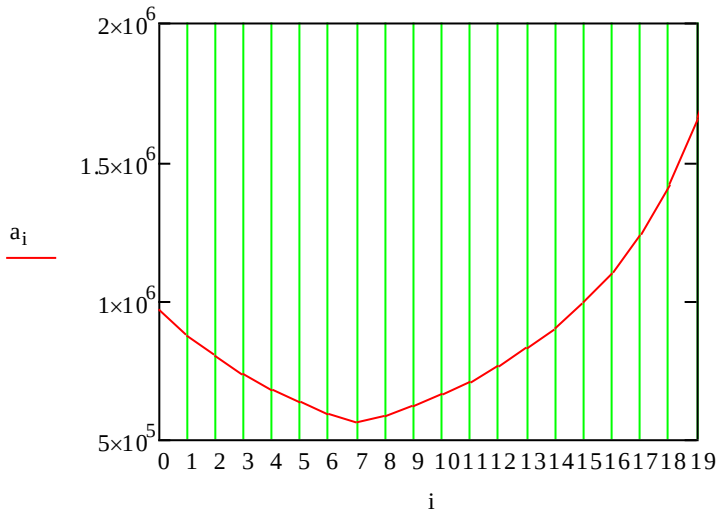
$P_{eb}(b,i) := P_{eer}(b,i) + P_{ef}(b,i)$

$pc(b,i) := \left(\log\left(P_{eb}(b,i)\cdot 10^{3}\right) + 6\right)$ Set for 1 in 10^9 errors

$a_i := \text{root}(pc(b,i),b)$ Find the root to give 1 in 10^9

minimum := min(a)

minimum = 5.678×10^{5}



$a_i =$

$9.702\cdot 10^5$
$8.774\cdot 10^5$
$8.008\cdot 10^5$
$7.365\cdot 10^5$
$6.818\cdot 10^5$
$6.346\cdot 10^5$
$5.937\cdot 10^5$
$5.678\cdot 10^5$
$5.867\cdot 10^5$
$6.228\cdot 10^5$
$6.643\cdot 10^5$
$7.118\cdot 10^5$
$7.666\cdot 10^5$
$8.304\cdot 10^5$
$9.059\cdot 10^5$
...

$b \equiv 5\cdot 10^{3}$

$v_{off} \equiv 0.97$ range ≡ 100

$f_n \equiv 0.43$

b := minimur $b = 5.678\times 10^{5}$

$$dBm := 10\cdot\log\left[b\cdot\frac{photon\_energy}{10^{-3}}\cdot\left[\frac{n+1}{2\cdot(2)\cdot n}\right]\cdot B\right]$$

dBm = −16.982

$$dBm_{guardslots} := 10\cdot\log\left[b\cdot\frac{photon\_energy}{10^{-3}}\cdot\left[\frac{n+1}{4\cdot(2)\cdot n}\right]\cdot B\right]$$

$dBm_{guardslots} = -19.992$

i := 7

$v_i = 0.982$

$\text{minimum}10^{-3} = 567.79$

$P_{eer}(b,i)\cdot 10^{10} = 4.16$

$P_{er0}(b,i)\cdot 10^{10} = 2.08$

$P_{ef}(b,i)\cdot 10^{10} = 5.84$

$\left(P_{ef0post1}(b,i) + P_{ef0post0}(b,i)\right)\cdot 10^{10} = 5.84$

$\left(P_{ef1post1}(b,i) + P_{ef1post0}(b,i)\right)\cdot 10^{10} = 0$

Appendix 2.4

DuoPPM MLSD Mathcad Results

Sensitivities of DuoPPM, DuoPPM with two guard slots (DuoPPMw2guradslots) for normalised fibre bandwidth (f_n) between 0.46 to 100 given below. All simulations done for 1 Gbps data rate.

freq :=	DuoPPM :=	DuoPPMw2guardslots :=
0.46	–30.219	–33.23
0.5	–30.881	–33.891
0.6	–32.073	–35.083
0.7	–32.949	–35.959
0.8	–33.466	–36.476
0.9	–33.943	–36.973
1	–34.159	–37.209
1.2	–34.607	–37.667
1.5	–35.027	–38.087
1.8	–35.366	–38.427
2	–35.535	–38.554
3	–36.194	–39.204
4	–36.682	–39.692
5	–37.072	–40.082
6	–37.495	–40.475
7	–37.753	–40.803
8	–38.035	–41.045
9	–38.218	–41.229
10	–38.48	–41.481
12	–38.788	–41.798
15	–39.182	–42.202
18	–39.491	–42.542
20	–39.682	–42.693
30	–40.356	–43.356
40	–40.735	–43.775
50	–41.043	–44.053
60	–41.242	–44.252
70	–41.432	–44.441
80	–41.597	–44.608
90	–41.743	–44.754
100	–41.787	–44.798

Sensitivities of digital PPM (DPPM), optimised digital PPM (optDPPM), dicode PPM (Dicode) and Dicode PPM with two guard slots (Dicodew2guradslots) for normalised fibre bandwidth (f_n) between 0.46 to 100 given below. All simulations done for 1 Gbps data rate.

$$DPPM := \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ -25.939 \\ -27.112 \\ -28.543 \\ -29.709 \\ -30.382 \\ -33.12 \\ -34.962 \\ -36.38 \\ -37.529 \\ -38.493 \\ -39.318 \\ -40.016 \\ -40.589 \\ -40.998 \\ -41.389 \\ -41.767 \\ -42.009 \\ -42.678 \\ -43.096 \\ -43.383 \\ -43.595 \\ -43.757 \\ -43.886 \\ -43.991 \\ -44.079 \end{pmatrix} \quad optDPPM := \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ -30.606 \\ -31.764 \\ -33.019 \\ -33.461 \\ -34.5 \\ -36.18 \\ -37.346 \\ -38.021 \\ -38.959 \\ -39.306 \\ -39.583 \\ -40.016 \\ -40.589 \\ -40.892 \\ -41.319 \\ -41.687 \\ -42.009 \\ -42.678 \\ -43.096 \\ -43.383 \\ -43.595 \\ -43.757 \\ -43.886 \\ -43.991 \\ -44.079 \end{pmatrix}$$

$$Dicode := \begin{pmatrix} -28.479 \\ -29.151 \\ -30.372 \\ -31.279 \\ -32.036 \\ -32.582 \\ -32.979 \\ -33.488 \\ -33.956 \\ -34.326 \\ -34.546 \\ -35.394 \\ -36.002 \\ -36.472 \\ -36.854 \\ -37.175 \\ -37.45 \\ -37.691 \\ -37.904 \\ -38.265 \\ -38.695 \\ -39.031 \\ -39.219 \\ -39.885 \\ -40.307 \\ -40.586 \\ -40.769 \\ -40.89 \\ -41.088 \\ -41.193 \\ -41.283 \end{pmatrix} \quad Dicodew2guardslots := \begin{pmatrix} -31.489 \\ -32.161 \\ -33.383 \\ -34.289 \\ -35.046 \\ -35.593 \\ -35.989 \\ -36.489 \\ -36.967 \\ -37.337 \\ -37.557 \\ -38.404 \\ -39.012 \\ -39.482 \\ -39.865 \\ -40.185 \\ -40.461 \\ -40.702 \\ -40.914 \\ -41.276 \\ -41.705 \\ -42.041 \\ -42.229 \\ -42.895 \\ -43.307 \\ -43.596 \\ -43.807 \\ -43.97 \\ -44.098 \\ -44.204 \\ -44.293 \end{pmatrix}$$

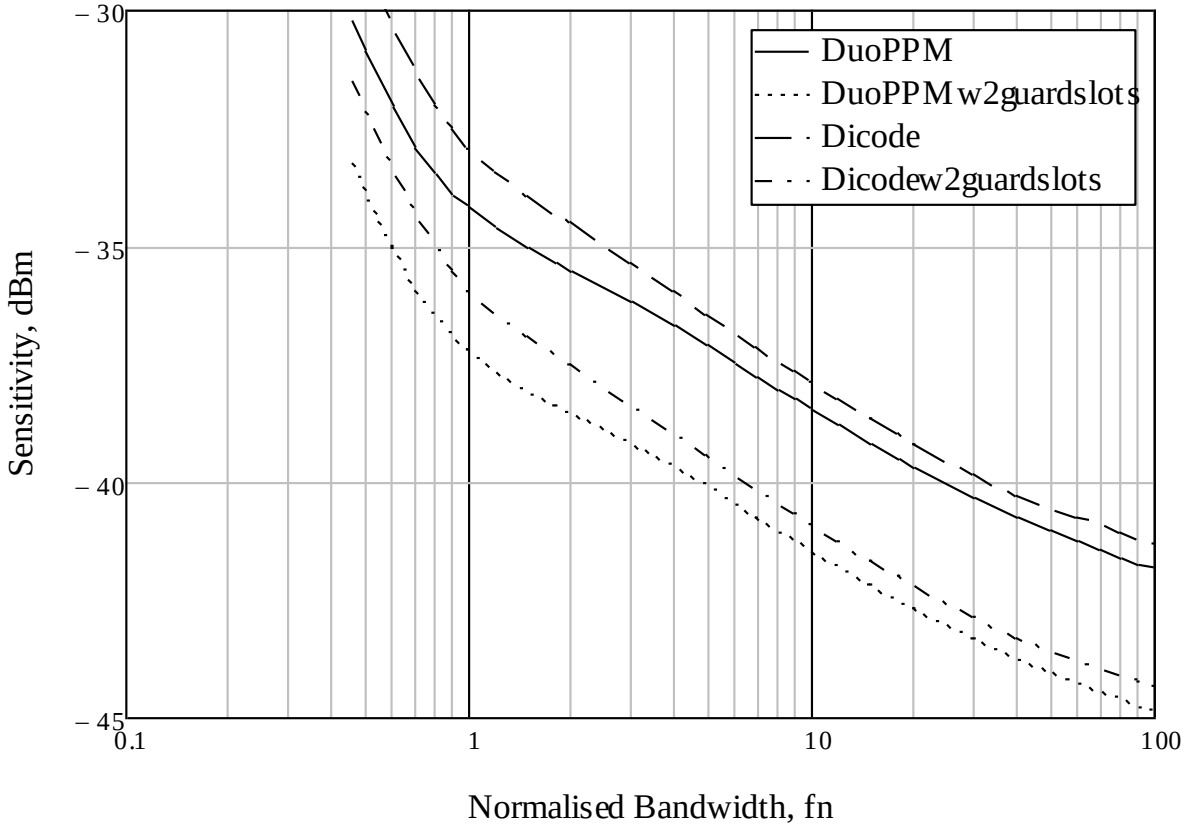


Fig. A2 - 2.3: Sensitivity comparisons of DuoPPM and dicode PPM (Dicode) both with and without 2 guard slots at 1 Gbps data rate.

Photons/pulse count of DuoPPM, Dicode, digital PPM (DPPM) and optimised digital PPM (optDPPM) for normalised fibre bandwidth (f_n) between 0.46 to 100 given below. All simulations done for 1 Gbps data rate.

freq :=	DuoPPM :=	Dicode :=	DPPM :=
0.46	27012	40326	0
0.5	23193	34545	0
0.6	17626	26073	0
0.7	14406	21163	0
0.8	12790	17778	0
0.9	11459	15674	0
1	10903	14308	139000
1.2	9835	12752	106100
1.5	8928	11423	76290
1.8	8258	10490	58330
2	7943	9972	49957
3	6824	8205	26595
4	6099	7133	17402
5	5575	6402	12554
6	5058	5861	9636
7	4766	5445	7718
8	4466	5110	6383
9	4282	4834	5435
10	4031	4603	4763
12	3755	4235	4335
15	3430	3837	3962
18	3194	3551	3632
20	3057	3401	3435
30	2617	2917	2944
40	2399	2653	2674
50	2234	2482	2503
60	2134	2365	2384
70	2043	2278	2297
80	1967	2212	2229
90	1902	2158	2176
100	1883	2114	2133

$$optDPPM := \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 20330 \\ 8295 \\ 5634 \\ 4307 \\ 3687 \\ 2971 \\ 2743 \\ 2573 \\ 2330 \\ 2041 \\ 1472 \\ 1262 \\ 1146 \\ 1073 \\ 1022 \\ 984 \\ 956 \\ 933 \\ 914 \end{pmatrix} \qquad freq1 := \begin{pmatrix} 0.46 \\ 0.5 \\ 0.6 \\ 0.7 \\ 0.8 \\ 0.9 \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \\ 8 \\ 9 \\ 10 \\ 20 \\ 30 \\ 40 \\ 50 \\ 60 \\ 70 \\ 80 \\ 90 \\ 100 \end{pmatrix}$$

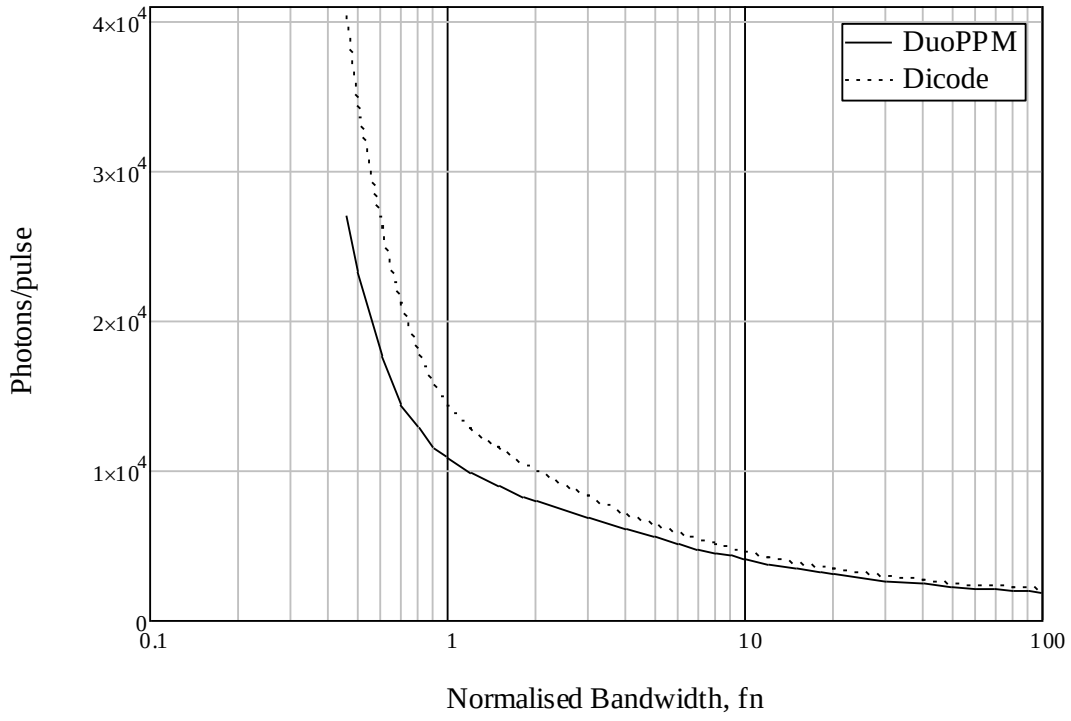


Fig. A2 - 2.4: Comparisons of photons per pulse of DuoPPM and dicode PPM (Dicode) at 1 Gbps data rate.

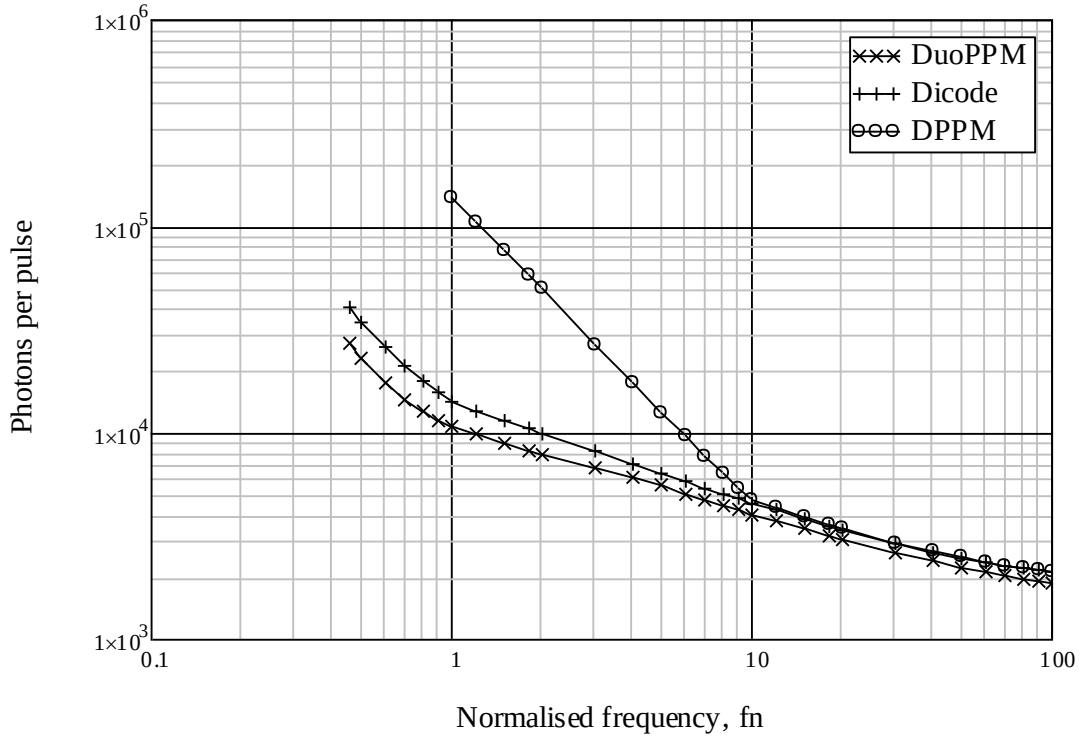


Fig. A2 - 2.5: Comparisons of photons per pulse of DuoPPM, dicode PPM (Dicode) and digital PPM (DPPM) at 1 Gbps data rate.

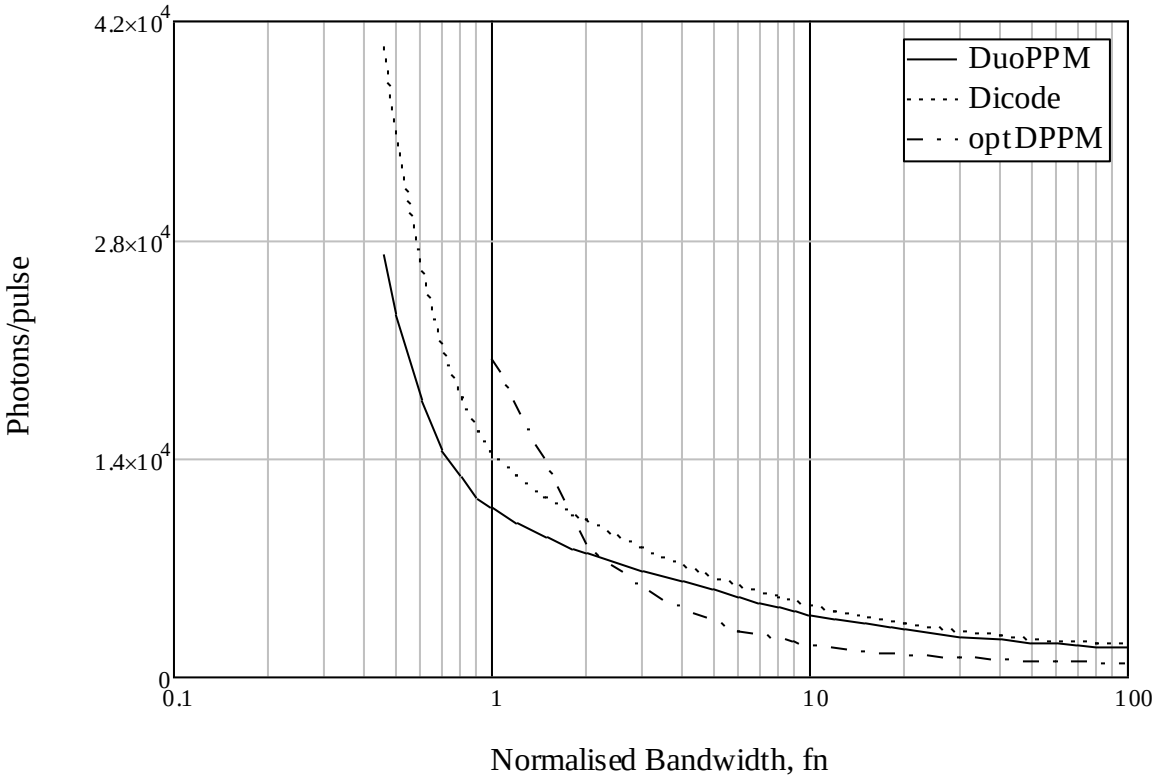


Fig. A2 - 2.6: Comparisons of photons per pulse of DuoPPM, Dicode PPM (Dicode) and optimised digital PPM (optDPPM) at 1 Gbps data rate.

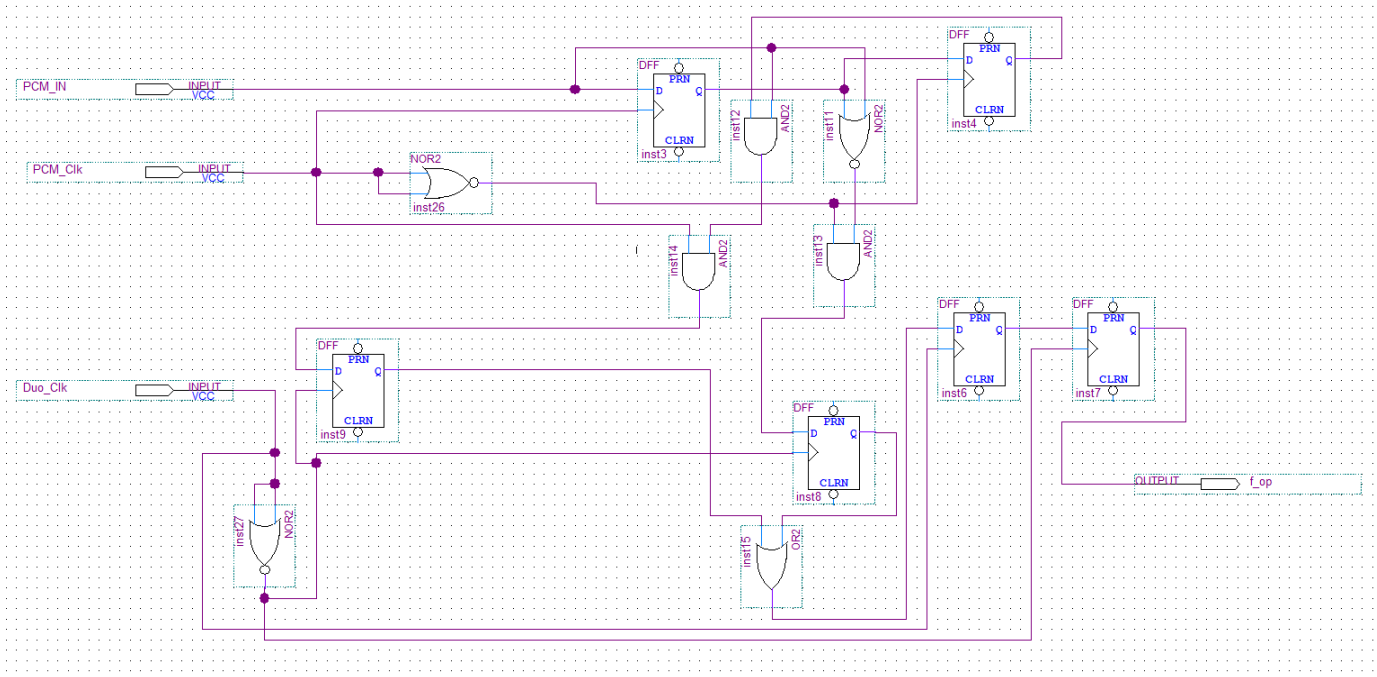
Appendix 3

All VHDL codes and schematics for the DuoPPM system are provided in this section.

Appendix 3.1: PRBS PCM Generator

```
1  --K Mostafa--
2  --University of Huddersfield--
3  --DuoPPM Project--
4  --PRBS PCM Generator--
5
6  LIBRARY IEEE;
7  USE IEEE.std_logic_1164.ALL;
8  USE IEEE.std_logic_arith.ALL;
9  USE IEEE.std_logic_unsigned.ALL;
10
11
12 ENTITY PCM_Gen is
13
14     PORT(SIGNAL Clkin           :   IN std_logic;
15          SIGNAL Reset           :   IN std_logic;
16          SIGNAL O_Put           :   OUT std_logic);
17
18 END PCM_Gen;
19
20 ARCHITECTURE archi OF PCM_Gen IS
21
22   SIGNAL Tmp                    : std_logic_vector(0 TO 7):= "10000101";
23
24 BEGIN
25     PROCESS
26         VARIABLE first_tap  : std_logic;
27         VARIABLE second_tap : std_logic;
28         VARIABLE third_tap  : std_logic;
29
30 BEGIN
31     WAIT UNTIL (Clkin' EVENT AND Clkin = '0');
32         IF (Reset = '0') THEN
33         Tmp <= "10000101";
34
35         ELSE IF (Reset = '1') THEN
36             first_tap   := Tmp (3) xor Tmp (4);
37             second_tap  := Tmp (5) xor Tmp (7);
38             third_tap   := first_tap xor second_tap;
39             Tmp         <= third_tap & Tmp (0 TO 6);
40         END IF;
41         END IF;
42 END PROCESS;
43
44 O_Put <= Tmp (0);
45
46 END archi;
```

Appendix 3.2: Implemented Coder Using Logic Gates



Appendix 3.3: SIPO Two-Bit for MLSD

```
1  --K Mostafa--
2  --University of Huddersfield--
3  --DuoPPM Project--
4  --SIPO Two Bit for MLSD--
5
6  library ieee;
7  use ieee.std_logic_1164.all;
8  use ieee.std_logic_arith.all;
9  use ieee.std_logic_unsigned.all;
10
11 entity err_det_cor is
12
13     port(signal Clk2            :   IN std_logic;
14          signal SI              :   IN std_logic;
15          signal Reset           :   IN std_logic;
16          signal OP1             :   OUT std_logic_vector (1 DOWNTO 0));
17
18 end err_det_cor;
19
20
21 architecture func of err_det_cor is
22
23 SIGNAL cntrl1           : std_logic_vector (1 downto 0):="10";
24 SIGNAL Tmpr1            : std_logic_vector (1 downto 0);
25
26 BEGIN
27
28     PROCESS
29     BEGIN
30     WAIT UNTIL (Clk2'EVENT AND Clk2 = '1');
31
32         IF (Reset = '0') THEN
33
34         cntrl1 <= "01";
35
36         ELSE
37
38         Tmpr1(1) <= Tmpr1(0);
39
40         Tmpr1(0) <= SI;
41         cntrl1 <= (cntrl1(0)& cntrl1 (1));
42
43      END IF;
44
45      END PROCESS;
46
47     PROCESS
48     BEGIN
49     WAIT UNTIL (Clk2'EVENT AND Clk2 = '0');
50
51         IF cntrl1 = "01" THEN
52
53             OP1  <= Tmpr1;
54
55         END IF;
56     END PROCESS;
57
58     END func;
```

Appendix 3.4: Error Detector and Corrector Module

```
1  --K Mostafa--
2  --University of Huddersfield--
3  --DuoPPM Project--
4  --Error Detector and Corrector--
5
6  library ieee;
7  use ieee.std_logic_1164.all;
8  use ieee.std_logic_arith.all;
9  use ieee.std_logic_unsigned.all;
10
11
12
13 entity det_cor is
14
15     generic (n: natural := 48);
16
17     port(signal Clk             :   IN std_logic;
18          signal IP1             :   IN std_logic_vector (1 DOWNTO 0);
19          signal Reset           :   IN std_logic;
20          signal load_D3         :   IN std_logic;
21          signal Clk2            :   IN std_logic;
22          signal OP_F            :   OUT std_logic;
23          signal OP_ws           :   OUT std_logic;
24          signal OP_wsr          :   OUT std_logic;
25          signal OP_fa           :   OUT std_logic);
26
27
28 end det_cor;
29
30
31
32 architecture func of det_cor is
33
34 SIGNAL regConCat        : std_logic_vector (1 downto 0):= "00";
35
36 SIGNAL tmp              : std_logic_vector (1 DOWNTO 0);
37 SIGNAL shift_reg3       : std_logic_vector (1 DOWNTO 0);
38 SIGNAL o_f              : std_logic;
39 SIGNAL f                : std_logic;
40 SIGNAL one              : std_logic;
41
42 SIGNAL countC           : std_logic_vector (3 downto 0):= "0000";
43 SIGNAL countSR          : std_logic_vector (3 downto 0):= "0000";
44 SIGNAL dly_C            : std_logic_vector (3 downto 0):= "0000";
45 SIGNAL dly_SR           : std_logic_vector (3 downto 0):= "0000";
46
47 SIGNAL regDIN1          : std_logic_vector (n-1 downto 0);
48 SIGNAL regOP1           : std_logic_vector (n-1 downto 0);
49 SIGNAL regOP2           : std_logic_vector (n-1 downto 0);
50
51 SIGNAL f_num            : std_logic_vector (1 downto 0):= "00";
52 SIGNAL f_ovrr           : std_logic_vector (1 downto 0):= "00";
53 SIGNAL cc               : std_logic_vector (1 downto 0):= "00";
54
55
56 SIGNAl w_slot           : std_logic;
57 SIGNAl w_slotR          : std_logic;
58 SIGNAl f_alrm           : std_logic;
```

```
59    SIGNAl wrongslot_det    : std_logic_vector (1 downto 0);
60    SIGNAl wrongslot_flg    : std_logic_vector (3 downto 0);
61    SIGNAl wrongslotR_flg   : std_logic_vector (4 downto 0);
62    SIGNAL false_alm        : std_logic_vector (5 downto 0);
63
64
65
66
67  BEGIN
68
69
70      PROCESS
71
72      BEGIN
73
74      WAIT UNTIL (Clk' EVENT AND Clk = '0');
75
76      regConCat <= IP1;
77
78      END PROCESS;
79
80
81
82      PROCESS
83
84      BEGIN
85
86
87      WAIT UNTIL (Clk' EVENT AND Clk = '1');
88
89      IF (regConCat = "00")THEN
90
91
92                      countSR <= "0000";
93                      countC <= countC + "0001";
94                      f_num  <= cc;
95
96
97      ELSIF (regConCat = "10")OR (regConCat = "01") THEN
98
99
100                     countC <= "0000";
101                     countSR <= countSR + "0001";
102                     cc <= regConCat;
103
104                     IF (regConCat = "10")THEN
105
106                     one <= '1';
107
108                     ELSE
109
110                     one <= '0';
111
112                     END IF;
113
114     END IF;
115
```

```
116     END PROCESS;
117
118
119     PROCESS
120     BEGIN
121     WAIT UNTIL (Clk' EVENT AND Clk = '0');
122
123     f <= one;
124
125     END PROCESS;
126
127     PROCESS
128     BEGIN
129     WAIT UNTIL (Clk' EVENT AND Clk = '1');
130
131     o_f <= f;
132
133     END PROCESS;
134
135     PROCESS
136
137     BEGIN
138
139     WAIT UNTIL (Clk' EVENT AND Clk = '0');
140
141     IF countC > "0000" THEN
142
143     dly_C <= countC;
144
145     ELSIF countC = "0000" THEN
146
147     dly_C <= dly_C;
148
149         IF countSR >= "1111" THEN
150
151             dly_C <= "0000";
152
153         ELSE dly_C <= dly_C;
154
155     END IF;
156     END IF;
157
158     END PROCESS;
159
160
161     PROCESS
162
163     BEGIN
164
165     WAIT UNTIL (Clk' EVENT AND Clk = '0');
166
167     IF countSR > "0000" THEN
168
169     dly_SR <= countSR;
170
171     ELSIF countSR = "0000" THEN
```

```
172
173       dly_SR <= dly_SR;
174
175       END IF;
176
177       END PROCESS;
178
179
180
181
182       PROCESS
183
184       BEGIN
185
186       WAIT UNTIL (Clk' EVENT AND Clk = '0');
187
188       IF Reset = '0' THEN
189
190                   wrongslot_det   <= "00";
191                   wrongslot_flg   <= "0000";
192                   wrongslotR_flg  <= "00000";
193                   w_slot          <= '0';
194                   w_slotR         <= '0';
195                   false_alm <= "000000";
196                   f_alrm      <= '0';
197
198
199       ELSIF Reset = '1' THEN
200
201
202           IF (wrongslot_det = "01") AND (cc = "01") THEN --err of 101
203
204
205                   wrongslot_flg   <= "0101";
206                   wrongslot_det   <= "00";
207                   w_slot          <= '1';
208
209           ELSIF (wrongslot_det = "10") AND (cc = "10") THEN --err of 010
210
211
212                   wrongslot_flg   <= "0110";
213                   wrongslot_det   <= "00";
214                   w_slot          <= '1';
215
216
217
218
219           ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
220                 AND (f_num = "01") AND (cc = "01")AND (dly_C = "0001") THEN --1C1
221
222                 false_alm <= "000001";
223
224           ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
225                 AND (f_num = "01") AND (cc = "10")AND (dly_C = "0010") THEN
226
227                 false_alm <= "000010";
228
```

```
229         ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
230               AND (f_num = "01") AND (cc = "01")AND (dly_C = "0011") THEN
231
232               false_alm <= "000011";
233
234         ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
235                 AND (f_num = "01") AND (cc = "10")AND (dly_C = "0100") THEN
236
237               false_alm <= "000100";
238
239         ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
240               AND (f_num = "01") AND (cc = "01")AND (dly_C = "0101") THEN
241
242               false_alm <= "000101";
243
244         ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
245               AND (f_num = "01") AND (cc = "10")AND (dly_C = "0110") THEN
246
247               false_alm <= "000110";
248
249         ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
250               AND (f_num = "01") AND (cc = "01")AND (dly_C = "0111") THEN
251
252               false_alm <= "000111";
253
254         ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
255               AND (f_num = "01") AND (cc = "10")AND (dly_C = "1000") THEN
256
257               false_alm <= "001000";
258
259         ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
260               AND (f_num = "01") AND (cc = "01")AND (dly_C = "1001") THEN
261
262               false_alm <= "001001";
263
264
265         ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
266               AND (f_num = "10") AND (cc = "10")AND (dly_C = "0001") THEN
267                 --0C0
268
269               false_alm <= "001010";
270
271         ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
272         AND (f_num = "10") AND (cc = "01")AND (dly_C = "0010") THEN
273
274               false_alm <= "001011";
275
276         ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
277               AND (f_num = "10") AND (cc = "10")AND (dly_C = "0011") THEN
278
279               false_alm <= "001100";
280
281         ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
282               AND (f_num = "10") AND (cc = "01")AND (dly_C = "0100") THEN
283
```

```
284                   false_alm <= "001101";
285             ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
286                   AND (f_num = "10") AND (cc = "10")AND (dly_C = "0101") THEN
287
288                   false_alm <= "001110";
289
290             ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
291                   AND (f_num = "10") AND (cc = "01")AND (dly_C = "0110") THEN
292
293                   false_alm <= "001111";
294             ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
295                   AND (f_num = "10") AND (cc = "10")AND (dly_C = "0111") THEN
296
297                   false_alm <= "010000";
298
299             ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
300                   AND (f_num = "10") AND (cc = "01")AND (dly_C = "1000") THEN
301
302                   false_alm <= "010001";
303             ELSIF (countSR = "0001") AND (wrongslot_flg = "0000")
304                   AND (f_num = "10") AND (cc = "10")AND (dly_C = "1001") THEN
305
306                   false_alm <= "010010";
307
308             ELSIF (countSR = "0010") AND (false_alm > "0000")
309                   AND (o_f = '1') AND (cc = "01")THEN
310
311                   false_alm <= "010011";
312                   f_alrm    <= '1';
313                   wrongslot_det <= "00";
314
315             ELSIF (countSR = "0010") AND (false_alm > "0000")
316                   AND (o_f = '0') AND (cc = "10")THEN
317
318                   false_alm <= "010100";
319                   f_alrm    <= '1';
320                   wrongslot_det <= "00";
321
322             ELSIF (countSR = "0010") AND (false_alm > "0000")
323                   AND (o_f = '1') AND (cc = "10")THEN
324
325                   false_alm <= false_alm;
326                   f_alrm    <= '1';
327
328             ELSIF (countSR = "0010") AND (false_alm > "0000")
329                   AND (o_f = '0') AND (cc = "01")THEN
330
331                   false_alm <= false_alm;
332                   f_alrm    <= '1';
333
334
```

```
335         ELSIF (false_alm > "000000") AND (dly_SR = "0001")
336               AND (countC = "0001") AND (f_num = "01") THEN
337
338               false_alm <= false_alm;
339               f_alrm    <= '1';
340               w_slotR   <= '0';
341               wrongslot_flg <= "0001";
342
343         ELSIF (false_alm > "000000") AND (dly_SR = "0001")
344               AND (countC = "0001") AND (f_num = "10") THEN
345
346               false_alm <= false_alm;
347               f_alrm    <= '1';
348               w_slotR   <= '0';
349               wrongslot_flg <= "0010";
350
351         ELSIF (countC >= "0010") AND (dly_SR = "0001")
352               AND (wrongslot_flg = "0001")THEN
353         --err of 01C
354
355                 wrongslot_flg   <= wrongslot_flg;
356                 w_slotR         <= '0';
357                 wrongslotR_flg  <= "00000";
358                 false_alm <= "000000";
359                 f_alrm  <= '0';
360
361         ELSIF (countC >= "0010") AND (dly_SR = "0001")
362               AND (wrongslot_flg = "0010") THEN
363
364                 wrongslot_flg   <= wrongslot_flg;
365                 w_slotR         <= '0';
366                 wrongslotR_flg  <= "00000";
367                 false_alm <= "000000";
368                 f_alrm  <= '0';
369
370         ELSIF (wrongslot_det = "01") AND (countC = "0001")
371               AND (dly_SR >= "0010") THEN
372         --err of 10C & 01C and Corr
373
374
375                 wrongslot_flg   <= "0010";
376                 w_slotR         <= '1';
377                 wrongslotR_flg  <= "00100";
378                 wrongslot_det <= "00";
379
380         ELSIF (wrongslot_det = "10") AND (countC = "0001")
381               AND (dly_SR >= "0010") THEN
382         --err of 10C & 01C and Corr
383
384
385                 wrongslot_flg   <= "0001";
386                 w_slotR         <= '1';
387                 wrongslotR_flg  <= "00100";
388                 wrongslot_det <= "00";
389
```

```
390         ELSIF (countC > "0000") AND (dly_SR >= "0010")
391               AND (wrongslot_flg = "0001")THEN
392         --err of 01C
393                 wrongslot_flg   <= wrongslot_flg;
394                 w_slotR         <= '0';
395                 wrongslotR_flg  <= "00000";
396                 false_alm <= "000000";
397                 f_alrm  <= '0';
398
399         ELSIF (countC > "0000") AND (dly_SR >= "0010")
400               AND (wrongslot_flg = "0010")THEN
401         --err of 01C
402                 wrongslot_flg   <= wrongslot_flg;
403                 w_slotR         <= '0';
404                 wrongslotR_flg  <= "00000";
405                 false_alm <= "000000";
406                 f_alrm  <= '0';
407
408         ELSIF (wrongslot_flg    = "0001") AND (countSR = "0001")
409               AND (dly_C = "0001") AND (cc = "01") THEN
410         --err of 01C 1 iCorrect
411
412                 wrongslot_flg   <= "0000";
413                 w_slotR         <= '1';
414                 wrongslotR_flg  <= "01010";
415                 false_alm <= "000000";
416                 f_alrm  <= '0';
417
418         ELSIF (wrongslot_flg    = "0001") AND (countSR = "0001")
419               AND (dly_C = "0010") AND (cc = "10") THEN
420         --err of 01C 2 iCorrect
421
422                 wrongslot_flg   <= "0000";
423                 w_slotR         <= '1';
424                 wrongslotR_flg  <= "01011";
425                 false_alm <= "000000";
426                 f_alrm  <= '0';
427
428         ELSIF (wrongslot_flg    = "0001") AND (countSR = "0001")
429               AND (dly_C = "0011") AND (cc = "01") THEN
430         --err of 01C 3 iCorrect
431
432                 wrongslot_flg   <= "0000";
433                 w_slotR         <= '1';
434                 wrongslotR_flg  <= "01100";
435                 false_alm <= "000000";
436                 f_alrm  <= '0';
437
438         ELSIF (wrongslot_flg    = "0001") AND (countSR = "0001")
439               AND (dly_C = "0100") AND (cc = "10") THEN
440         --err of 01C 4 iCorrect
441
442                 wrongslot_flg   <= "0000";
443                 w_slotR         <= '1';
444                 wrongslotR_flg  <= "01101";
445                 false_alm <= "000000";
446                 f_alrm  <= '0';
```

```
447
448         ELSIF (wrongslot_flg    = "0001") AND (countSR = "0001")
449               AND (dly_C = "0101") AND (cc = "01") THEN
450         --err of 01C 5 iCorrect
451
452                 wrongslot_flg   <= "0000";
453                 w_slotR         <= '1';
454                 wrongslotR_flg  <= "01110";
455                 false_alm <= "000000";
456                 f_alrm  <= '0';
457
458         ELSIF (wrongslot_flg    = "0001") AND (countSR = "0001")
459               AND (dly_C = "0110") AND (cc = "10") THEN
460         --err of 01C 6 iCorrect
461
462                 wrongslot_flg   <= "0000";
463                 w_slotR         <= '1';
464                 wrongslotR_flg  <= "01111";
465                 false_alm <= "000000";
466                 f_alrm  <= '0';
467
468         ELSIF (wrongslot_flg    = "0001") AND (countSR = "0001")
469               AND (dly_C = "0111") AND (cc = "01") THEN
470         --err of 01C 7 iCorrect
471
472                 wrongslot_flg   <= "0000";
473                 w_slotR         <= '1';
474                 wrongslotR_flg  <= "10000";
475                 false_alm <= "000000";
476                 f_alrm  <= '0';
477
478         ELSIF (wrongslot_flg    = "0001") AND (countSR = "0001")
479               AND (dly_C = "1000") AND (cc = "10") THEN
480         --err of 01C 8 iCorrect
481
482                 wrongslot_flg   <= "0000";
483                 w_slotR         <= '1';
484                 wrongslotR_flg  <= "10001";
485                 false_alm <= "000000";
486                 f_alrm  <= '0';
487
488         ELSIF (wrongslot_flg    = "0001") AND (countSR = "0001")
489               AND (dly_C = "1001") AND (cc = "01") THEN
490         --err of 01C 9 iCorrect
491
492                 wrongslot_flg   <= "0000";
493                 w_slotR         <= '1';
494                 wrongslotR_flg  <= "10010";
495                 false_alm <= "000000";
496                 f_alrm  <= '0';
497
498
```

```
499         ELSIF (wrongslot_flg    = "0010") AND (countSR = "0001")
500               AND (dly_C = "0001") AND (cc = "10") THEN
501         --err of 10C 1 iCorrect
502
503                 wrongslot_flg   <= "0000";
504                 w_slotR         <= '1';
505                 wrongslotR_flg  <= "10011";
506                 false_alm <= "000000";
507                 f_alrm  <= '0';
508
509
510         ELSIF (wrongslot_flg    = "0010") AND (countSR = "0001")
511               AND (dly_C = "0010") AND (cc = "01") THEN
512         --err of 10C 2 iCorrect
513
514                 wrongslot_flg   <= "0000";
515                 w_slotR         <= '1';
516                 wrongslotR_flg  <= "10100";
517                 false_alm <= "000000";
518                 f_alrm  <= '0';
519
520         ELSIF (wrongslot_flg    = "0010") AND (countSR = "0001")
521               AND (dly_C = "0011") AND (cc = "10") THEN
522         --err of 10C 3 iCorrect
523
524                 wrongslot_flg   <= "0000";
525                 w_slotR         <= '1';
526                 wrongslotR_flg  <= "10101";
527                 false_alm <= "000000";
528                 f_alrm  <= '0';
529
530         ELSIF (wrongslot_flg    = "0010") AND (countSR = "0001")
531               AND (dly_C = "0100") AND (cc = "01") THEN
532         --err of 10C 4 iCorrect
533
534                 wrongslot_flg   <= "0000";
535                 w_slotR         <= '1';
536                 wrongslotR_flg  <= "10110";
537                 false_alm <= "000000";
538                 f_alrm  <= '0';
539
540         ELSIF (wrongslot_flg    = "0010") AND (countSR = "0001")
541               AND (dly_C = "0101") AND (cc = "10") THEN
542         --err of 10C 5 iCorrect
543
544                 wrongslot_flg   <= "0000";
545                 w_slotR         <= '1';
546                 wrongslotR_flg  <= "10111";
547                 false_alm <= "000000";
548                 f_alrm  <= '0';
549
550         ELSIF (wrongslot_flg    = "0010") AND (countSR = "0001")
551               AND (dly_C = "0110") AND (cc = "01") THEN
552         --err of 10C 6 iCorrect
553
```

```
554                 wrongslot_flg   <= "0000";
555                 w_slotR         <= '1';
556                 wrongslotR_flg  <= "11000";
557                 false_alm <= "000000";
558                 f_alrm  <= '0';
559
560           ELSIF (wrongslot_flg    = "0010") AND (countSR = "0001")
561                 AND (dly_C = "0111") AND (cc = "10") THEN
562           --err of 10C 7 iCorrect
563
564                 wrongslot_flg   <= "0000";
565                 w_slotR         <= '1';
566                 wrongslotR_flg  <= "11001";
567                 false_alm <= "000000";
568                 f_alrm  <= '0';
569
570
571           ELSIF (wrongslot_flg    = "0010") AND (countSR = "0001")
572                 AND (dly_C = "1000") AND (cc = "01") THEN
573           --err of 10C 8 iCorrect
574
575                 wrongslot_flg   <= "0000";
576                 w_slotR         <= '1';
577                 wrongslotR_flg  <= "11010";
578                 false_alm <= "000000";
579                 f_alrm  <= '0';
580
581           ELSIF (wrongslot_flg    = "0010") AND (countSR = "0001")
582                 AND (dly_C = "1001") AND (cc = "10") THEN
583           --err of 10C 9 iCorrect
584
585                 wrongslot_flg   <= "0000";
586                 w_slotR         <= '1';
587                 wrongslotR_flg  <= "11011";
588                 false_alm <= "000000";
589                 f_alrm  <= '0';
590
591           ELSIF (wrongslot_det = "01") AND (cc = "10")
592                 AND (countSR >= "0011") THEN
593           --err of 100 sr >= 3
594
595
596                 wrongslot_flg   <= "1000";
597                 wrongslot_det   <= "00";
598                 w_slot          <= '1';
599
600           ELSIF (wrongslot_det = "10") AND (cc = "01")
601                 AND (countSR >= "0011") THEN
602           --err of 011 sr >= 3
603
604
605                 wrongslot_flg   <= "1000";
606                 wrongslot_det   <= "00";
607                 w_slot          <= '1';
608
```

```
609
610
611         ELSIF (countSR >= "0010")AND (cc = "10")
612               AND (o_f = '0') AND (wrongslot_det = "00")THEN
613         --err bit of 0
614
615
616                 wrongslot_det   <= "01";
617                 w_slotR         <= '0';
618                 wrongslotR_flg  <= "00000";
619
620         ELSIF (countSR >= "0010")AND (cc = "01")
621               AND (o_f = '1')AND (wrongslot_det = "00")THEN
622         --err bit of 1
623
624
625                 wrongslot_det   <= "10";
626                 w_slotR         <= '0';
627                 wrongslotR_flg  <= "00000";
628
629         ELSE
630                 wrongslot_det   <= "00";
631                 wrongslot_flg   <= "0000";
632                 wrongslotR_flg  <= "00000";
633                 w_slot          <= '0';
634                 w_slotR         <= '0';
635                 false_alm <= "000000";
636                 f_alrm      <= '0';
637
638
639         END IF;
640
641     END IF;
642     OP_ws <= w_slot;
643     OP_wsr <= w_slotR;
644     OP_fa <= f_alrm;
645
646
647
648     END PROCESS;
649
650     PROCESS
651
652     BEGIN
653
654     WAIT UNTIL (Clk' EVENT AND Clk = '1');
655
656     IF Reset = '0' THEN
657
658             regOP1  <= "00000000000000000000000000000000000000000000000000";
659             regOP2  <= "00000000000000000000000000000000000000000000000000";
660
661     ELSIF Reset = '1' THEN
662
663                 regOP1  <= IP1 & regOP1 (47 downto 2);
664                 regOP2  <= IP1 & regOP2 (47 downto 2);
665
```

```
666                 IF (w_slot = '1') THEN
667
668                 CASE wrongslot_flg IS
669
670                 WHEN "0110" => regOP1  <= IP1 & regOP1  (n-1 downto 42) &
671                  "10" & regOP1  (39 downto 2);
672                 WHEN "0101" => regOP1  <= IP1 & regOP1  (n-1 downto 42) &
673                  "01" & regOP1  (39 downto 2);
674                 WHEN "1000" => regOP1  <= IP1 & regOP1  (n-1 downto 42) &
675                  "00" & regOP1  (39 downto 2);
676                 WHEN OTHERS => regOP1  <= regOP1;
677
678                 END CASE;
679
680
681                 ELSIF (w_slotR = '1') THEN
682
683
684                 CASE wrongslotR_flg IS
685
686                 WHEN "00100" => regOP1  <= IP1 & regOP1  (n-1 downto 42) &
687                  "00" & regOP1  (39 downto 2);
688                                 regOP2  <= IP1 & regOP1 (n-1 downto 2);
689                 WHEN "01010" => regOP1  <= IP1 & regOP2  (n-1 downto 40) &
690                  "10" & regOP2  (37 downto 2);
691                 WHEN "01011" => regOP1  <= IP1 & regOP2  (n-1 downto 38) &
692                  "10" & regOP2  (35 downto 2);
693                 WHEN "01100" => regOP1  <= IP1 & regOP2  (n-1 downto 36) &
694                  "10" & regOP2  (33 downto 2);
695                 WHEN "01101" => regOP1  <= IP1 & regOP2  (n-1 downto 34) &
696                  "10" & regOP2  (31 downto 2);
697                 WHEN "01110" => regOP1  <= IP1 & regOP2  (n-1 downto 32) &
698                  "10" & regOP2  (29 downto 2);
699                 WHEN "01111" => regOP1  <= IP1 & regOP2  (n-1 downto 30) &
700                  "10" & regOP2  (27 downto 2);
701                 WHEN "10000" => regOP1  <= IP1 & regOP2  (n-1 downto 28) &
702                  "10" & regOP2  (25 downto 2);
703                 WHEN "10001" => regOP1  <= IP1 & regOP2  (n-1 downto 26) &
704                  "10" & regOP2  (23 downto 2);
705                 WHEN "10010" => regOP1  <= IP1 & regOP2  (n-1 downto 24) &
706                  "10" & regOP2  (21 downto 2);
707                 WHEN "10011" => regOP1  <= IP1 & regOP2  (n-1 downto 40) &
708                  "01" & regOP2  (37 downto 2);
709                 WHEN "10100" => regOP1  <= IP1 & regOP2  (n-1 downto 38) &
710                  "01" & regOP2  (35 downto 2);
711                 WHEN "10101" => regOP1  <= IP1 & regOP2  (n-1 downto 36) &
712                  "01" & regOP2  (33 downto 2);
713                 WHEN "10110" => regOP1  <= IP1 & regOP2  (n-1 downto 34) &
714                  "01" & regOP2  (31 downto 2);
715                 WHEN "10111" => regOP1  <= IP1 & regOP2  (n-1 downto 32) &
716                  "01" & regOP2  (29 downto 2);
717                 WHEN "11000" => regOP1  <= IP1 & regOP2  (n-1 downto 30) &
718                  "01" & regOP2  (27 downto 2);
719                 WHEN "11001" => regOP1  <= IP1 & regOP2  (n-1 downto 28) &
720                  "01" & regOP2  (25 downto 2);
721                 WHEN "11010" => regOP1  <= IP1 & regOP2  (n-1 downto 26) &
722                  "01" & regOP2  (23 downto 2);
```

```
723                 WHEN "11011" => regOP1  <= IP1 & regOP2  (n-1 downto 24) &
724                  "01" & regOP2  (21 downto 2);
725                 WHEN OTHERS  => regOP1  <= regOP1;
726
727                 END CASE;
728
729
730                 ELSIF (f_alrm = '1') THEN
731
732                 regOP2  <= IP1 & regOP1 (n-1 downto 2);
733
734                 CASE false_alm IS
735
736                 WHEN "010011" =>   regOP1  <= IP1 & regOP1  (n-1 downto 42) &
737                  "01" & regOP1  (39 downto 2);
738                 WHEN "010100" =>   regOP1  <= IP1 & regOP1  (n-1 downto 42) &
739                  "10" & regOP1  (39 downto 2);
740                 WHEN "000001" =>   regOP1  <= IP1 & regOP1  (n-1 downto 40) &
741                  "01" & regOP1  (37 downto 2);
742                 WHEN "000010" =>   regOP1  <= IP1 & regOP1  (n-1 downto 40) &
743                  "10" & regOP1  (37 downto 2);
744                 WHEN "000011" =>   regOP1  <= IP1 & regOP1  (n-1 downto 38) &
745                  "10" & regOP1  (35 downto 2);
746                 WHEN "000100" =>   regOP1  <= IP1 & regOP1  (n-1 downto 38) &
747                  "01" & regOP1  (35 downto 2);
748                 WHEN "000101" =>   regOP1  <= IP1 & regOP1  (n-1 downto 36) &
749                  "01" & regOP1  (33 downto 2);
750                 WHEN "000110" =>   regOP1  <= IP1 & regOP1  (n-1 downto 36) &
751                  "10" & regOP1  (33 downto 2);
752                 WHEN "000111" =>   regOP1  <= IP1 & regOP1  (n-1 downto 34) &
753                  "10" & regOP1  (31 downto 2);
754                 WHEN "001000" =>   regOP1  <= IP1 & regOP1  (n-1 downto 34) &
755                  "01" & regOP1  (31 downto 2);
756                 WHEN "001001" =>   regOP1  <= IP1 & regOP1  (n-1 downto 32) &
757                  "01" & regOP1  (29 downto 2);
758                 WHEN "001010" =>   regOP1  <= IP1 & regOP1  (n-1 downto 40) &
759                  "10" & regOP1  (37 downto 2);
760                 WHEN "001011" =>   regOP1  <= IP1 & regOP1  (n-1 downto 40) &
761                  "01" & regOP1  (37 downto 2);
762                 WHEN "001100" =>   regOP1  <= IP1 & regOP1  (n-1 downto 38) &
763                  "01" & regOP1  (35 downto 2);
764                 WHEN "001101" =>   regOP1  <= IP1 & regOP1  (n-1 downto 38) &
765                  "10" & regOP1  (35 downto 2);
766                 WHEN "001110" =>   regOP1  <= IP1 & regOP1  (n-1 downto 36) &
767                  "10" & regOP1  (33 downto 2);
768                 WHEN "001111" =>   regOP1  <= IP1 & regOP1  (n-1 downto 36) &
769                  "01" & regOP1  (33 downto 2);
770                 WHEN "010000" =>   regOP1  <= IP1 & regOP1  (n-1 downto 34) &
771                  "01" & regOP1  (31 downto 2);
772                 WHEN "010001" =>   regOP1  <= IP1 & regOP1  (n-1 downto 34) &
773                  "10" & regOP1  (31 downto 2);
774                 WHEN "010010" =>   regOP1  <= IP1 & regOP1  (n-1 downto 32) &
775                 "10" & regOP1  (29 downto 2);
776                 WHEN OTHERS   =>   regOP1  <= regOP1;
777
778                 END CASE;
779
```

```
780
781                 END IF;
782
783         END IF;
784
785
786
787
788         END PROCESS;
789
790
791         PROCESS
792         BEGIN
793
794         WAIT UNTIL (Clk2'event and Clk2='0');
795
796                 IF (Reset = '0') THEN
797
798                 shift_reg3  <= "00";
799
800                 ELSE IF (load_D3 = '1') THEN
801
802                 shift_reg3  <= regOP1 (1 downto 0);
803
804                 ELSE IF(Reset = '1' ) THEN
805
806                 shift_reg3  <= shift_reg3  (0) & shift_reg3  (1);
807
808                 END IF;
809                 END IF;
810                 END IF;
811
812                 OP_F <= shift_reg3  (1);
813
814         END PROCESS;
815
816
817 END func;
```

Appendix 3.5: Load Data from MLSD Block

```
1  --K Mostafa--
2  --University of Huddersfield--
3  --DuoPPM Project--
4  --DuoPPM Data Loading--
5  --Load Data From MLSD Block--
6
7  library ieee;
8  use ieee.std_logic_1164.all;
9  use ieee.std_logic_arith.all;
10 use ieee.std_logic_unsigned.all;
11
12 entity Para_load is
13
14     port(signal Clk2            :   IN std_logic;
15          signal Reset           :   IN std_logic;
16          signal load_D3     :   OUT std_logic);
17
18 end Para_load;
19
20 architecture func of Para_load is
21
22 SIGNAL ctrl2        :STD_LOGIC_VECTOR (1 DOWNTO 0):="01";
23 SIGNAL regload3     :std_logic := '0';
24
25 BEGIN
26
27         PROCESS (Clk2, Reset, ctrl2)
28
29         BEGIN
30
31           IF (Reset = '0') THEN
32
33           ctrl2 <= "01";
34
35           ELSE IF(Clk2'event and Clk2='0') THEN
36
```

```
37            ctrl2 <= (ctrl2(0))& (ctrl2(1));
38
39            END IF;
40            END IF;
41
42          END PROCESS;
43
44          PROCESS
45
46          BEGIN
47
48          WAIT UNTIL (Clk2'EVENT AND Clk2 = '1');
49          IF(ctrl2 = "10" ) THEN
50          regload3 <= '1';
51
52          ELSE
53          regload3 <= '0';
54
55          END IF;
56
57          load_D3 <= regload3;
58
59          END PROCESS;
60
61  END func;
```

Appendix 3.6: SIPO Two-Bit for Decoder

```
1  --K Mostafa--
2  --University of Huddersfield--
3  --DuoPPM Project--
4  --SIPO Two Bit for Decoder--
5
6  LIBRARY IEEE;
7  USE IEEE.std_logic_1164.ALL;
8  USE IEEE.std_logic_arith.ALL;
9  USE IEEE.std_logic_unsigned.ALL;
10
11
12 ENTITY duoppm_decoder is
13
14     PORT(SIGNAL Clk_duppm          :   IN std_logic;
15          SIGNAL Reset              :   IN std_logic;
16          SIGNAL duoppm             :   IN std_logic;
17          SIGNAL output             :   OUT std_logic_vector (1 DOWNTO 0))
18
19 END duoppm_decoder;
20
21
22 ARCHITECTURE behavior OF duoppm_decoder IS
23
24   SIGNAL ctrl       : std_logic_vector (1 DOWNTO 0):="01";
25   SIGNAL duo_bit    : std_logic;
26   SIGNAL one_zero   : std_logic_vector (1 DOWNTO 0):="00";
27
28 BEGIN
29
30     PROCESS
31     BEGIN
32         WAIT UNTIL (Clk_duppm' EVENT AND Clk_duppm = '1');
33
34             IF (Reset = '0') THEN
35             duo_bit <= '0';
36
37             ELSE
38             duo_bit <= duoppm;
39             END IF;
40
41     one_zero <= (one_zero (0)& duo_bit);
42     ctrl <= (ctrl(0)&ctrl(1));
43
```

```
44      END PROCESS;
45
46      PROCESS
47      BEGIN
48          WAIT UNTIL (Clk_duppm' EVENT AND Clk_duppm = '0');
49
50          IF (Reset = '0') THEN
51          output  <= "00";
52
53          ELSIF (Reset = '1') THEN
54          IF (ctrl="10") THEN
55
56          output <= one_zero;
57
58          END IF;
59          END IF;
60
61      END PROCESS;
62  END behavior;
```

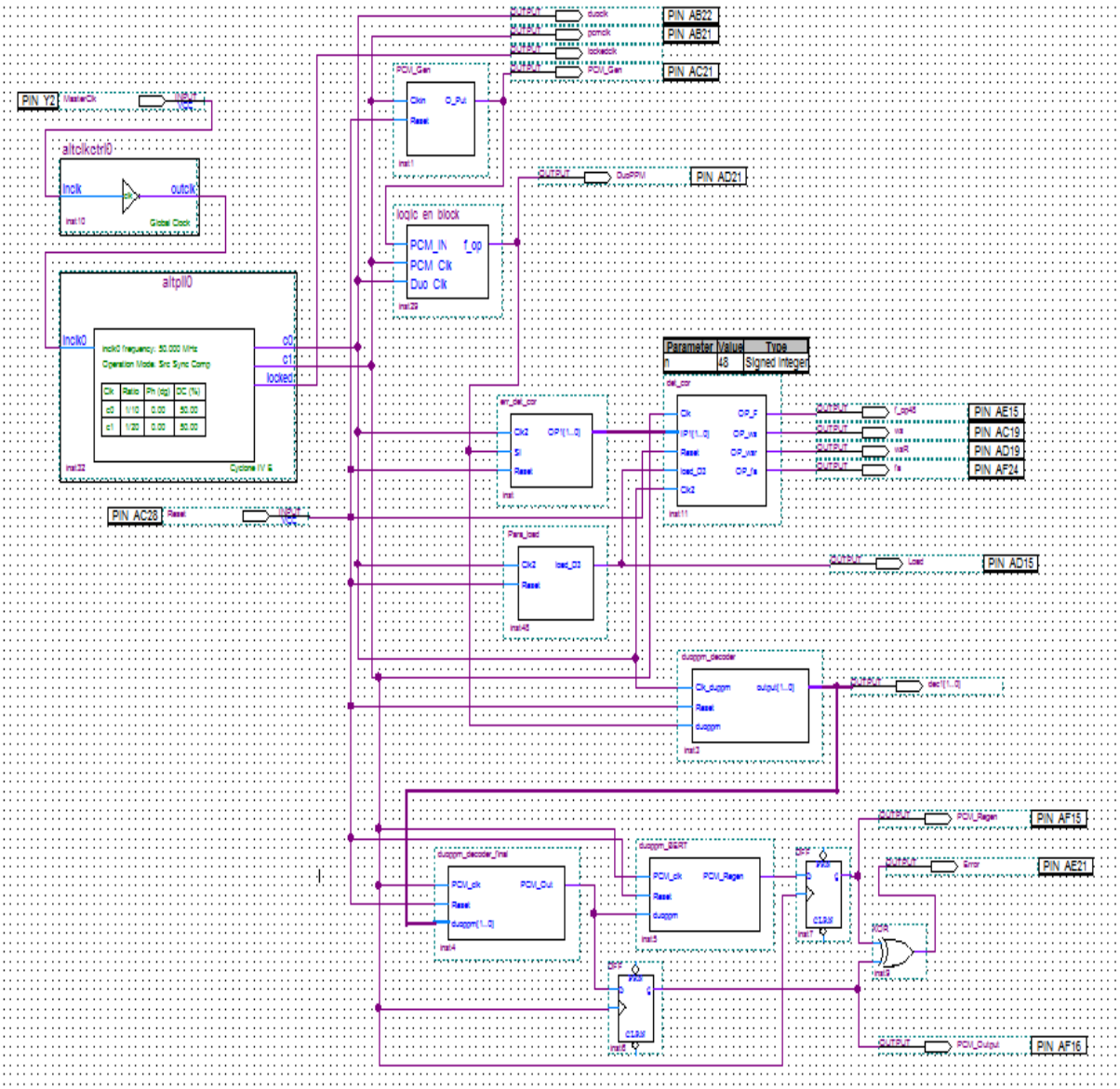
Appendix 3.7: DuoPPM to PCM Decoder

```
1
2  --K Mostafa--
3  --University of Huddersfield--
4  --DuoPPM Project--
5  --DuoPPM to PCM Decoder--
6
7  LIBRARY IEEE;
8  USE IEEE.std_logic_1164.ALL;
9  USE IEEE.std_logic_arith.ALL;
10 USE IEEE.std_logic_unsigned.ALL;
11
12 ENTITY duoppm_decoder_final is
13
14     PORT(SIGNAL PCM_clk             :   IN std_logic;
15          SIGNAL Reset               :   IN std_logic;
16          SIGNAL duoppm              :   IN std_logic_vector (1 DOWNTO 0);
17          SIGNAL PCM_Out             :   OUT std_logic);
18
19 END duoppm_decoder_final;
20
21
22 ARCHITECTURE bhv OF duoppm_decoder_final IS
23
24     SIGNAL Start_temp   : std_logic := '1';
25
26     BEGIN
27     PROCESS
28
29         BEGIN
30         WAIT UNTIL (PCM_clk' EVENT AND PCM_clk = '1');
31
32         IF (Reset = '0') THEN
33
34         Start_temp <= '1';
35
36         ELSIF (Reset = '1') THEN
37
38           IF(duoppm = "00")and(Start_temp = '1')THEN
39            Start_temp <= '0';
40            PCM_out <= Start_temp;
41
42           ELSIF(duoppm = "00")and(Start_temp = '0')THEN
43            Start_temp <= '1';
44            PCM_out <= Start_temp;
45
46           ELSIF(duoppm = "01")THEN
47            Start_temp <= '1';
48            PCM_out <= Start_temp;
49
50           ELSIF(duoppm = "10")THEN
51            Start_temp <= '0';
52            PCM_out <= Start_temp;
53
54           END IF;
55           END IF;
56
57 END PROCESS;
```

Appendix 3.7: PRBS PCM Regenerator from Received PCM for Bit Error Rate Test

```
1
2  --K Mostafa--
3  --University of Huddersfield--
4  --DuoPPM Project--
5  --PRBS PCM Regenerator from Received PCM--
6
7  LIBRARY IEEE;
8  USE IEEE.std_logic_1164.ALL;
9  USE IEEE.std_logic_arith.ALL;
10 USE IEEE.std_logic_unsigned.ALL;
11
12 ENTITY duoppm_BERT is
13
14     PORT(SIGNAL PCM_clk             :   IN std_logic;
15          SIGNAL Reset               :   IN std_logic;
16          SIGNAL duoppm              :   IN std_logic;
17          SIGNAL PCM_Regen           :   OUT std_logic);
18
19 END duoppm_BERT;
20
21
22 ARCHITECTURE bhv OF duoppm_BERT IS
23
24     SIGNAL internal_reg1    : std_logic_vector (0 TO 7) := "00000000";
25     SIGNAL Tmp              : std_logic_vector (0 TO 7)  := "01111111";
26     SIGNAL load             : std_logic := '1';
27
28     BEGIN
29     PROCESS
30
31         VARIABLE first_tap  : std_logic;
32         VARIABLE second_tap : std_logic;
33         VARIABLE third_tap  : std_logic;
34
35         BEGIN
36         WAIT UNTIL (PCM_clk' EVENT AND PCM_clk = '0');
37
38         IF (Reset = '0') THEN
39
40         internal_reg1 <= "00000000";
41         Tmp           <= "01111111";
42         load          <= '1';
43
44         ELSIF (Reset = '1') THEN
45
46             IF (internal_reg1 = "11111111") THEN
47
48             load        <= '0';
49             first_tap   := Tmp (3) xor Tmp (4);
50             second_tap  := Tmp (5) xor Tmp (7);
51             third_tap   := first_tap xor second_tap;
52             Tmp         <= third_tap & Tmp (0 TO 6);
53
54             PCM_Regen <= Tmp (0);
55
56             ELSIF (load = '1') THEN
57             internal_reg1 <= internal_reg1 (1 TO 7) & duoppm;
58
59
60           END IF;
61           END IF;
62
63 END PROCESS;
64
65 END bhv;
```

Appendix 3.8: Schematic of the Complete DuoPPM System



Appendix 4

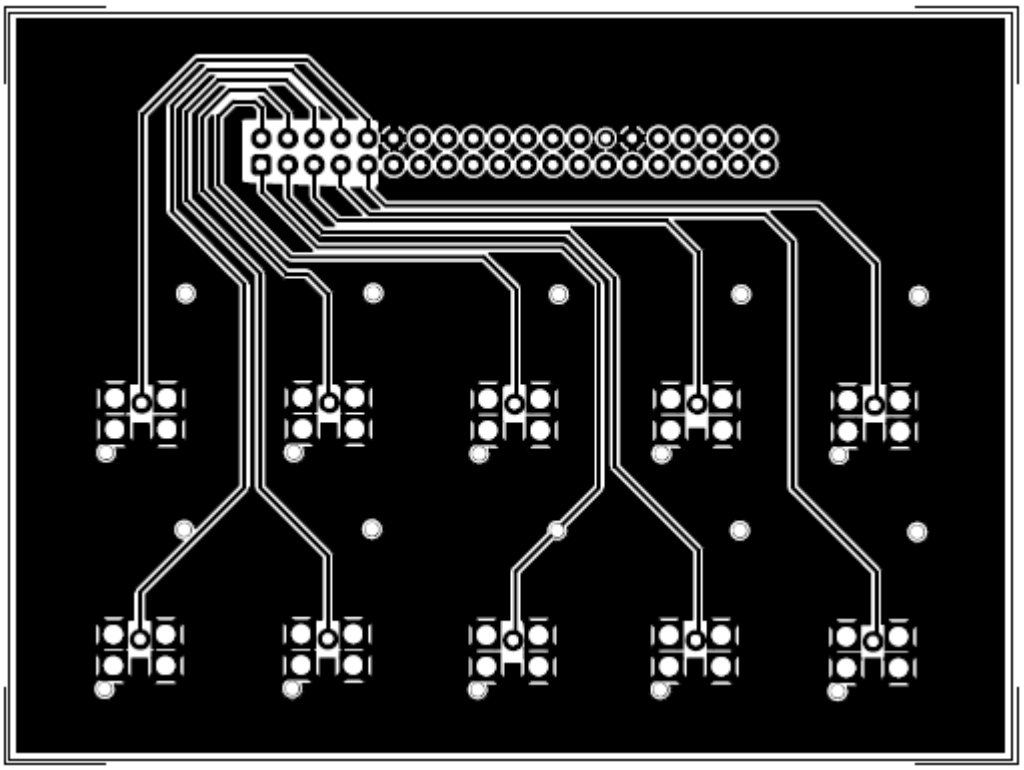


Fig. A4 – 4.1: PCB layout of the Interface Card for the FPGA GPIO interface.

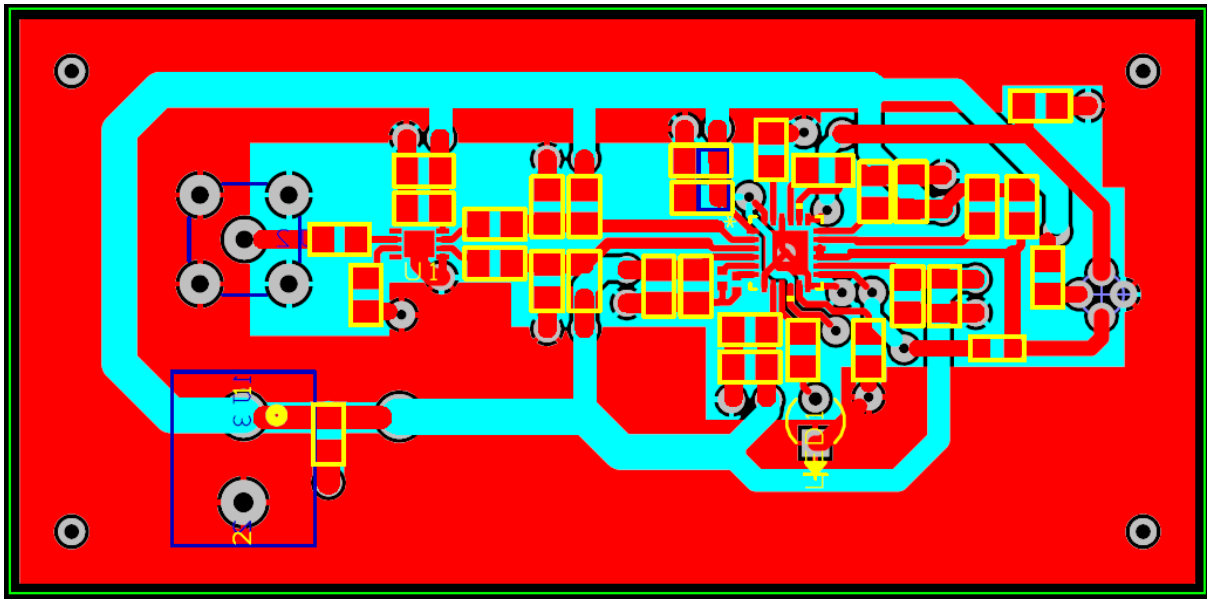


Fig. A4 – 4.2: VCSEL driver circuit board PCB layout.

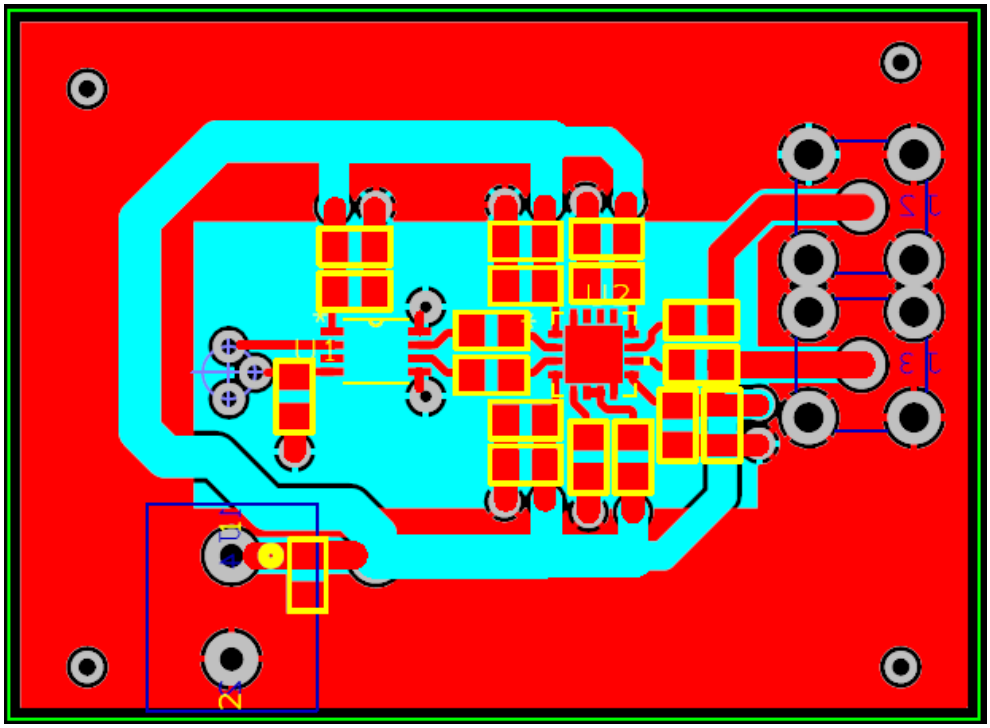


Fig. A4 – 4.3: Transimpedance preamplifier and limiting amplifier for the photodiode receiver PCB layout.

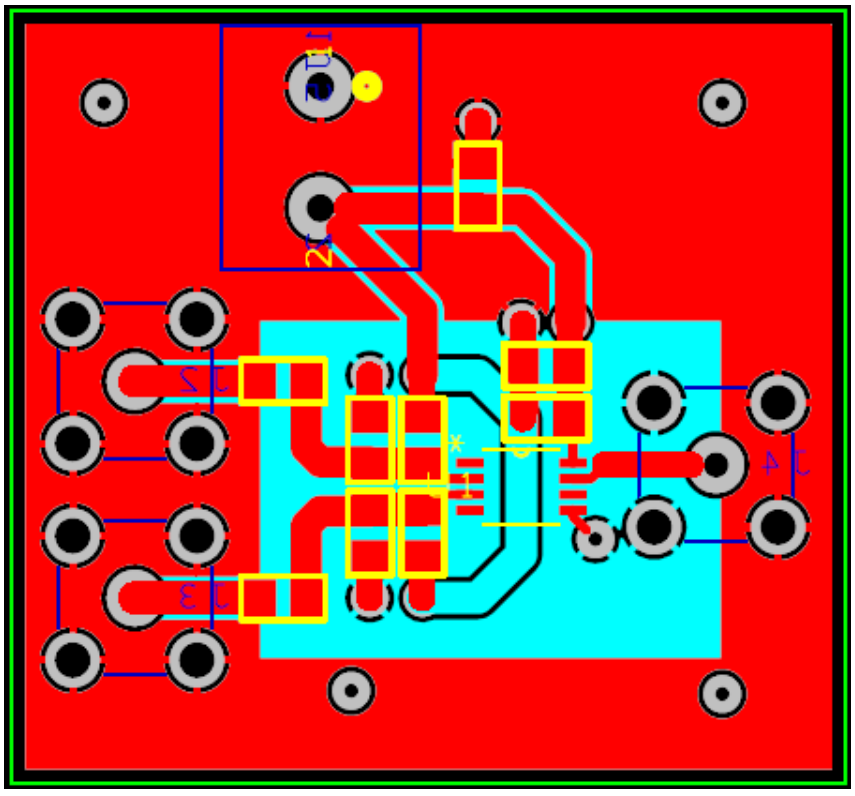


Fig. A4 – 4.4: PCB layout of Current Mode Logic (CML) to LVTTL voltage translator for receiver and FPGA development board interface matching.

Appendix 5

MLSD Theoretical Error Sequences.

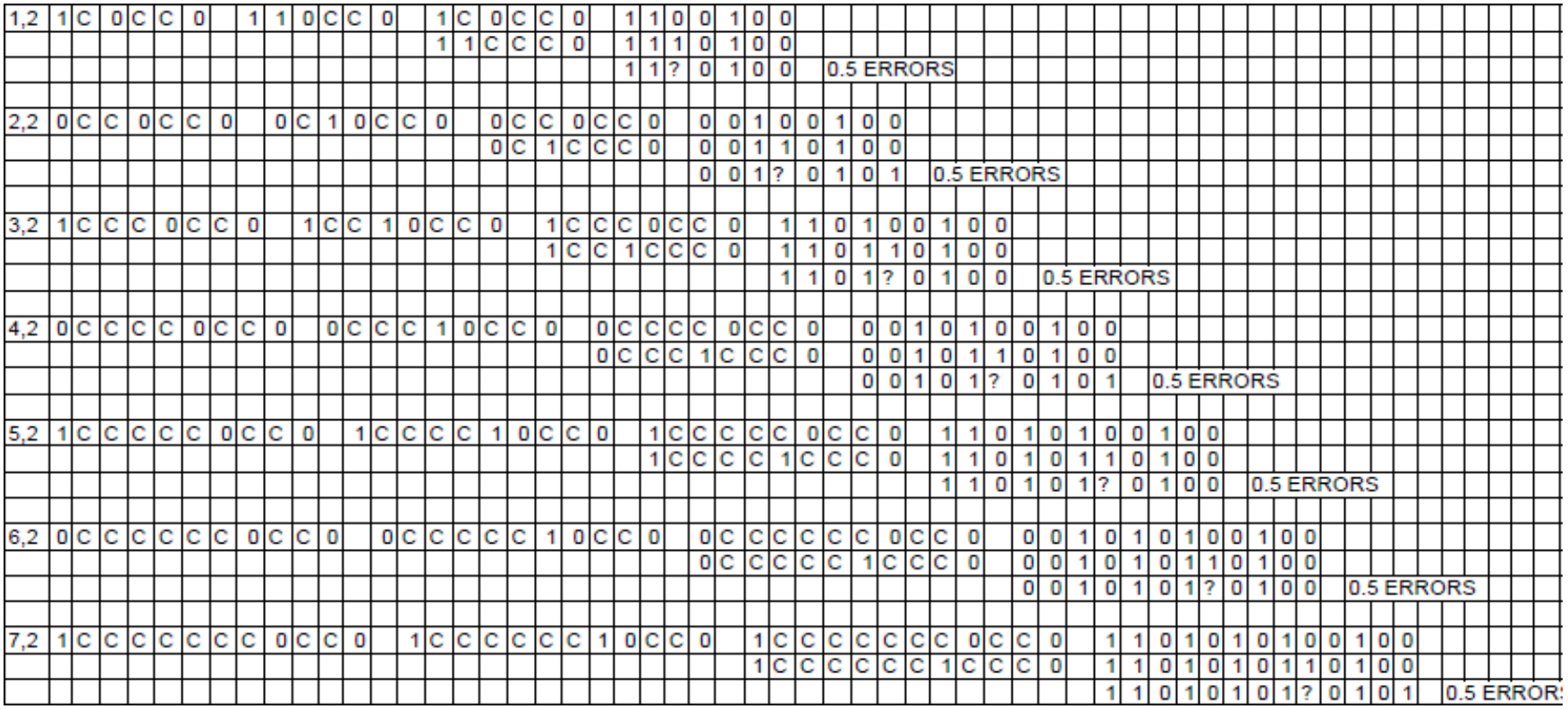
In order to implement the MLSD for DuoPPM, the MLSD algorithm for the possible errors were developed first. Using the devised algorithm, number of equivalent PCM errors in a given erroneous DuoPPM sequence can be calculated theoretically. Two key assumptions that have been made are: number of DuoPPM errors in any one data sequence is no more than 1 and maximum number of consecutive C (Change) symbols in any given sequence is 9. As it can be seen from the table in the following page, there is no need to devise equations for wrong-slot errors since all wrong-slot errors will be detected and corrected by the MLSD. It is also noticeable from the table that the erasure error of 1 and 0 in a sequence of same characteristics will result in same number of equivalent PCM errors. However, false alarm of same symbol (0 in 0C1 and 1 in 1C0) and different symbol (0 in 1C0 and 1 in 0C1) will result in different numbers of equivalent PCM errors which have been shown in the table in the next page. In the table for false alarm sequences, two columns for 'CODE': number in first column is number of Cs in the first sequence and number in second column is number of Cs in the second sequence. 'K' is the position in the second sequence where error has been detected.

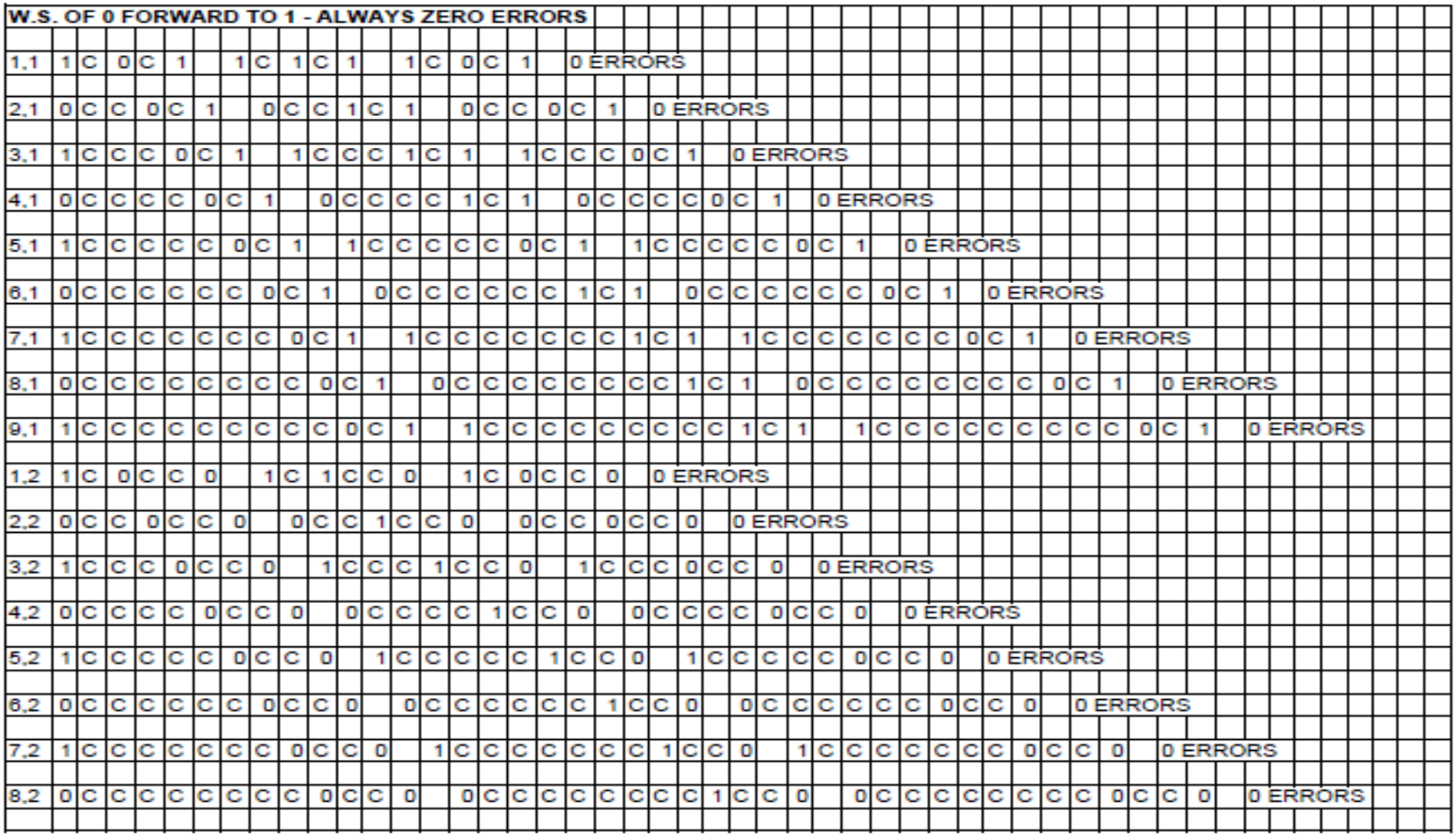
After the table in the following page, all possible correct sequences have been tabulated considering the aforementioned assumptions. Errors are injected in all possible positions in each sequence and MLSD has been used to resolve the erroneous sequences. Equivalent PCM errors have been found which conforms to the algorithms developed, thus confirming the validity of the MLSD.

ALL ERRORS IN xC + yC + 4 PCM BITS	
WRONG SLOTS	**PCM ERRORS**
0→1	0
0←1	0 - double pulse
ERASURE	
0	mod(x-y)/2
1	mod(x-y)/2
FALSE ALARM	(combs-1)/2
DIFFERENT	k ODD - combs=k+1
	k EVEN - combs=y-k+1
SAME	k ODD - combs=y-k+1
	k EVEN - combs=k+1

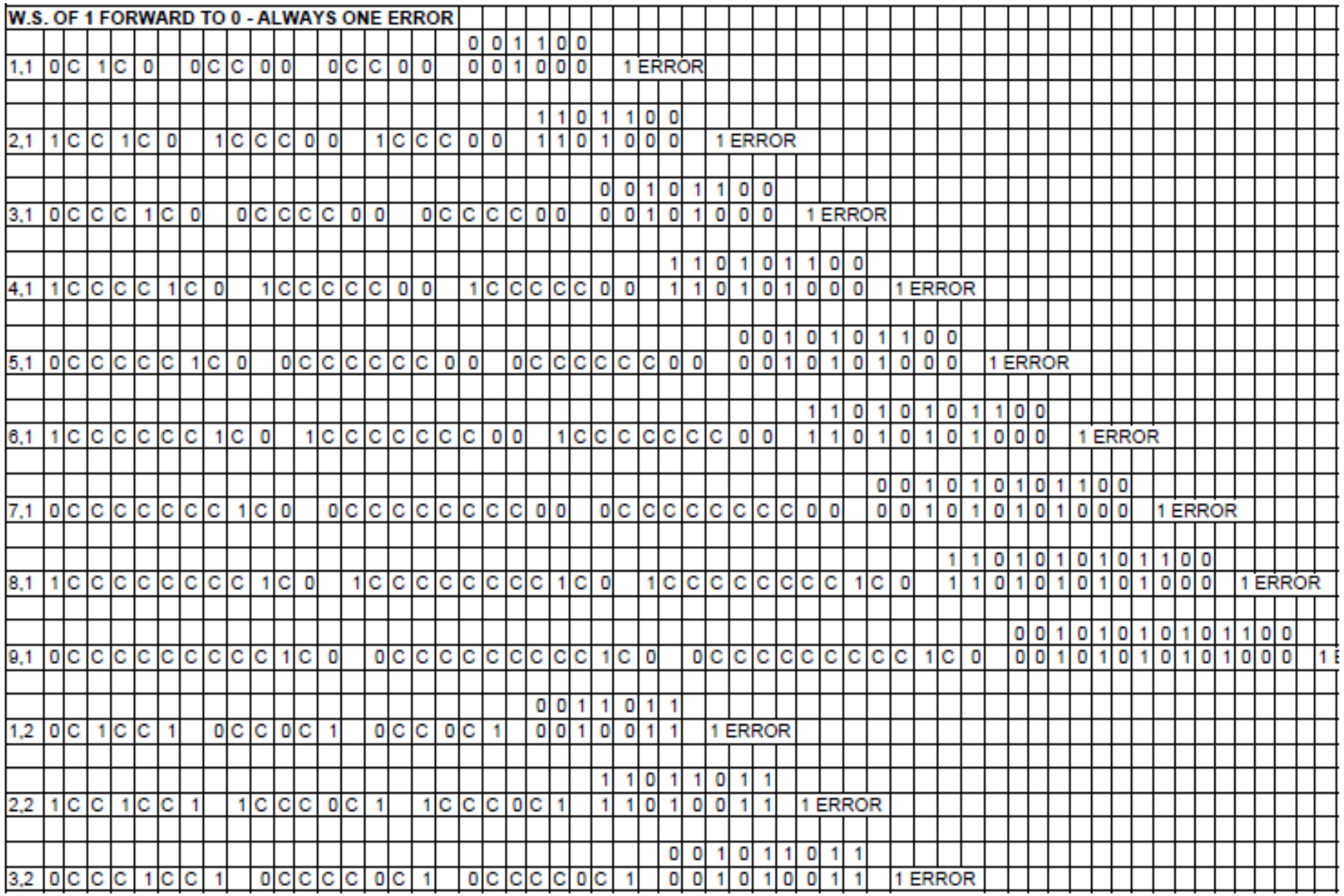
CODE						**k**					**F.A. DIFFERENT - 0 in 1C0 or 1 in 0C1**
			1	2	3	4	5	6	7	8	9	
1	1		2									k ODD - combs=k+1
1	2		2	1								k EVEN - combs=y-k+1
1	3		2	2	4							ERRORS=(combs-1)/2 in usual
1	4		2	3	4	1						
1	5		2	4	4	2	6					
1	6		2	5	4	3	6	1				
1	7		2	6	4	4	6	2	8			
1	8		2	7	4	5	6	3	8	1		
1	9		2	8	4	6	6	4	8	2	10	
CODE						**k**					**F.A. SAME - 0 in 0C1 or 1 in 1C0**
			1	2	3	4	5	6	7	8	9	
1	1		1									k ODD - combs=y-k+1
1	2		2	3								k EVEN - combs=k+1
1	3		3	3	1							ERRORS=(combs-1)/2 in usual
1	4		4	3	2	5						
1	5		5	3	3	5	1					
1	6		6	3	4	5	2	7				
1	7		7	3	5	5	3	7	1			
1	8		8	3	6	5	4	7	2	9		
1	9		9	3	7	5	5	7	3	9	1	

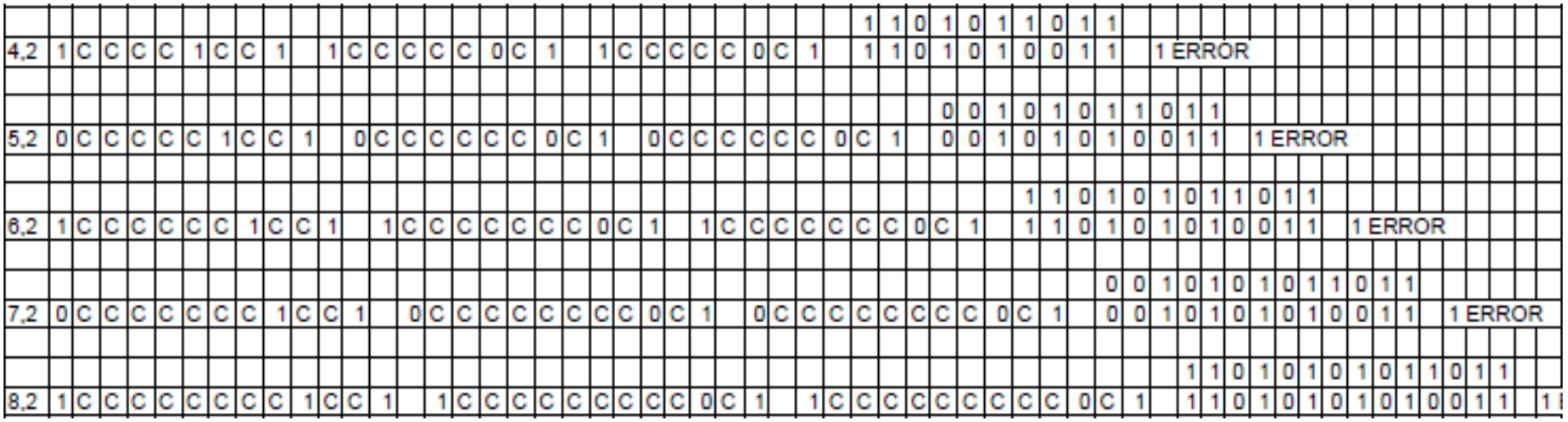
Table. A5 -5.1: Devised equations to calculate equivalent PCM errors in all possible erroneous sequences.

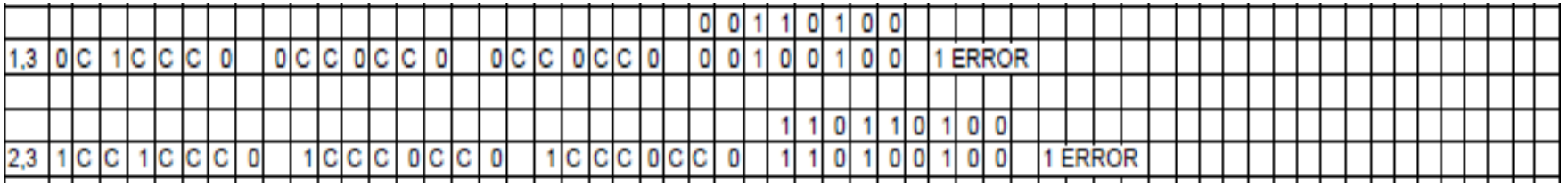

1,2
0.5 ERRORS
2,2
0.5 ERRORS
3,2
0.5 ERRORS
4,2
0.5 ERRORS
5,2
0.5 ERRORS
6,2
0.5 ERRORS
7,2
0.5 ERROR
1,3
0.5 ERRORS
2,3
0.5 ERRORS

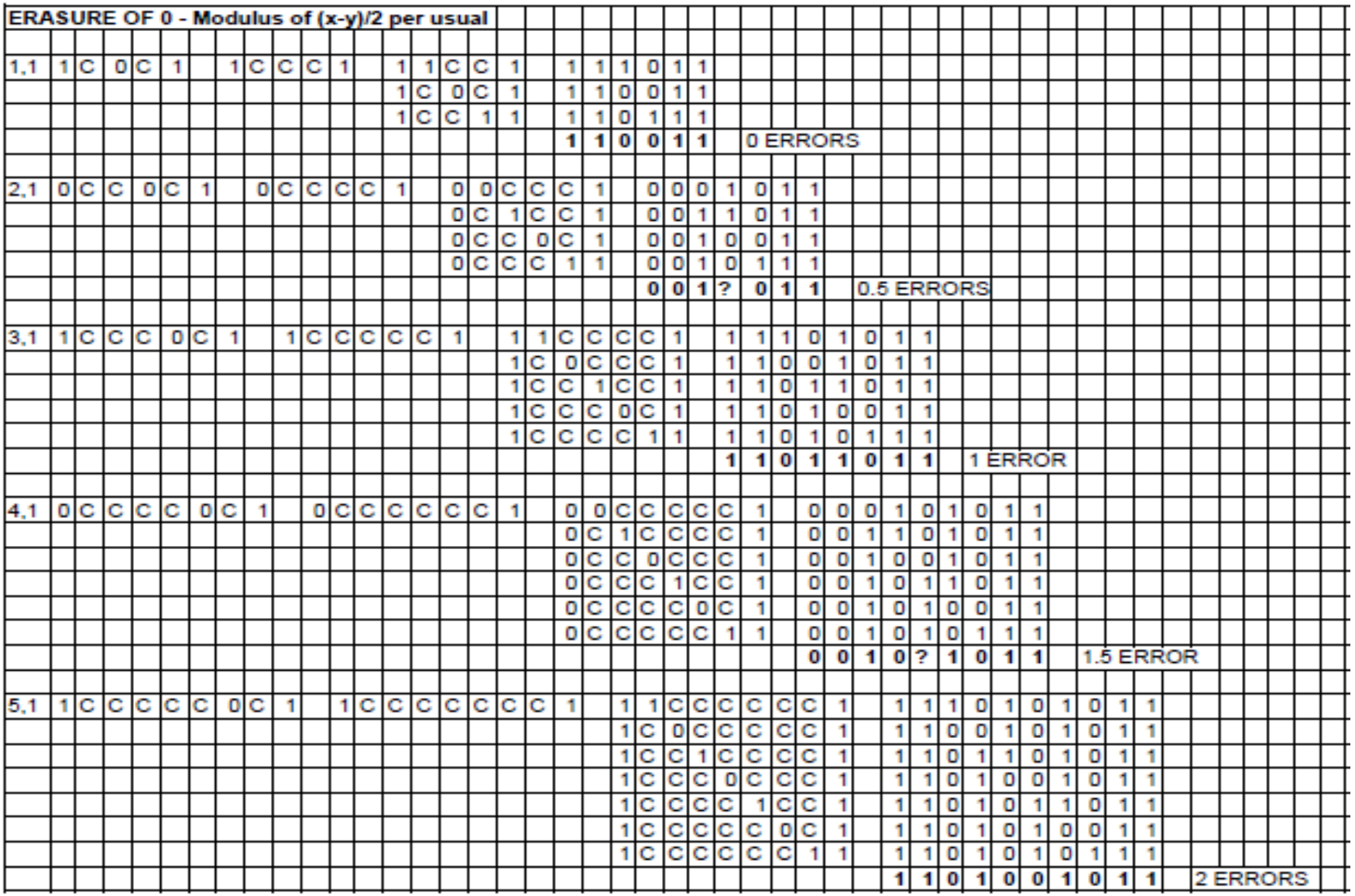


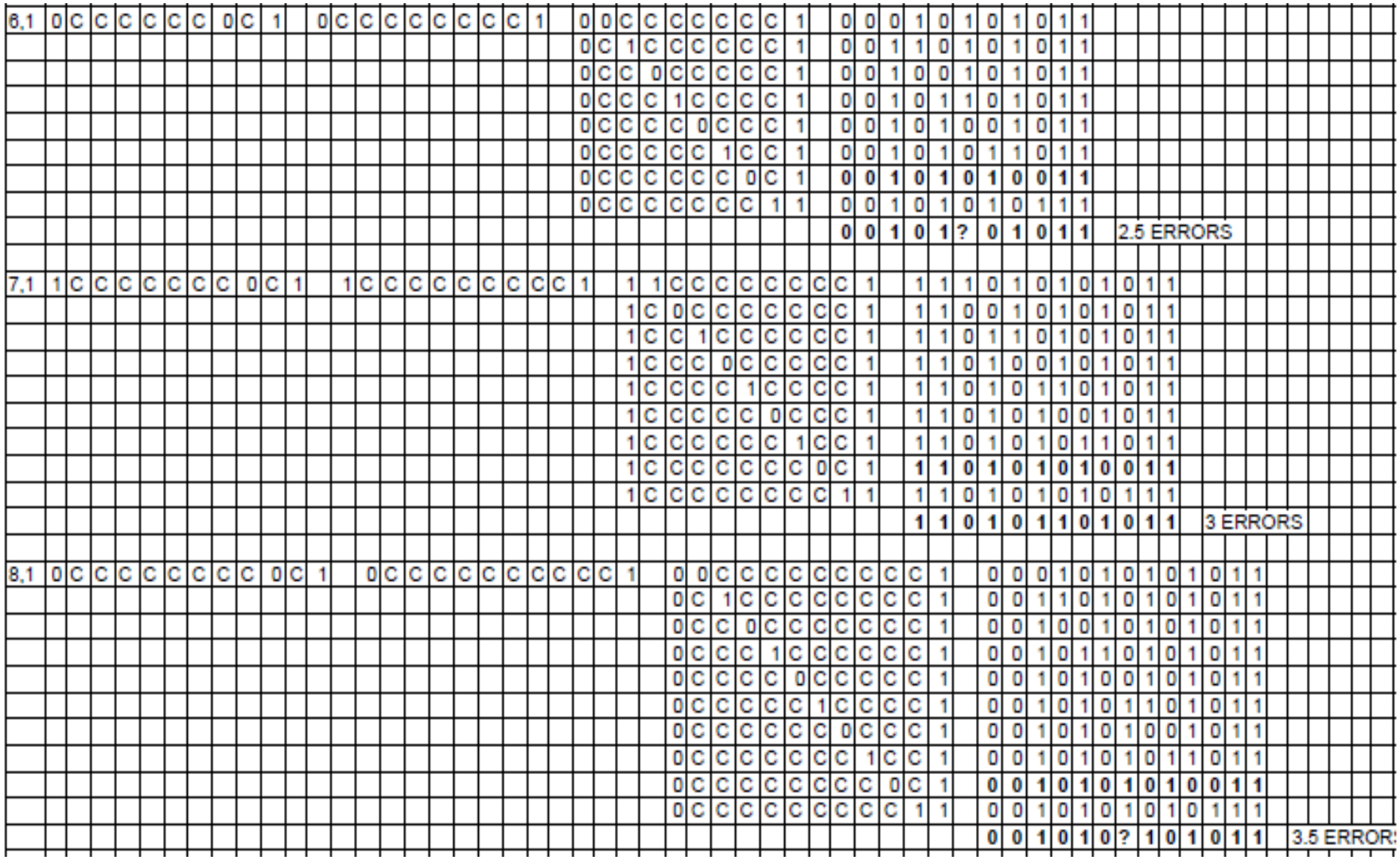
Wrong-slot of 1 back to 0 will always produce zero errors because it will consist two pulses in the same data frame which is not allowed for DuoPPM coding scheme and will be detected by the MLSD code.

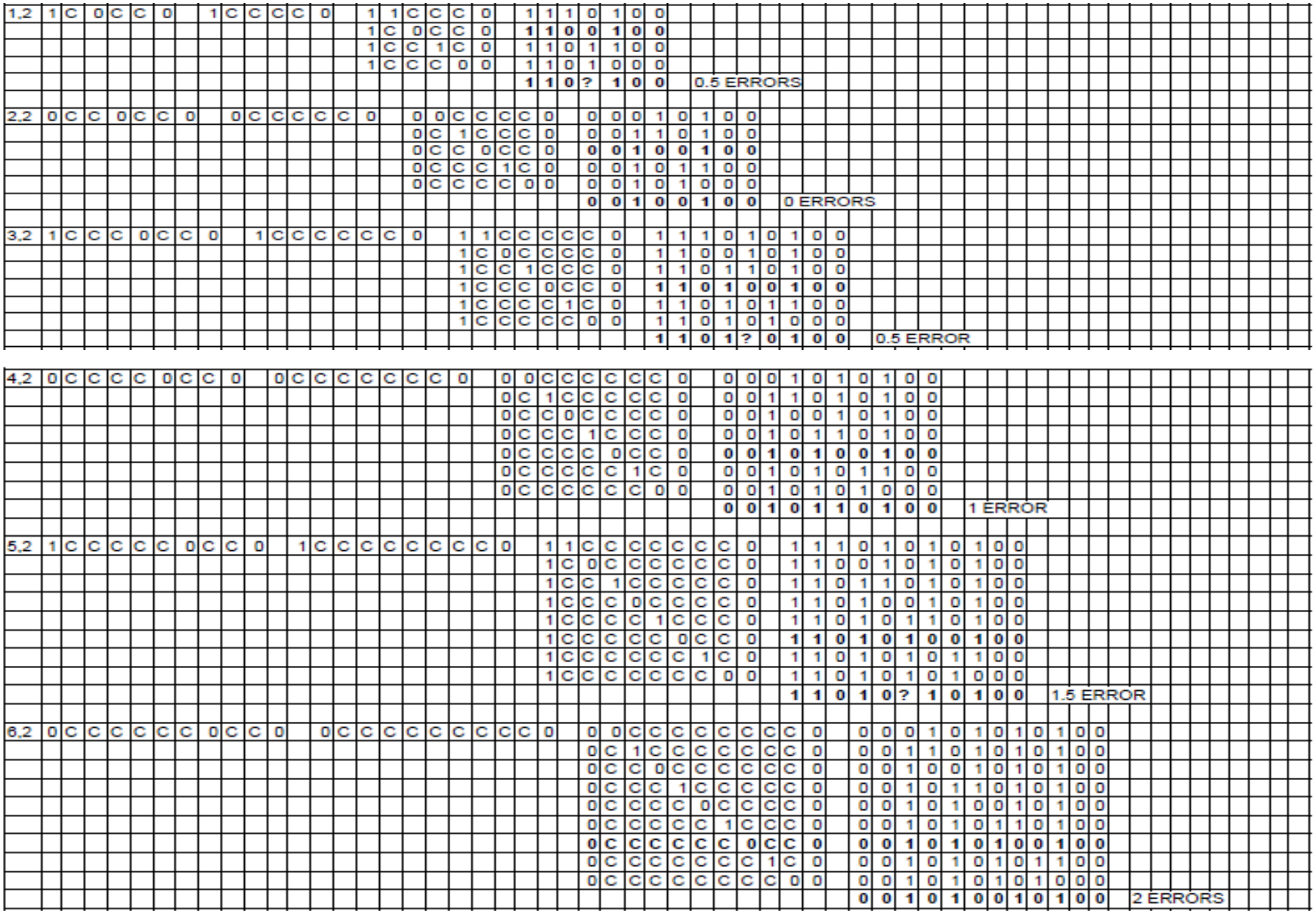

W.S. OF 1 FORWARD TO 0 - ALWAYS ONE ERROR
1,1
1 ERROR
2,1
1 ERROR
3,1
1 ERROR
4,1
1 ERROR
5,1
1 ERROR
6,1
1 ERROR
7,1
1 ERROR
8,1
1 ERROR
9,1
1,2
1 ERROR
2,2
1 ERROR
3,2
1 ERROR

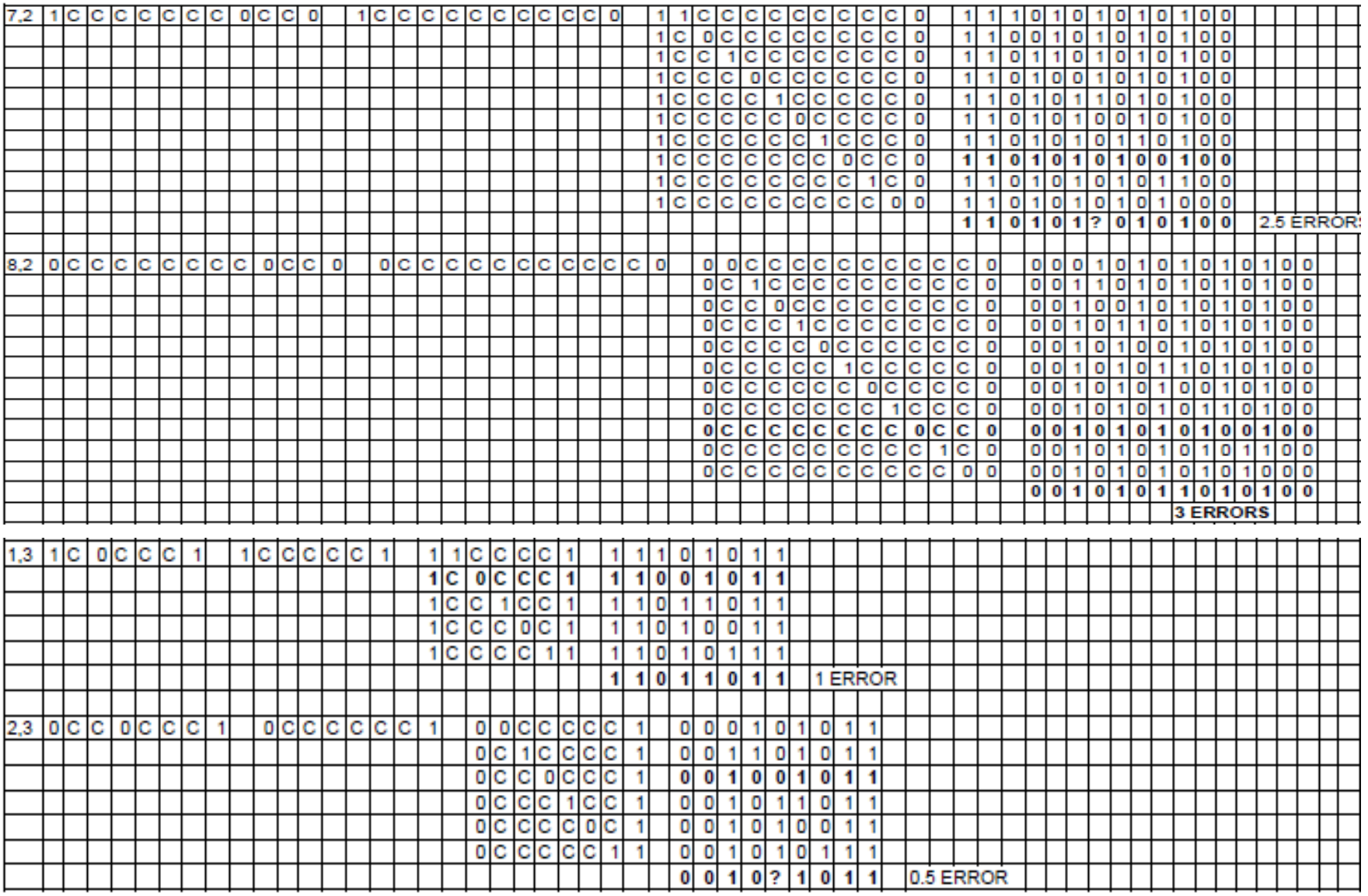

4,2
1 ERROR
5,2
1 ERROR
6,2
1 ERROR
7,2
1 ERROR
8,2

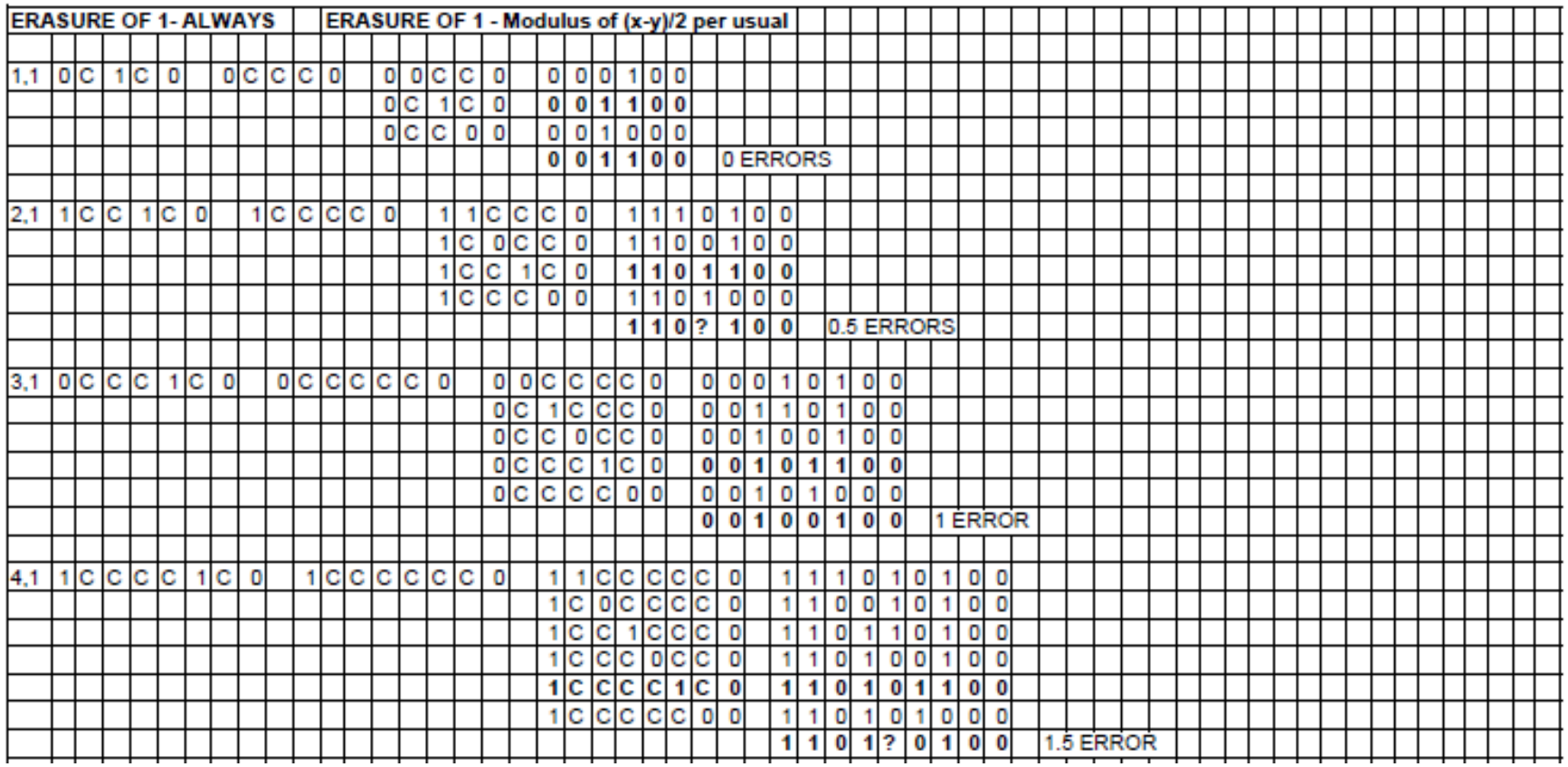

1,3
1 ERROR
2,3
1 ERROR

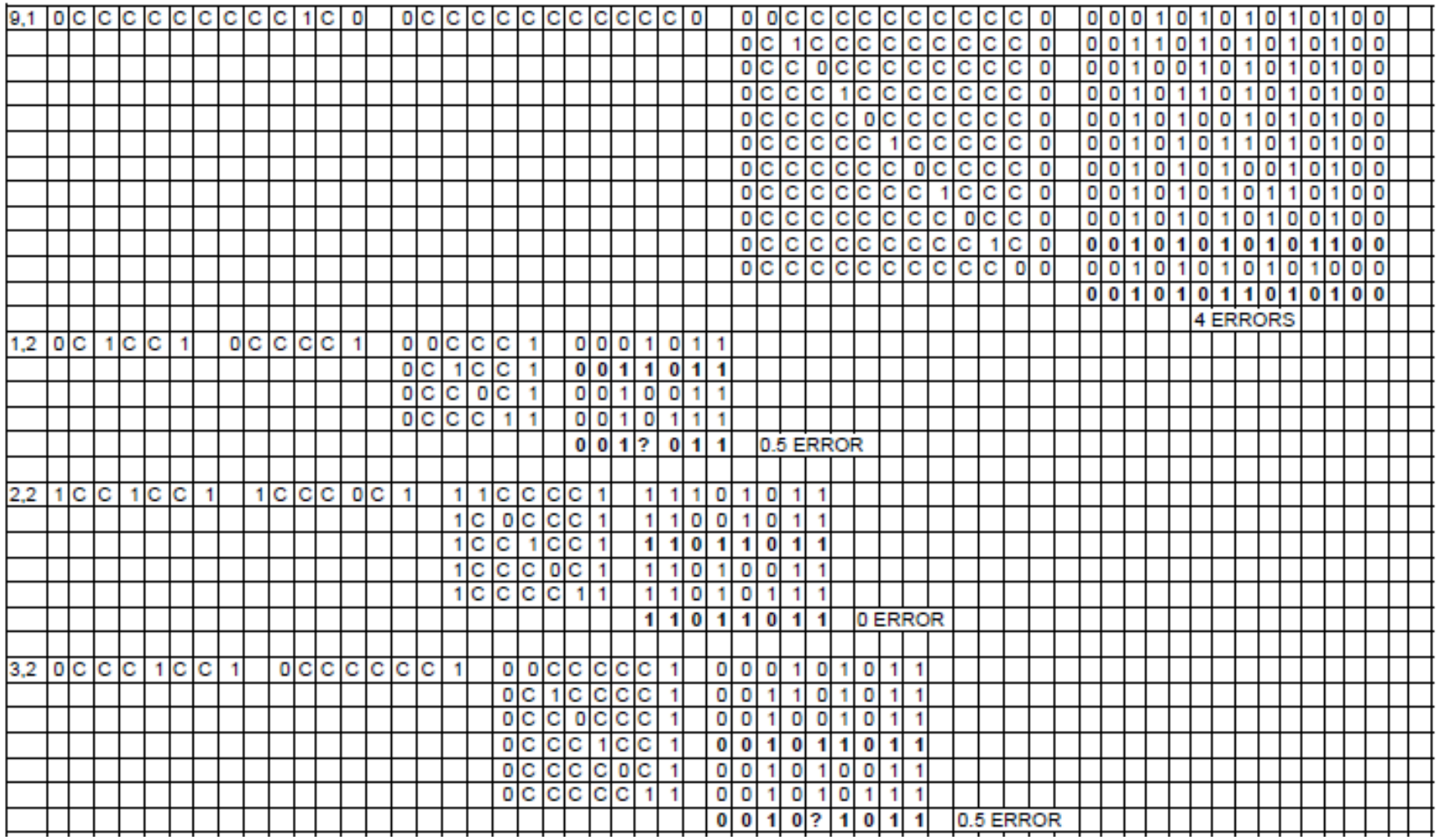

ERASURE OF 0 - Modulus of (x-y)/2 per usual
0 ERRORS
0.5 ERRORS
1 ERROR
1.5 ERROR
2 ERRORS

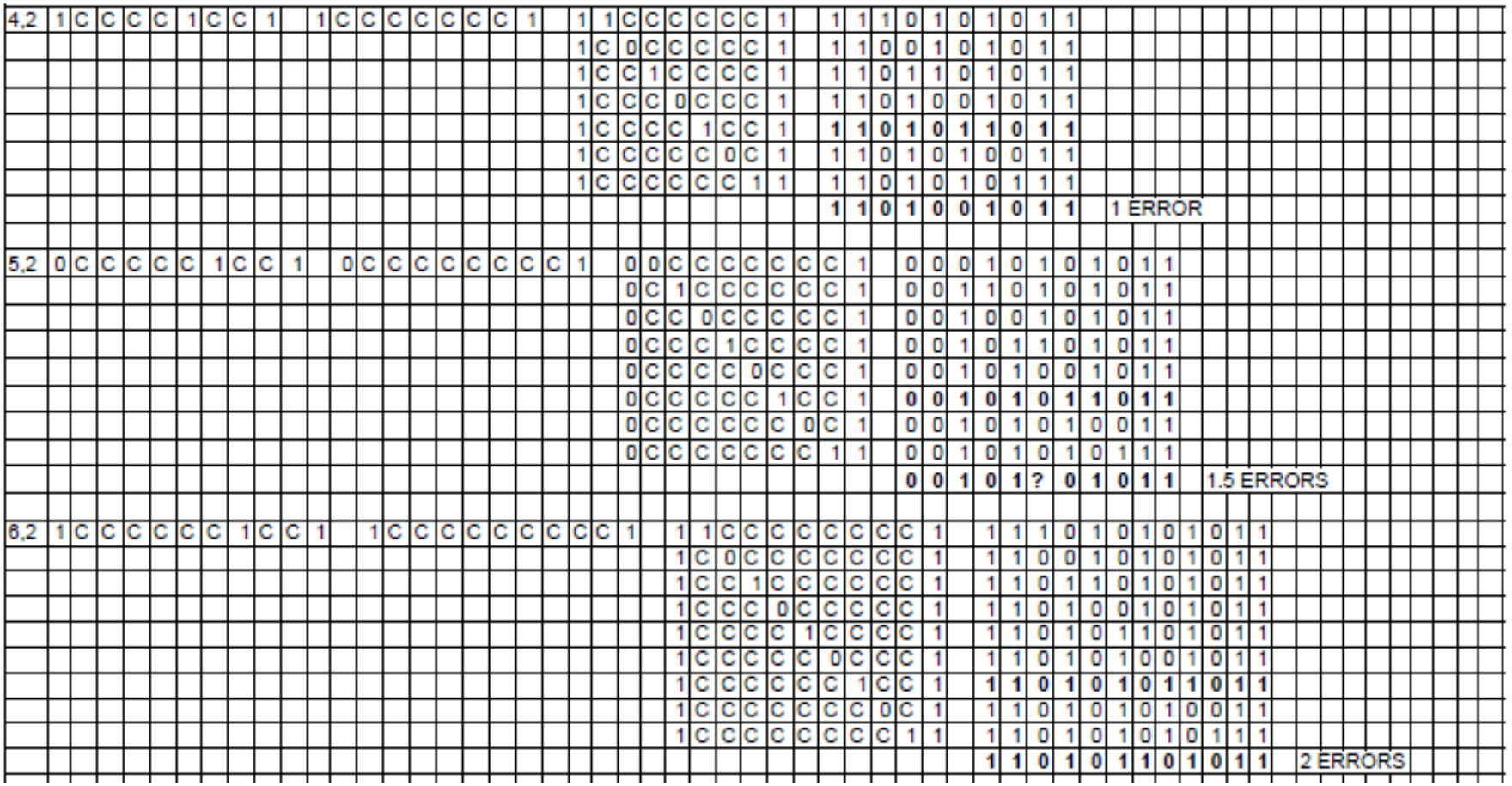

6,1
2.5 ERRORS
7,1
3 ERRORS
8,1
3.5 ERROR


1,2
0.5 ERRORS
2,2
0 ERRORS
3,2
0.5 ERROR
4,2
1 ERROR
5,2
1.5 ERROR
6,2
2 ERRORS

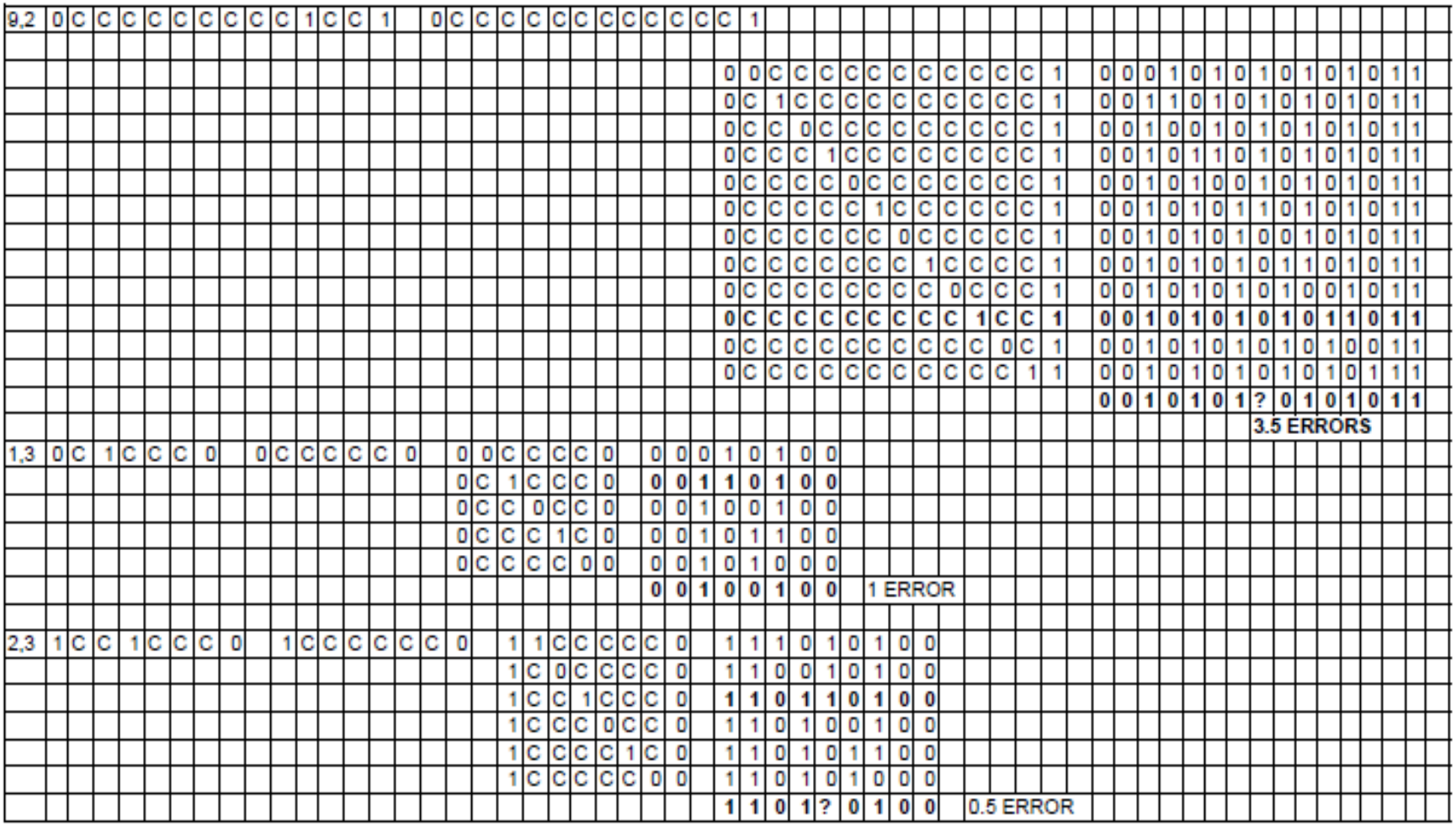

7,2
8,2
1,3
2,3
2.5 ERROR
3 ERRORS
1 ERROR
0.5 ERROR


ERASURE OF 1- ALWAYS
ERASURE OF 1 - Modulus of (x-y)/2 per usual
1,1
0 ERRORS
2,1
0.5 ERRORS
3,1
1 ERROR
4,1
1.5 ERROR


9,1
4 ERRORS
1,2
0.5 ERROR
2,2
0 ERROR
3,2
0.5 ERROR


4,2
1 ERROR
5,2
1.5 ERRORS
6,2
2 ERRORS

7,2	0 C C C C C C C 1 C C 1	0 C C C C C C C C C C 1	0 0 C C C C C C C C C 1	0 0 0 1 0 1 0 1 0 1 0 1 1
			0 C 1 C C C C C C C C 1	0 0 1 1 0 1 0 1 0 1 0 1 1
			0 C C 0 C C C C C C C 1	0 0 1 0 0 1 0 1 0 1 0 1 1
			0 C C C 1 C C C C C C 1	0 0 1 0 1 1 0 1 0 1 0 1 1
			0 C C C C 0 C C C C C 1	0 0 1 0 1 0 0 1 0 1 0 1 1
			0 C C C C C 1 C C C C 1	0 0 1 0 1 0 1 1 0 1 0 1 1
			0 C C C C C C 0 C C C 1	0 0 1 0 1 0 1 0 0 1 0 1 1
			0 C C C C C C C 1 C C 1	**0 0 1 0 1 0 1 0 1 1 0 1 1**
			0 C C C C C C C C 0 C 1	0 0 1 0 1 0 1 0 1 0 0 1 1
			0 C C C C C C C C C 1 1	0 0 1 0 1 0 1 0 1 0 1 1 1
				0 0 1 0 1 0 ? 1 0 1 0 1 1
				2.5 ERRORS
8,2	1 C C C C C C C C 1 C C 1	1 C C C C C C C C C C C 1	1 1 C C C C C C C C C C 1	1 1 1 0 1 0 1 0 1 0 1 0 1 1
			1 C 0 C C C C C C C C C 1	1 1 0 0 1 0 1 0 1 0 1 0 1 1
			1 C C 1 C C C C C C C C 1	1 1 0 1 1 0 1 0 1 0 1 0 1 1
			1 C C C 0 C C C C C C C 1	1 1 0 1 0 0 1 0 1 0 1 0 1 1
			1 C C C C 1 C C C C C C 1	1 1 0 1 0 1 1 0 1 0 1 0 1 1
			1 C C C C C 0 C C C C C 1	1 1 0 1 0 1 0 0 1 0 1 0 1 1
			1 C C C C C C 1 C C C C 1	1 1 0 1 0 1 0 1 1 0 1 0 1 1
			1 C C C C C C C 0 C C C 1	1 1 0 1 0 1 0 1 0 0 1 0 1 1
			1 C C C C C C C C 1 C C 1	**1 1 0 1 0 1 0 1 0 1 1 0 1 1**
			1 C C C C C C C C C 0 C 1	1 1 0 1 0 1 0 1 0 1 0 0 1 1
			1 C C C C C C C C C C 1 1	1 1 0 1 0 1 0 1 0 1 0 1 1 1
				1 1 0 1 0 1 0 0 1 0 1 0 1 1
				3 ERRORS


9,2
1,3
2,3
3.5 ERRORS
1 ERROR
0.5 ERROR

FALSE 0 - (COMBS-1)/2 - COMBS = 2,1..,4,1..,6,1..,8,1..,10 - See end of Appendix 5	combinations	error
1,1 0 C 1 C 0 0 C 1 0 0	2	0.5
1,2 0 C 1 C C 1 0 C 1 0 C 1	2	0.5
0 C 1 C 0 1	1	0
1,3 0 C 1 C C C 0 0 C 1 0 C C 0	2	0.5
0 C 1 C 0 C 0	2	0.5
0 C 1 C C 0 0	4	1.5
1,4 0 C 1 C C C C 1 0 C 1 0 C C C 1	2	0.5
0 C 1 C 0 C C 1	3	1
0 C 1 C C 0 C 1	4	1.5
0 C 1 C C C 0 1	1	0
1,5 0 C 1 C C C C C 0 0 C 1 0 C C C C 0	2	0.5
0 C 1 C 0 C C C 0	4	1.5
0 C 1 C C 0 C C 0	4	1.5
0 C 1 C C C 0 C 0	2	0.5
0 C 1 C C C C 0 0	6	2.5
1,6 0 C 1 C C C C C C 1 0 C 1 0 C C C C C 1	2	0.5
0 C 1 C 0 C C C C 1	5	2
0 C 1 C C 0 C C C 1	4	1.5
0 C 1 C C C 0 C C 1	3	1
0 C 1 C C C C 0 C 1	6	2.5
0 C 1 C C C C C 0 1	1	0
1,7 0 C 1 C C C C C C C 0 0 C 1 0 C C C C C C 0	2	0.5
0 C 1 C 0 C C C C C 0	6	2.5
0 C 1 C C 0 C C C C 0	4	1.5
0 C 1 C C C 0 C C C 0	4	1.5
0 C 1 C C C C 0 C C 0	6	2.5
0 C 1 C C C C C 0 C 0	2	0.5
0 C 1 C C C C C C 0 0	8	3.5

1,8 0 C 1 C C C C C C C C C 1 0 C 1 0 C C C C C C C 1	2	0.5
0 C 1 C 0 C C C C C C C 1	7	3
0 C 1 C C 0 C C C C C C 1	4	1.5
0 C 1 C C C 0 C C C C C 1	5	2
0 C 1 C C C C 0 C C C C 1	6	2.5
0 C 1 C C C C C 0 C C C 1	3	1
0 C 1 C C C C C C 0 C C 1	8	3.5
0 C 1 C C C C C C C 0 1	1	0
1,9 0 C 1 C C C C C C C C C C 0 0 C 1 0 C C C C C C C C 0	2	0.5
0 C 1 C 0 C C C C C C C C 0	8	3.5
0 C 1 C C 0 C C C C C C C 0	4	1.5
0 C 1 C C C 0 C C C C C 0	6	2.5
0 C 1 C C C C 0 C C C C 0	6	2.5
0 C 1 C C C C C 0 C C C 0	4	1.5
0 C 1 C C C C C C 0 C C 0	8	3.5
0 C 1 C C C C C C C 0 C 0	2	0.5
0 C 1 C C C C C C C C 0 0	10	4.5

1,1	2								
1,2	2	1							
1,3	2	2	4						
1,4	2	3	4	1					
1,5	2	4	4	2	6				
1,6	2	5	4	3	6	1			
1,7	2	6	4	4	6	2	8		
1,8	2	7	4	5	6	3	8	1	
1,9	2	8	4	6	6	4	8	2	10

FALSE 1 - (COMBS-1)/2 - COMBS = 2,1..,4,1..,6,1..,8,1..																												Combinations	error
1,1	1	C	0	C	1		1	C	0	1	1																	2	0.5
1,2	1	C	0	C	C	0		1	C	0	1	C	0															2	0.5
								1	C	0	C	1	0															1	0
1,3	1	C	0	C	C	C	1		1	C	0	1	C	C	1													2	0.5
								1	C	0	C	1	C	1														2	0.5
								1	C	0	C	C	1	1														4	1.5
1,4	1	C	0	C	C	C	C	0		1	C	0	0	C	C	C	0											2	0.5
										1	C	0	C	0	C	C	0											3	1
										1	C	0	C	C	0	C	0											4	1.5
										1	C	0	C	C	C	0	0											1	0
1,5	1	C	0	C	C	C	C	C	1		1	C	0	0	C	C	C	C	1									2	0.5
											1	C	0	C	0	C	C	C	1									4	1.5
											1	C	0	C	C	0	C	C	1									4	1.5
											1	C	0	C	C	C	0	C	1									2	0.5
											1	C	0	C	C	C	C	0	1									6	2.5
1,6	1	C	0	C	C	C	C	C	C	0		1	C	0	0	C	C	C	C	C	0							2	0.5
												1	C	0	C	0	C	C	C	C	0							5	2
												1	C	0	C	C	0	C	C	C	0							4	1.5
												1	C	0	C	C	C	0	C	C	0							3	1
												1	C	0	C	C	C	C	0	C	0							6	2.5
												1	C	0	C	C	C	C	C	0	0							1	0
1,7	1	C	0	C	C	C	C	C	C	C	1		1	C	0	0	C	C	C	C	C	C	1					2	0.5
													1	C	0	C	0	C	C	C	C	C	1					6	2.5
													1	C	0	C	C	0	C	C	C	C	1					4	1.5
													1	C	0	C	C	C	0	C	C	C	1					4	1.5
													1	C	0	C	C	C	C	0	C	C	1					6	2.5
													1	C	0	C	C	C	C	C	0	C	1					2	0.5
													1	C	0	C	C	C	C	C	C	0	1					8	3.5
1,8	1	C	0	C	C	C	C	C	C	C	C	C	0		1	C	0	0	C	C	C	C	C	C	0			2	0.5
															1	C	0	C	0	C	C	C	C	C	C	0		7	3
															1	C	0	C	C	0	C	C	C	C	C	0		4	1.5
															1	C	0	C	C	C	0	C	C	C	C	0		5	2
															1	C	0	C	C	C	C	0	C	C	C	0		6	2.5
															1	C	0	C	C	C	C	C	0	C	C	0		3	1
															1	C	0	C	C	C	C	C	C	0	C	0		8	3.5
															1	C	0	C	C	C	C	C	C	C	0	0		1	0
1,9	1	C	0	C	C	C	C	C	C	C	C	C	C	1		1	C	0	0	C	C	C	C	C	C	C	C	2	0.5
																1	C	0	C	0	C	C	C	C	C	C	C	8	3.5
																1	C	0	C	C	0	C	C	C	C	C	C	4	1.5
																1	C	0	C	C	C	0	C	C	C	C	C	6	2.5
																1	C	0	C	C	C	C	0	C	C	C	C	6	2.5
																1	C	0	C	C	C	C	C	0	C	C	C	4	1.5
																1	C	0	C	C	C	C	C	C	0	C	C	8	3.5
																1	C	0	C	C	C	C	C	C	C	0	C	2	0.5
																1	C	0	C	C	C	C	C	C	C	C	0	10	4.5
1,1	2																												
1,2	2	1																											
1,3	2	2	4																										
1,4	2	3	4	1																									
1,5	2	4	4	2	6																								
1,6	2	5	4	3	6	1																							
1,7	2	6	4	4	6	2	8																						
1,8	2	7	4	5	6	3	8	1																					
1,9	2	8	4	6	6	4	8	2	10																				

FALSE 0 - (COMBS-1)/2 - COMBS = 1..,3,1..,5,1..,7,1..,9,1..																												Combinations	error
1,1	1	C	0	C	1		1	C	0	0	1																	1	0
1,2	1	C	0	C	C	0		1	C	0	0	C	0															2	0.5
								1	C	0	C	0	0															3	1
1,3	1	C	0	C	C	C	1		1	C	0	0	C	C	1													3	1.5
								1	C	0	C	0	C	1													3	1.5
								1	C	0	C	C	0	1													1	0
1,4	1	C	0	C	C	C	C	0		1	C	0	0	C	C	C	0											4	1.5
									1	C	0	C	0	C	C	0											3	1
									1	C	0	C	C	0	C	0											2	0.5
									1	C	0	C	C	C	0	0											5	2
1,5	1	C	0	C	C	C	C	C	1		1	C	0	0	C	C	C	C	1									5	2
											1	C	0	C	0	C	C	C	1								3	1
											1	C	0	C	C	0	C	C	1								3	1
											1	C	0	C	C	C	0	C	1								5	2
											1	C	0	C	C	C	C	0	1								1	0
1,6	1	C	0	C	C	C	C	C	C	0		1	C	0	0	C	C	C	C	C	0							6	2.5
												1	C	0	C	0	C	C	C	C	0							3	1
												1	C	0	C	C	0	C	C	C	0							4	1.5
												1	C	0	C	C	C	0	C	C	0							5	2
												1	C	0	C	C	C	C	0	C	0							2	0.5
												1	C	0	C	C	C	C	C	0	0							7	3
1,7	1	C	0	C	C	C	C	C	C	C	1		1	C	0	0	C	C	C	C	C	C	1					7	3
													1	C	0	C	0	C	C	C	C	C	1					3	1
													1	C	0	C	C	0	C	C	C	C	1					5	2
													1	C	0	C	C	C	0	C	C	C	1					5	2
													1	C	0	C	C	C	C	0	C	C	1					3	1
													1	C	0	C	C	C	C	C	0	C	1					7	3
													1	C	0	C	C	C	C	C	C	0	1					1	0.5
1,8	1	C	0	C	C	C	C	C	C	C	C	C	0		1	C	0	0	C	C	C	C	C	C	C	0		8	3.5
															1	C	0	C	0	C	C	C	C	C	C	0		3	1
															1	C	0	C	C	0	C	C	C	C	C	0		6	2.5
															1	C	0	C	C	C	0	C	C	C	C	0		5	2
															1	C	0	C	C	C	C	0	C	C	C	0		4	1.5
															1	C	0	C	C	C	C	C	0	C	C	0		7	3
															1	C	0	C	C	C	C	C	C	0	C	0		2	0.5
															1	C	0	C	C	C	C	C	C	C	0	0		9	4
1,9	1	C	0	C	C	C	C	C	C	C	C	C	C	1		1	C	0	0	C	C	C	C	C	C	C	C	9	4
																1	C	0	C	0	C	C	C	C	C	C	1	3	1
																1	C	0	C	C	0	C	C	C	C	C	1	7	3
																1	C	0	C	C	C	0	C	C	C	C	1	5	2
																1	C	0	C	C	C	C	0	C	C	C	1	5	2
																1	C	0	C	C	C	C	C	0	C	C	1	7	3
																1	C	0	C	C	C	C	C	C	0	C	1	3	1
																1	C	0	C	C	C	C	C	C	C	0	1	9	4
																1	C	0	C	C	C	C	C	C	C	C	0	1	0
1,1	1																												
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1,7	7	3	5	5	3	7	1																						
1,8	8	3	6	5	4	7	2	9																					
1,9	9	3	7	5	5	7	3	9	1																				

FALSE 1 - (COMBS-1)/2 - COMBS = 1..,3,1..,5,1..,7,1..,9,1..																													Combinations	Errors
1,1	0	C	1	C	0		0	C	1	1	0																		1	0
1,2	0	C	1	C	C	1		0	C	1	1	C	1																2	0.5
								0	C	1	C	1	1																3	1
1,3	0	C	1	C	C	C	0		0	C	1	1	C	C	0														3	1
									0	C	1	C	1	C	0														3	1
									0	C	1	C	C	1	0														1	0
1,4	0	C	1	C	C	C	C	1		0	C	1	1	C	C	C	1												4	1.5
										0	C	1	C	1	C	C	1												3	1
										0	C	1	C	C	1	C	1												2	0.5
										0	C	1	C	C	C	1	1												5	2
1,5	0	C	1	C	C	C	C	C	0		0	C	1	1	C	C	C	C	0										5	2
											0	C	1	C	1	C	C	C	0										3	1
											0	C	1	C	C	1	C	C	0										3	1
											0	C	1	C	C	C	1	C	0										5	2
											0	C	1	C	C	C	C	1	0										1	0
1,6	0	C	1	C	C	C	C	C	C	1		0	C	1	1	C	C	C	C	C	1								6	2.5
												0	C	1	C	1	C	C	C	C	1								3	1
												0	C	1	C	C	1	C	C	C	1								4	1.5
												0	C	1	C	C	C	1	C	C	1								5	2
												0	C	1	C	C	C	C	1	C	1								2	0.5
												0	C	1	C	C	C	C	C	1	1								7	3
1,7	0	C	1	C	C	C	C	C	C	C	0		0	C	1	1	C	C	C	C	C	C	0						7	3
													0	C	1	C	1	C	C	C	C	C	0						3	1
													0	C	1	C	C	1	C	C	C	C	0						5	2
													0	C	1	C	C	C	1	C	C	C	0						5	2
													0	C	1	C	C	C	C	1	C	C	0						3	1
													0	C	1	C	C	C	C	C	1	C	0						7	3
													0	C	1	C	C	C	C	C	C	1	0						1	0
1,8	0	C	1	C	C	C	C	C	C	C	C	1		0	C	1	1	C	C	C	C	C	C	1					8	3.5
														0	C	1	C	1	C	C	C	C	C	1					3	1
														0	C	1	C	C	1	C	C	C	C	1					6	2.5
														0	C	1	C	C	C	1	C	C	C	1					5	2
														0	C	1	C	C	C	C	1	C	C	1					4	1.5
														0	C	1	C	C	C	C	C	1	C	1					7	3
														0	C	1	C	C	C	C	C	C	1	1					2	0.5
														0	C	1	C	C	C	C	C	C	C	1	1				9	4
1,9	0	C	1	C	C	C	C	C	C	C	C	C	C	0		0	C	1	1	C	C	C	C	C	C	C	C	0	9	4
																0	C	1	C	C	C	C	C	C	C	C	C	0	3	1
																0	C	1	C	C	1	C	C	C	C	C	C	0	7	3
																0	C	1	C	C	C	1	C	C	C	C	C	0	5	2
																0	C	1	C	C	C	C	1	C	C	C	C	0	5	2
																0	C	1	C	C	C	C	C	1	C	C	C	0	7	3
																0	C	1	C	C	C	C	C	C	1	C	C	0	3	1
																0	C	1	C	C	C	C	C	C	C	1	C	0	9	4
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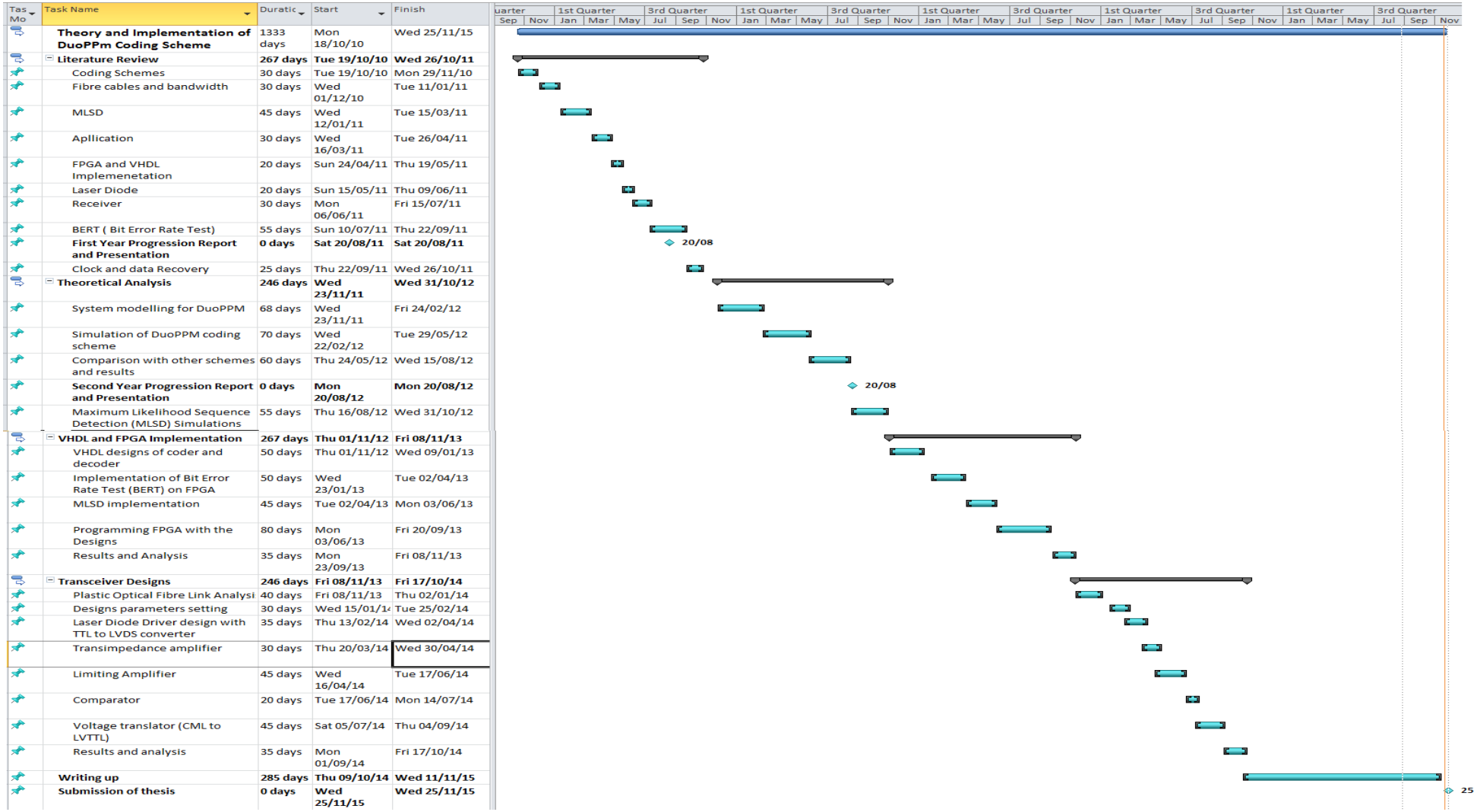
1,6	6	3	4	5	2	7																								
1,7	7	3	5	5	3	7	1																							
1,8	8	3	6	5	4	7	2	9																						
1,9	9	3	7	5	5	7	3	9	1																					

Appendix 6



Tas Mo	Task Name	Duratic	Start	Finish
	Theory and Implementation of DuoPPm Coding Scheme	1333 days	Mon 18/10/10	Wed 25/11/15
	Literature Review	**267 days**	**Tue 19/10/10**	**Wed 26/10/11**
	Coding Schemes	30 days	Tue 19/10/10	Mon 29/11/10
	Fibre cables and bandwidth	30 days	Wed 01/12/10	Tue 11/01/11
	MLSD	45 days	Wed 12/01/11	Tue 15/03/11
	Apllication	30 days	Wed 16/03/11	Tue 26/04/11
	FPGA and VHDL Implemenetation	20 days	Sun 24/04/11	Thu 19/05/11
	Laser Diode	20 days	Sun 15/05/11	Thu 09/06/11
	Receiver	30 days	Mon 06/06/11	Fri 15/07/11
	BERT (Bit Error Rate Test)	55 days	Sun 10/07/11	Thu 22/09/11
	First Year Progression Report and Presentation	**0 days**	**Sat 20/08/11**	**Sat 20/08/11**
	Clock and data Recovery	25 days	Thu 22/09/11	Wed 26/10/11
	Theoretical Analysis	**246 days**	**Wed 23/11/11**	**Wed 31/10/12**
	System modelling for DuoPPM	68 days	Wed 23/11/11	Fri 24/02/12
	Simulation of DuoPPM coding scheme	70 days	Wed 22/02/12	Tue 29/05/12
	Comparison with other schemes and results	60 days	Thu 24/05/12	Wed 15/08/12
	Second Year Progression Report and Presentation	**0 days**	**Mon 20/08/12**	**Mon 20/08/12**
	Maximum Likelihood Sequence Detection (MLSD) Simulations	55 days	Thu 16/08/12	Wed 31/10/12
	VHDL and FPGA Implementation	**267 days**	**Thu 01/11/12**	**Fri 08/11/13**
	VHDL designs of coder and decoder	50 days	Thu 01/11/12	Wed 09/01/13
	Implementation of Bit Error Rate Test (BERT) on FPGA	50 days	Wed 23/01/13	Tue 02/04/13
	MLSD implementation	45 days	Tue 02/04/13	Mon 03/06/13
	Programming FPGA with the Designs	80 days	Mon 03/06/13	Fri 20/09/13
	Results and Analysis	35 days	Mon 23/09/13	Fri 08/11/13
	Transceiver Designs	**246 days**	**Fri 08/11/13**	**Fri 17/10/14**
	Plastic Optical Fibre Link Analysi	40 days	Fri 08/11/13	Thu 02/01/14
	Designs parameters setting	30 days	Wed 15/01/14	Tue 25/02/14
	Laser Diode Driver design with TTL to LVDS converter	35 days	Thu 13/02/14	Wed 02/04/14
	Transimpedance amplifier	30 days	Thu 20/03/14	Wed 30/04/14
	Limiting Amplifier	45 days	Wed 16/04/14	Tue 17/06/14
	Comparator	20 days	Tue 17/06/14	Mon 14/07/14
	Voltage translator (CML to LVTTL)	45 days	Sat 05/07/14	Thu 04/09/14
	Results and analysis	35 days	Mon 01/09/14	Fri 17/10/14
	Writing up	**285 days**	**Thu 09/10/14**	**Wed 11/11/15**
	Submission of thesis	**0 days**	**Wed 25/11/15**	**Wed 25/11/15**

Datasheets

1.25Gbps 850nm VCSEL diode in ST receptacle with monitor PD

LASERMATE GROUP, INC.
THE FRIEND OF LASERS

Model No. TST-M85A426-2H

1.25Gbps 850nm VCSEL diode in ST receptacle with monitor PD

FEATURES:

- Industry standard connector of metallic ST*-type receptacle.
- Pre-aligned for multi-mode fiber communication.
- With monitoring PD.
- Data rate operation from DC to 1.25Gbps

ELECTRO-OPTICAL CHARACTERISTICS:

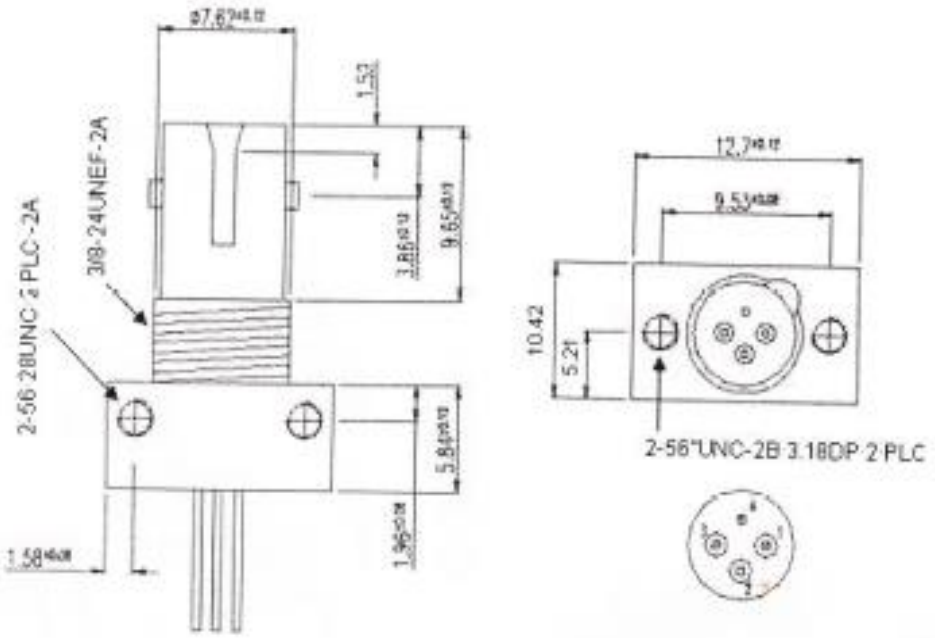
PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS(1)
Threshold Current	I_{th}		2	3.5	mA	
Wavelength	λ_P	830	850	860	nm	I_F=6 mA
Fiber Coupled Power	Po	1	1.7		mW	I_F=6 mA
Forward Voltage	V_F	1.6	1.8	2.1	V	I_F=6 mA
Breakdown voltage	V_{BD}	5	14		V	I_R=10 μA
Rise Time/Fall Time	Tr			0.15	ns	Ib = Ith, 20%~80%
Series Resistance	R_S	35	45	65	Ω	I_F=6 mA
Spectral width (RMS)	Δλ			0.85	nm	I_F=6 mA
Relative Intensity Noise	RIN			-122	dB/Hz	I_F=6 mA ,f=1 GHz
Monitor Current	I_M		50		μA	

ABSOLUTE MAXIMUM RATINGS:

PARAMETERS	MIN	MAX	UNIT	CONDITIONS
Storage Temperature	-40	85	°C	
Operating Temperature	0	70	°C	
Lead Solder Temperature		260	°C	10 seconds
Solder Time		10	sec	
Forward Current (LD)		20	mA	
Reverse Voltage (LD)		5	V	

LASERMATE GROUP, INC.
THE FRIEND OF LASERS

Mechanical Outline (unit: mm):



Pinout:

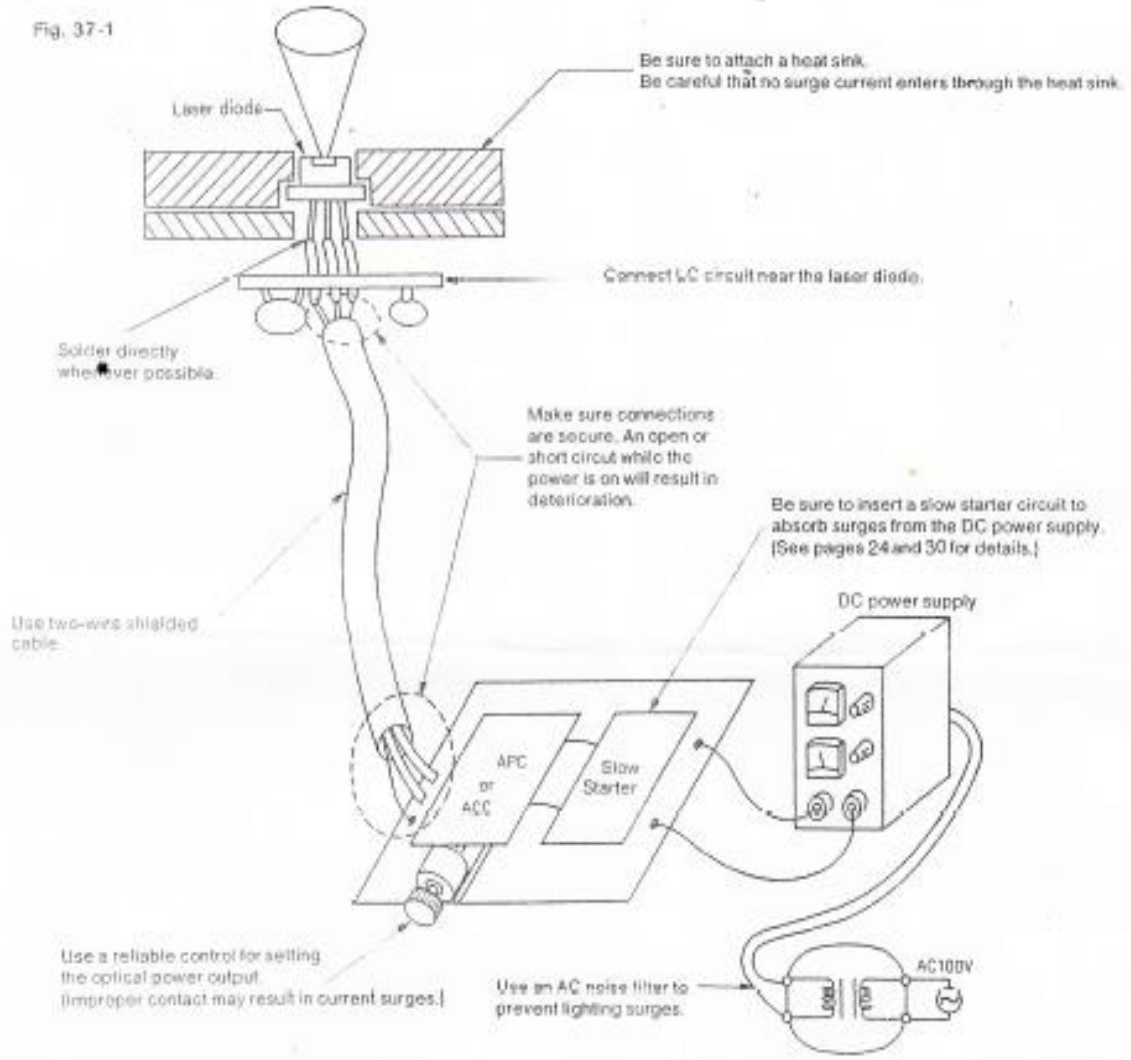
TST-M85A426-2H	
Number	**Function**
1	VCSEL Cathode
2	VCSEL Anode/PD Cathode
3	PD Anode
4	Case

WARNING:
The VCSEL is a class IIIb laser in the safety standard ANSI Z136.1 and should be treated as a potential eye hazard.

Circuit and Circuit Board Precautions

While operating, a laser diode can be easily damaged by surge currents which may occur during power on and off of the drive circuit or while adjusting the power output. Care must also be taken to prevent surge currents from entering the circuit from external sources.

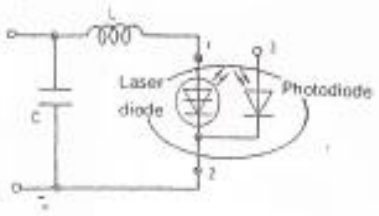
Fig. 37-1



- While the laser diode is powered up, do not touch probes from a synchroscope or voltmeter against the circuitry or laser diode terminals.
- If even an instantaneous excessive optical power output should be emitted while the laser diode is operating, the mirror surfaces of the laser diode chip will be damaged. Even if the drive current supply has an APC, ACC, or both, be sure to monitor the optical power output while setting it. It is not safe to estimate the optical power output only from the drive current.

Note: Added protection from electrostatic surges or surges from the circuitry can be obtained by inserting a coil and capacitor near the laser diode as shown in Fig. 37-2.

Fig. 37-2

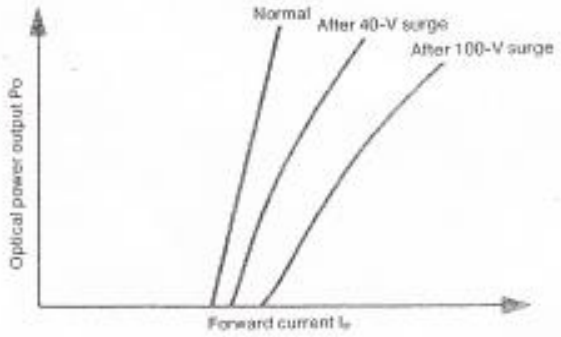


L: Inductor 10~100μH
C: Monolithic ceramic capacitor 0.3~1.5μF
When applying high speed modulation to the laser diode, make the LC time constant small relative to the required response time.

Handling Precautions

Because of their quick response (greater than 1 GHz) and low operating voltage (typically about 2 V), laser diodes are extremely susceptible to damage caused by surge currents.
If excessive current is allowed to flow through the laser diode, the optical power output would become too large and rapid deterioration of the device will result. Application of an electrostatic charge will cause a change in the optical power output vs. forward current characteristic, as shown in Fig. 36-1. Even an instantaneous application of a 40volt charge will increase the drive current and limit the usability of the laser diode. Whenever handling laser diodes, please pay strict attention to the following precautions.

Fig 36-1 Changes in Optical Power Output vs. Forward Current Characteristic after Surge Current

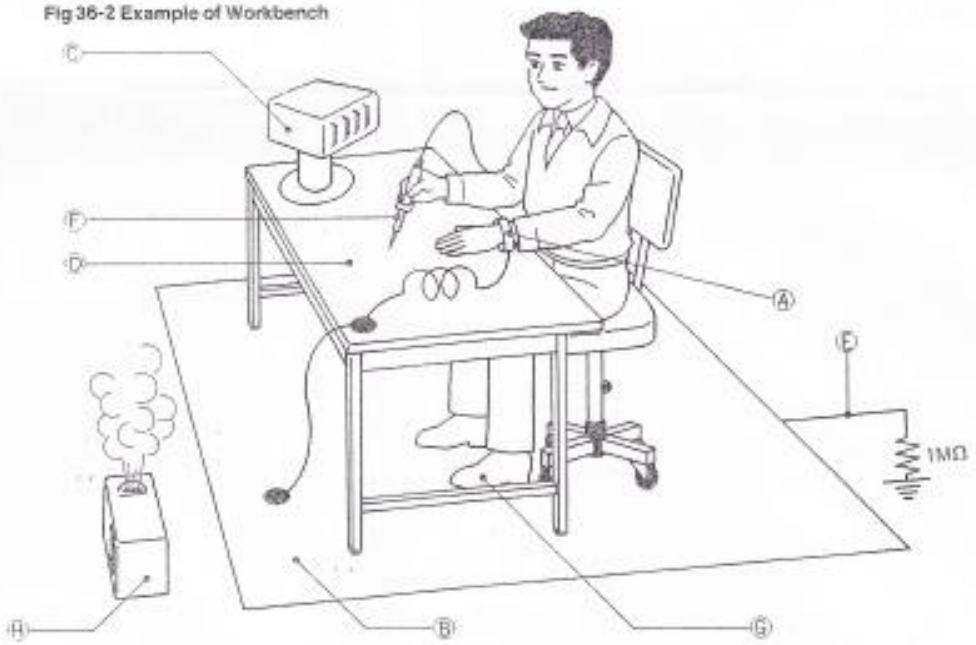


Electrostatic Surge Prevention

Laser diodes are even more sensitive to electrostatic discharge than CMOS LSI's, and require even more preventive measures.

Example of Laser Diode Workbench

Fig 36-2 Example of Workbench



[A] Wrist strap
[B] Conductive floor mat
[C] Ionized air blower
[D] Conductive table mat
Must have the same potential as the floor mat.
[E] Ground
Ground through a 1-MΩ resistance.
[F] Grounded soldering iron
[G] Antistatic shoes
[H] Humidifier

When shipping laser diodes, they should be inserted in antistatic bags to prevent electrostatic charging due to vibration.

LASERMATE GROUP, INC.
THE FRIEND OF LASERS

RST-M85A306

Connectorized High-speed GaAs PIN Photodiode in ST Receptacle

FEATURES:

- Industry standard connector of metallic ST*-type receptacle.
- For detecting 850 nm
- Pre-aligned for 62.5/125 μm multi-mode fibers.
- High Speed up to 1.25Gbps
- Low dark current and low capacitance.

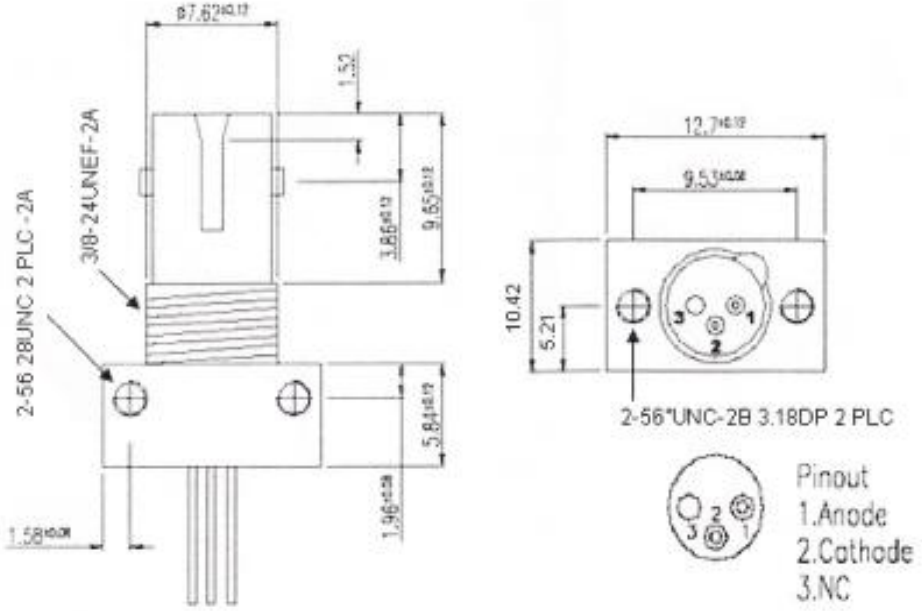
ELECTRO-OPTICAL CHARACTERISTICS:

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Responsivity	R	0.4	0.6		A/W	V_R = 5 V, λ = 850 nm
Dark Current	I_D			3	nA	V_R = 5 V, T_A=25°C
Breakdown Voltage	V_{BD}	50		1	V	Vr=5V
Rise/Fall Time	Tr / Tf			1.15	nsec	Vr=5V
Bandwidth	BW		1.2	1.5	GHz	

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	MIN	MAX	UNIT	CONDITIONS
Storage Temperature	-40	85	°C	
Operating Temperature	-40	85	°C	
Lead Solder Temperature		260	°C	10 seconds
Forward current		5	mA	
Reverse current		1	mA	
Reverse voltage		30	V	

OUTLINE DIMENSIONS (unit: mm):



Custom Fiber Optic Patch Cables

Patch Configurator | Fiber Overview | Fiber Options | Connector Options | Related Products | Accessories | Related Items | Feedback | Tag Cloud

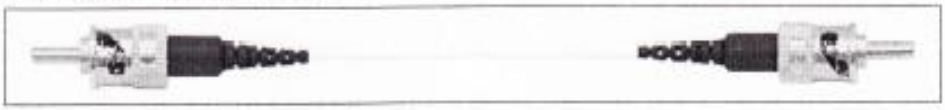
Thorlabs stocks the largest selection of single mode and multimode optical fibers in the photonics industry. If our selection of stocked patch cables does not meet your needs, we also offer custom patch cable services. Please use the form below to build and order your custom cable. If you find your needs are not met by the options in the form below, please contact us and we will design a specialty cable to meet your needs.

Fast Turnaround Service
Need a cable right away to finish your project? If your order is placed before 2 PM EST and the request is for five or less SM or MM cables, each with a maximum individual length of 20 m, we will manufacture and ship them the same day (PM cables ship in 2 days).

OEM Patch Cables
We offer scheduled deliveries, competitive pricing, account support, and kanban stocking agreements. Please contact us with any questions you may have so we can better meet your OEM needs.

Click to Enlarge
Custom Patch Cable Manufacturing Area
at Thorlabs' Newton, NJ Facility

Build Your Custom Patch Cable



Step 1: Select Your Fiber Type

Please select Single Mode (SM), Multimode (MM), Polarization-Maintaining (PM), Doped, or Plastic Fiber. Alternatively, enter the item number of the specific fiber you require. If you are unsure which fiber type will best meet your needs, please go to the *Fiber Options* tab for more information on each fiber option.

SM | PM | MM | Doped | * Plastic | or Part Number: | Lookup

Step 2: Select Your Fiber

GIPOF50-P - (0.19 NA)

Step 3: Select Your Tubing

(Preferred options will be noted with an asterisk (*))
None - None (*)

Step 4: Select Your Connectors

(Preferred options will be noted with an asterisk (*))
Connector 1: ST
Connector 2: ST

Step 5: Select Your Length and Quantity

Length: 100 meters. Tolerance of ±1% or ±7 cm, Whichever is Greater
Quantity: 1

Price and Shipping Information

Price (each): £168.20

Ships: Lead Time - Delivery date to be provided upon Order Confirmation

Notes:

The pricing above reflects the choices made in the form. If you require greater tolerances or any other specialty request, please contact us (contains all selections made in form) and we will be happy to speak with you as to how we can best meet your needs.

3.3V 2.5Gbps ANY INPUT-to-LVPECL DIFFERENTIAL TRANSLATOR

Precision Edge®
SY89327L

FEATURES

- Input accepts virtually all logic standards:
  - Single-ended: SSTL, TTL, CMOS
  - Differential: LVDS, HSTL, CML
- Guaranteed AC performance over temp and voltage:
  - DC-to >2.5Gbps data rate throughput
  - DC-to >2.5GHz clock f_{MAX}
  - < 400ps In-to-Out t_{pd}
  - < 200ps t_r/t_f
- Ultra-low jitter design:
  - 75fs RMS phase jitter
- Low power: 46mW (typ)
- 100k LVPECL output
- Flow-through pinout and fully differential design
- Power supply 3.3V ±10%
- –40°C to +85°C temperature range
- Available in ultra-small 8-lead 2mm x 2mm QFN package

Precision Edge®

DESCRIPTION

The SY89327L is a fully differential, high-speed translator optimized to accept any logic standard from single-ended TTL/CMOS to differential LVDS, HSTL, or CML and translate it to LVPECL. Translation is guaranteed for speeds up to 2.5Gbps (2.5GHz toggle frequency). The SY89327L does not internally terminate its inputs because different interfacing standards have different termination requirements.

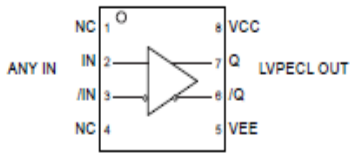
The SY89327L is a member of Micrel's Precision Edge® family of high-speed logic devices. This family features ultra-small packaging, as well as high signal integrity and operation at many different supply voltages.

All support documentation can be found on Micrel's web site at www.micrel.com.

APPLICATIONS

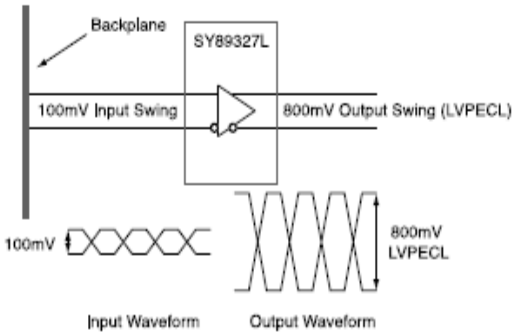
- High-speed logic
- Data communications systems
- Wireless communications systems
- Telecom systems

FUNCTIONAL BLOCK DIAGRAM

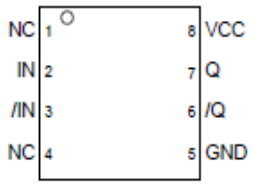


8-Pin QFN (2mm x 2mm)

TYPICAL APPLICATIONS CIRCUIT



PACKAGE/ORDERING INFORMATION



8-Pin QFN

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89327LMGTR	QFN-8	Industrial	327 with Pb-Free bar-line indicator	Pb-Free NiPdAu

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
2, 3	IN, /IN	Differential inputs: This input is the differential signal input to the device. This input accepts AC- or DC-coupled signals as small as 100mV. External termination is required. Please refer to the "Input Interface Applications" section for more details.
8	VCC	Positive power supply. Bypass with 0.1µF ||0.01µF low ESR capacitors.
7, 6	Q, /Q	Differential LVPECL Output: Terminate with 50Ω to V_{CC}–2V. See "Output Interface Applications" section. Output pair is 100k temperature compensated LVPECL compatible.
5	GND, Exposed Pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.
1, 4	NC	No connect.

FUNCTIONAL DESCRIPTION

Establishing Static Logic Inputs

Do not leave unused inputs floating. Tie either the true or complement input to ground. A logic zero is achieved by connecting the complement input to ground with the true input floating. For a TTL input, tie a 2.5kΩ resistor between the complement input and ground. See "Input Interface" section.

Input Levels

LVDS, CML, and HSTL differential signals may be connected directly to the D inputs. Depending on the actual worst case voltage seen, the SY8327L's performance varies as per the following table:

Input Voltage Range	Minimum Voltage Swing	Maximum Translation Speed
0 to 2.4V	100mV	2.5Gbps
0 to V_{CC} +0.3V	200mV	1.25Gbps

For LVDS applications, only point-to-point interfaces are supported. Due to the current required by the input structure shown in Figure 1, multi-drop and multi-point architectures are not supported.

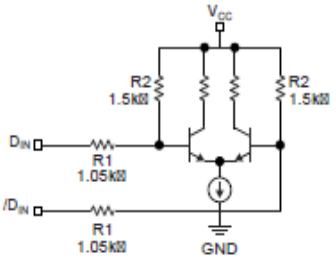


Figure 1. Simplified Input Structure

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to + 4.0V
Input Voltage (VIN) ..... –0.5V to V_{CC}
Input Current
  Source or sink current on IN, /IN ..... ±50mA
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... 3.0V to 3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
QFN (Θ_{JA})
  Still-Air ..... 93°C/W
  500lfpm ..... 87°C/W
QFN (Ψ_{JB})
  Junction-to-Board ..... 32°C/W

DC ELECTRICAL CHARACTERISTICS[4]

T_A = –40°C to +85°C; unless stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}[5]		28	45	mA

INPUT ELECTRICAL CHARACTERISTICS[4]

V_{CC} = 3.3V ±10%; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC}–2V, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	V_{IH} min must be ≥ 1.2V			V_{CC}+0.3	V
V_{IL}	Input LOW Voltage		–0.3			V
V_{IN}	Input Voltage Swing	See Figure 2a, V_{IH} < 2.4V	100			mV
		See Figure 2a, V_{IH} < V_{CC} +0.3V	200			mV

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS[4]

V_{CC} = 3.3V ±10%; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC}–2V, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Output HIGH Voltage Q, /Q		V_{CC}–1.945		V_{CC} –1.695	V
V_{OH}	Output Common Mode Range Q, /Q		V_{CC}–1.145		V_{CC} –0.895	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 2a	550	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q, /Q	See Figure 2b	1100	1600		mV_{PP}

Notes:

1. Permanent device damage may occur if the "Absolute Maximum Ratings" are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices' most negative potential on the PCB. Ψ_{JB} uses 4-layer Θ_{JA} in still-air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS [5]

V_{CC} = 3.3V ±10%; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC}–2V, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	2.5			Gbps
		V_{OUT} ≥ 200mV Clock		2.5		GHz
t_{pd}	Propagation Delay IN-to-Q, /IN-to-/Q	V_{IN} ≥ 100mV			400	ps
t_{JITTER}	RMS Phase Jitter	Output = 622MHz Integration Range: 12kHz - 20MHz		75		fs
t_r, t_f	Rise / Fall Time (20% to 80%) Q, /Q	At full output swing			200	ps

Notes:

5. See "Timing Diagrams" section for definition of parameters. High frequency AC-parameters are guaranteed by design and characterization.

19-2529; Rev 2; 7/04

EVALUATION KIT AVAILABLE

MAXIM

2.7Gbps, Low-Power SFP Laser Drivers

MAX3735/MAX3735A

General Description

The MAX3735/MAX3735A are +3.3V laser drivers for SFP/SFF applications from 155Mbps up to 2.7Gbps. The devices accept differential input data and provide bias and modulation currents for driving a laser. DC-coupling to the laser allows for multirate applications and reduces the number of external components. The MAX3735/MAX3735A are fully compliant with the SFP MSA timing and the SFF-8472 transmit diagnostic requirements.

An automatic power-control (APC) feedback loop is incorporated to maintain a constant average optical power over temperature and lifetime. The wide modulation current range of 10mA to 60mA (up to 85mA AC-coupled) and bias current of 1mA to 100mA make this product ideal for driving FP/DFB laser diodes in fiber-optic modules. The resistor range for the laser current settings is optimized to interface with the DS1858 SFP controller IC.

The MAX3735/MAX3735A provide transmit-disable control, a single-point latched transmit-failure monitor output, photocurrent monitoring, and bias-current monitoring to indicate when the APC loop is unable to maintain the average optical power. The MAX3735A also features improved multirate operation.

The MAX3735/MAX3735A come in package and die form, and operate over the extended temperature range of -40°C to +85°C.

Applications

Gigabit Ethernet SFP/SFF Transceiver Modules

1G/2G Fibre Channel SFP/SFF Transceiver Modules

Multirate OC3 to OC48-FEC SFP/SFF Transceiver Modules

Features

- SFP Reference Design Available
- Fully Compliant with SFP and SFF-8472 MSAs
- Programmable Modulation Current from 10mA to 60mA (DC-Coupled)
- Programmable Modulation Current from 10mA to 85mA (AC-Coupled)
- Programmable Bias Current from 1mA to 100mA
- Edge Transition Times <51ps
- 27mA (typ) Power-Supply Current
- Multirate 155Mbps to 2.7Gbps Operation
- Automatic Average Power Control
- On-Chip Pullup Resistor for TX_DISABLE
- 24-Pin 4mm × 4mm QFN package

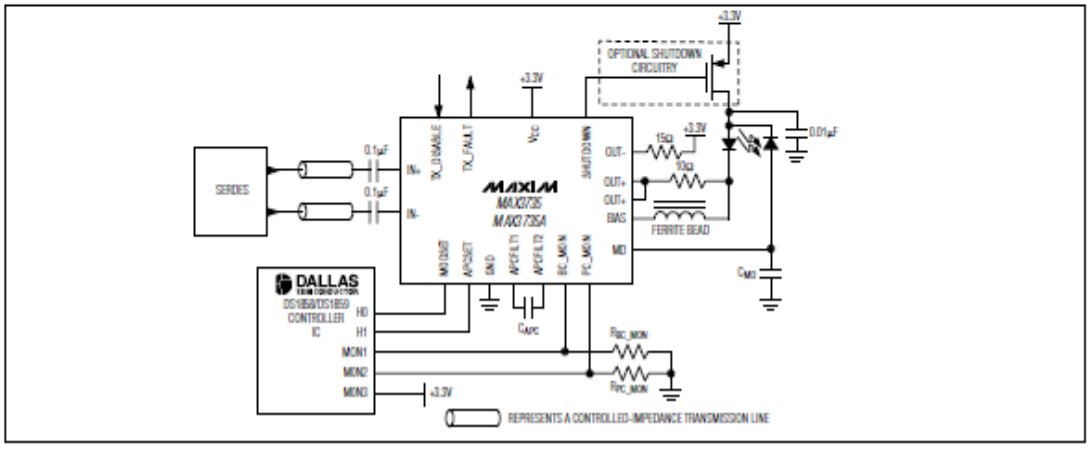
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3735E/D	-40°C to +85°C	Dice*
MAX3735ETG	-40°C to +85°C	24 Thin QFN-EP**
MAX3735EGG	-40°C to +85°C	24 QFN-EP**
MAX3735AETG	-40°C to +85°C	24 Thin QFN-EP**
MAX3735AETG+	-40°C to +85°C	24 Thin QFN-EP**

*Dice are designed to operate from -40°C to +85°C, but are tested and guaranteed only at T_A = +25°C.
**EP = Exposed pad.
+Denotes lead-free package.

Pin Configuration appears at end of data sheet.

Typical Application Circuit



2.7Gbps, Low-Power SFP Laser Drivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... -0.5V to +6.0V
Current into BIAS, OUT+, OUT- ..... -20mA to +150mA
Current into MD ..... -5mA to +5mA
Voltage at IN+, IN-, TX_DISABLE, TX_FAULT, SHUTDOWN ..... -0.5V to (V_{CC} + 0.5V)
Voltage at BIAS, PC_MON, BC_MON, MODSET, APCSET ..... -0.5V to (V_{CC} + 0.5V)
Voltage at OUT+, OUT- ..... +0.5V to (V_{CC} + 1.5V)
Voltage at APCFILT1, APCFILT2 ..... -0.5V to +3V

Continuous Power Dissipation (T_A = +85°C)
24-Lead Thin QFN (derate 20.8mW/°C above +85°C) 1354mW
24-Lead QFN (derate 20.8mW/°C above +85°C) 1354mW
Operating Ambient Temperature Range (T_A) ..... -40°C to +85°C
Storage Ambient Temperature Range ..... -55°C to +150°C
Die Attach Temperature ..... +400°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +85°C. Typical values at V_{CC} = +3.3V, I_{BIAS} = 20mA, I_{MOD} = 30mA, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power-Supply Current	I_{CC}	Excludes the laser bias and modulation currents (Note 2)			27	50	mA
I/O SPECIFICATIONS							
Differential Input Voltage	V_{ID}	$V_{ID} = (V_{IN+}) - (V_{IN-})$, Figure 1		200		2400	mV_{P-P}
Common-Mode Input Voltage					0.6 × V_{CC}		V
Differential Input Resistance				85	100	115	Ω
TX_DISABLE Input Pullup Resistance	R_{PULL}			4.7	7.4	10.0	kΩ
TX_DISABLE Input Current		$V_{HIGH} = V_{CC}$				15	µA
		V_{LOW} = GND, V_{CC} = 3.3V, R_{PULL} = 7.4kΩ			-450		
TX_DISABLE Input High Voltage	V_{IH}			2			V
TX_DISABLE Input Low Voltage	V_{IL}					0.8	V
TX_FAULT Output High Voltage	V_{OH}	I_{OH} = 100µA sourcing (Note 3)		2.4			V
TX_FAULT Output Low Voltage	V_{OL}	I_{OL} = 1mA sinking (Note 3)				0.4	V
SHUTDOWN Output High Voltage	V_{OH}	I_{OH} = 100µA sourcing		V_{CC} - 0.4			V
SHUTDOWN Output Low Voltage	V_{OL}	I_{OL} = 100µA sinking				0.4	V
BIAS GENERATOR							
Bias On-Current Range	I_{BIAS}	Current into BIAS pin		1		100	mA
Bias Off-Current	$I_{BIASOFF}$	Current into BIAS pin during TX_FAULT or TX_DISABLE				100	µA
Bias Overshoot		During SFP module hot plugging (Notes 4, 5, 11)				10	%
Bias-Current Monitor Gain	I_{BC_MON}	External resistor to GND defines the voltage gain, I_{BIAS} = 1mA, R_{BC_MON} = 69.28kΩ		10.0	12	13.5	mA/A
		I_{BIAS} = 100mA, R_{BC_MON} = 693.25Ω		11.5	13	13.5	
Bias-Current Monitor Gain Stability		1mA ≤ I_{BIAS} ≤ 100mA (Notes 4, 6)	MAX3735	-8		+8	%
			MAX3735A	-6		+6	

2.7Gbps, Low-Power SFP Laser Drivers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +85°C. Typical values at V_{CC} = +3.3V, I_{BIAS} = 20mA, I_{MOD} = 30mA, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AUTOMATIC POWER-CONTROL LOOP							
MD Reverse Bias Voltage		18µA ≤ I_{MD} ≤ 1500µA		1.6			V
MD Average Current Range	I_{MD}	Average current into MD pin		18		1500	µA
Average Power-Setting Stability		APC closed loop (Notes 4, 7)	I_{BIAS} = 1mA (MAX3735)	-880		+880	ppm/°C
			I_{BIAS} = 1mA (MAX3735A)	-110		+110	
			I_{BIAS} = 100mA	-650		+650	
Average Power Setting Accuracy		APC Closed Loop 1mA ≤ I_{BIAS} ≤ 100mA (Note 8)		-16		+16	%
MD-Current Monitor Gain	I_{PC_MON}	External resistor to GND defines the voltage gain; I_{MD} = 18µA, R_{PC_MON} = 50kΩ	MAX3735	0.8	1	1.23	A/A
			MAX3735A	0.9		1.1	
		I_{MD} = 1.5mA, R_{PC_MON} = 600Ω		0.95	1	1.05	
MD-Current Monitor Gain Stability		18µA ≤ I_{MD} ≤ 1500µA (Notes 4, 6)	MAX3735	-10		+10	%
			MAX3735A	-4		+4	
LASER MODULATOR							
Modulation On-Current Range	I_{MOD}	Current into OUT+ pin; R_L ≤ 15Ω, V_{OUT+}, V_{OUT-} ≥ 0.6V (DC-coupled)		10		60	mA
		Current into OUT+ pin; R_L ≤ 15Ω, V_{OUT+}, V_{OUT-} ≥ 2.0V (AC-coupled)		10		85	
Modulation Off-Current	I_{MODOFF}	Current into OUT+ pin during TX_FAULT or TX_DISABLE				100	µA
Modulation-Current Stability (Note 4)		I_{MOD} = 10mA		-480		+480	ppm/°C
		I_{MOD} = 60mA		-255		+255	
Modulation-Current Absolute Accuracy		10mA ≤ I_{MOD} ≤ 60mA (Note 8)		-15		+15	%
Modulation-Current Rise Time	t_R	20% to 80%, 10mA ≤ I_{MOD} ≤ 60mA (Note 4)			42	65	ps
Modulation-Current Fall Time	t_F	20% to 80%, 10mA ≤ I_{MOD} ≤ 60mA (Note 4)			50	80	ps
Deterministic Jitter		10mA ≤ I_{MOD} ≤ 60mA at 2.67Gbps (Notes 4, 9, 10)			18	38	ps
		At 1.25Gbps (K28.5 pattern)			11.5		
		At 622Mbps (Note 9)			18		
		At 155Mbps (Note 9)			40		
Random Jitter	RJ	10mA ≤ I_{MOD} ≤ 60mA (Note 4)			0.7	1.0	ps_{RMS}

2.7Gbps, Low-Power SFP Laser Drivers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +85°C. Typical values at V_{CC} = +3.3V, I_{BIAS} = 20mA, I_{MOD} = 30mA, T_A= +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SAFETY FEATURES							
Excessive Bias-Current Comparator Threshold Range		TX_FAULT always occurs for $V_{BC\_MON} \geq$ 1.38V, TX_FAULT never occurs for $V_{BC\_MON} \leq$ 1.22V		1.22	1.30	1.39	V
Excessive MD-Current Comparator Threshold Range		TX_FAULT always occurs for $V_{PC\_MON} \geq$ 1.38V, TX_FAULT never occurs for $V_{PC\_MON} \leq$ 1.22V		1.22	1.30	1.39	V
SFP TIMING REQUIREMENTS							
TX_DISABLE Assert Time	t_off	Time from rising edge of TX_DISABLE to $I_{BIAS} = I_{BIASOFF}$ and $I_{MOD} = I_{MODOFF}$ (Note 4)			0.14	5	µs
TX_DISABLE Negate Time	t_on	Time from falling edge of TX_DISABLE to I_{BIAS} and I_{MOD} at 95% of steady state when TX_FAULT = 0 before reset	C_{APC} = 2.7nF, MAX3735 (Note 4)			1	ms
			MAX3735A (Note 11)			600	µs
TX_DISABLE Negate Time During FAULT Recovery	t_onFAULT	Time from falling edge of TX_DISABLE to I_{BIAS} and I_{MOD} at 95% of steady state when TX_FAULT = 1 before reset (Note 4)			60	200	ms
TX_FAULT Reset Time or Power-On Time	t_init	From power-on or negation of TX_FAULT using TX_DISABLE (Note 4)			60	200	ms
TX_FAULT Assert Time	t_fault	Time from fault to TX_FAULT on, $C_{FAULT} \leq$ 20pF, R_{FAULT} = 4.7kΩ (Note 4)			3.3	50	µs
TX_DISABLE to Reset		Time TX_DISABLE must be held high to reset TX_FAULT (Note 4)				5	µs

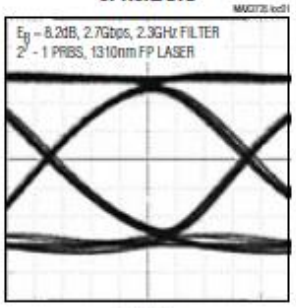
Note 1: Specifications at -40°C are guaranteed by design and characterization. Dice are tested at T_A = +25°C only.
Note 2: Maximum value is specified at I_{MOD} = 60mA, I_{BIAS} = 100mA.
Note 3: TX_FAULT is an open-collector output and must be pulled up with a 4.7kΩ to 10kΩ resistor.
Note 4: Guaranteed by design and characterization.
Note 5: V_{CC} turn-on time must be ≤ 0.8s, DC-coupled interface.
Note 6: Gain stability is defined by the digital diagnostic document (SFF-8472, rev. 9.0) over temperature and supply variation.
Note 7: Assuming that the laser diode to photodiode transfer function does not change with temperature.
Note 8: Accuracy refers to part-to-part variation.
Note 9: Deterministic jitter is measured using a 2^{23} - 1 PRBS or equivalent pattern.
Note 10: Broadband noise is filtered through the network as shown in Figure 3. One capacitor, C < 0.47µF, and one 0603 ferrite bead or inductor can be added (optional). This supply voltage filtering reduces the hot-plugging inrush current. The supply noise must be < 100mV$_{P-P}$ up to 2MHz.
Note 11: C_{APC} values chosen as shown in Table 4 (MAX3735A).

2.7Gbps, Low-Power SFP Laser Drivers

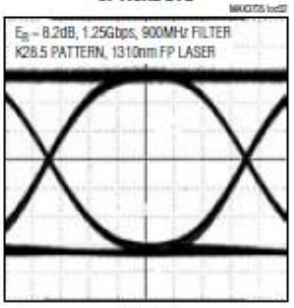
Typical Operating Characteristics

(V_{CC} = +3.3V, C_{APC} = 0.01µF, I_{BIAS} = 20mA, and I_{MOD} = 30mA, T_A = +25°C, unless otherwise noted.)

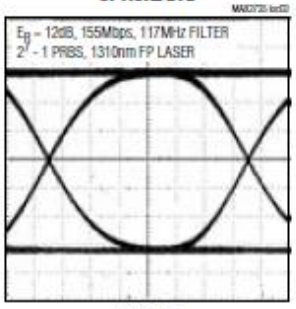
OPTICAL EYE



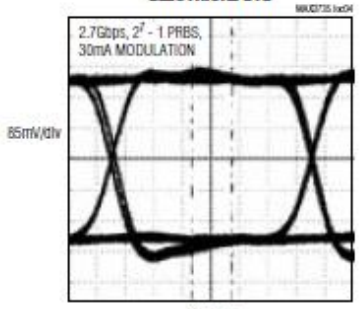
OPTICAL EYE



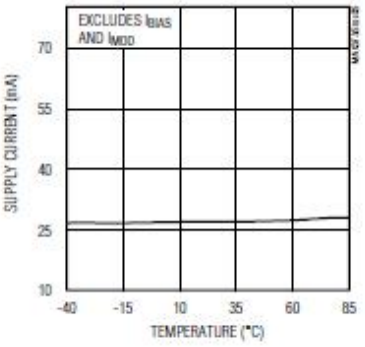
OPTICAL EYE



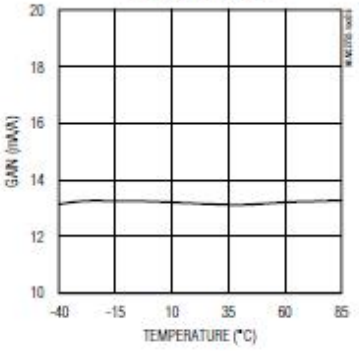
ELECTRICAL EYE



SUPPLY CURRENT vs. TEMPERATURE



BIAS-CURRENT MONITOR GAIN vs. TEMPERATURE

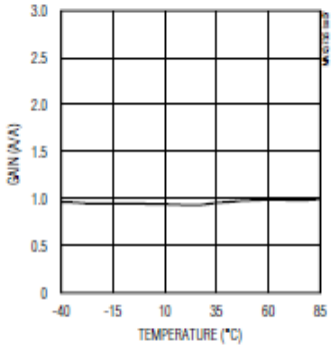


2.7Gbps, Low-Power SFP Laser Drivers

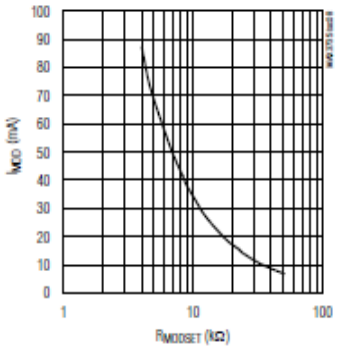
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, C_{APC} = 0.01µF, I_{BIAS} = 20mA, and I_{MOD} = 30mA, T_A = +25°C, unless otherwise noted.)

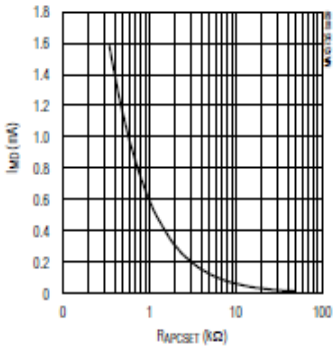
PHOTOCURRENT MONITOR GAIN vs. TEMPERATURE



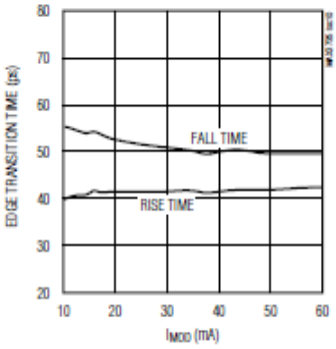
MODULATION CURRENT vs. R_{MODSET}



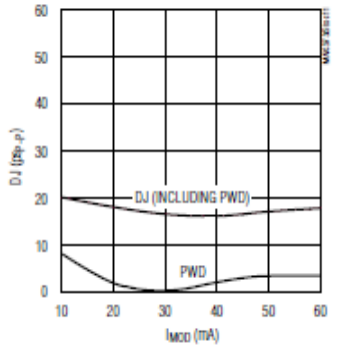
MONITOR DIODE CURRENT vs. R_{APCSET}



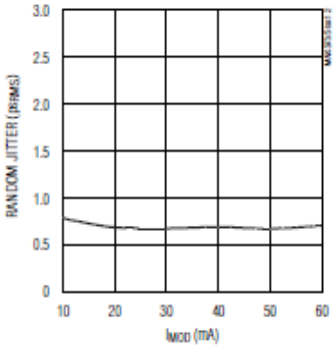
EDGE TRANSITION TIME vs. MODULATION CURRENT



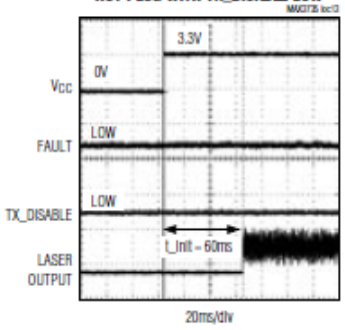
DETERMINISTIC JITTER vs. MODULATION CURRENT



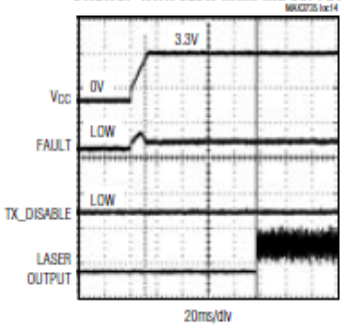
RANDOM JITTER vs. MODULATION CURRENT



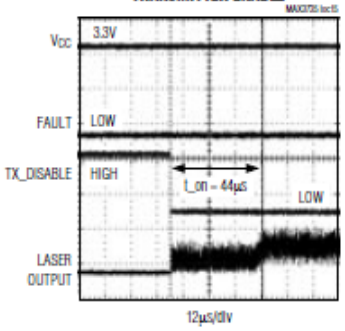
HOT PLUG WITH TX_DISABLE LOW



STARTUP WITH SLOW RAMPING SUPPLY



TRANSMITTER ENABLE

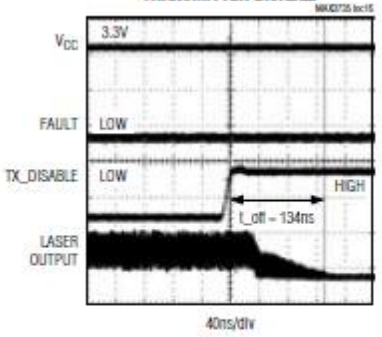


2.7Gbps, Low-Power SFP Laser Drivers

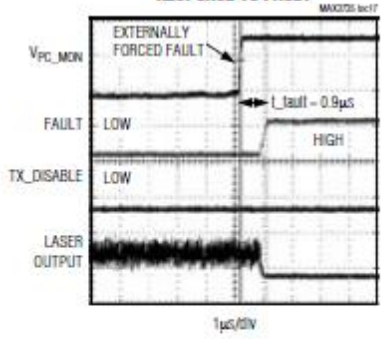
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, C_{APC} = 0.01µF, I_{BIAS} = 20mA, and I_{MOD} = 30mA, T_A = +25°C, unless otherwise noted.)

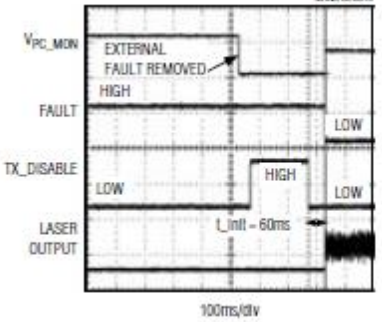
TRANSMITTER DISABLE



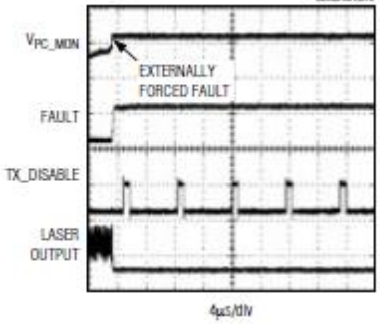
RESPONSE TO FAULT



FAULT RECOVERY TIME



FREQUENT ASSERTION OF TX_DISABLE



2.7Gbps, Low-Power SFP Laser Drivers

Pin Description

PIN	NAME	FUNCTION
1, 4, 8, 14, 18	V_{CC}	+3.3V Supply Voltage
2	IN+	Noninverted Data Input
3	IN-	Inverted Data Input
5	PC_MON	Photodiode Current Monitor Output. Current out of this pin develops a ground-referenced voltage across an external resistor that is proportional to the monitor diode current.
6	BC_MON	Bias Current Monitor Output. Current out of this pin develops a ground-referenced voltage across an external resistor that is proportional to the bias current.
7, 12, 22	GND	Ground
9	SHUTDOWN	Shutdown Driver Output. Voltage output to control an external transistor for optional shutdown circuitry.
10	TX_FAULT	Open-Collector Transmit Fault Indicator (Table 1).
11	MODSET	A resistor connected from this pad to ground sets the desired modulation current.
13	BIAS	Laser Bias Current Output
15, 16	OUT+	Noninverted Modulation Current Output. Connect pins 15 and 16 externally to minimize parasitic inductance of the package. I_{MOD} flows into this pin when input data is high.
17	OUT-	Inverted Modulation Current Output. I_{MOD} flows into this pin when input data is low.
19	MD	Monitor Diode Input. Connect this pin to the anode of a monitor photodiode. A capacitor to ground is required to filter the high-speed AC monitor photocurrent.
20	APCFILT1	Connect a capacitor (C_{APC}) between pin 20 (APCFILT1) and pin 21 (APCFILT2) to set the dominant pole of the APC feedback loop.
21	APCFILT2	See APCFILT1
23	APCSET	A resistor connected from this pin to ground sets the desired average optical power.
24	TX_DISABLE	Transmitter Disable, TTL. Laser output is disabled when TX_DISABLE is asserted high or left unconnected. The laser output is enabled when this pin is asserted low.
EP	Exposed Pad	Ground. Must be soldered to the circuit board ground for proper thermal and electrical performance (see the *Exposed Pad Package* section).

Detailed Description

The MAX3735/MAX3735A laser drivers consist of three parts: a high-speed modulation driver, a laser-biasing block with automatic power control (APC), and safety circuitry (Figure 4). The circuit design is optimized for high-speed and low-voltage (+3.3V) operation.

High-Speed Modulation Driver

The output stage are composed of a high-speed differential pair and a programmable modulation current source. The MAX3735/MAX3735A are optimized for driving a 15Ω load; the minimum instantaneous voltage required at OUT+ is 0.6V. Modulation current swings up to 60mA are possible when the laser diode is DC-coupled to the driver and up to 85mA when the laser diode is AC-coupled to the driver.

To interface with the laser diode, a damping resistor (R_D) is required for impedance matching. The combined resistance of the series damping resistor and the equivalent series resistance of the laser diode should equal 15Ω. To reduce optical output aberrations and duty-cycle distortion caused by laser diode parasitic inductance, an RC shunt network might be necessary. Refer to Maxim Application Note HFAN 02.0: *Interfacing Maxim's Laser Drivers to Laser Diodes* for more information.

At data rates of 2.7Gbps, any capacitive load at the cathode of a laser diode degrades optical output performance. Because the BIAS output is directly connected to the laser cathode, minimize the parasitic capacitance associated with the pin by using an inductor to isolate the BIAS pin parasitics from the laser cathode.

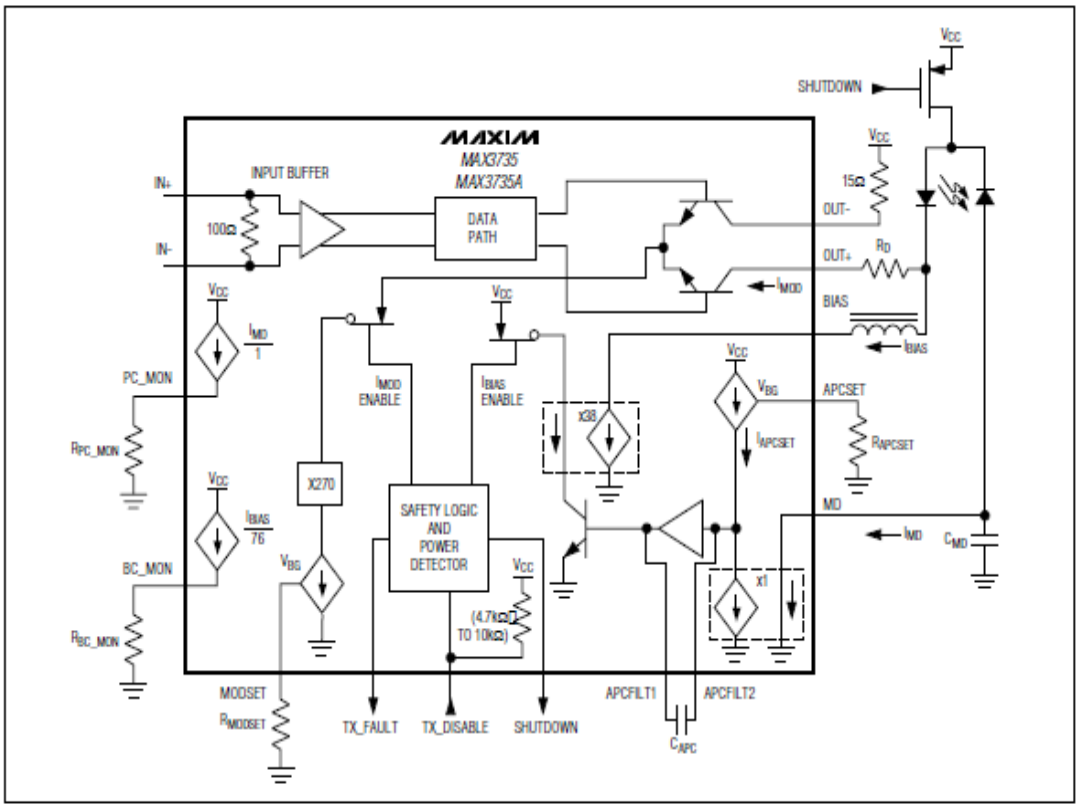


Figure 4. Functional Diagram

Laser-Biasing and APC

To maintain constant average optical power, the MAX3735/MAX3735A incorporate an APC loop to compensate for the changes in laser threshold current over temperature and lifetime. A back-facet photodiode mounted in the laser package is used to convert the optical power into a photocurrent. The APC loop adjusts the laser bias current so that the monitor current is matched to a reference current set by R_{APCSET}. The time constant of the APC loop is determined by an external capacitor (C_{APC}). For possible C_{APC} values, see the *Applications Information* section.

Safety Circuitry

The safety circuitry contains an input disable (TX_DISABLE), a latched fault output (TX_FAULT), and fault detectors (Figure 5). This circuitry monitors the operation of the laser driver and forces a shutdown if a fault is detected (Table 1). A single-point fault can be a short to V_{CC} or GND. See Table 2 to view the circuit response to various single-point failures. The transmit fault condition is latched until reset by a toggle of TX_DISABLE or V_{CC}. The laser driver offers redundant laser diode shutdown through the optional shutdown circuitry (see the *Typical Applications Circuit*). The TX_FAULT pin should be pulled high with a 4.7kΩ to 10kΩ resistor to V_{CC} as required by the SFP MSA.

Safety Circuitry Current Monitors

The MAX3735/MAX3735A feature monitors (BC_MON, PC_MON) for bias current (I_{BIAS}) and photo current (I_{MD}). The monitors are realized by mirroring a fraction of the currents and developing voltages across external resistors connected to ground. Voltages greater than 1.38V at PC_MON or BC_MON result in a fault state. For example, connecting a 100Ω resistor to ground on each monitor output gives the following relationships:

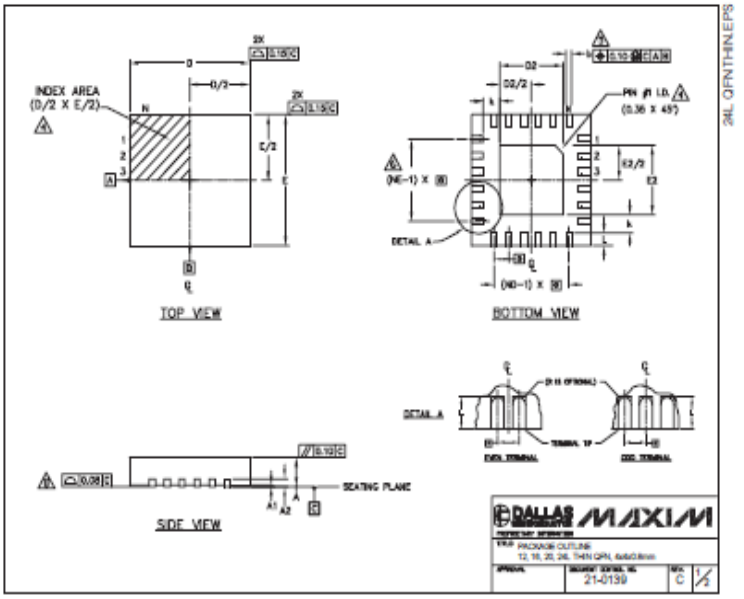
$$V_{BC\_MON} = (I_{BIAS} / 76) \times 100\Omega$$

$$V_{PC\_MON} = I_{MD} \times 100\Omega$$

2.7Gbps, Low-Power SFP Laser Drivers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG.	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2		0.20 REF			0.20 REF			0.20 REF			0.20 REF	
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e		0.50 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.	
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
JEDEC SPEC	WGEB			WGEC			WGED-1			WGED-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3 AND T2444-4.

DALLAS MAXIM
21-0139

19-1601; Rev 2; 11/05

EVALUATION KIT AVAILABLE

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

MAX3665

General Description

The MAX3665 low-power transimpedance preamplifier for 622Mbps SDH/SONET applications consumes only 70mW at V_{CC} = 3.3V. Operating from a single +3.3V or +5.0V supply, it converts a small photodiode current to a measurable differential voltage. A DC cancellation circuit provides a true differential output swing over a wide range of input current levels, thus reducing pulse-width distortion. The differential outputs are back-terminated with 50Ω per side.

The overall transimpedance gain is nominally 8kΩ. For input signal levels beyond approximately 50µAp-p, the amplifier will limit the output swing to 250mV. The MAX3665's low 55nA input noise provides a typical sensitivity of -33.2dBm in 1300nm, 622Mbps receivers.

The MAX3665 is designed to be used in conjunction with the MAX3676 clock recovery and data retiming IC with limiting amplifier. Together they form a complete 3.3V or 5.0V 622Mbps SDH/SONET receiver.

In die form, the MAX3665 is designed to fit on a header with a PIN diode. It includes a filter connection that provides positive bias for the photodiode through a 1.5kΩ resistor to V_{CC}. The device is available in an 8-pin µMAX® package.

Applications

SDH/SONET Receivers

PIN Photodiode Preamplifiers and Receivers

Regenerators for SDH/SONET

Features

- +3.3V or +5.0V Single-Supply Operation
- 55nA$_{RMS}$ Input-Referred Noise
- 70mW Power Consumption at V_{CC} = 3.3V
- 8kΩ Gain
- 450µA Peak Input Current
- 260ps (max) Deterministic Jitter
- Differential Output Drives 100Ω Load
- 470MHz Bandwidth

Ordering Information

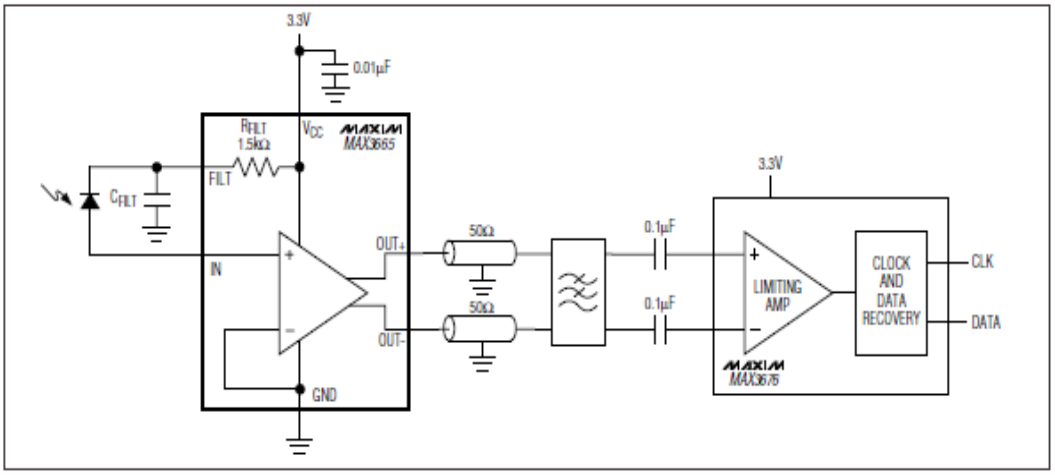
PART	TEMP RANGE	PIN-PACKAGE
MAX3665EUA	-40°C to +85°C	8 µMAX
MAX3665E/D	(see Note)	Dice

Note: *Dice are designed to operate over a -40°C to +140°C junction temperature (T_J) range, but are tested and guaranteed at T_A = +25°C.*

Pin Configuration appears at end of data sheet.

µMAX is a registered trademark of Maxim Integrated Products, Inc.

Typical Application Circuit



622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.5V to +6.5V
Continuous Current at IN ..... ±5mA
Voltage at OUT+, OUT- ..... (V_{CC} - 1.5V) to (V_{CC} + 0.5V)
Voltage at FILT ..... -0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
8-Pin µMAX (derate 4.5mW/°C above +85°C) 295mW
Operating Junction Temperature (die) ..... -55°C to +150°C
Processing Temperature (die) ..... +400°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V ±10% or +5.0V ±10%, 100Ω load between OUT+ and OUT-, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Voltage	V_{IN}	I_{IN} = 0 to 300µA		0.8	0.95	V
Gain Nonlinearity		I_{IN} = 0 to 10µA$_{P-P}$			±5	%
Supply Current	I_{CC}	I_{IN} = 0		21	30	mA
Small-Signal Transimpedance	z_{21}	Differential output	7	8		kΩ
Output Common-Mode Voltage				V_{CC} - 0.15		V
Differential Output Offset	ΔV_{OUT}	I_{IN} = 300µA		±5		mV
Output Impedance (per side)	Z_{OUT}		48	50	52	Ω
Maximum Output Voltage	$V_{OUT(MAX)}$	I_{IN} = 450µA$_{P-P}$		260	450	mV$_{P-P}$
Filter Resistor	R_{FILT}			1.5		kΩ

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V ±10% or +5.0V ±10%, 100Ω load between OUT+ and OUT-, source capacitance = 0.5pF, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Notes 1 and 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Bandwidth	BW_{-3dB}	Relative to gain at 10MHz	404	470		MHz
Low-Frequency Cutoff		-3dB with I_{IN} = 5µA		20	40	kHz
Deterministic Jitter	J_D	2^{13} - 1 PRBS with 100 CIDs		100	260	ps
RMS Noise Referred to Input	i_n			55	72	nA
Power-Supply Rejection Ratio	PSRR	f < 1MHz, differential referred to output, ΔV_{CC} = 30mV$_{P-P}$ (Note 3)	36	47		dB

Note 1: AC characteristics are guaranteed by design.
Note 2: Measured with a 3-pole filter at the output. C_{IN} = 0.5pF, I_{IN} = 0, C_{FILT} = 1000pF.
Note 3: PSRR = -20log (ΔV_{OUT} / ΔV_{CC}).

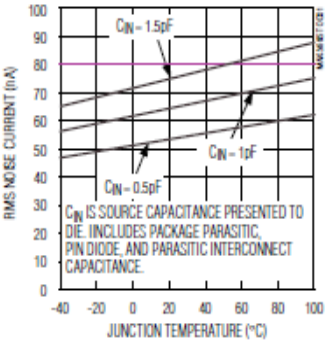
622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

MAX3665

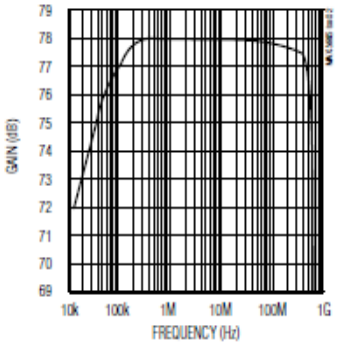
Typical Operating Characteristics

(V_{CC} = +3.3V, includes off-chip filter, see Figure 3b, T_A = +25°C, unless otherwise noted.)

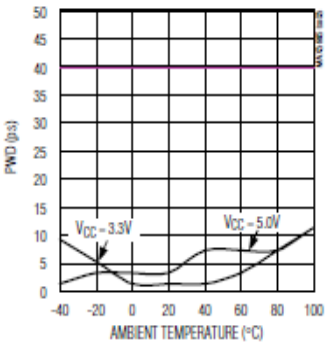
INPUT-REFERRED NOISE vs. TEMPERATURE



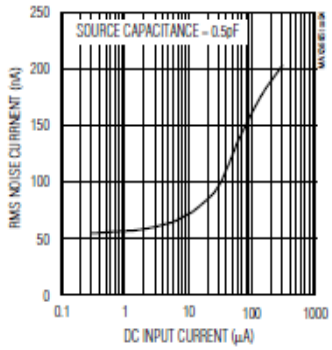
SMALL-SIGNAL GAIN vs. FREQUENCY



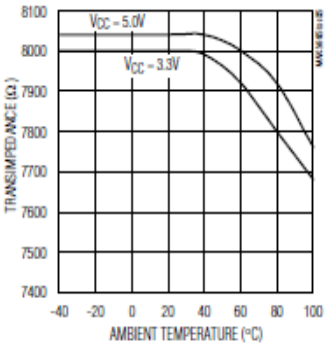
PULSE-WIDTH DISTORTION vs. TEMPERATURE (INPUT = 100µAp-p)



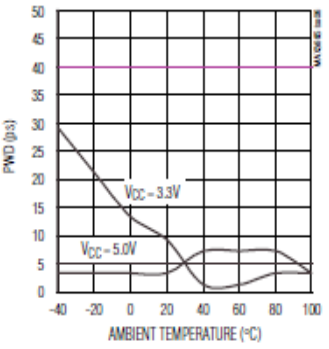
INPUT-REFERRED NOISE vs. DC INPUT CURRENT



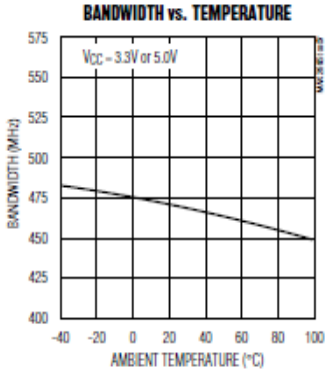
SMALL-SIGNAL TRANSIMPEDANCE vs. TEMPERATURE



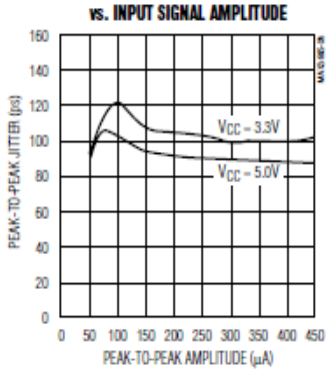
PULSE-WIDTH DISTORTION vs. TEMPERATURE (INPUT = 450µAp-p)



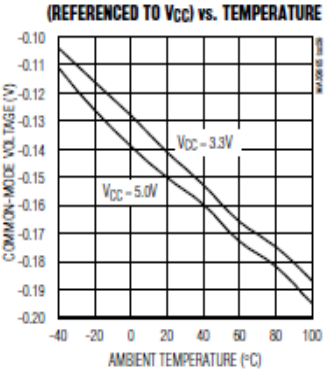
BANDWIDTH vs. TEMPERATURE



DATA-DEPENDENT JITTER vs. INPUT SIGNAL AMPLITUDE



OUTPUT COMMON-MODE VOLTAGE (REFERENCED TO VCC) vs. TEMPERATURE



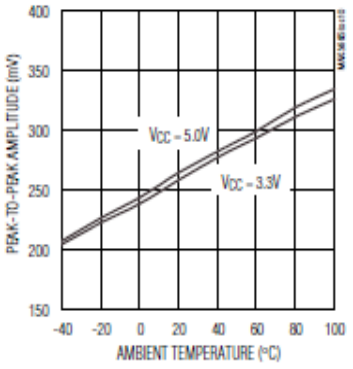
622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

MAX3665

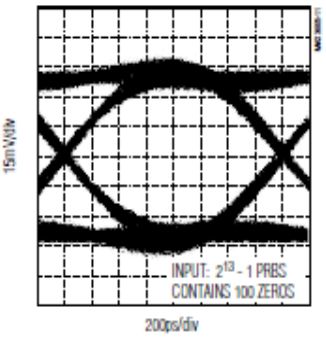
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, includes off-chip filter, see Figure 3b, T_A = +25°C, unless otherwise noted.)

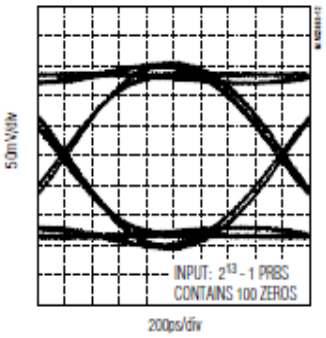
DIFFERENTIAL OUTPUT AMPLITUDE vs. TEMPERATURE (INPUT = 450µAp-p)



EYE DIAGRAM (INPUT = 10µAp-p)



EYE DIAGRAM (INPUT = 450µAp-p)



Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	+3.3V or +5.0V Supply Voltage
2	IN	Signal Input (From Photodiode)
3	N.C.	No Connection. Not internally connected.
4	FILT	On-Chip Resistor for Filtering Photodiode Supply Voltage
5, 8	GND	Ground
6	OUT+	Noninverting Voltage Output. Current flowing into IN causes V_{OUT+} to increase.
7	OUT-	Inverting Voltage Output. Current flowing into IN causes V_{OUT-} to decrease.

Detailed Description

The MAX3665 is a transimpedance amplifier designed for 622Mbps SDH/SONET applications. It comprises a transimpedance amplifier, a paraphase amplifier with CML differential outputs, and a DC cancellation loop. Figure 1 shows a functional diagram of the MAX3665.

Transimpedance Amplifier

The signal current at IN flows into the summing node of a high-gain amplifier. Shunt feedback through R_F converts this current to a voltage. Diodes D1 and D2 clamp the output voltage for large input currents.

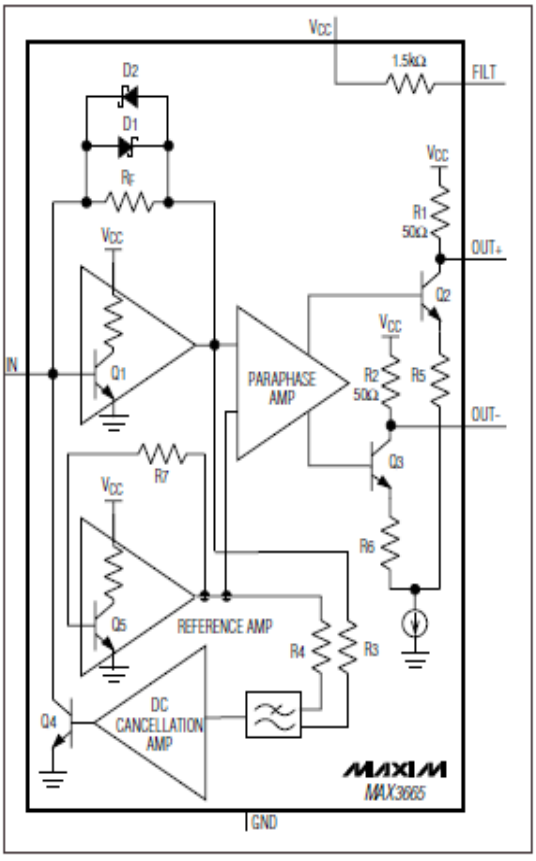
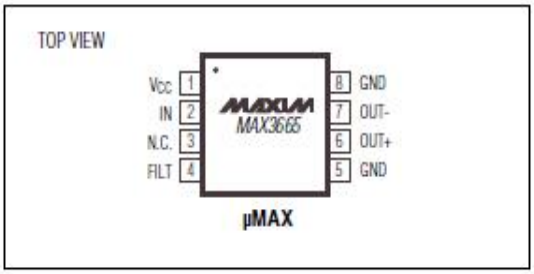


Figure 1. Functional Diagram

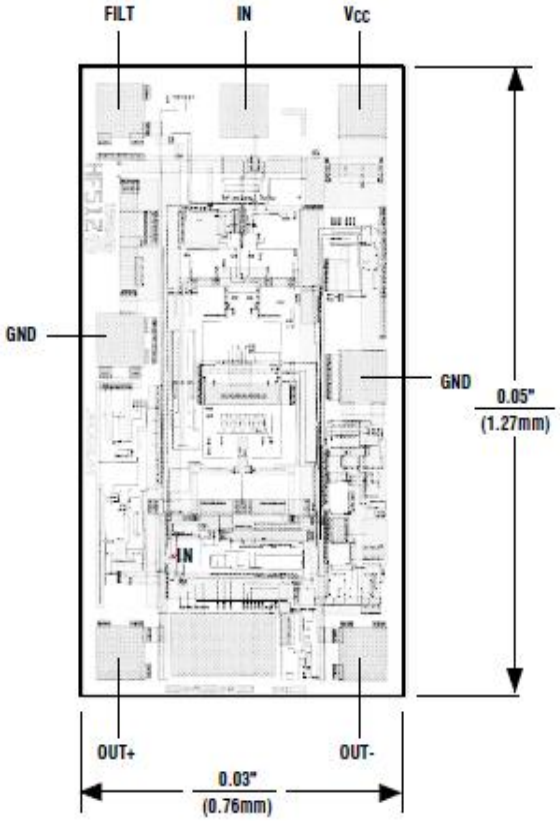
622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

MAX3665

Pin Configuration



Chip Topography



TRANSISTOR COUNT: 443
SUBSTRATE CONNECTED TO GND

19-2717; Rev 6; 6/11

EVALUATION KIT AVAILABLE

Compact 155Mbps to 4.25Gbps Limiting Amplifier

MAX3748

General Description

The MAX3748 multirate limiting amplifier functions as a data quantizer for SONET, Fibre Channel, and Gigabit Ethernet optical receivers. The amplifier accepts a wide range of input voltages and provides constant-level current-mode logic (CML) output voltages with controlled edge speeds.

A received-signal-strength indicator (RSSI) is available when the MAX3748 is combined with the MAX3744 SFP transimpedance amplifier (TIA). A receiver consisting of the MAX3744 and the MAX3748 can provide up to 19dB RSSI dynamic range. Additional features include a programmable loss-of-signal (LOS) detect, an optional disable function (DISABLE), and an output signal polarity reversal (OUTPOL). Output disable can be used to implement squelch.

The combination of the MAX3748 and the MAX3744 allows for the implementation of all the small-form-factor SFF-8472 digital diagnostic specifications using a standard 4-pin TO-46 header. The MAX3748 is packaged in a 3mm x 3mm, 16-pin thin QFN package with an exposed pad.

Applications

Gigabit Ethernet SFF/SFP Transceiver Modules

Fibre Channel SFF/SFP Transceiver Modules

Multirate OC-3 to OC-48-FEC SFF/SFP Transceiver Modules

Features

- **SFP Reference Design Available**
- **16-Pin TQFN Package with 3mm x 3mm Footprint**
- **Single 3.3V Supply Voltage**
- **86ps Rise and Fall Time**
- **Loss of Signal with Programmable Threshold**
- **RSSI Interface (with MAX3744 TIA)**
- **Output Disable**
- **Polarity Select**
- **8.7psP-P Deterministic Jitter (4.25Gbps)**

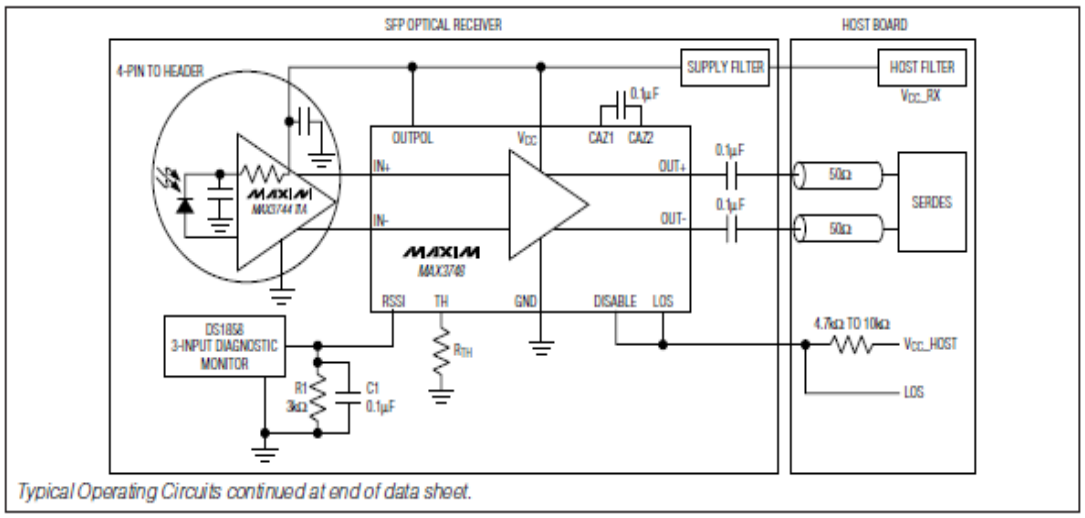
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3748HETE#G16*	-40°C to +85°C	16 TQFN-EP**
MAX3748ETE	-40°C to +85°C	16 TQFN-EP**

*H = hybrid lead-free package. *See Detailed Description for more information. The MAX3748H is the MAX3748 in a hybrid lead-free package.*
#Denotes a RoHS-compliant device that may include lead that is exempt under the RoHS requirements.
***EP = Exposed pad.*

Functional Diagram and Pin Configuration appear at end of data sheet.

Typical Operating Circuits



Typical Operating Circuits continued at end of data sheet.

Compact 155Mbps to 4.25Gbps Limiting Amplifier

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}) ..... -0.5V to +6.0V
Voltage at IN+, IN- ..... (V_{CC} - 2.4V) to (V_{CC} + 0.5V)
Voltage at DISABLE, OUTPOL, RSSI, CAZ1, CAZ2, LOS, TH ..... -0.5V to (V_{CC} + 0.5V)
Current into LOS ..... -1mA to +9mA
Differential Input Voltage (IN+ - IN-) 2.5V
Continuous Current at CML Outputs (OUT+, OUT-) ..... -25mA to +25mA

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 17.7mW above +70°C) 1.4W
Operating Junction Temperature Range (T_J) ..... -55°C to +150°C
Storage Ambient Temperature Range (T_S) ..... -55°C to +150°C
Lead Temperature (soldering, 10s) ..... +260°C
Soldering Temperature (reflow)
TQFN ..... +240°C
Hybrid TQFN ..... +250°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.97V to 3.63V, ambient temperature = -40°C to +85°C, CML output load is 50Ω to V_{CC}, C_{AZ} = 0.1µF, typical values are at +25°C, V_{CC} = 3.3V, unless otherwise specified. The data input transition time is controlled by a 4th-order Bessel filter with f_{-3dB} = 0.75 × 2.667GHz for all data rates of 2.667Gbps and below, and with f_{-3dB} = 0.75 × data rate for data rates > 3.2Gbps.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Single-Ended Input Resistance		Single ended to V_{CC}	42	50	58	Ω
Input Return Loss		Differential, f < 3GHz, DUT is powered on		13		dB
Input Sensitivity	V_{IN-MIN}	(Note 1)			5	mV_{p-p}
Input Overload	V_{IN-MAX}	(Note 1)	1200			mV_{p-p}
Single-Ended Output Resistance		Single ended to V_{CC}	42	50	58	Ω
Output Return Loss		Differential, f < 3GHz, DUT is powered on		10		dB
Differential Output Voltage			600	780	1200	mV_{p-p}
Differential Output Signal when Disabled		Outputs AC-coupled, V_{IN-MAX} applied to input (Note 2)			10	mV_{p-p}
Deterministic Jitter (Notes 2, 3)	DJ	K28.5 pattern at 4.25Gbps		8.7	25	ps_{p-p}
		K28.5 pattern at 3.2Gbps		8.5	25	
		2^{23}- 1 PRBS equivalent pattern at 2.7Gbps (Note 4)		9.3	30	
		K28.5 pattern at 2.1Gbps		7.8	25	
		2^{23}- 1 PRBS equivalent pattern at 155Mbps		25	50	
Random Jitter (Note 5)		Input = 5mVp-p		6.5		ps_{RMS}
		Input = 10mVp-p		3		
Data Output Transition Time		20% to 80%, 4.25Gbps 3.1875GHz Bessel input filter V_{IN} = 20mVp-p		60		ps
		20% to 80% (Note 2)		86	115	
Input-Referred Noise				185		$µV_{RMS}$
Low-Frequency Cutoff		C_{AZ} = open		70		kHz
		C_{AZ} = 0.1µF		0.8		
Power-Supply Current	I_{CC}	(Note 6)		32	49	mA
		LOS disabled			37	
Power-Supply Noise Rejection	PSNR	f < 2MHz		26		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to 3.63V, ambient temperature = -40°C to +85°C, CML output load is 50Ω to V_{CC}, C_{AZ} = 0.1µF, typical values are at +25°C, V_{CC} = 3.3V, unless otherwise specified. The data input transition time is controlled by a 4th-order Bessel filter with f_{-3dB} = 0.75 x 2.667GHz for all data rates of 2.667Gbps and below, and with f_{-3dB} = 0.75 x data rate for data rates > 3.2Gbps.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOSS OF SIGNAL at 4.25Gbps K28.5 pattern (Note 2)						
LOS Hysteresis		10log ($V_{DEASSERT}/V_{ASSERT}$)	1.25	2.2		dB
LOS Assert/Deassert Time		(Note 8)	2		100	µs
LOS Assert		R_{TH} = 280kΩ		18.5		mVp-p
LOS Deassert		R_{TH} = 280kΩ		28		mVp-p
LOSS OF SIGNAL at 2.5Gbps (Notes 2, 7)						
LOS Hysteresis		10log ($V_{DEASSERT}/V_{ASSERT}$)	1.25	2.2		dB
LOS Assert/Deassert Time		(Note 8)	2		100	µs
Low LOS Assert Level		R_{TH} = 20kΩ	2.8	4.1		mVp-p
Low LOS Deassert Level		R_{TH} = 20kΩ		6.7	11.6	mVp-p
Medium LOS Assert Level		R_{TH} = 280Ω	10.3	15.2		mVp-p
Medium LOS Deassert Level		R_{TH} = 280Ω		25	38.6	mVp-p
High LOS Assert Level		R_{TH} = 80Ω	22.8	38.3		mVp-p
High LOS Deassert Level		R_{TH} = 80Ω		65.2	99.3	mVp-p
LOSS OF SIGNAL at 155Mbps (Note 7)						
LOS Hysteresis		10log ($V_{DEASSERT}/V_{ASSERT}$)		2.1		dB
LOS Assert/Deassert Time		(Note 8)		20		µs
Low LOS Assert Level		R_{TH} = 20kΩ		3.5		mVp-p
Low LOS Deassert Level		R_{TH} = 20kΩ		5.6		mVp-p
Medium LOS Assert Level		R_{TH} = 280Ω		13.3		mVp-p
Medium LOS Deassert Level		R_{TH} = 280Ω		21.2		mVp-p
High LOS Assert Level		R_{TH} = 80Ω		33.3		mVp-p
High LOS Deassert Level		R_{TH} = 80Ω		55.5		mVp-p
RSSI						
RSSI Current Gain (Note 9)	A_{RSSI}	A_{RSSI} = I_{RSSI}/I_{CM_RSSI}		0.03		
Input-Referred RSSI Current Stability		I_{RSSI}/A_{RSSI} (Note 10) I_{CM_INPUT} < 6.6mA	-31		+33	µA
		I_{RSSI}/A_{RSSI} (Note 10) I_{CM_INPUT} > 6.6mA	-73		+90	µA
TTL/CMOS I/O						
LOS Output High Voltage	V_{OH}	R_{LOS} = 4.7kΩ to10kΩ to V_{CC_host} (3V)	2.4			V
LOS Output Low Voltage	V_{OL}	R_{LOS} = 4.7kΩ to10kΩ to V_{CC_host} (3.6V)			0.4	V
LOS Output Current		R_{LOS} = 4.7kΩ to10kΩ to V_{CC_host} (3.3V); IC is powered down			40	µA
DISABLE Input High	V_{IH}		2.0			V
DISABLE Input Low	V_{IL}				0.8	V
DISABLE Input Current		R_{LOS} = 4.7kΩ to 10kΩ to V_{CC_host}			10	µA

Note 1: Between sensitivity and overload, all AC specifications are met.
Note 2: Guaranteed by design and characterization.
Note 3: The deterministic jitter caused by this filter is not included in the DJ generation specifications (input).

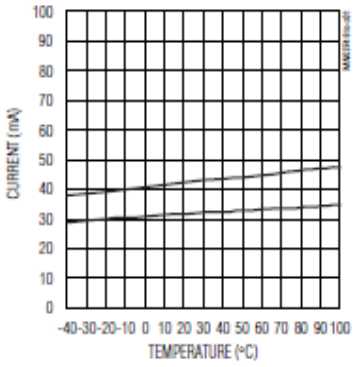
Compact 155Mbps to 4.25Gbps Limiting Amplifier

MAX3748

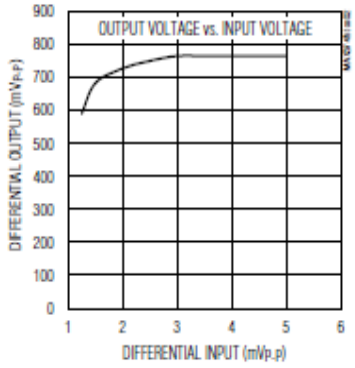
Typical Operating Characteristics

(T_A = +25°C and V_{CC} = 3.3V, unless otherwise specified.)

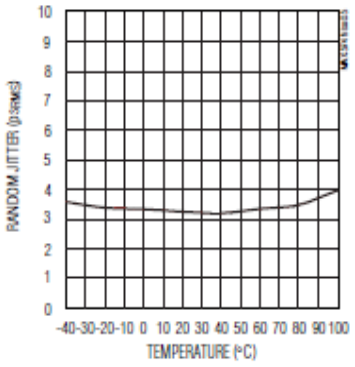
SUPPLY CURRENT vs. TEMPERATURE



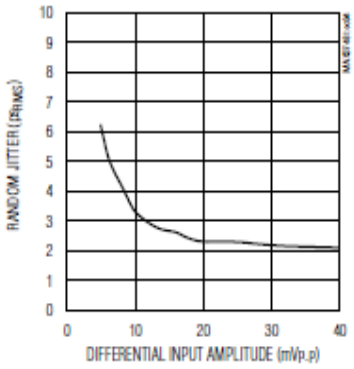
TRANSFER FUNCTION



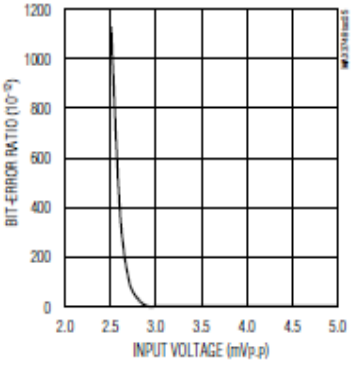
RANDOM JITTER vs. TEMPERATURE (INPUT LEVEL 10mVp-p)



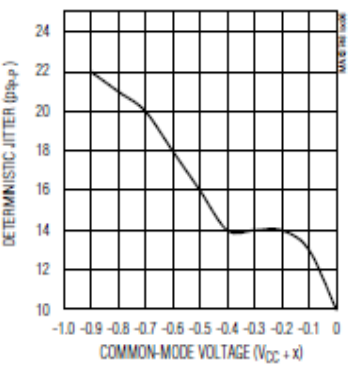
RANDOM JITTER vs. INPUT AMPLITUDE



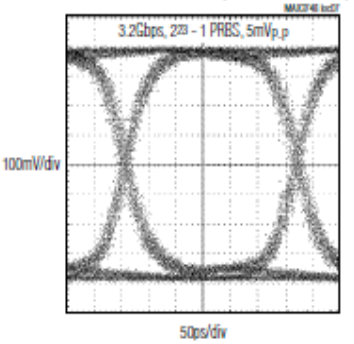
BIT-ERROR RATIO vs. INPUT VOLTAGE



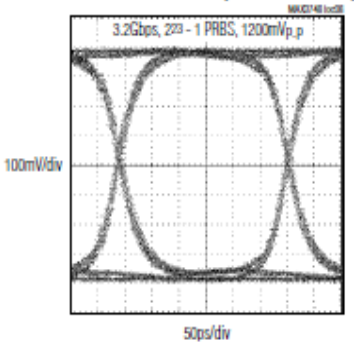
DETERMINISTIC JITTER vs. INPUT COMMON-MODE VOLTAGE (V_{CC} TO V_{CC} - 0.8V)



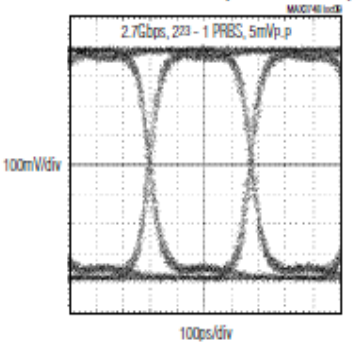
OUTPUT EYE DIAGRAM (MINIMUM INPUT)



OUTPUT EYE DIAGRAM (MAXIMUM INPUT)



OUTPUT EYE DIAGRAM (MINIMUM INPUT)

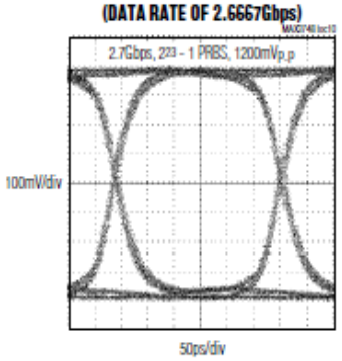


Compact 155Mbps to 4.25Gbps Limiting Amplifier

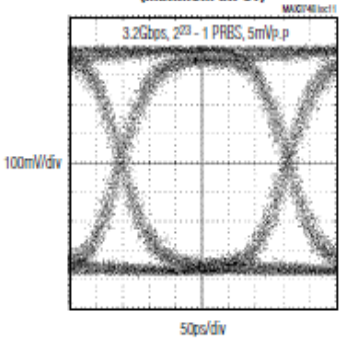
Typical Operating Characteristics (continued)

(T_A = +25°C and V_{CC} = 3.3V, unless otherwise specified.)

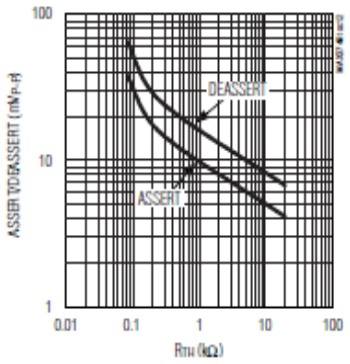
OUTPUT EYE DIAGRAM WITH MAXIMUM INPUT (DATA RATE OF 2.6667Gbps)



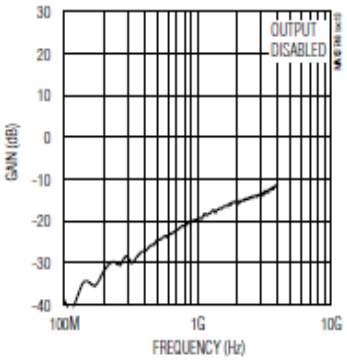
OUTPUT EYE DIAGRAM AT +100°C (MINIMUM INPUT)



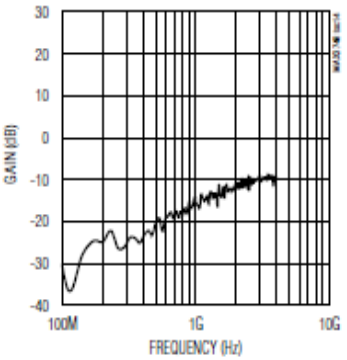
ASSERT/DEASSERT LEVELS vs. R_{TH}



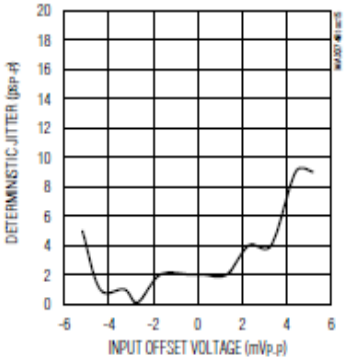
INPUT RETURN GAIN vs. FREQUENCY (SDD11) (INPUT SIGNAL LEVEL = -40dBm)



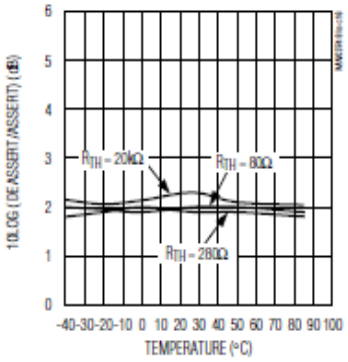
OUTPUT RETURN GAIN vs. FREQUENCY (SDD22) (INPUT SIGNAL LEVEL = -40dBm)



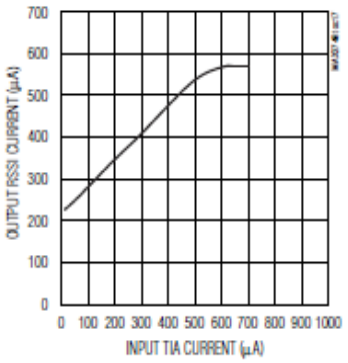
DETERMINISTIC JITTER vs. INPUT OFFSET VOLTAGE (2.667Gbps, K28.5)



LOS HYSTERESIS vs. TEMPERATURE (2.667bps, 2^{10} - 1 PRBS)



RSSI CURRENT GAIN vs. INPUT TIA CURRENT (MAX3744 AND MAX3748)



Compact 155Mbps to 4.25Gbps Limiting Amplifier

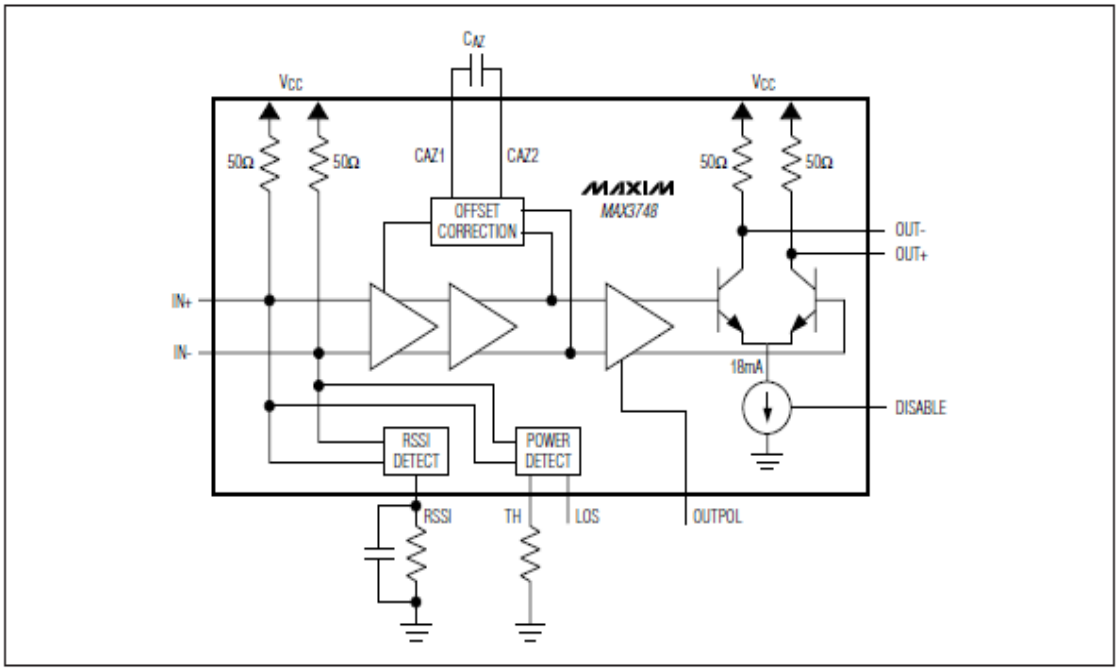
Pin Description

PIN	NAME	FUNCTION
1, 4, 12	V_{CC}	Supply Voltage
2	IN+	Noninverted Input Signal, CML
3	IN-	Inverted Input Signal, CML
5	TH	Loss-of-Signal Threshold Pin. Resistor to ground (R_{TH}) sets the LOS threshold. Connecting this pin to V_{CC} disables the LOS circuitry and reduces power consumption.
6	DISABLE	Disable Input, CMOS/TTL. The data outputs are held static when this pin is asserted high. The LOS function remains active when the outputs are disabled. If routed through the DS1858/DS1859 controller IC, no additional ESD protection is required.
7	LOS	Noninverted Loss-of-Signal Output. LOS is asserted high when the signal drops below the assert threshold set by the TH input. The output is open collector (Figure 5). If routed through the DS1858/DS1859 controller IC, no additional ESD protection is required.
8, 16	GND	Supply Ground
9	OUTPOL	Output Polarity Control Input. Connect to GND for an inversion of polarity through the limiting amplifier and connect to V_{CC} for normal operation.
10	OUT-	Inverted Data Output, CML
11	OUT+	Noninverted Data Output, CML
13	RSSI	Received-Signal-Strength Indicator. This current output can be used to obtain a ground-referenced voltage proportional to photodiode current with the MAX3744 by connecting an external resistor between this pin and GND.
14	CAZ2	Offset Correction Loop Capacitor Connection. A capacitor connected between this pin and CAZ1 extends the time constant of the offset correction loop. Typical value of C_{AZ} is 0.1µF. The offset correction is disabled when the CAZ1 and CAZ2 pins are shorted together.
15	CAZ1	Offset Correction Loop Capacitor Connection. A capacitor connected between this pin and CAZ2 extends the time constant of the offset correction loop. Typical value of C_{AZ} is 0.1µF. The offset correction is disabled when the CAZ1 and CAZ2 pins are shorted together.
—	EP	Exposed Paddle. Connect the exposed paddle to board ground for optimal electrical and thermal performance.

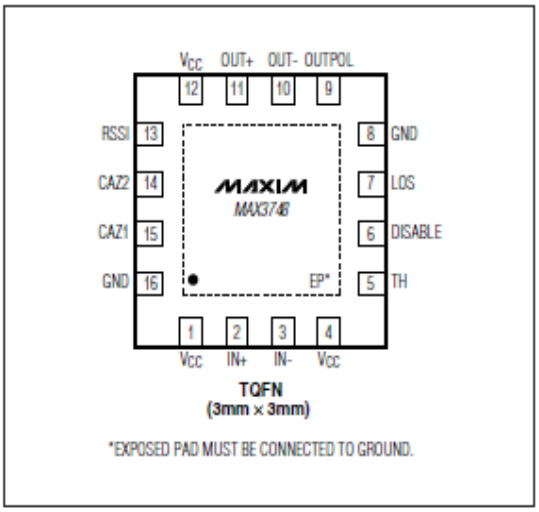
Compact 155Mbps to 4.25Gbps Limiting Amplifier

MAX3748

Functional Diagram



Pin Configuration



TQFN
(3mm × 3mm)

*EXPOSED PAD MUST BE CONNECTED TO GROUND.

Chip Information

PROCESS: SiGe BIPOLAR

Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1633F-3, T1633FH-3	21-0136	90-0033

MC100EPT21

3.3V Differential LVPECL/LVDS/CML to LVTTL/LVCMOS Translator

The MC100EPT21 is a Differential LVPECL/LVDS/CML to LVTTL/LVCMOS translator. Because LVPECL (Positive ECL), LVDS, and positive CML input levels and LVTTL/LVCMOS output levels are used, only +3.3 V and ground are required. The small outline 8–lead SOIC package makes the EPT21 ideal for applications which require the translation of a clock or data signal.

The V_{BB} output allows this EPT21 to be cap coupled in either single–ended or differential input mode. When single–ended cap coupled, V_{BB} output is tied to the $\overline{D}$ input and D is driven for a non–inverting buffer, or V_{BB} output is tied to the D input and $\overline{D}$ is driven for an inverting buffer. When cap coupled differentially, V_{BB} output is connected through a resistor to each input pin. If used, the V_{BB} pin should be bypassed to V_{CC} via a 0.01 µF capacitor. For additional information see AND8020/D. For a single–ended direct connection use an external voltage reference source such as a resistor divider. Do not use V_{BB} for a single–ended direct connection or port to another device.

Features

- 1.4 ns Typical Propagation Delay
- Maximum Frequency > 275 MHz Typical
- LVPECL/LVDS/CML Inputs, LVTTL/LVCMOS Outputs
- 24 mA TTL outputs
- Operating Range: V_{CC} = 3.0 V to 3.6 V with GND = 0 V
- The 100 Series Contains Temperature Compensation
- V_{BB} Output
- These Devices are Pb–Free and are RoHS Compliant

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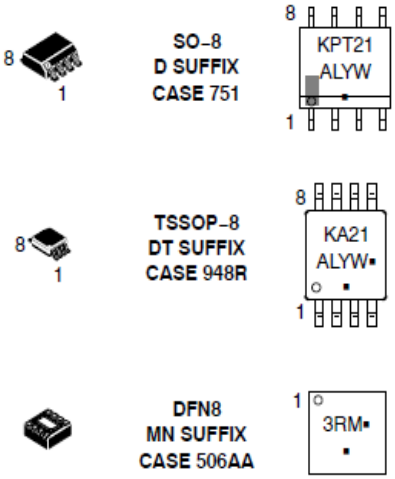
MARKING DIAGRAMS*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
M = Date Code
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

MC100EPT21

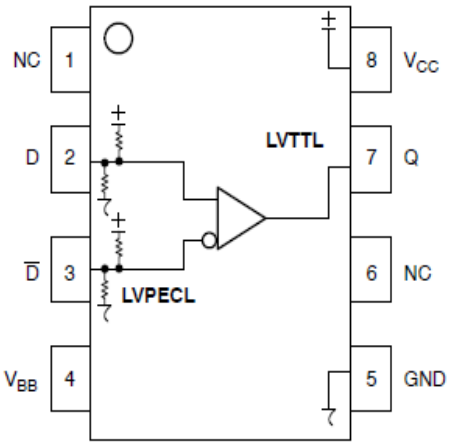


Figure 1. Logic Diagram and 8−Lead Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
Q	LVTTL/LVCMOS Output
D*, $\overline{D}$*	Differential LVPECL/LVDS/CML Input
V_{CC}	Positive Supply
V_{BB}	Output Reference Voltage
GND	Ground
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

* Pin will default to 1/2 of V_{CC} when left open.

Table 2. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor	D	50 kΩ
Internal Input Pulldown Resistor	$\overline{D}$	50 kΩ
Internal Input Pullup Resistor	D, $\overline{D}$	50 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 1.5 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) SOIC−8 TSSOP−8 DFN8		 Level 1 Level 3 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		81 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MC100EPT21

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Power Supply	GND = 0 V		3.8	V
V_{IN}	PECL Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	0 to 3.8	V
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SO−8 SO−8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	SO−8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−8 TSSOP−8	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	TSSOP−8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W °C/W
T_{sol}	Wave Solder Pb Pb−Free	< 2 to 3 sec @ 248°C <2 to 3 sec @ 260°C		265 265	°C
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power)

Table 4. PECL INPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0.0 V (Note 3)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage (Single−Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single−Ended)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	−150			−150			−150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input parameters vary 1:1 with V_{CC}.
4. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC100EPT21

Table 5. LVTTL/LVCMOS OUTPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0.0 V, T_A = −40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.0 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA			0.5	V
I_{CCH}	Power Supply Current	Outputs set to HIGH	5	17	25	mA
I_{CCL}	Power Supply Current	Outputs set to LOW	8	21	30	mA
I_{OS}	Output Short Circuit Current		−130		−80	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. AC CHARACTERISTICS V_{CC} = 3.0 V to 3.6 V, GND = 0.0 V (Note 5)

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Frequency (Figure 2)	275	350		275	350		275	350		MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	800 1200	1400 1400	2050 1800	800 1200	1400 1400	2250 1800	900 1100	1600 1300	2950 1900	ps
t_{SKEW}	Duty Cycle Skew (Note 6)	45	50	55	45	50	55	45	50	55	%
t_{SKPP}	Part−to−Part Skew (Note 6)			500			500			500	ps
t_{JITTER}	Random Clock Jitter (RMS)		3.5	5		3.5	5		3.5	5	ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (0.8V − 2.0V) Q, $\overline{Q}$	250	600	900	250	600	900	250	600	900	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Measured with a 750 mV 50% duty−cycle clock source. R_L = 500 Ω to GND and C_L = 20 pF to GND. Refer to FIgure 3.
6. Skews are measured between outputs under identical transitions. Duty cycle skew is measured between differential outputs using the deviations of the sum Tpw− and Tpw+.