OPTIMISATION OF A VOLTAGE MEASUREMENT AND CONTROL CIRCUIT FOR AN IMAGING ELECTROMAGNETIC FLOW METER

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ABSTRACT

This paper describes the optimisations conducted on an existing voltage measurement and control circuit to allow its use in a novel imaging electromagnetic flow meter. This flow meter is a multi-electrode device that can construct a velocity profile in both single and multiphase flow applications. Voltages are induced in the fluid flowing through the flow meter section due to the interaction of the fluid and the locally generated magnetic field. These voltages are detected by an array of electrodes and measured by a 7-channel system, based on the voltage measurement and control circuit. Each channel measures the potential difference between two electrodes in the flow cross section. The voltage measurement and control circuit comprises a very high amplification stage and an integral controller. The amplification stage is required to amplify the induced voltages of mV to V, suitable for analogue-to-digital conversion. The integral controller acts to eliminate the DC error component introduced in the amplification stage to prevent the circuit from exceeding its operational dynamic range limit. The existing voltage measurement and control circuit design has several drawbacks. The very high amplification stage occasionally causes the circuit to exceed its operational dynamic range. In addition, the integral controller has a slow action response which results in a long settling time and offset error. These drawbacks were overcome in the optimised design - discussed in this paper.

Keywords electromagnetic, flow meter, induced voltage, multi-electrode, DC error component.

1 INTRODUCTION

Conventional Electromagnetic flow meters (EMFM) have been utilised successfully in a wide range of industrial applications to measure the volumetric flow rate of a conductive fluid, such as water, in single phase pipe flows. Recent EMFMs measure the volumetric flow rate of a conductive fluid with an axisymmetric velocity profile to an accuracy of $\pm 0.05\%$. However, in horizontal and upward inclined multiphase flows, the axial velocity varies significantly due to gravity; the minimum and maximum axial velocity occur at the lower and higher side of the inclined pipe respectively. Such configurations are common in the oil industry: for example, horizontal and upward inclined oil-in-water flow and solid-in-water flow. Conventional EMFMs provide inaccurate readings when used in such settings and their application is therefore unsuitable.

Although previous research has investigated non-uniform velocity measurement using multi-electrode EMFMs, most of this research focused on single phase flow rather than multiphase flow applications [1][2]. The imaging electromagnetic flow meter (IEF) represents a novel design for velocity profile measurement in multiphase flows with non-uniform axial velocity profiles [3]. It was developed and patented by the Systems Engineering Research Group at University of Huddersfield [4].

2 THE IMAGING ELECTROMAGNETIC FLOW METER

The novel imaging electromagnetic flow meter design is divided into two parts: (i) the mechanical design and (ii) the electrical/electronic circuitry [5]. The mechanical design of the flow meter comprises a Delrin (non-conducting) pipe, Helmholtz coil and an electrode array embedded on the internal surface of the pipe wall (see Figure 1). The Helmholtz coil is a configuration of two coils, made with a radius equal to the distance between them. Both coils are positioned in parallel at the sides of the pipe where their centre is equal to the plane $z = 0$ of the flow cross section. At any given instant, the current flowing in both coils has equal magnitude and direction. As a result, the magnetic field generated in the y-direction of the flow cross section at the plane of the electrode array is near-uniform.

The electrode array consists of 16 electrodes, which are equally spaced and mounted at the same z-plane coordinate as the centre of the coils. Stainless steel electrodes are used due to their very low permeability and high resistance to corrosion. The electrode array detects any induced potential

differences in the flow cross section due to the interaction between the flowing fluid and the imposed magnetic field (Faraday's Law of Induction). The flow cross section is divided into 7 pixels, in which 7 potential difference measurements are performed between the electrodes (see Figure 2). Electrodes e13 and e5 are not used in this case. However, they are required for additional pixels. The cables connecting the electrodes to the electronic circuitry are positioned in parallel to the local magnetic field. This is essential to eliminate any 'cable loops', which cause unrelated flow potentials to be induced in the cables.

The electronic circuits are the coil driver, the voltage measurement and control and the signal processing circuits. The coil driver circuit comprises four solid-state relays (SSR) connected in an H-bridge configuration. The SSR network is controlled by a microcontroller to generate a 'hybrid square wave' voltage from a DC power supply unit (see Figure 3a). The output of the network is connected to the Helmholtz coil. The latter generates a magnetic field in the same form as the SSR relay network voltage (see Figure 3b). The transients in the magnetic field - as illustrated in Figure 3b - are due to the time constant τ of the coils ($\tau = L/R$), as the current increases until it reaches its final value (after $5\,\tau$). The magnetic flux density that was generated for the experiments included in this paper was around ± 90 gauss.

The voltage measurement and control circuit is the interface between the electrodes and the signal processing circuit. It measures the flow induced voltages between the 7 pairs of electrodes and amplifies them to a readable range to be further processed. This circuit is analysed in depth in Section 3. The signal processing circuit is the microcontroller and its associated peripherals. The flow induced voltages measured between the 7 pairs of electrodes are digitised by the analogue-to-digital converter. The microcontroller performs the reconstruction of the velocity profile, based on the voltage measurements. This paper focuses on the optimisation of the voltage measurement and control circuit. The theory used for velocity profile construction is therefore not explained as it is beyond the scope of this paper. The theory is explained in detail in [5].

3 THE VOLTAGE MEASUREMENT AND CONTROL CIRCUIT

The flow cross section of the current IEF is divided into 7 pixels between the pairs of the electrodes - as illustrated in Figure 2. Hence, a voltage measurement across each pair is required. For ease of explanation, the number of the pixel is denoted as i ($i = 1$ to 7), the number of each electrode pair is j ($j = 1$ to 7) and the flow induced voltage is U_j^*. For example, for pixel $i = 2$, the potential difference across the 4th pair of electrodes ($j = 4$) is U_4^*. Each pair of electrodes j requires a voltage measurement and control circuit, as all flow induced voltages must be made simultaneously at any given instant. Hence, this circuit must be built for every pair of electrodes j, and thus the 7-channel system – based on the VMC circuit – was developed.

3.1 The Existing Voltage Measurement and Control Circuit

The existing voltage measurement and control (VMC) circuit is illustrated in Figure 4. Typically, the amplitude of the flow induced voltage U_j^* across the electrode pair j - caused by the interaction of the flowing fluid and the local magnetic field - is only few millivolts. This very small voltage amplitude is not significant enough for the ADC to detect. Hence, U_j^* is amplified by the high gain amplifier 'HGA' which has a gain A, where A is equal to 1000. The voltage followers 'VF' decrease the output impedance of the electrodes, which is in the range of mega-ohms, to avoid voltage amplitude attenuation. The high-pass filters 'HPF' are used to remove the significant DC error component, which can appear on each electrode due to electrochemical effects (polarisation). The output voltage of the high gain amplifier $U_{x,j}$ is passed to the low-pass filter 'LPF1' with a cut-off frequency f_{c1} to remove any imposed noise (EMI and RFI).

The differential voltage at the inputs of the high gain amplifier 'HGA' is the sum of two components; the flow induced voltage U_j^* and a residual, undesirable slowly varying DC voltage U_0 that is not entirely eliminated by the high pass filters 'HPF'. The amplitude of DC error component U_0 is significantly larger than the amplitude of the induced voltage U_j^*. If the voltage U_0 is not removed, it will be amplified by the 'HGA' amplifier, i.e. AU_0 and the output voltage will be $U_{x,j} = A(U_0 + U_j^*)$. The resultant DC component AU_0 causes the output of the 'HGA' amplifier to exceed its operational dynamic range limit and therefore, its output saturates.

The solution to this problem is the control circuit, which applies an appropriate reference voltage U_{sp} to 'HGA' amplifier to remove the DC error component U_0. The output voltage of 'HGA' amplifier $U_{x,j} = A(U_0 + U_j^*)$ is fed to a low-pass filter 'LPF2' with extremely low cut-off frequency f_{c2} to obtain only the DC error component AU_0 of the 'HGA' output signal x. The DC component AU_0 is subtracted from the set point U_{sp} by the difference amplifier 'DA'. The set point voltage U_{sp} is set to $2.5V$ - which is the mid dynamic range of the ADC - to improve sampling accuracy. The resultant output of the 'DA' is the error $U_e = U_{sp} - U_0$, which is fed to the integrator (integral control). The latter integrates or continually sums the error U_e over time, eliminating the DC error component AU_0 gradually .

Currently, the VMC circuit has several drawbacks when used with the IEF in the laboratory. At circuit start-up, the output of some channels (a channel refers to one voltage measurement and control circuit) exceeds the dynamic range of the circuit, i.e. goes into a saturated state. This happens as a result of the large gain A of the 'HGA' amplifier, which is set to 1000. The dual power supply used has a range of $\pm 15V$. If the DC component U_0, is greater than $\pm 15mV$ at the inputs of 'HGA' amplifier, it is amplified by 1000, causing the output of the 'HGA' amplifier to saturate.

A DC component of 15mV is likely to occur. In addition to polarisation, it also caused by the leakage current flowing from 'HPF' filters into the 'HGA' amplifier inputs. Furthermore, there is a mismatch between the 'HPF' components actual value. This is due to component tolerance and ambient temperature fluctuations. When the output of the 'HGA' amplifier saturates, the output of the integral amplifier goes into saturated state and thus, the control circuit does not work. Consequently, the circuit will remain in saturation as there is no control action. Additionally, the integral control is not tuned and therefore, at circuit start-up, the output of the circuit requires a significant amount of time to settle at the set point voltage U_{sp}. This is a problem because the ADC device cannot sample any measurement until the dynamic range of the signal is between 0 and $5V$. The response of the control circuit is also too slow to respond to the constantly changing DC error component. This means that the output of the VMC circuit does not reach the set point voltage. This reduces the accuracy of the sampling performed by the ADC.

3.2 The Optimised Voltage Measurement and Control Circuit

Analysis of the existing VMC circuit (further discussed in Section 4) indicates that it is optimised effectively via utilisation of two-stage amplification - as depicted in Figure 5. In the optimised design, the gain A of the first-stage amplifier 'HGA1' is set to 20 and the gain B of the second-stage amplifier 'HGA2' is set to 50. The overall gain $A.B$ remains the same, i.e. 1000. However, any DC error component U_0 up to $\pm 750mV$ ($\pm 15V/A$) at the inputs of 'HGA1' amplifier can be compensated by the control circuit. This was found practically to be a suitable range, avoiding saturation. The low-pass filter 'LPF2' extracts the DC error component AU_0 from the output signal $U_{x,j} = A(U_0 + U_j^*)$ of the 'HGA1' amplifier. The difference amplifier 'DA' subtracts the set point value U_{sp}, which, in this case was set to zero, from AU_0, and therefore, the error $U_e = AU_0$. Practically, the difference amplifier is not required. However, it remains included in Figure 5 to clearly demonstrate the operation of the control circuit.

The integrator amplifier had to be tuned - by adjusting its time constant value $\tau_{int} = R_{int}C_{int}$ - to ensure stability of the overall system, reduce the settling time to minimum and increase the action response speed. The second-stage amplifier was configured to a reference voltage U_{ref2} of $2.5V$ to ensure accurate ADC sampling. The output of the 'HGA2' amplifier is fed to the low pass filter 'LPF1' to remove any imposed noise. Further optimisation may be achieved through the replacement of the RC components of the 'HPF' filters with low-tolerance, low-leakage-current and low-temperature coefficient RC components. The resistor and the capacitor components that are currently used for the 'HPF' filters have a tolerance of 5% and 10% respectively. This optimisation will be implemented at a later stage in this project.

4 EXPERIMENTAL RESULTS

The test rig was set up in the laboratory to examine the performance of the existing and the optimised VMC circuits comparatively. The IEF (Figure 1) was positioned vertically and connected to a flow loop. Water was pumped into the flow loop at a velocity appropriate for testing. The existing 7-channel VMC system was used for testing. A single channel of the optimised VMC circuit was built and tested

with the IEF. Electrodes e1 and e9 (Pixel 4) were connected to the inputs of the optimised VMC circuit. The aim of testing was to verify the causes of the 'HGA' amplifier saturation in the existing VMC circuit. The normal and transient operations of both circuits were also monitored. During testing, the DC error component U_0 was measured to be in the range of 8-12mV at the inputs of the 'HGA' amplifier. This meant that the DC error component U_0 was very close to the circuit dynamic range limit which is $\pm 15V$, taking into account that it is multiplied by a gain of 1000. Moreover, this DC error component varies from one channel to another, depending on the actual value of the components of the 'HPF' filters and the pair of electrodes being measured. It also changes as the temperature of the surrounding environment fluctuates. Hence, it is essential that the overall gain of the circuit should be divided into two stages, as per the optimised circuit design. This eliminates the risk of exceeding the operational dynamic range limit.

Figure 6a presents the induced voltages U_4^*, U_5^* and U_6^* in flow pixels 4, 5 and 6 of the flow cross section of the IEF (see Figure 2) measured by the existing 7-channel VMC system. It also shows the induced voltage U_4^*, as measured by the optimised circuit. The induced voltages in the selected flow pixels measured by the existing 7-channel VMC system should theoretically have a set point of $2.5V$. However, it can be seen that neither of the channels actually settles at this set point voltage. This is due to the slow response of the control circuit to rectify the constantly changing DC error component U_0 during measurements. In contrast, the optimised circuit successfully measured the induced voltage U_4^* and eliminated the DC error component U_0. It must be noted that the difference in amplitude of the induced voltage U_4^* measured by both circuits is due to use of different flow velocities.

Figure 6b shows the transient operation of both circuits when measuring induced voltage U_4^* in the IEF flow cross section for a nearly constant DC error component. In this test, the water flows in the loop at an appropriate velocity, however, the local magnetic field is zero (Helmholtz coils are turned off). It can be observed that the settling time of the existing circuit in comparison with the optimised circuit is 240s to 100s. This demonstrates a significant improvement in the settling time by the optimised design. It is also appropriate to suggest that the ADC may begin sampling after 20s using the optimised circuit, compared to 100s using the existing design.

5 CONCLUSIONS & FURTHER WORK

The existing design for the VMC circuit was studied and tested with the IEF. The experimental results confirmed that the drawbacks of the existing VMC circuit are critical and required optimisation. The modifications implemented in the optimised VMC circuit are: 1) two-stage amplification and 2) fast and tuned integral control circuit. The two-stage amplification approach prevents the circuit exceeding its operational dynamic range limit, i.e. $\pm 15V$. This ensures a normal operation of the circuit, even if a significant DC error component is present at the inputs of the first-stage amplifier 'HGA1'. A faster and tuned integral control circuit improves the overall circuit settling time during normal operation. It also enables the circuit to reach its set point voltage even if the DC error component is constantly changing. The optimisations implemented in the new design were tested successfully. The experimental results demonstrate significant improvement in the overall VMC circuit functionality.

The optimised VMC circuit design will be used to develop a 7-channel VMC system on a printed circuit board to suit the IEF. This system will be thoroughly tested and compared with the existing 7-channel VMC system in terms of normal and transient operations. The effects of low-tolerance, low-leakage-current and low-temperature coefficient RC components for the high-pass filters 'HPF' on the optimised VMC circuit will also be investigated.

6 REFERENCES

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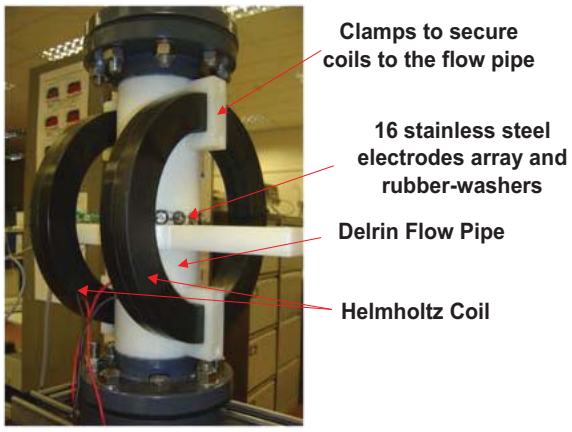

Figure 1: The imaging electromagnetic flow meter

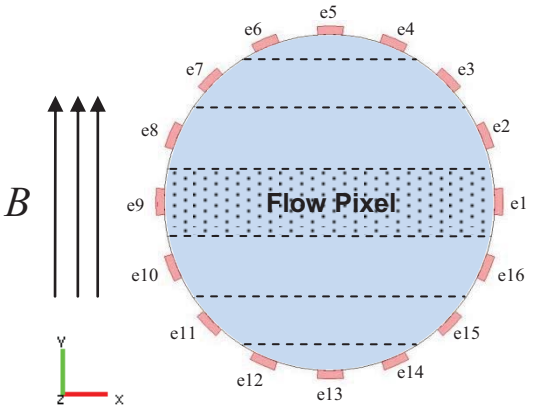

Figure 2: The flow cross section and the electrode pairs from e1 to e16

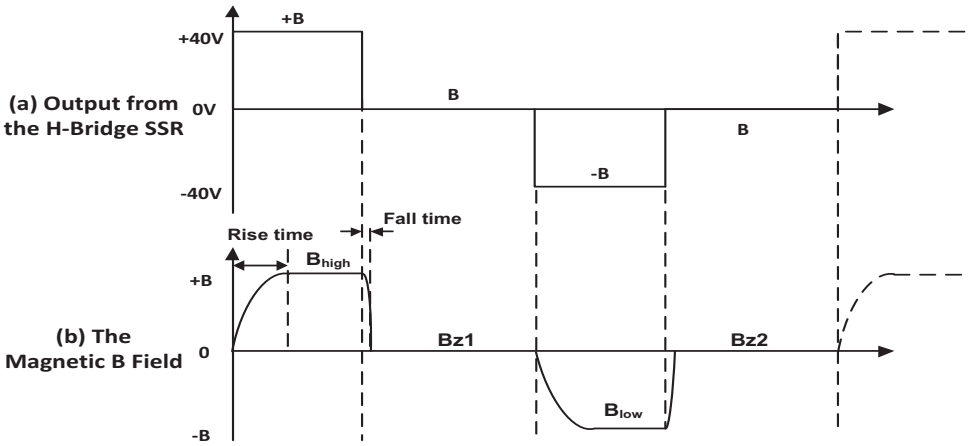

Figure 3: a) The output voltage of the H-bridge SSR network b) The generated magnetic B field.

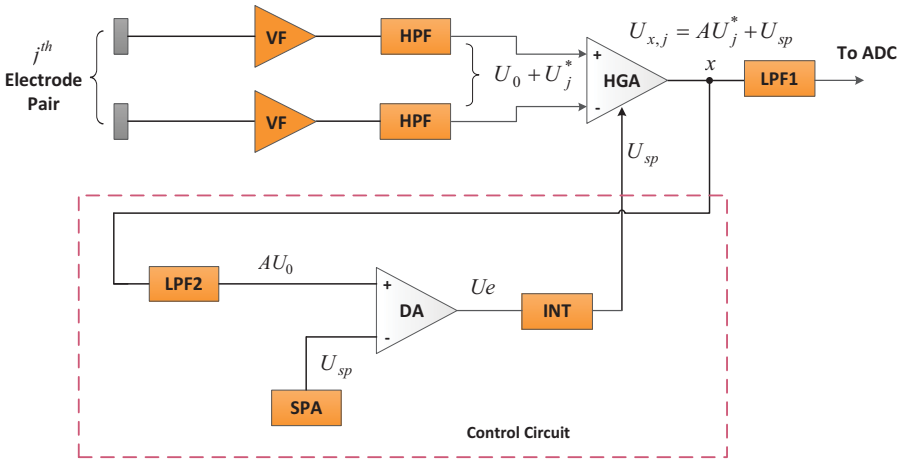

Figure 4: The existing design of the voltage measurement and control circuit

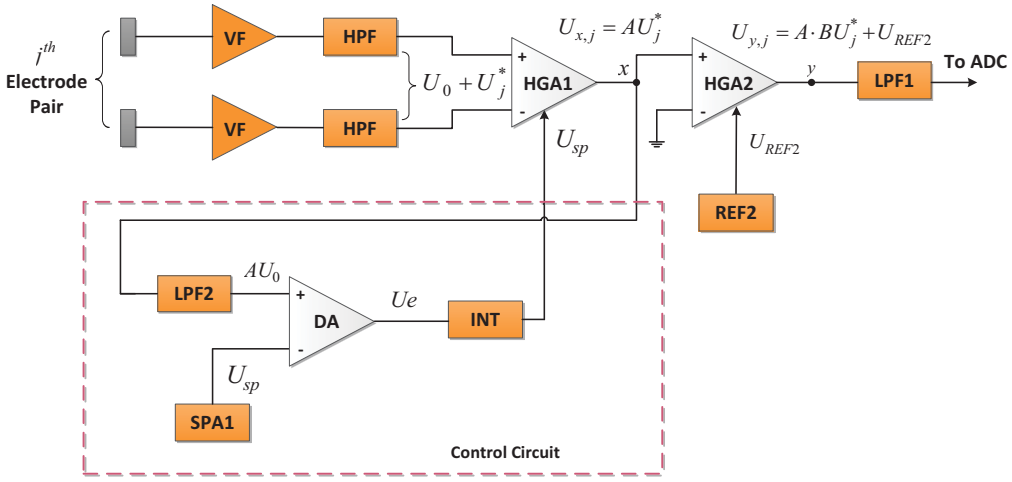

Figure 5: The optimised design of voltage measurement and control circuit

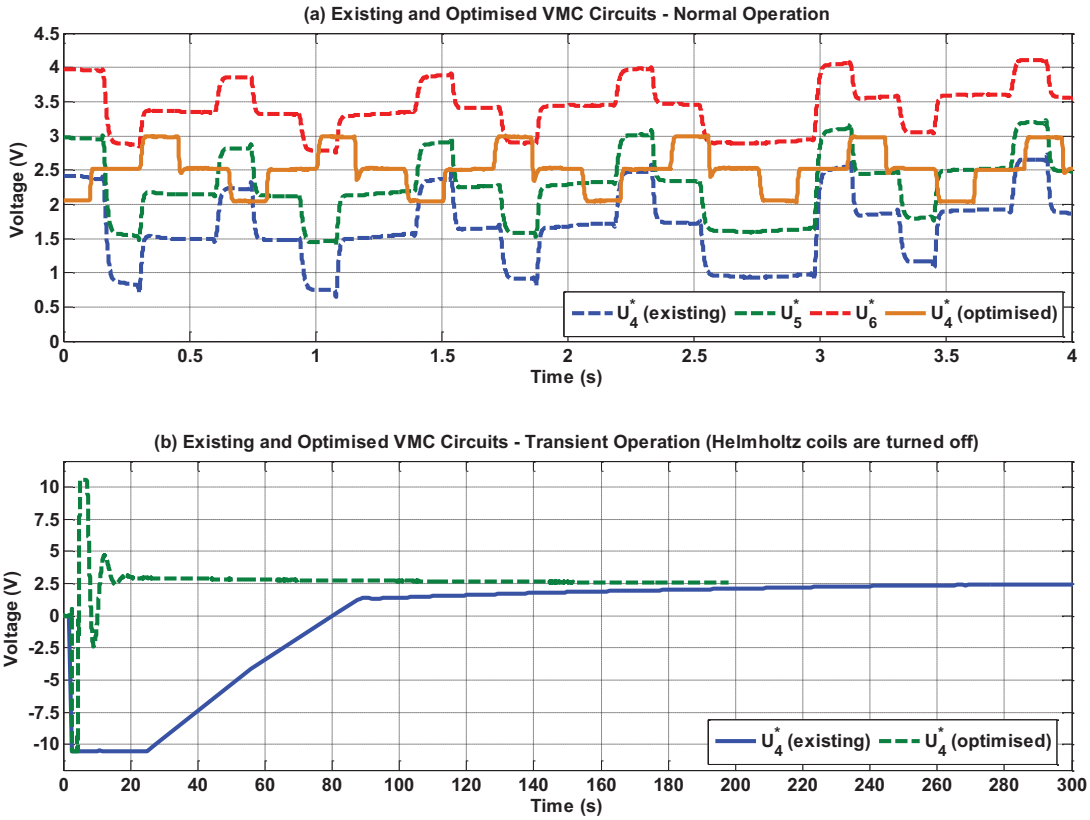

Figure 6: a) Normal operation of the existing and optimised VMC circuits.
b) Transient operation of both circuits at start-up.