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Microelectronic implementation of error correcting codes for dicode pulse position modulation

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ABSTRACT

Dicode pulse position modulation (DiPPM) was proposed by Sibley as a more advantageous form of PPM. DiPPM can be efficiently implemented as it employs two abilities to transmit one bit of pulse code modulation PCM. Thus a PCM conversion from zero to one provides a pulse in slot reset (R) and from one to zero provides a pulse in slot set (S). No signal is transmitted in the PCM data is unvarying. The line rate is two times the minimum PCM, a significant reduction in speed compared to digital PPM. As the bandwidth requirement is much smaller than digital PPM, DiPPM could be used in dense wavelength division multiplexing (DWDM) systems. DiPPM systems suffer from three types of pulse detection errors: wrong-slot, false-alarm and erasure. This project will use a field programmable gate array (FPGA), to build an error correction code circuit (Reed Solomon Code) and dicode PPM (coder & decoder). This will be expected to reduce the error sources in DiPPM. According to initial results the conclusion is that the Reed Solomon error correction coded system offers improvement over uncoded DiPPM, when operating at the approximately 4.5 code rate.

AIM & OBJECTIVE

This project proposes three objectives which include:

1. Reducing DiPPM errors as much as possible using Reed Solomon (RS) codes.
2. Designing Reed Solomon encoder and decoder circuits.
3. Implementation and experimental work of DiPPM encoder and decoder circuit by using FPGA.
4. Verifying theoretical predictions with measurements.

Sources of Error in DiPPM

DiPPM systems suffer from three types of pulse detection errors:

- **Wrong slot error.**
  - Wrong slot errors occur when noise on the rising edge of a detected pulse causes the pulse to appear in adjacent time slots.

- **Erasure error.**
  - Erasure errors occur when the signal voltage is so great as to reduce the peak signal voltage to below the threshold level.

- **False alarm.**
  - Due to ISI, there can be a signal voltage in the slots surrounding the one containing a pulse. Noise on this voltage can lead to a threshold crossing event wherein pulse is presented as false alarm errors.

FUTURE WORK

- Design RS encoder and decoder circuits by choosing the proper parameters.
- Implement RS, DiPPM encoder and decoder circuit by programming the FPGA using VHDL.
- Verify theoretical predictions with measurements.

CONCLUSIONS

A system model tries to simulate some characteristics of a system. The model corresponds to the forward error correction (FEC) communication scheme, which is dependent on a RS error-control code. The behaviour of each block of the model is described in Mathcad software.

SYSTEM MODEL

This research will concentrate on employing Reed Solomon (RS) codes to code the Diode Pulse Position Modulation System (DiPPM). RS is expected to reduce the source of errors, which a DiPPM system suffers from. In this report a literature review has been written to explain the problems of DiPPM system and trying to find a solution, the general block diagram of the system has been given. According to initial results the conclusion is that the Reed Solomon error correction coded system offers improvement over uncoded DiPPM, when operating at approximately (4.5) code rate, and this will lead to a general RS system (coder & decoder). Finally, the overall system will be implemented using FPGA and the results will be compared with maximum likelihood sequence detection (MLSD).

2. REED SOLOMON CODE

In 1960, Irving Reed and Gust Solomon published a paper in which they described a new type of error-correcting codes that are now called Reed Solomon (RS) codes. RS codes are a powerful class of non-binary forward error-correcting that can correct the maximum possible number of errors with the minimum data overhead. RS codes are the most commonly used error codes in practice. It is used in many applications like magnetic and optical data storage, wireline and wireless communications, and satellite communications. RS decoder has the ability to correct up to t symbols that contain errors in a codeword, where t can be defined as:

\[ t = [n-k]/2 \]

Where:

- n Number of code word symbols.
- k Number of data symbols.
- t Number of redundancy symbols.