Electron multiplier supply and signal processing: working towards a *system on chip* solution

Toby D. Izod

Submitted for the Degree of Master of Science

University of Huddersfield

11th April 2018

Acknowledgements

I would like to thank my mother, father and step brother Joshua for their continued support, Dr Alan James Bell, Dr Martin Sibley, Dr Peter Mather and my colleagues at Kromek: Dr Ed Marsden and Richard Haigh.

Abstract

Despite the primitive operation and challenging practicalities of electron multipliers, they still outperform solid state equivalents in professional level equipment that requires single electron or photon resolution. The advent of the Micro Electronic and Mechanical (MEMs) fabrication process has the potential to miniaturise electron multipliers to allow mass production, reduce physical volume, and minimise part to part variation. The potential impact of MEMs is greatly reduced if secondary electronics associated with such devices cannot be reduced by a similar magnitude.

The primary purpose of this research project was to develop the secondary electronics (power supply, divider and decoupling) to enable electron multiplier-based detectors to rival solid-state counterparts in terms of size and power consumption for use in a device the size of a mobile phone. To be comparable with solid state alternatives a *System in Package* (SiP) specification was targeted, with all specialised circuitry occupying the same package as the detector.

To realise the reduction in size required, a number of practical limitations were identified and addressed, including standard capacitor values, behaviour under DC bias and dark discharge across PCBs. These were characterized through hardware measurement, fed into theoretical models and finally electronic assemblies were then designed around these. This bottom-up methodology was shown to have performance advantages when optimising proven topologies under restrictive design limitations.

To demonstrate the size and power reduction available to new detectors, two existing topologies were optimized and evaluated using this bottom-up method. A third new topology was synthesised to better overcome identified shortcomings at a conceptual level. Performance of all three designs is reported.

This proof of concept project was based around a scintillation detector employing a photomultiplier tube. However, it is equally applicable to any discrete dynode or microchannel plate electron multiplier, such as high gain pixilated imaging systems. Devices were tested in a spectroscopic scintillation radiation detection system to evaluate performance deficiencies introduced by reduction of both size and power consumption.

As MEMS manufactured devices are still in an early stage of development, this work did not attempt to demonstrate any overall comparison against solid state equivalents' performance but demonstrated that the secondary electronics would not be the limiting factor in terms of cost or performance in the application to MEMs manufactured electron multipliers.

The project delivered three prototypes that performed against the specification, with limitations highlighted, and a brief for a SoC solution was constructed.

Contents

1 Introduction

Despite over 80 years having passed since the discovery of electron multipliers, they still have advantages over solid-state devices for critical, professional level applications. These include mass spectrometry, high gain imaging systems such as night vision, Raman spectroscopy, and scintillation radiation detection. In these applications the main advantages over solid state technology are higher speed due to lower intrinsic capacitance and lower self-noise.

The comparative electronic simplicity of solid-state devices has reduced the usage of vacuum electron multipliers based on practicalities, rather than performance. An example of this is spectroscopic scintillation detection for the identification of radio isotopes.

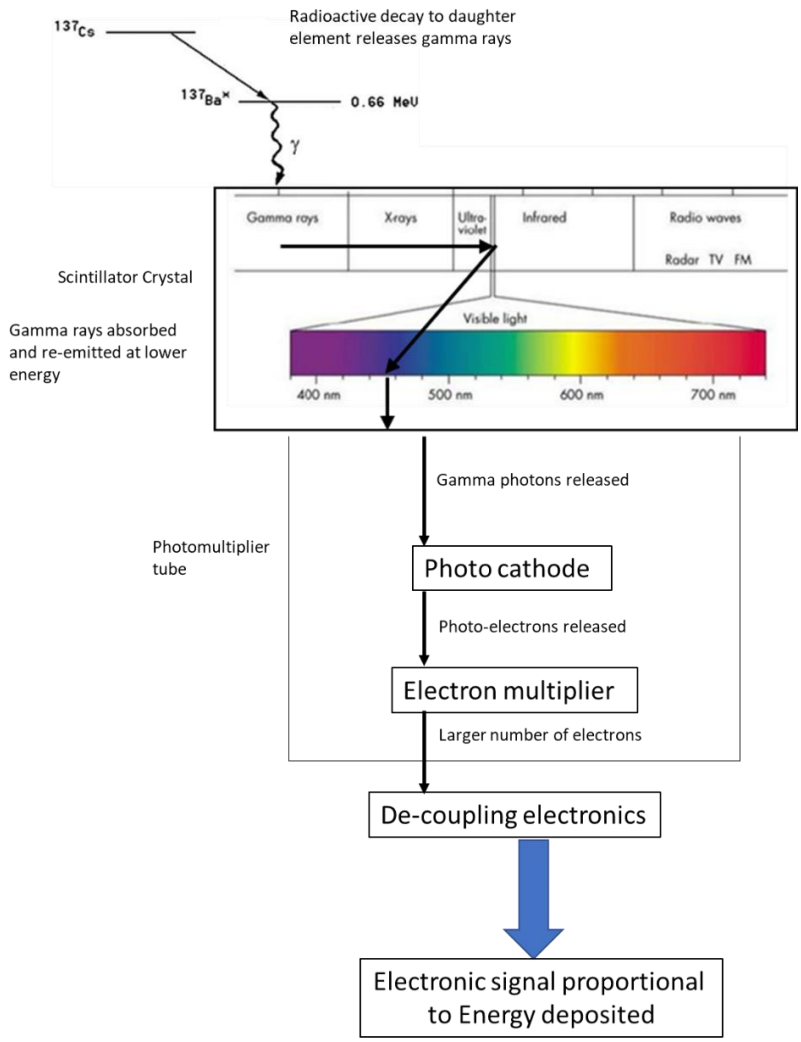

Figure 1.1: *Signal flow within a scintillation radiation detector*

Scintillation detection is the mechanism in which ionising radiation deposits energy into a crystalline structure which then releases this energy at a longer wavelength [1]. When coupled to a photodetector the emitted energy is converted to a current which is proportional to the energy deposited into the scintillator. The mechanics of such a system is detailed in figure 1.1.

The photodetector needs to have a noise flaw sufficiently low to allow detection with single photon resolution, along with a gain sufficient to couple the signal through to more conventional electronics. One such detector is an electron multiplier coupled to a photo electric cathode forming a Photo Multiplier Tube (PMT).

The current industry options for such a photodetector are either based around a vacuum *Photo Multiplier Tube* (PMT) or a silicon avalanche photo diode array referred to as a *Silicon Photo Multiplier* (SiPM). Both the PMT and SiPM are commonly used, but PMTs have advantages in resolution, temperature stability, speed and range of operation. The disadvantages of PMT detectors are complexity of electronics, physical fragility (especially above atmospheric pressure), susceptibility to magnetic field interference, and greater physical size than solid state alternatives.

When considering hand-held devices, such as personal radiation detectors[1], the secondary electronics can present a limitation in the selection of a PMT both in terms of power consumption and size. A differentiator between SiPMs and PMT detectors is that the former leads itself to self-contained integrated sensor/electronics designs whereas PMTs tend to require more complex non-integrated electronics. Incorporating electronics into a single package along with the electron multiplier is the main drive behind this research.

[1] Typical commercial hand held radiation detectors include:https://en.polimaster.com/catalog/prd-gamma/personal-radiation-detector-pm1703ma/ https://www.kromek.com/product/d3s_riid/

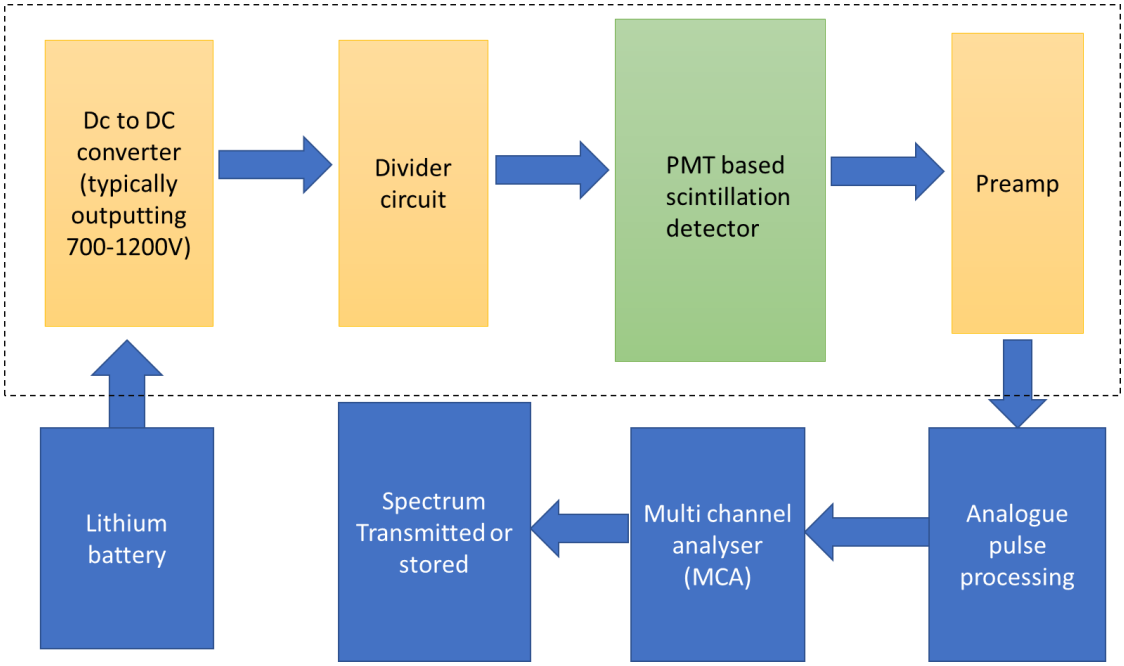

***Figure 1.2**: Typical hand-held radiation detector block diagram*

Figure 1.2 illustrates the block diagram of a spectroscopic detection system, with the front-end module comprising the top half of the diagram. As can be seen this front end needs to accept a varying power source such as a lithium battery and present an electronic derivation of the energy deposited in the scintillation event to be processed by the MCA system.

Advances to the silicon process used to manufacture solid state devices has led to *Micro Electronic and Mechanical System*s (MEMS) manufacturing [2] being used to produce photo multiplier tubes at significantly reduced physical volume. The potential advantages are being able to 'tile' the devices in a modular fashion, lower accelerating voltage requirements [3], reduced susceptibility to magnetic disruptions and less part to part variation. This would also allow certain elements of the electronics to be integrated with the PMT's silicon wafer.

This work aimed to match the miniaturisation of photo multipliers by providing a proof of concept of a System in Package (SiP) electronics design for voltage generation and signal processing. This would enable the identification of layout considerations of external passive components in a future single chip solution. A spectroscopic radiation detector was used as an application example for this project. The output from the design will feed an external

pulse processing circuit (figure 1.2) and multi-channel analyser (MCA). As imaging tubes could be an alternative application for this development, other output configurations were also considered for practicality. These could feature an optical output from a phosphor screen directly mounted directly on the tube or a fast electron detector mounted in place of the anode electrode. Potential applications in this area are discussed later in this work.

In order to demonstrate the outcomes of this project two key areas of improvement over current commercial solutions needed to be addressed: firstly, to reduce the size of the circuitry in order to be consistent with the anticipated size of a MeMs manufactured. Secondly, to reduce power consumption, without a significant reduction in performance to permit integration into hand held instrumentation.

To methodically ensure the final solution presented represents a fully optimised system the following steps were taken:

- Technology review of electron multipliers and power supplies (Chapter 2&3).
- Known practical limitations detailing ceramic capacitors' behaviour under DC bias and air breakdown on Compact PCBs (Chapter 4&5).
- Universal high voltage module design (Chapter 6).
- Design, simulate, optimise and evaluate two industry standard concepts (Chapter 6).
- Synthesise 3rd alternate design with practical advantage (Chapter 6).
- Spectroscopic radiation testing in a detection system (Chapter 7)
- Present SoC solution at block diagram based on results from SiP hardware testing (Chapter 7)

The deliverable of this project was to provide a proof of concept design of a DC to DC converter, divider system and first stage amplifier suitable for translation into a single chip design. This was built as an ultra-high-density surface mount prototype on the same footprint as a Hamamatsu commercially available compact PMT [4].

2 Photo Multiplier Tubes

2.1 Electron-Multiplier Principles

The first report on a secondary emissive surface was made by Austin in 1902 [5] . Initially observed as a hindrance to designers of tetrode valves before the introduction of the pentode and its suppression grid, secondary emission is the mechanism in which an electron directed to a dynode (intermediate electrode) structure via an accelerating voltage will release a number of secondary electrons from this structure [3]. This number of secondary electrons for each collision (A) is based on the accelerating voltage between the dynode and electron source. Figure 2.1 illustrates the effect of varying accelerating voltage on gain of such a device.

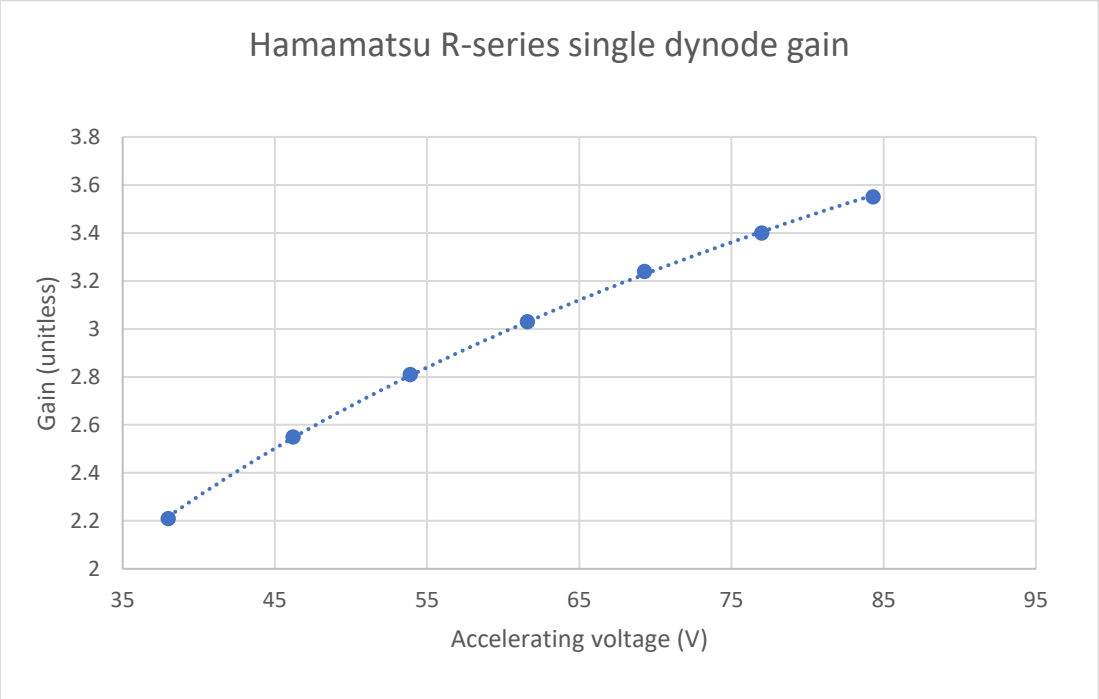

***Figure 2.1**: Effect of supply voltage on gain of a photomultiplier tube* [6]

By cascading dynode structures with accelerating voltages between them (as shown in figure 2.2) electrons released at the final stage becomes A^n.

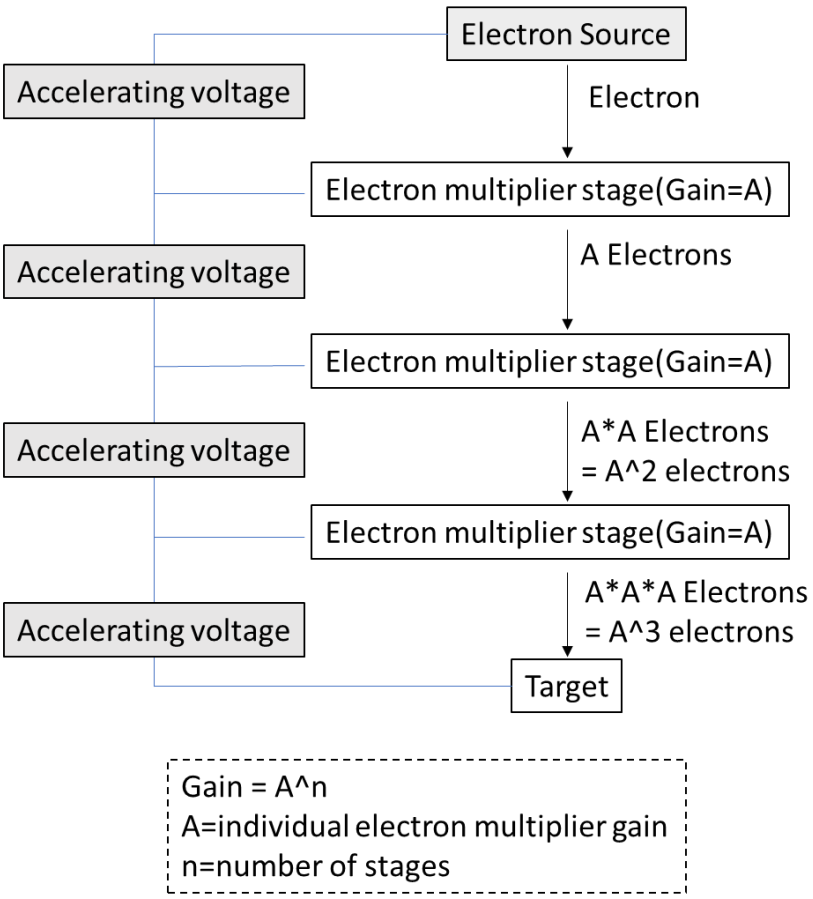

Figure 2.2: *Illustration of the concept of cascaded secondary emission dynodes* [6]

2.2 The introduction of the photocathode

The electron multiplier cascade described in section 2.1 relies on an accelerating voltage between stages to function; however, creating the input conditions for this system are more complex. This takes the form of a Faraday Cup to capture Ions, electrons, or charged particles in a vacuum with an accelerating voltage between the cup and the first dynode.

It can also take the form of a photocathode which, in accordance with the photoelectric effect, will release an electron when struck with a photon. When this is coupled to an electron multiplier it forms the basis of the PMT [5] [6].

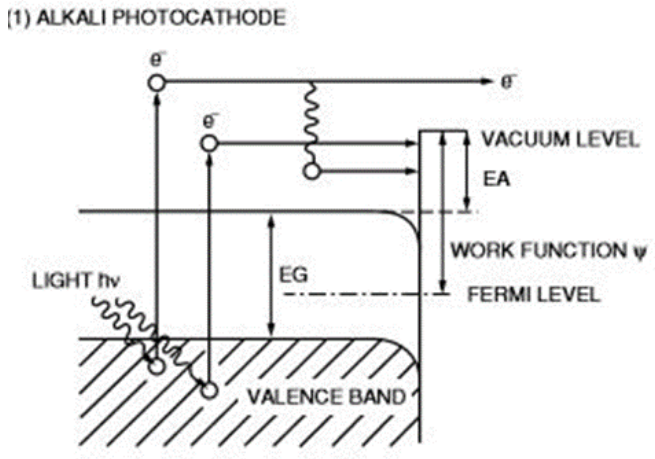

Figure 2.3: *Photocathode mechanism showing how light releases electrons* [6]

The gain in the PMT is carried out in the electron multiplier stage, with no amplification occurring on a photon level. The electrons released by a photocathode are sometimes referred to as *photo-electrons,* although this is in reference to their origin rather than state.

The photocathode functions by releasing an electron via energy transfer from a photon. The photon needs to have sufficient energy to overcome the work function of the semiconductor to release an electron, as illustrated in figure 2.3. As with secondary emission, such low numbers of interactions occur that the relationship between photons that strike the cathode and electrons released is termed quantum probability. The quantum efficiency for the entire device (including the electron multiplier) is a common metric for evaluation of devices [7].

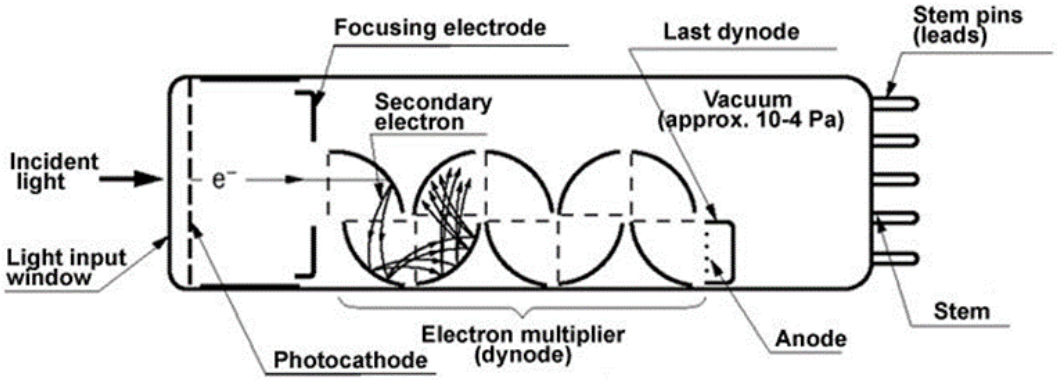

Figure 2.4: *Basic vacuum photomultiplier operation* [6]

The photocathode takes the form of vapour deposited onto a transparent window of either borosilicate glass, high purity glass, or quartz. This forms the end of an envelope, usually glass, which also contains the electron multiplier. A typical assembly is shown in figure 2.4.

Under normal operation the noise model is single electrons thermally released from either the photocathode or dynodes. These propagate through the electron multiplier mechanism to form thermally triggered false events.

If the accelerating voltage is sufficiently high to cause an electron beam between any pairs of electrodes the PMT will form more conventional shot noise.

2.3 Conventional current model

Assuming a scintillator has been correctly specified for the given detector application, the operating point of the tube can then be correctly modelled for a lean electronic design. Figure 2.4 shows a simple, steady state model of a PMT, and this is developed in figure 2.5 with the introduction of the time-domain, a scintillator and corresponding energy of a scintillation event.

The scintillator used for this simulation is *BilLanCe* [8], a lanthanum bromide-based scintillator manufactured by Saint-Gobain crystals. This is brighter (63 Photons/KeV) than many alternative scintillators as photons from the event are delivered in a short window (typically below 0.5µS) and low deviation between identical energy events (resolution).

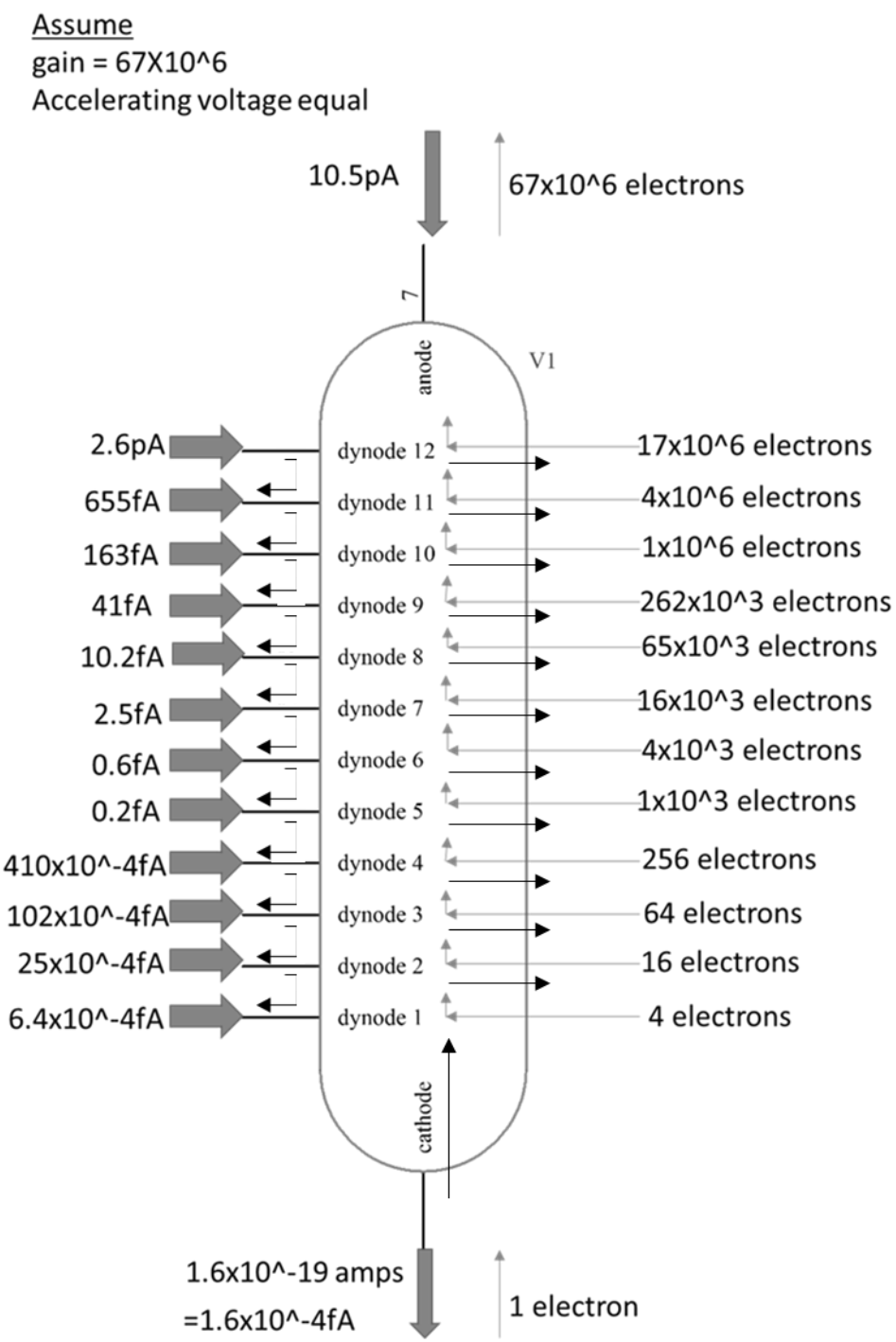

Figure 2.4: *Steady state single photon operation of a 12-dynode photomultiplier showing both electron flow and equivalent conventional current.*

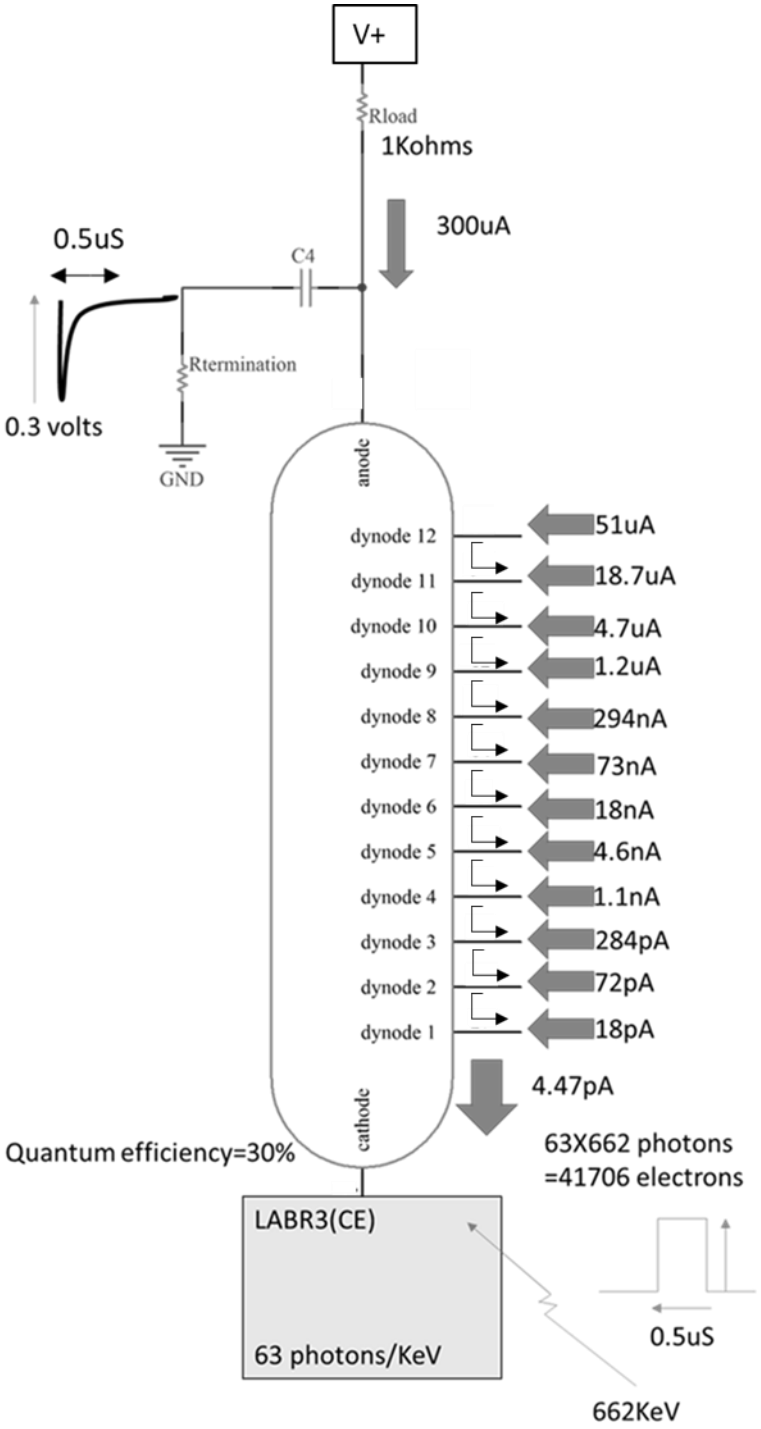

***Figure 2.5**: Dynamic operation during a scintillation event.*

2.4 Dynode supply dividers

Figure 2.5 demonstrates the typical dynamic elements of current required by the dynode structures from a scintillation event. Figure 2.2 illustrates the function of an electron multiplier with individual power supplies. To use a single, rather than multiple, individual dynode supplies, a single high voltage supply can be divided down to power each individual stage.

2.4.1 Resistive

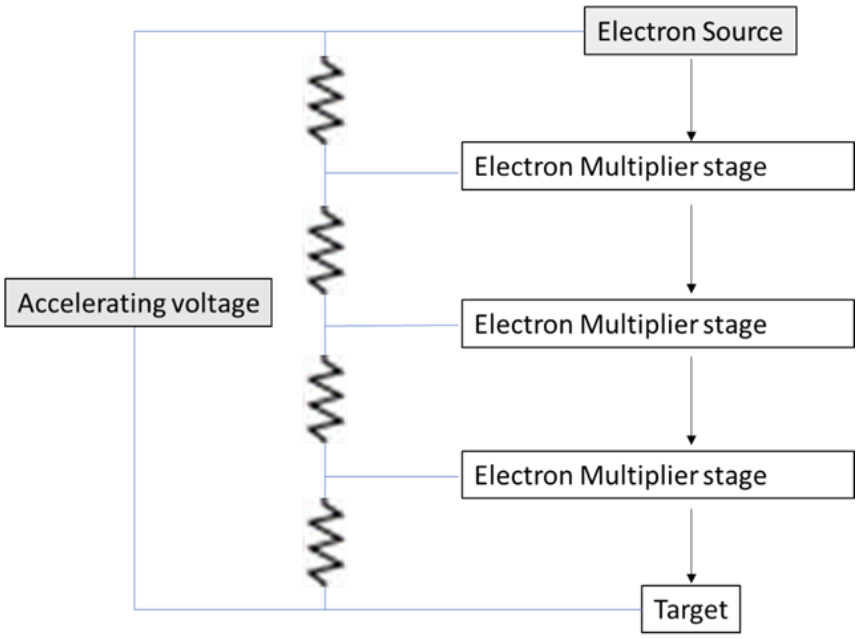

Figure 2.6: *Resistive based supply.* [6]

The least complex method of achieving this is to use a multi-stage potential divider (as shown in figure 2.6) from a single supply. An example design would be as follows:

A factor of 5X peak dynode current would therefore be:

$$Peak\ dynode\ current\ (from\ simulation) = 115.6\mu A$$

$$115.6 \times 10^{-6} \times 5 = 580 \times 10^{-6}$$

$$= 580\mu A$$

Assuming 60% supply efficiency at 1000V this would be:

$$Total\ Power = \frac{V \times I}{efficency}$$

$$= \frac{580 \times 10^{-6} \times 1000}{0.6}$$

$$= \mathbf{0.986W}$$

This power is predominantly dissipated as heat in the resistors making the circuit unsuitable for portable equipment relying on battery power or situations where heat dissipation is problematic, for example space applications.

2.4.2 Active divider biasing

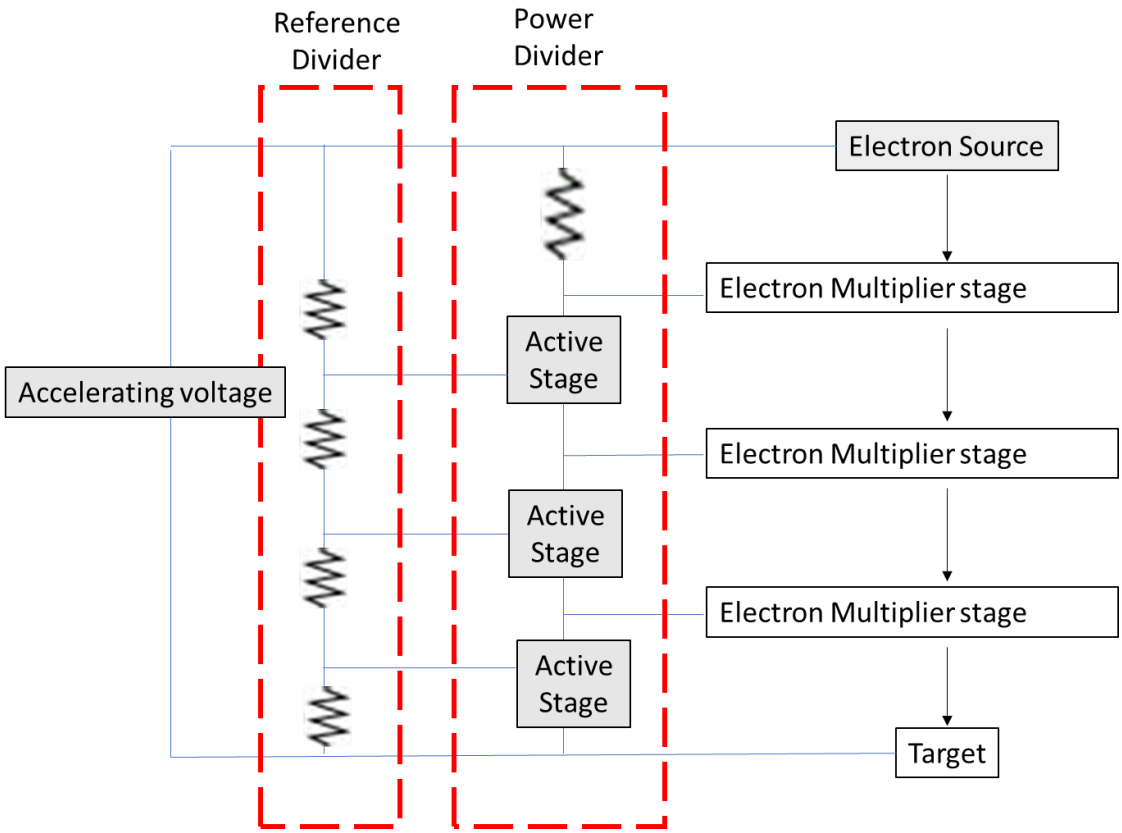

Figure 2.7: *Active divider-based supply* [6]

Figure 2.7 illustrates the concept of dividing down a single voltage rail to cascaded electron multiplier stages using active devices rather than a resistive potential divider. The active stages typically take the form of a cascode chain of source or emitter follower

amplifiers. These take a voltage input from the (high impedance) reference divider chain and provide sufficient drive to supply the dynode's current requirements. A single supply is used driving both a low current reference chain and a dynode driving chain in parallel. The principle is that any differential voltage between the reference and dynode chains will cause an increase in base current in the active elements, increasing current through that element of the dynode chain and enabling the dynode to be held at the correct accelerating voltage and supply ample current during an event.

At least one resistive element must be included in the dynode chain at the emitter (or source) of the lowest active device which provides the limitation to the system for the illustrated active system. An example design would be as follows:

Assuming 5MΩ leakage resistance, 5µA reference chain current, 12 active stages and a 1000V supply the quiescent current draw would become:

$$I = \left(\frac{V}{R}\right) + reference\ current$$

$$= \left(\frac{1000}{5 \times 10^6 + (12\ \times 5 \times 10^6)}\right) + 5 \times 10^{-6}$$

$$= \left(\frac{1000}{65 \times 10^6}\right) + 5 \times 10^{-6}$$

$$= 20\mu A$$

Assuming 60% supply efficiency at 1000V this would be:

$$Total\ power = \frac{V \times I}{efficency}$$

$$= \frac{1000 \times 20 \times 10^{-6}}{0.6}$$

$$= 33 \times 10^{-3}$$

$$= \boldsymbol{33mW}$$

Significantly lower than the resistive only design

2.4.3 *Voltage multiplier biasing*

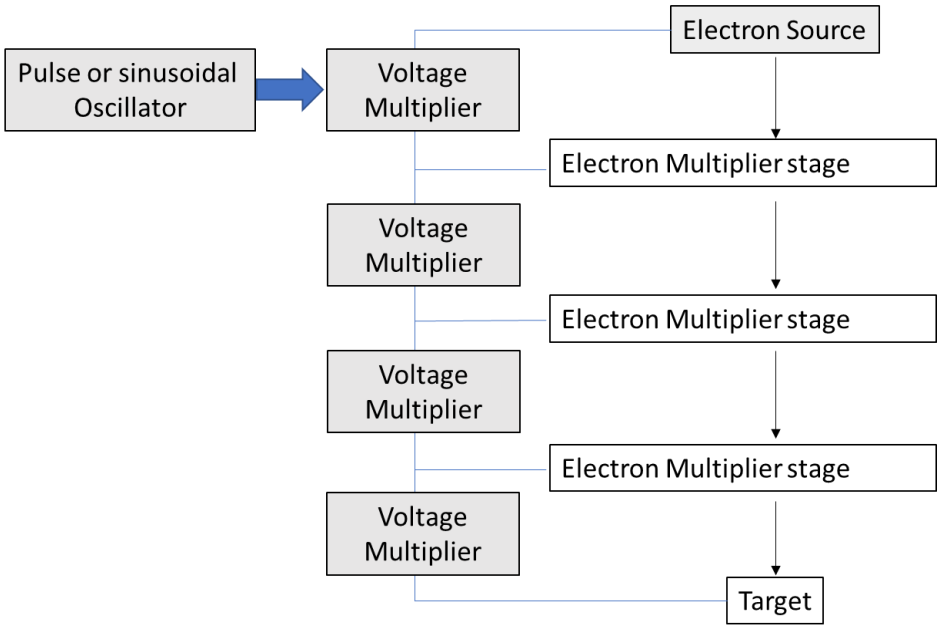

Figure 2.8: *Series rectifier-based supply* [6]

Figure 2.8 illustrates a third possible method of powering the PMTs dynode chain. The Cockcroft Walton series voltage rectifier is commonly used for generating a single high voltage supply; however if the number of stages exceeds the number of dynodes in the PMT then outputs can be taken from each multiplier stage. In comparison with the previous examples, the steady state current draw is only the leakage, however it potentially requires a filter stage for every dynode as well as the anode supply, making it either bulky or noisy. CW ladders can also suffer from complex droop effects, to be discussed in 3.1.

2.5 *Coupling techniques*

Although the previous section has detailed the mechanics of the photon activated electron multiplication within the photomultiplier, the current proportional to any optical event needs to be coupled through to subsequent measurement circuits.

This can be achieved through a variety of means, each of which will have differing effects on linearity, resolution, dynamic range, and ease of coupling to following stages.

At an early stage in the design the decision must be made as to whether AC or DC coupling will be more suitable for the system. AC coupling will introduce signal artefacts related to the coupling capacitor charging and discharging, resulting in a rate dependant baseline shift if these effects overlap (see figure 2.9) as well as capacitive fly back effects. DC coupling on the other hand will result in an offset varying with temperature due to Dark current components and DC leakage across the component.

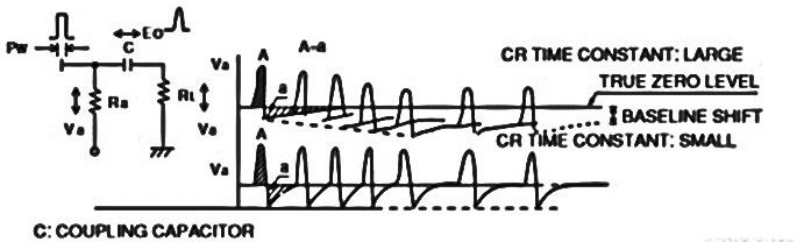

Figure 2.9: *Effect of count rate on baseline for a capacitively coupled system.* [6]

The relevance of this is that typically thermal offset variation will be far slower than rate dependant baseline shift, and so is easier to correct. The advantage of AC coupling is that it requires no active components so is likely to be more robust, considering the high voltages involved.

Finally, when dealing with the practicalities of producing a high-performance system, simplicity of PCB layout and vulnerability to induced noise need to be considered.

2.5.1 Resistor-capacitor

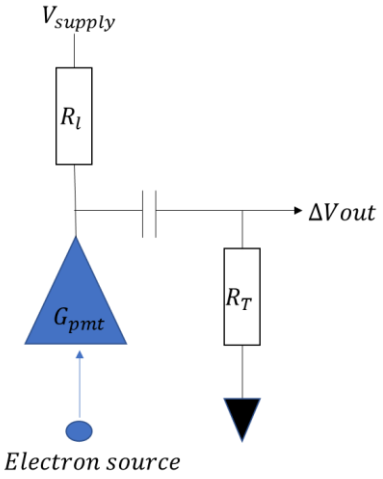

Figure 2.10: *Resistive loading of a photomultiplier tube.*

Figure 2.10 illustrates the most common form of decoupling a PMT, the resistively loaded AC coupled anode follower. Varying PMT current through R_L results in a voltage swing across the anode resistor in proportion to anode current. As the coupling capacitor is charged to the supply voltage (V+) the AC signal is coupled through to the terminating resistor, R_T.

The major advantage of this circuit is its simplicity. It only requires 3 additional components and as an industry standard produces results in line with end user expectations.

The disadvantages associated with AC coupling have been discussed previously. In addition to this, the voltage developed across R_L is subtracted from the anode voltage. As this anode voltage has a linear relationship with gain of the electron multiplier this produces a non-linearity in proportion to the load value.

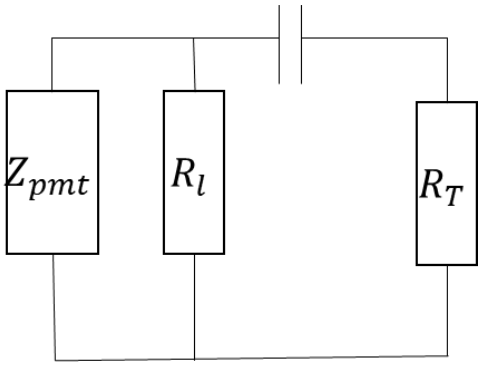

Figure 2.11: *Resistive loaded photomultiplier tube equivalent output impedance.*

The small signal output impedance (as shown in Figure 2.11) becomes the PMT in parallel with R_{load}.The PMTs impedance is typically orders of magnitude higher than the load resistance so output impedance can be considered as $R_L||R_T$.

The relationship between energy deposited in a scintillation event and the output voltage is given in the following example:

Ignoring any dark current in the PMT the dynamic current will be:

$$I_{Rl\_Event} = Single\ electron\ event \times G_{pmt}$$

$$V_{RL} = I_{RL\_Event} \times R_L$$

After introducing the AC coupling stage:

$$\Delta V_{out} = I_{RL\_Event} \times (R_L||R_T)$$

So the output voltage when used with a scintillation radiation detector could be calculated as the following simplified example (ignoring time domain):

$$Scintillator\ sensitivity = 50\ photons\ per\ KeV,\ Event\ energy = 1KeV$$

$$Photocathode\ efficency = 30\%,\ G_{pmt} = 60 \times 10^6$$

$$R_l = 1K\Omega\ , R_T = 10K\Omega$$

$$Electron\ current = 0.16 \times 10^{-15}A$$

$$Electrons\ released = Event\ energy \times Scintillator\ sensitivity\ \times Cathode\ efficency$$

$$= 1 \times 50 \times 0.3$$

$$= 15\ photoelectrons$$

$$\Delta Vout = photoelectrons(I_{RL_{event}} \times (R_L||R_T))$$

$$= photoelectrons(electron\ current\ \times\ G_{pmt} \times (R_L||R_T))$$

$$= 15(0.16 \times 10^{-15} \times 6 \times 10^6 \times (1 \times 10^3||10 \times 10^3)$$

$$= 15(9.6 \times 10^{-9} \times (909))$$

$$= \mathbf{0.131mV/KeV}$$

2.5.2 *Transimpedance and charge amplifiers*

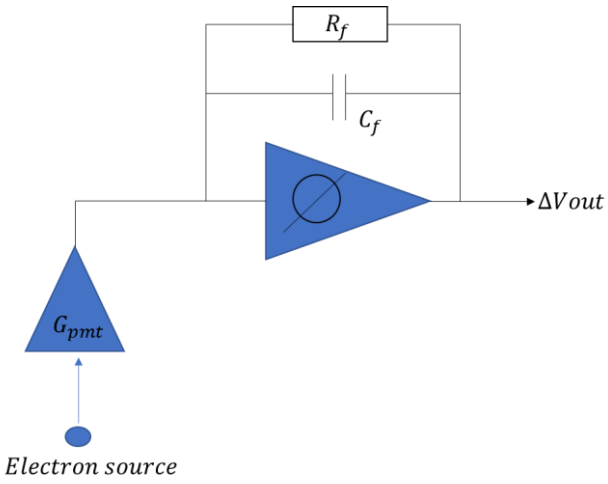

Figure 2.12: *Transimpedance coupling of a photomultiplier tube.*

Figure 2.12 illustrates the coupling of a PMT to a transimpedance or charge amplifier. This is DC coupled so will also amplify the dark current associated with the tube but avoid rate dependant baseline shifts where a capacitively coupled device would tend toward AC. A negative high voltage supply is typically applied to the cathode with the anode at 0V to allow coupling to low voltage circuitry.

The disadvantages to such a system are that inverting high ratio power supplies require more components to produce and PMTs with exposed metalwork often have it connected to the cathode internally creating isolation concerns.

If the amplifier's feedback is predominantly resistive it will be in transimpedance mode of operation with change in output given as the following:

$$\Delta\mathrm{Vout} = -\mathrm{I_{PMT}} \times \mathrm{R_f}$$

So, to give the same sensitivity as the previous resistively coupled example:

$$\Delta Vout = 0.131 mV/KeV$$

$$Scintillator\ sensitivity = 50\ photons\ per\ KeV$$

$$Event\ energy = 1KeV,\ Photocathode\ efficency = 30\%$$

$$G_{pmt} = 60 \times 10^6$$

$$Electron\ current = 0.16 \times 10^{-15}A$$

$$Electrons\ released = Event\ energy \times Scintillator\ sensitivity\ \times Cathode\ efficency$$

$$= 1 \times 50 \times 0.3$$

$$= 15\ photoelectrons$$

$$R_f = \Delta Vout/-I_{in}$$

$$= \frac{0.131 \times 10^{-3}}{electron\ current \times G_{pmt} \times electrons}$$

$$= \frac{0.131 \times 10^{-3}}{0.16 \times 10^{-15} \times 60 \times 10^6 \times 15}$$

$$= \frac{0.131 \times 10^{-3}}{1.44 \times 10^{-7}}$$

$$\boldsymbol{R_f = 909\Omega}$$

If the amplifier's feedback is set to be predominantly capacitive then it becomes a charge sensitive amplifier.

Gain becomes:

$$\Delta Vout = Q/C_f,\ Q = It, \Delta Vout = (I \times t)/(C_f)$$

The feedback resistor (R_f) is still included to discharge C_f between events and so sets the time constant of the circuit. To set gain to that of previous examples C_f would become equal to:

$$\Delta Vout = 0.131mV/KeV$$

$$Scintillator\ sensitivity = 50\ photons\ per\ KeV$$

$$Event\ duration = 1us,\ Event\ energy = 1KeV$$

$$Photocathode\ efficency = 30\%, G_{pmt} = 60 \times 10^6$$

$$Electron\ current = 0.16 \times 10^{-15} A$$

$$Electrons\ released = Event\ energy \times Scintillator\ sensitivity\ \times Cathode\ efficency$$

$$= 1 \times 50 \times 0.3$$

$$= 15\ photoelectrons$$

$$Input\ charge = It$$

$$= electron\ current \times photoelectrons \times G_{pmt} \times t$$

$$= 0.16 \times 10^{-15} \times 60 \times 10^6 \times 15 \times 1 \times 10^{-6}$$

$$= 14.4 \times 10^{-12}$$

$$= 0.144pC$$

$$\Delta Vout = Q/C_f$$

$$C_f = \frac{Q}{\Delta Vout}$$

$$= \frac{14.4 \times 10^{-14}}{0.131 \times 10^{-3}}$$

$$= 1.01 \times 10^{-9}$$

$$= \mathbf{1.01nF}$$

2.5.3 *Current mirror*

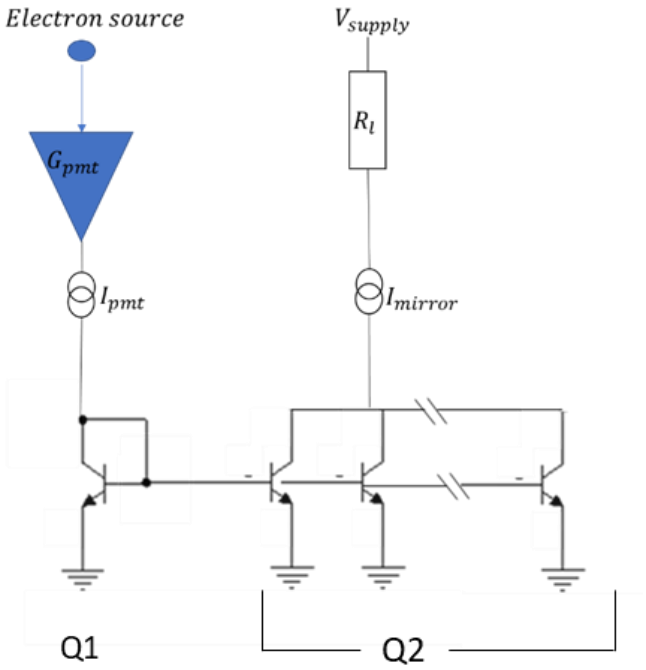

Figure 2.13: *Current mirror coupling of a photomultiplier tube.*

Figure 2.13 demonstrates the application of a bipolar current mirror to couple anode current (through diode connected Q1) through to a separate chain from the collector of Q2.

This potentially removes the compression effects associated with resistive coupling and has none of the associated AC coupling effects. However, it does require a further element to decouple to a stage closer to ground for the positive HT variant, doubling the anode current.

For example, if the required 0.131mV/KeV was required with a 50Ω source impedance from a single current mirror stage the mirror ratio would be:

$$\Delta Vout = 0.131mV/KeV,\ Scintillator\ sensitivity = 50\ photons\ per\ KeV$$

$$Event\ energy = 1KeV,\ Photocathode\ efficency = 30\%$$

$$G_{pmt} = 60 \times 10^6$$

$$Electron\ current = 0.16 \times 10^{-15} A$$

$$R_l = 50\Omega$$

$$Electrons\ released = Event\ energy \times Scintillator\ sensitivity\ \times Cathode\ efficency$$

$$= 1 \times 50 \times 0.3$$

$$= 15\ photoelectrons$$

$$event\ current = electron\ current \times photoelectrons \times G_{pmt}$$

$$= 0.16 \times 10^{-15} \times 60 \times 10^{6} \times 15$$

$$= 14.4 \times 10^{-6}$$

$$= 144nA$$

$$mirrored\ current = \frac{\Delta V}{R_l}$$

$$= \frac{0.131 \times 10^{-3}}{50}$$

$$= 2.62 \times 10^{-6}$$

$$= 2.62\mu A$$

$$mirror\ ratio = \frac{mirrored\ current}{event\ current}$$

$$= \frac{2.62 \times 10^{-6}}{0.144 \times 10^{-6}}$$

$$\textbf{\textit{Mirror ratio}} = \mathbf{18.19}$$

2.5.4 *Signal transformer*

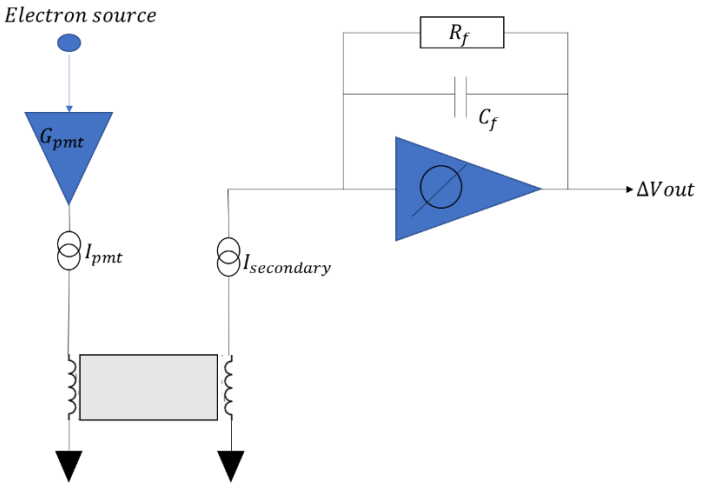

Figure 2.14: *Transformer coupled Photomultiplier tube*

Figure 2.14 illustrates a development of the resistive load of the previous example to introduce a pulse transformer. As the PMT pulls current through the primary winding of the transformer it is charged, which is then coupled to the secondary winding. In this example the current induced in the secondary is coupled to a transimpedance amplifier.

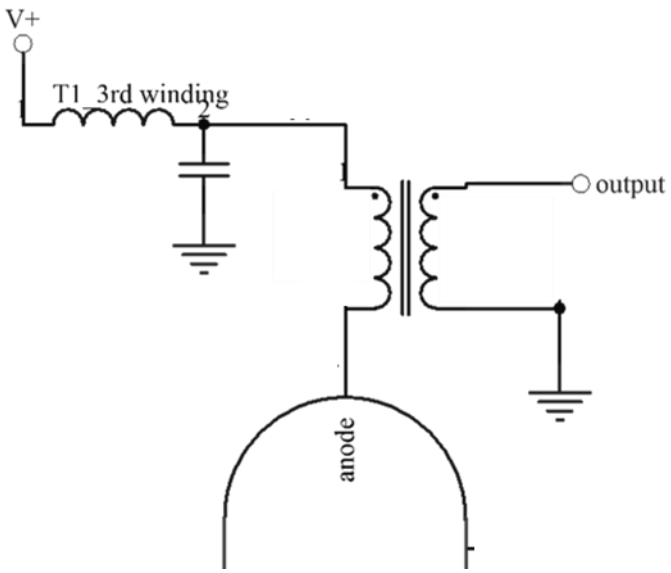

Figure 2.15: *Noise cancelling diagram*

Figure 2.15 highlights a potentially useful addition of a tertiary winding in series with the primary, with an intersecting node bypassed to ground [9] . This arrangement sums ripple in the primary with its inversion in order to common mode reject the ripple from the secondary (output) winding.

Although this adds to cost and component count it has an advantage over the previous DC coupled transimpedance method that less gain is required, allowing a lower specification amplifier to be used.

For example, if a 1:3 transformer were used to couple the PMT to transimpedance amplifier from the previous example the new value of R_f would be:

$$Event\ energy = 1KeV,\ Photocathode\ efficency = 30\%$$

$$G_{pmt} = 60 \times 10^6,\ Electron\ current = 0.16 \times 10^{-15}A$$

$$Turns\ ratio = 3:1$$

$$Electrons\ released = Event\ energy \times Scintillator\ sensitivity\ \times Cathode\ efficency$$

$$1 \times 50 \times 0.3\ = 15\ photoelectrons$$

$$Transfromer\ secondary\ current = (electron\ current \times G_{pmt} \times electrons) \times (\frac{1}{Turns\_ratio})$$

$$= 0.16 \times 10^{-15} \times 60 \times 10^6 \times 15 \times 3$$

$$= 1.44 \times 10^{-7} \times 3$$

$$= 4.32 \times 10^{-7}$$

$$=0.43\mu A$$

$$R_f = \Delta Vout/-I_{in}$$

$$= \frac{0.131 \times 10^{-3}}{0.43 \times 10^{-6}}$$

$$\boldsymbol{R_f = 304\Omega}$$

The required gain bandwidth product for the amplifier then can be reduced from the previous example as follows, assuming the following parameters:

$$C_{pmt} = 2pF, C_{transformer\ secondary} = 10pF,\ C_f = 20pF$$

$$F_{GBW} > (\frac{C_{in} + C_f}{2\pi R_f C_f^2})$$

So the required gain bandwidth for the DC coupled amplifier becomes:

$$R_f = 909\Omega$$

$$C_{pmt} = 2pF$$

$$= \frac{2 \times 10^{-12} + 20 \times 10^{-12}}{2\pi \times 909 \times \left((20 \times 10^{-12}) \times (20 \times 10^{-12})\right)}$$

$$= \frac{22 \times 10^{-12}}{2854.26 \times 400 \times 10^{-24}}$$

$$= \frac{22 \times 10^{-12}}{1.14 \times 10^{-18}}$$

$$= 19{,}298{,}245$$

For amplifier selection this would be rounded to:

$$\boldsymbol{F_{gbw} > 20MHz}$$

For the transformer coupled example:

$$C_{transformer\ secondary} = 10pF$$

$$R_f = 304\Omega$$

$$= \frac{10 \times 10^{-12} + 20 \times 10^{-12}}{2\pi \times 909 \times \left((20 \times 10^{-12}) \times (20 \times 10^{-12})\right)}$$

$$= \frac{30 \times 10^{-12}}{964.56 \times 400 \times 10^{-24}}$$

$$= \frac{30 \times 10^{-12}}{3.82 \times 10^{-19}}$$

$$= 7{,}853{,}403$$

For amplifier selection this would be rounded to:

$$\boldsymbol{F_{gbw} > 8MHz}$$

As can be seen from the previous example the required gain bandwidth from any opamp used as a transimpedance amplifier is significantly reduced with the inclusion on a coupling transformer, providing gain system gain requirements are equal. This also adds isolation from high voltage photomultiplier circuits at the expense of AC coupling.

3 High Voltage DC-DC Converters

3.1 Cascading power supply topologies

In order to achieve the high ratio power supply multiplication ratios required for reaching the required high voltage rail from a typical battery voltage, various topologies will be employed in combination. The nature of this development lent itself to a single feedback regulation loop so the various multipliers and first stage converters will be reviewed to this end. [10] [11]

As the development was intended to be equally applicable to most currently used image tubes and electron multipliers this ratio varies between 1:200 for a 650V PMT and 1:6000 for a 20KV micro channel plate base image intensifier. To encompass the required headroom for adjustment the PMT based scintillation detector used for this development required an initial 1:300 (1KV) capable system.

3.2 Voltage Multipliers

3.2.1 Cockcroft Walton multipliers

Although loosely based on the *Schenkel multiplier and Greinacher multiplier* the Cockcroft Walton designed by *John Cockroft* and *Ernest Walton* was famously used when they worked alongside *Ernest Rutherford* to split a lithium atom. Figures 3.1 & 3.2 shows the operation of the circuit. A 2-stage circuit is used as an example as it both illustrates the principal of operation and the cascode interaction between stages.

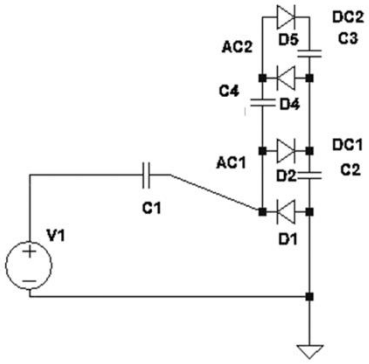

Figure 3.1: *Two stage Cockcroft Walton multiplier/ series rectifier.*

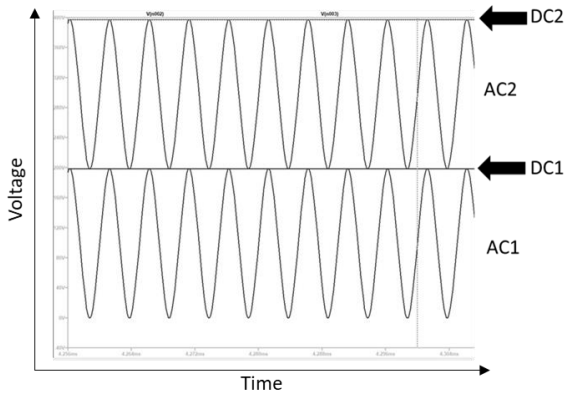

Figure 3.2: *Waveforms at points of a Cockcroft Walton multiplier.*

The original Cockcroft Walton multiplier generator used active stages (switched triodes) in the first stage, however these can be omitted to demonstrate the concept. [12] [13]

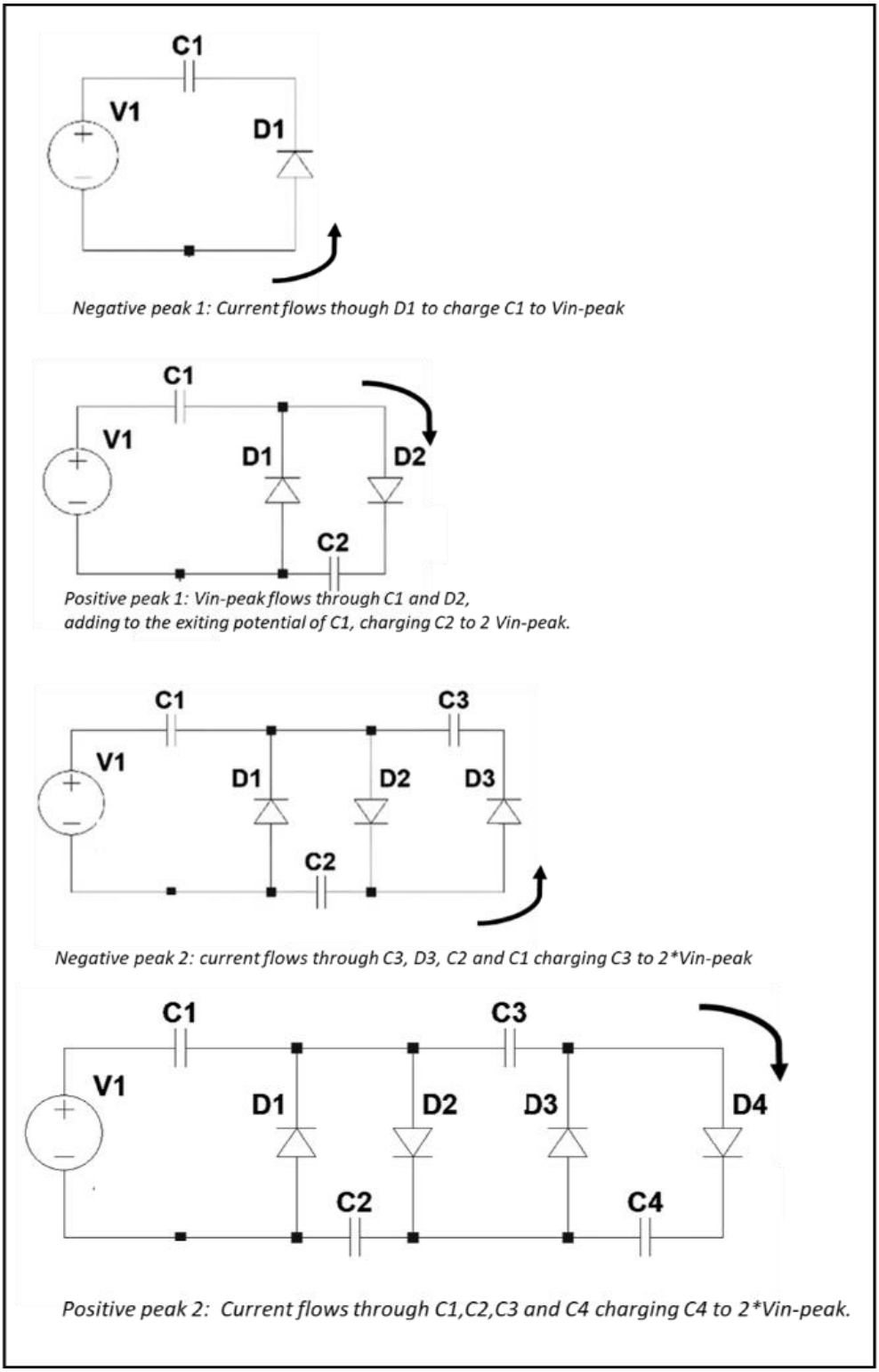

Figure 3.3: *The pumping mechanism of voltage multiplication in series rectifier circuits.*

Capacitors C1 and C3 can be considered as primarily coupling capacitors, whereas C2 and C4 are smoothing capacitors. These descriptions all assume zero supply impedance from the AC source so in application this will take significantly longer than the time period of a single wave for each stage to charge. [14] [15] [16]

Taking an output from the series combination of the C2-C4 chain:

$$V_{out} = V_{c2} + V_{c4}$$

$$= \left(2 \times V_{inpeak}\right) + \left(2 \times V_{inpeak}\right)$$

$$= 4\, V_{inpeak}$$

So for an n-stage network:

$$V_{out} = 2n(V_{inpeak})$$

Ignoring any diode losses, the intrinsic loss of the circuit is given by: (term removed)

$$I_l = output\ current, F = drive\ frequency, C = capacitance, n = nuber\ of\ stages$$

$$V_{droop} = (\frac{I_l}{6 \times F \times C}) \times (4n^3 + 3n^2 - n)$$

Which leads to an output of:

$$V_{out} = \left(2n \times V_{inpeak}\right) - \{\left(\frac{I_l}{6FC}\right) \times (4n^3 + 3n^2 - n)\}$$

$$V_{ripple} = \left(\frac{I_l}{2FC}\right) \times \left(n \times (n+1)\right) \qquad (x)$$

To build a high-performance system including these limitations can cause issues with dynamic noise flaws and an equivalent supply impedance, especially when as previously discussed a PMT has a voltage dependent gain. The polynomial nature (ix) of these can be difficult to compensate for and/or narrow the range of stable operation if this circuit is included in any closed loop control systems.

A development to this circuit is to taper the capacitor values so:

C1&2= nC, C3&4=(n-1)C, C5&6=(n-2)C, etc. *(xi)*

As this source of loss is caused by each stage being driven from a combination of the source voltage and the subsequent stage, tapering the capacitors in this manner reduces the losses to that of a single stage ladder, which due to the n^2 and n^3 terms can be significant in longer chains. The droop and ripple is given as:

$$V_{ripple} = n \times (\frac{I_l}{FC})$$

$$V_{droop} = n^2 \times \left(\frac{I_l}{FC}\right)$$

The circuit is equally suitable for pulsed circuits but 2. V_{in}- peak is substituted for V_{pulse}.

Table 1: *Approximation of linear multipliers for capacitor selection*

Required multiplier	Available multiplier
1	1
2	1.8
3	2.2
4	3.3
5	3.9
6	4.7
7	5.5
8	6.8
9	8.2
10	10

Although this removes the polynomial element of the transfer function it does rely on capacitors being available in suitable multipliers. Table 1 highlights the difference between desired and available multipliers for capacitor values.

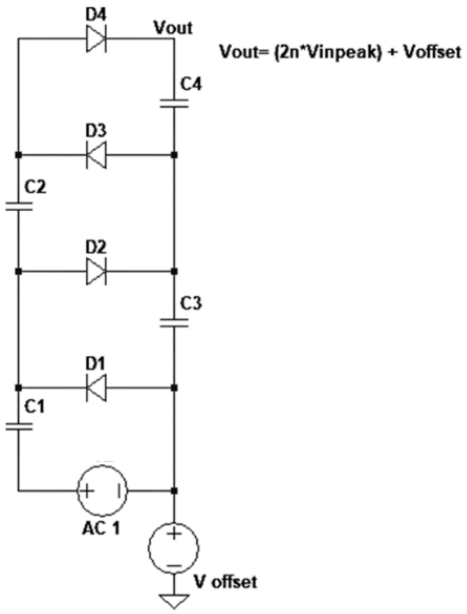

Figure 3.4: *Offset half wave series rectifier circuit*

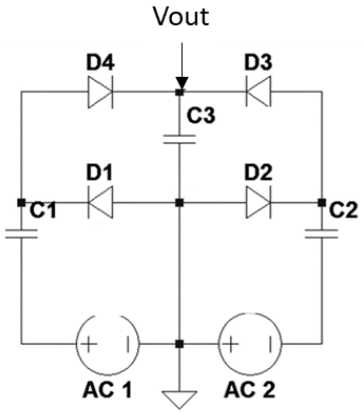

Figure 3.5: *Full wave series rectifier*

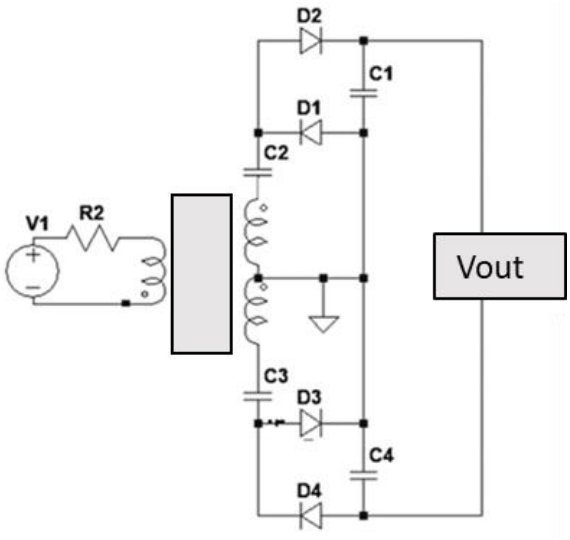

Figure 3.6: *Bipolar series rectifier example.*

Figures 3.4 to 3.6 and the following analysis demonstrates the half wave operation of the circuit; however, it can be used in full wave (figure 3.5), bipolar (figure 3.6), or with a DC offset (figure 3.4).

The advantage of this circuit is primarily its simplicity. Its passive nature making it extremely efficient for low load supplies, and as each stage is charged to the rectified input voltage. Bulky high voltage components are kept to a minimum. The disadvantages are that it has a complex transfer function for closed loop systems and requires careful selection of driver circuits.

3.2.2 Dickinson charge pump multipliers

An active alternative to the CW multiplier is the *Dickinson Charge pump voltage multiplier.* There are alternative charge pumps, but these are largely improved in low voltage performance. Its operation is demonstrated in figure 3.7. It consists of a DC input (V1), and output peak detector (D5&C5), a 2-phase oscillator (V2 & V3) and a number of switching stages.

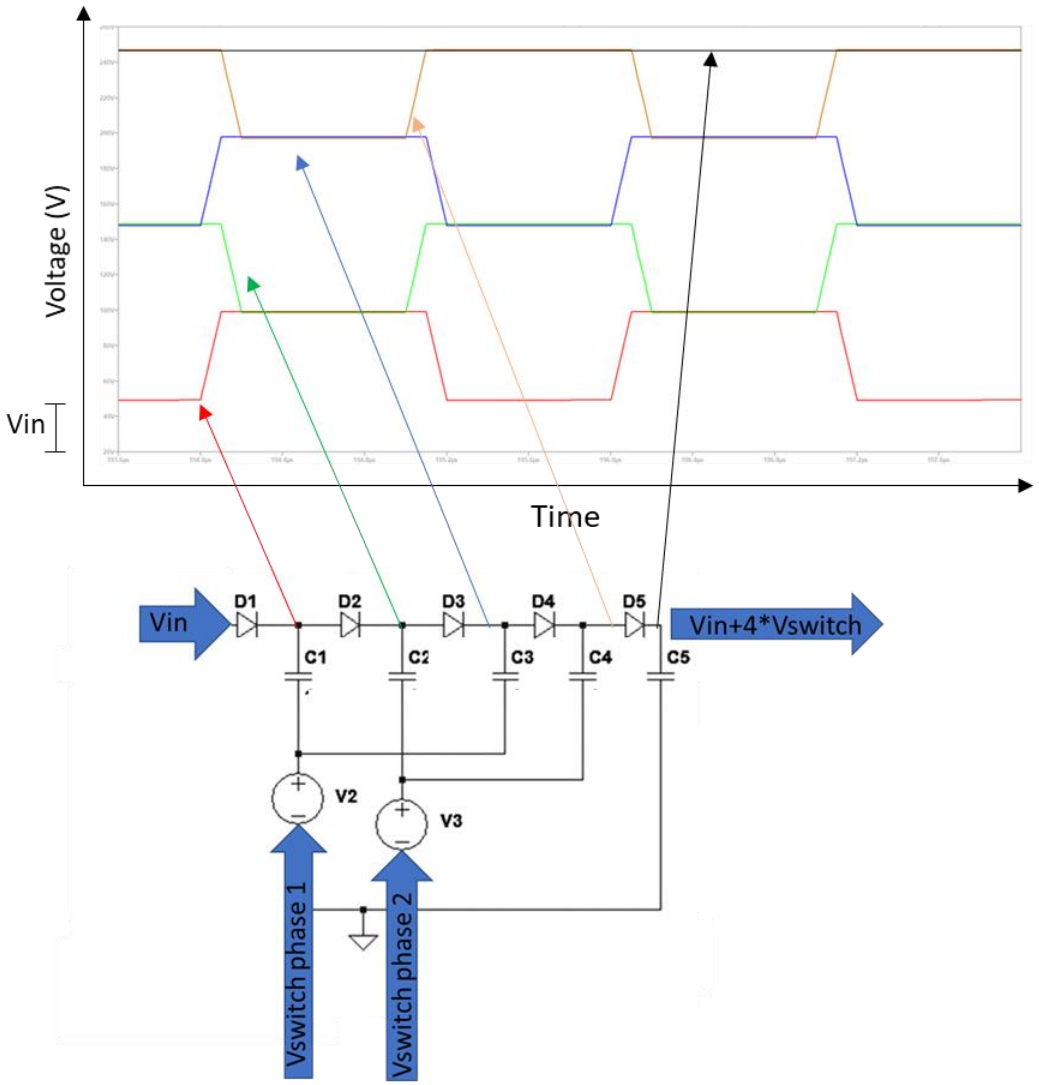

Figure 3.7: *Dickinson charge pump multiplier*

Whilst the oscillator is in its low state C1 charges to V1-diode drop. V2 pulses the lower side of C1 between V1 and V1+V2. Running V2 and V3 out of phase allows the D2 and C2 to act as a peak detector when V2 is high.

Therefore, the output becomes:

$$V_{out} = V_{in} + (V_{switch} \times n)$$

Or if $V_{in} = V_{switch}$ then:

$$V_{out} = V_{in}(n + 1)$$

This is not a direct replacement for a Cockcroft-Walton multiplier as it takes a DC input; however the switching pulse amplitude does need to be similar to that required to drive the previous multiplier in full wave form. In actuality it needs a DC and a 2 phase pulsed input, rather than the single pulsed input of the CW multiplier. The point where it fails to be competitive for high voltage circuits is that C1 needs to be rated to Vin, as with the CW multiplier, but C2 needs to be rated to 2*Vin and C3 to 3*Vin etc. This makes the circuit potentially bulky and expensive.

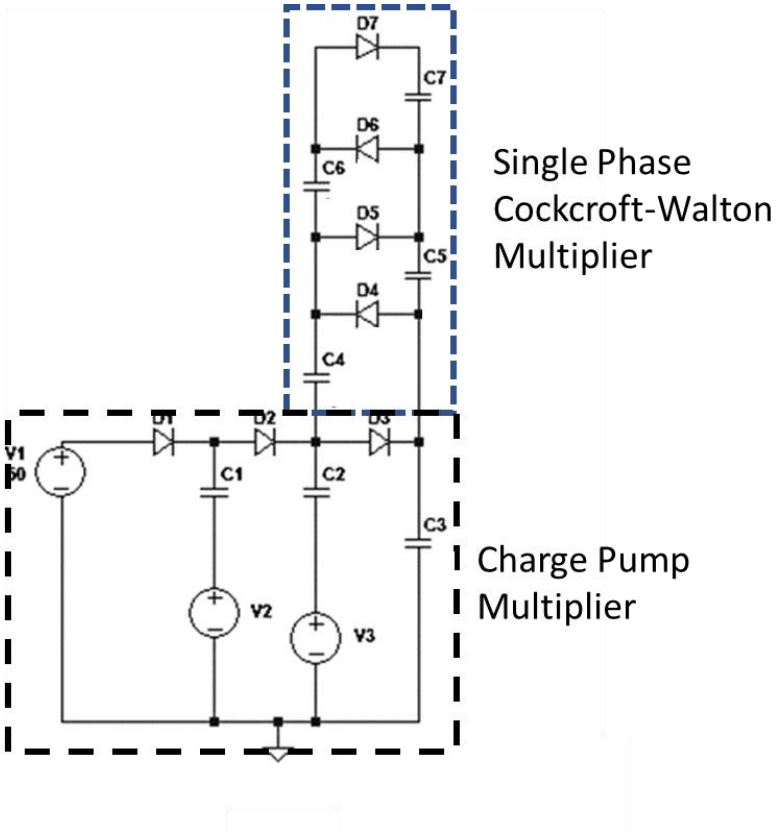

Figure 3.9: *Implementation of coupling a switched charge pump to a Cockcroft Walton stage*

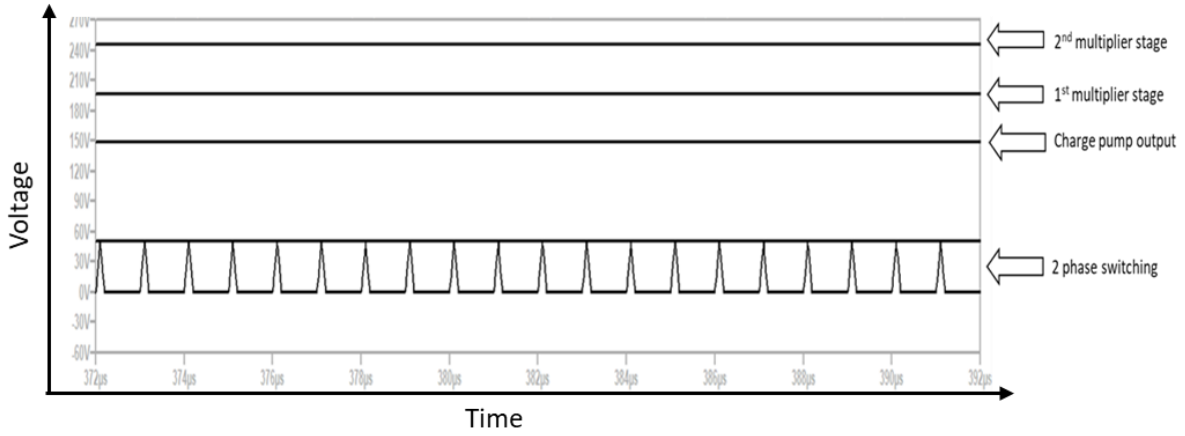

Figure3.10: *Operation of coupled circuit.*

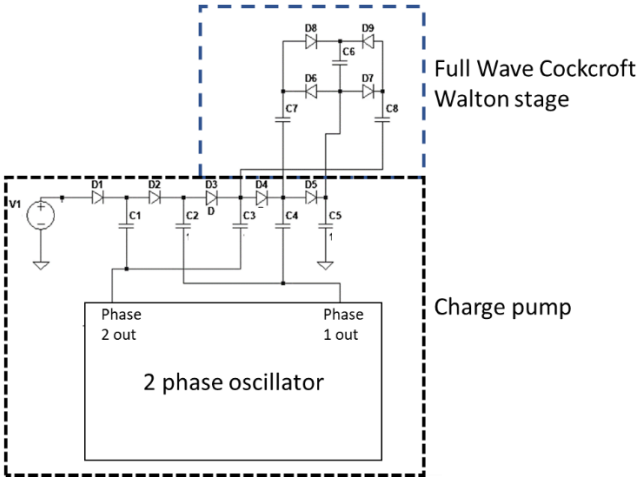

Figure 3.11: *Hybrid CW/Dickinson charge pump example*

3.3 Step-up converters

3.3.1 Fly back buck-boost converters

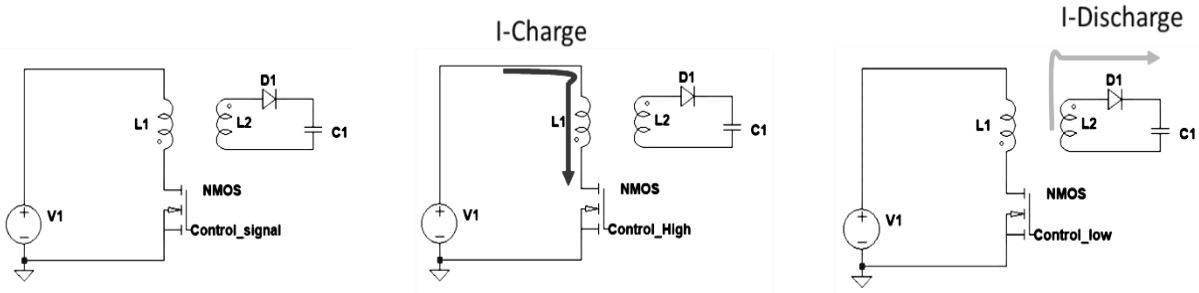

Figure 3.12: *Details of buck-boost operation.*

Often referred to simply as a Flyback converter, the *Flyback-buck-boost* converter is either a PWM (pulse width modulation) or PFM (pulse frequency modulation) topology. Only the flyback implementation is to be considered, as the ratio between input and output limits the use of simpler topologies.

The simplified principle of operation is demonstrated in figure 3.12; the switch is closed causing current *I_charge* to flow, charging the primary winding. During this period the rectifier diode is reverse biased. When the switch is opened the diode becomes forward biased, allowing current Id to flow, charging the smoothing capacitor from the transformer secondary. In its simplest terms the ratio of input to output voltage is based on the ratio the switch is closed to open.

The next level of complexity is that the converter can either be run in *continuous* or *discontinuous* mode, vastly altering its characteristics and transfer function:

- In continuous mode the inductor will not fully discharge on each cycle. This residual charge is given as a percentage of the inductors total charge.
- In discontinuous mode the primary completely discharges each time the switch is opened. A simplification of this is that discontinuous mode offers higher step up ratios at the expense of noise, efficiency and linearity, which equates to stability in a feedback-based system.

They can also be considered as a binary situation whereby a converter stage is either continuous or discontinuous as load conditions will dictate its operating region. It is therefore a case of managing the point at which a converter will switch between these conditions.

The distinction that enables this circuit to act as a switching regulator as opposed to a simple proportional voltage converter is the mechanism controlling the switching of the circuit. A control signal proportional to the output voltage is compared with a reference voltage (or ‘set-point’) to generate an error term which is in turn used to generate a control signal from a VCO (voltage-controlled oscillator). This VCO can either generate a suitable PWM or PFM to drive a suitable switching device. A PWM signal will consist of a constant

period, variable on time signal whereas a PFM will consist of a constant on time, variable period waveform.

The difficulty with this approach is that in an effort to raise efficiency of commercial amplifiers they typically use a combination of both current and voltage feedback along with burst mode PWM. This resembles PWM as a switching function superimposed upon a low frequency PFM and variable frequency PWM.

3.3.2 Blocking oscillators

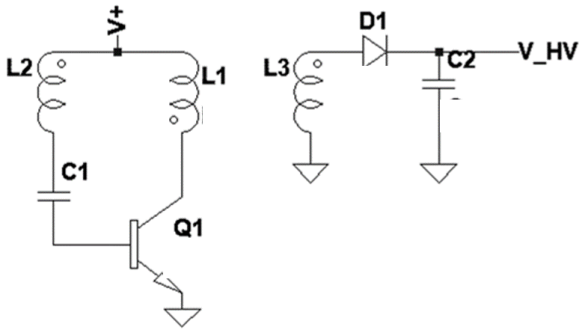

Figure 3.13: *Hartley/Blocking oscillator (L1,L2,L3 single transformer)*

The blocking oscillator is a relatively basic design dating from the mid-1930s in thermionic valve form. Shown in figure 3.13, It is based around a transformer with a primary either connected to the anode or collector circuit and a secondary driving either the grid or base circuit. The oscillation on the primary winding can either be rectified, or for higher voltages a tertiary winding of higher ratio (L3) can be used to step this up for increased output. Despite its simple nature this is still used for commercial low current high voltage supplies due to its small footprint, simple nature, low design cost, and proven results.

In operation the collector current charges L1 which couples through to L2 out of phase, blocking the collector current. This process will repeat resulting in sinusoidal oscillation of the collector current. The time constant of this is set by base capacitor C1. A tertiary winding with a high turns ratio relative to L1 steps up these oscillations and is then rectified (D1, C2) to form a DC output. This DC output is proportional to the input supply voltage without any means of adjustment. The resonance of the circuit will be affected by the forward current gain of Q1 so will vary dramatically with temperature.

Commercial examples [17] are commonly available but will typically have a several hundred-mW offset power along with a poor efficiency making them unsuitable for portable equipment. This is high enough to prevent battery powered equipment running for extended periods.

The fundamental disadvantage of this circuit is difficulty of adjustment as stated above. As has been discussed in section 1.1 the acceptable voltage variation is very small for a photo multiplier circuit, so feedback to compensate for voltage multiplier losses is an essential part of the system. The most common method of implementing this is to take the V+ input from the output of an operational amplifier (able to supply sufficient output current) controlled by a processed feedback signal post multiplier. This simple yet effective method has the disadvantage that losses are incurred in the voltage difference between the V+ level and the system input voltage along with the quiescent current of substantial operational amplifiers.

3.4 Phase margin considerations of cascaded systems

In a closed loop system the phase margin can be defined as a phase difference between nodes in the system, normally system input and returned feedback signal. Any significant lag (or lead) in this mechanism can result in system instability.

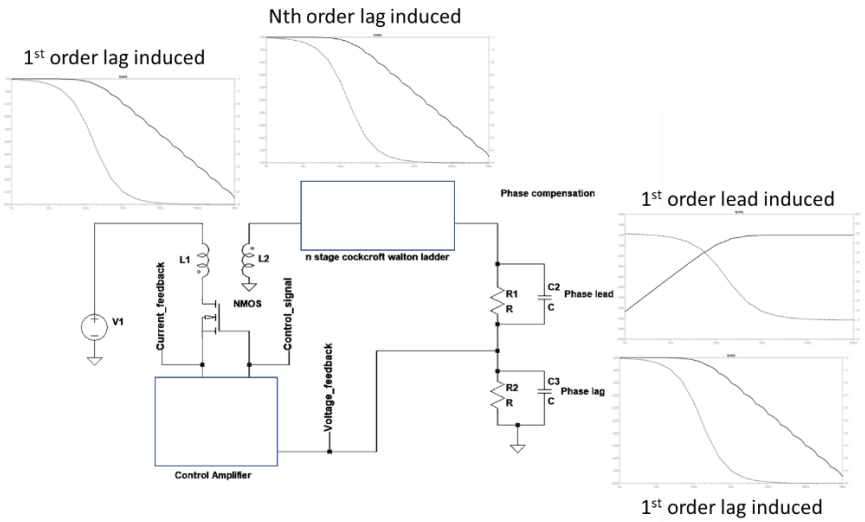

Figure 3.14: *illustration of the various potential phase margin factors in a complex switching regulator.*

Figure 3.14 illustrates some of the various factors affecting this phase throughout a typical system. In simpler systems the current through the switch can be monitored to control the output voltage, however this can do little to compensate for droop of a voltage multiplier included in the system. To maintain a stable system output using final voltage feedback the control input and switching behaviour needs to have a phase margin within certain limits to avoid instability.

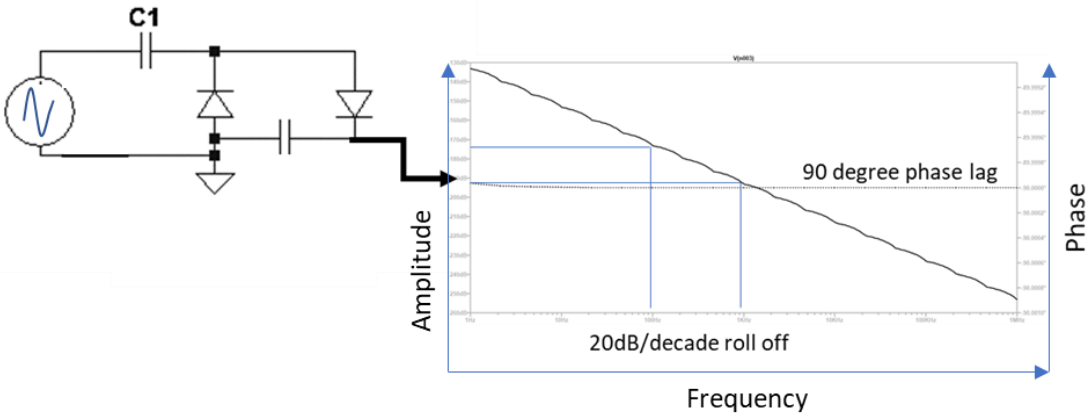

Figure 3.15: *Phase margin of a single Cockcroft Walton series rectifier.*

As can been seen in the simulation illustrated in figures 3.15 each Cockcroft Walton stage will introduce a 90-degree phase lag.

For example a converter based around a PWM flyback converter with an inverting transformer and 5 CW stages would have a phase margin of:

$$Converter\ margin + flyback\ margin + n(multiplier\ margin) = total\ phase\ margin$$

$$+90 + -180 + 5(-90) = -540°$$

Or in real terms a 180 degree phase margin

This would need to be corrected if used in the feedback loop of a 3rd party boost or flyback converter system intended for a less complex system. The equivalent 180° lag will create steady state instabilities whilst the actual 540° lag will cause higher inrush currents on start-up.

3.5 Design specifications

The following specification has drawn up for a System in Package (SiP) PMT module capable of competing with solid state alternatives at a practical level.

- Footprint equal to that of an equivalent area solid-state detector module.
- Power supply requirements equal to that of a solid-state module with the inclusion of a buffer amplifier.
- To provide positive going output signal to be retrofittable in the place of a solid-state detector.
- Suitable to be battery powered.
- To incur minimum degradation in performance of its low power consumption and reduced form factor.

4 Multi-layer Ceramic Capacitors (MLCC)

4.1 Overview

High density surface mount boards demand the use of MLCC on the grounds of cost, size and availability. The trade-off for a compact footprint is a varying capacitance with different AC and DC conditions. Under static conditions (such as simple power rails) such variance can be compensated for with larger values; however in closed loop control systems these can cause dynamic elements in otherwise static circuits resulting in varying phase margins and in turn circuit instability. Published datasheet parameters [18] vary from package to package and manufacturer to manufacturer.

Multilayer ceramic capacitors can be divided into 2 categories:

- Class 1 capacitors (e.g. C0G) which are typically *Calcium Zirconate* and;
- Class 2/3 (e.g. XR5/XR7) which are typically *Barium Titanite.*

The class dictates an overall stability rating with DC voltage, frequency, and temperature.

A concern in this compact high voltage design, as highlighted in chapter 3.1, is the number of capacitors required for either Dickinson charge pump or Cockcroft Walton circuits in order to achieve maximum functionality.

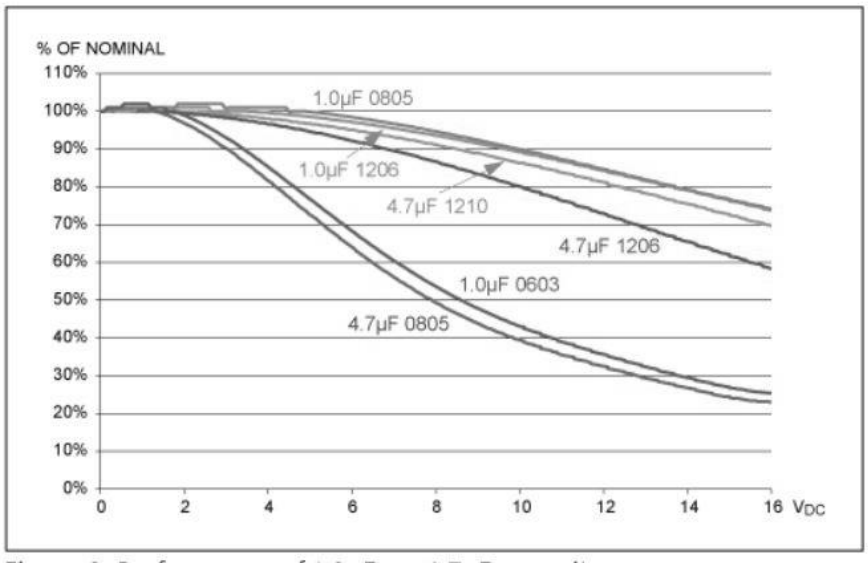

Figure 4.1: *Maxims study of MLCCs for power supply decoupling* [19]

Figure 4.1 and accompanying paper [19] highlight the variation of capacitance with DC bias of various decoupling capacitors' low voltage applications. As higher voltage capacitors require more dielectric material, they typically have fewer layers stacked in a larger package so have different characteristics.

4.2 Measured results

A non-taper multiplier is assumed, as the inaccuracies of a non-uniform taper would be too complex to draw conclusions from. A 22nF 600V rated XR7 1206 capacitor was chosen as a typical example for testing. Capacitance was measured by applying a DC bias across the capacitive element of a low pass filter.

Figures 4.2 and 4.3 show the results of bench testing using a test jig. For static voltage parts, such as supply decoupling capacitors the actual value can be obtained from this curve and the published (1V) value adjusted accordingly to achieve the correct capacitance under bias. Excel is used to estimate the best curve fit. A fourfold change in capacitance is observed with a variation of just under 1200v in the DC voltage

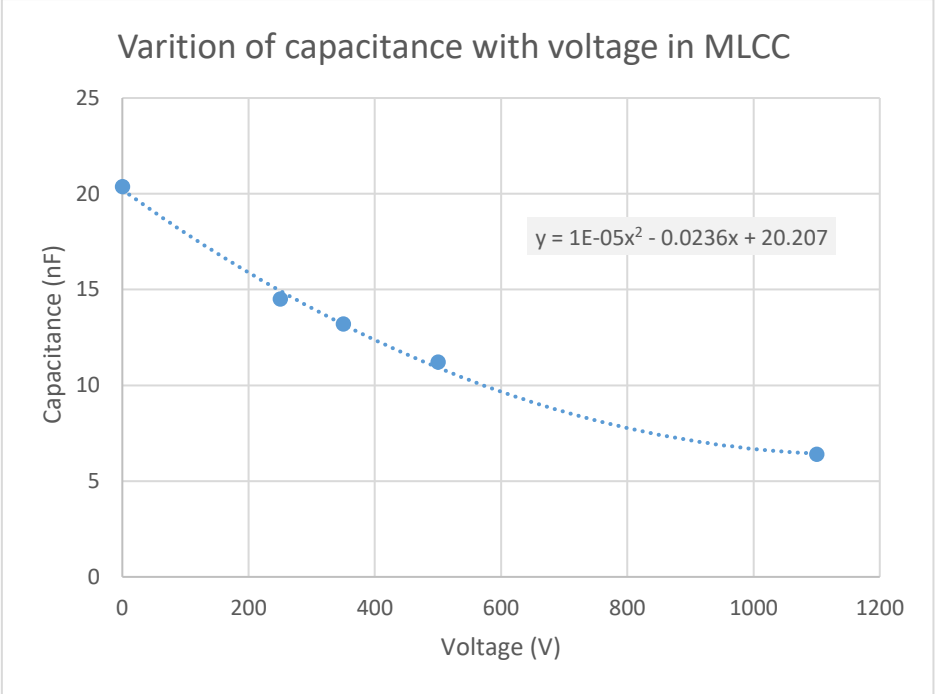

Figure 4.2: *Capacitance variation of a 1206 22nF 600v capacitor with voltage.*

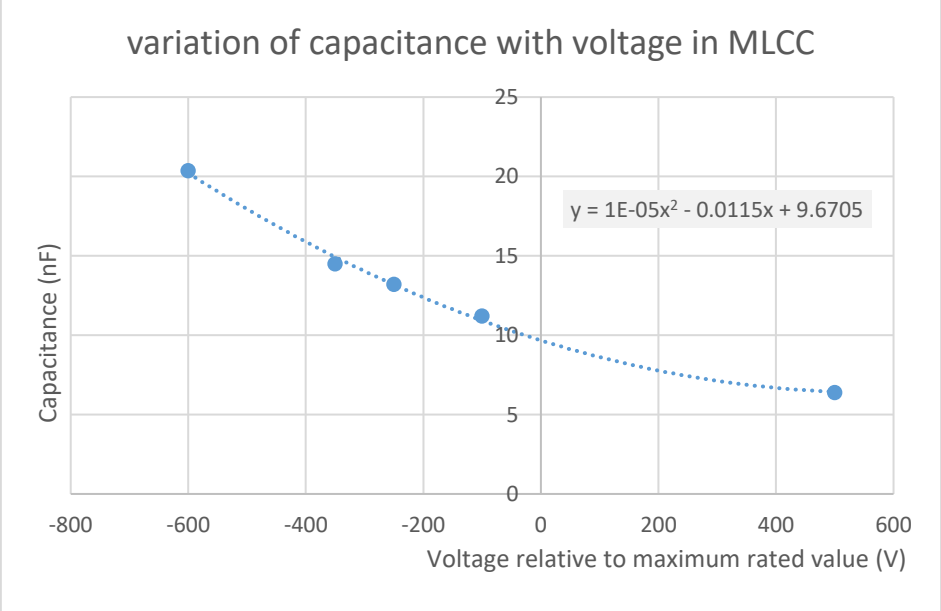

Figure 4.3: Capacitance variation of a 1206 22nF 600v capacitor adjusted for voltage rating of capacitor

4.3 *Implications for multiplier circuits*

The 50% variation in capacitance (up to its 600V rated maximum voltage) shown in the above plots must be taken into consideration when designing for dynamic operation of the voltage multiplier in a closed loop control system. In a system with ideal capacitors and fixed frequency, droop of the multiplier is proportional to current, so during the increased current of a radiation event the voltage drops and the driving source is increased to compensate. During this period if capacitance temporarily drops then there is potential for instability. Figure 4.4 shows a 10-stage ladder with the additional error induced by MLCC (over ideal capacitors) to quantify this variance.

The magnitude of the deviation only reached a maximum of 30V on a 1000V supply, or 3% assuming C9 and C10 22nf tapering down to 220nf for C1 and C2. This is for a 500uA load which is more that would be expected to be drawn by a scintillation PMT circuit. A potential compromise for the design phase will be making the capacitors sufficiently large for this error not to cause instabilities in a closed loop system whilst not making so large as to cause issues with system phase margin.

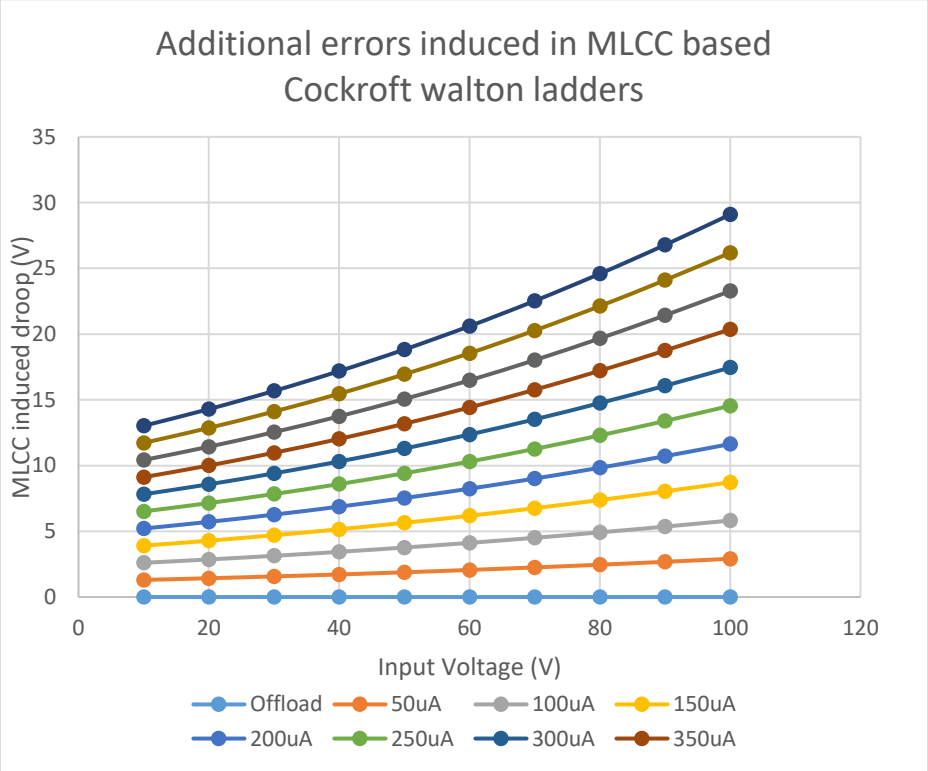

Figure 4.4: *Additional droop across a 10-stage ladder*

4.4 Implications for signal circuits

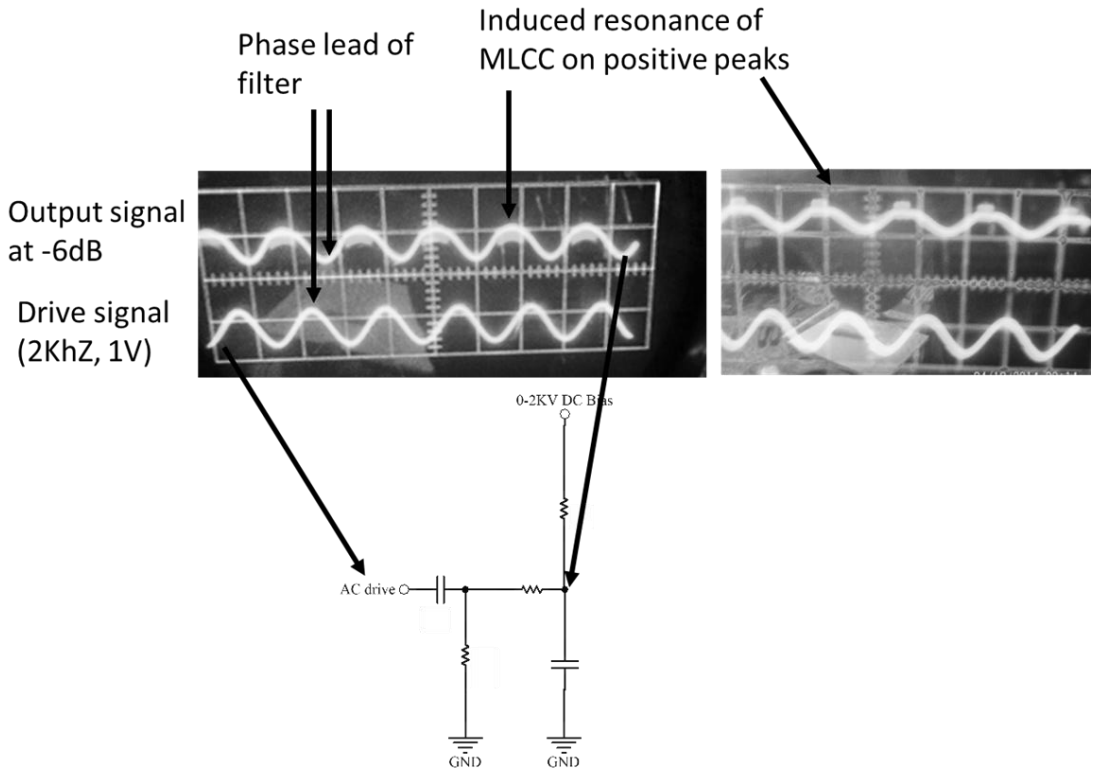

Figure 4.5: *Ringing within a DC biased capacitor (highlight filter and DC blocking capacitor)*

Although not the subject of the study, figure 4.5 demonstrates an artefact observed whilst conducting the investigation into DC capacitance variation. Unusually it shows a compression of the positive peak along with a ringing in this region when stimulated under sinusoidal and DC conditions simultaneously.

The conditions found to produce this were full voltage (600V across a 600V capacitor) with a 5Vp-p at 2KHz. The lower trace shows the signal directly from the signal generator. Barium Titanite as used in this XR7 capacitor is used for Piezo electric transducers, so this is hypothesized to be an electro mechanical artefact.

If further investigation is to be carried out this effect would need to be replicated on various packages and capacitor values using a spectrum analyser to characterise the relationship between these harmonics and the trigger conditions.

5 Air breakdown in High Density Printed Circuit Boards

5.1 Breakdown terms

Ordinarily the difference between high voltage and conventional circuit layout is that the track and component spacing are predominantly dictated by the avoidance of air breakdown rather than physical component size.

As the power supply module will include elements of low voltage feedback and signals from a detector, a system was synthesised to predict leakage from tangible data to allow the design to be as compact as possible without affecting performance.

The purpose for investigating current design rules is that if power supply sections cannot be reduced in size in proportion to that of the photomultiplier tube, then it will be impractical to use them in personal detector developments.

Glossary of terms

*__Dark discharge:__ *A leakage current that occurs between conductors with a voltage potential across them that fails to ionize the air between them.*

*__Glow discharge:__ *A current between conductors that causes a partial ionization along with a distinctive glow, although current flow is limited.*

*__Air breakdown:__ *When the voltage between a pair of conductors exceeds the insulation of the air (or other dielectric) between them current will flow with an equivalent negative resistance.*

*__Creep:__ *The surface distance of an electrical path between conductors. This would be given as equivalent distance of a straight line when quoting insulation gaps. Comparison between creep and electrode spacing are shown below in figure 5.1*

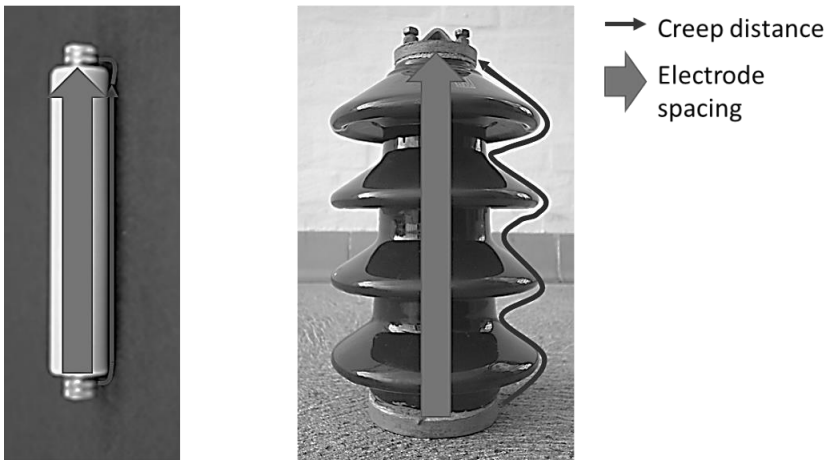

***Figure 5.1**: Illustration of creep distance*

Although much has been published about breakdown of air between pairs of circular or spherical electrodes, little has been published on the more specific area of discharge between PCB tracks. The effects of complex creep and rectangular profile conductors along with possible surface contaminants suspended in flux from the reflow process cannot be ignored when optimising compact PCBs. Surface mount solder paste must be far richer in flux than traditional solder, which itself is relatively nonconductive but can act as a suspension medium for conductive particles. Although this is largely removed in the washing process, FR4 fibreglass can be sufficiently porous that an element of this remains in the board even with a robust solder mask.

Rule of thumb figures [20] are given as 3000V/mm for full discharge and 1200V/mm for glow discharge; however these are only two points on a non-linear curve. The area of interest for the purposes of this project is dark discharge in relation to leakage from high voltage element to low voltage control systems, efficiency of power consumption, and protection of fragile components.

The scenarios in which these are of concern can be in 2 categories:

- Leakage between a supply rail and ground, causing system efficiency errors.
- Leakage over a single component not connected directly between the power rail and ground which disrupts the operation of the supply.

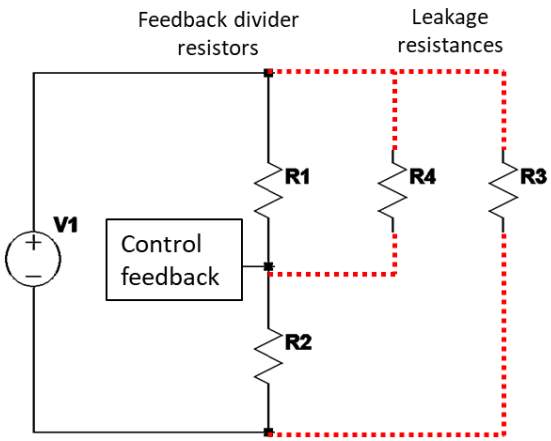

Figure 5.2: *Leakage resistances across a potential divider network. (R1>>R2)*

As illustrated in figure 5.2, R1 and R2 form a potential divider coupling high voltage and low voltage elements of the circuit. Discharge from the high voltage to ground is illustrated by R3 and leakage across a control element by R4. The effect of leakage illustrated by R3 is simply a reduction in power supply efficiency whereas R4 represents a signal error causing signal inaccuracies.

Any gas breakdown should follow a Townsend discharge curve (see figure 5.3) moving from dark discharge to glow discharge to air breakdown. The area for this study will be the dark discharge and low end of the glow discharge region as the intent is to be able to manage these artefacts, as opposed to accurately characterizing the full spectrum.

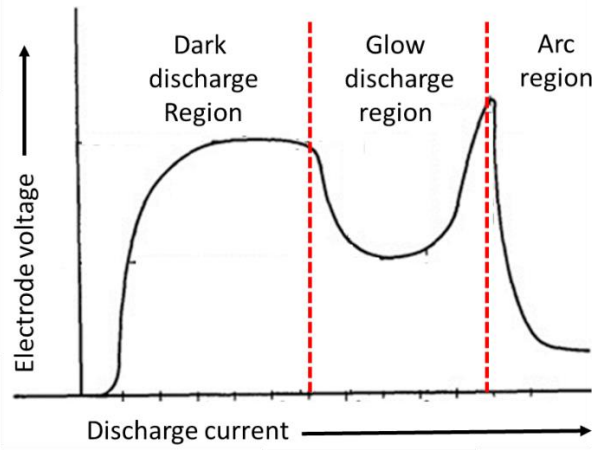

Figure 5.3: *Theoretical Townsend discharge curve* [21]

5.2 *Measurement of voltage breakdown*

Three circuits were tested for discharge effects: a pair of parallel cylindrical conductors of 1mm diameter in air, a pair of parallel PCB tracks of 35µm height and 0.254mm width on an FR4 sheet, and a second pair of PCB tracks coated in solder flux left to dry overnight then the excess wiped off with a lint free cloth. This aimed to separate the effects of air, clean FR4 surface discharge and discharge due to contamination of PCBs. These circuits were set up around a standard 1206 PCB component (based on anticipated critical component choices) footprint then tested for leakage with a variable 20KV supply. Results were taken using an *English Electric* isolation tester (measured 50MΩ source impedance), *MOD 30KV voltmeter* and a *Vacuum Generators* pico-ammeter. The equipment was selected on availability and did not have an up-to-date calibration. However, they were found to be consistent and gave reliable results when cross checked with other equipment.

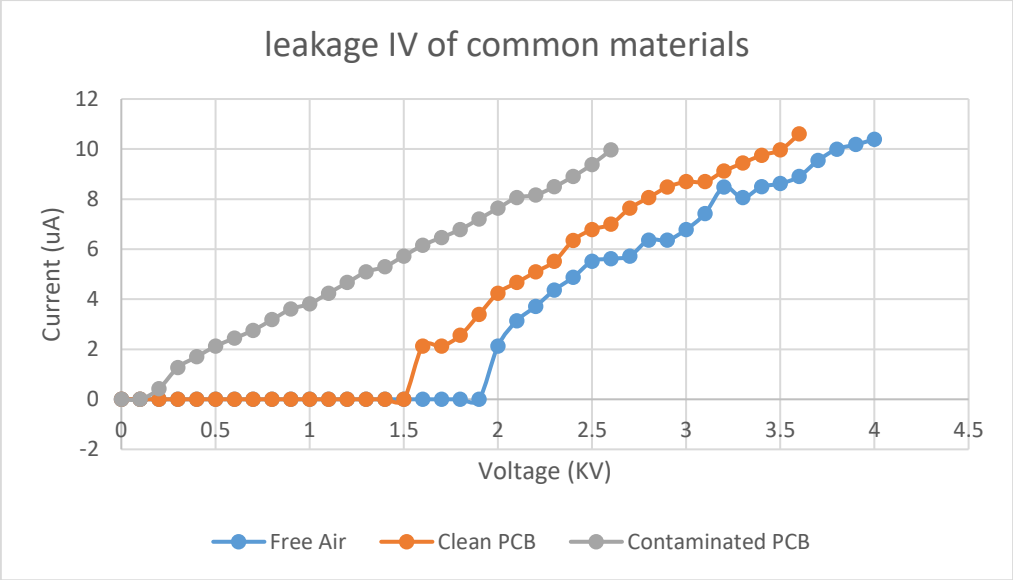

Figure 5.4: *Measured leakage resistance due to dark discharge in various materials.*

Figure 5.4 shows the results of this testing. There is a significant difference between the free air, clean and contaminated PCB behaviour. Before the experimental setup was stripped down the gapping was re-measured with feeler gauges and found to be correct.

5.3 Updated design rules

The contaminated PCB demonstrated by far the highest leakage of all the samples tested. This manifested itself as a roughly linear resistance beyond a 200V threshold.

Leakage beyond the 200V threshold is therefore:

$$R_{leakage} = \frac{V}{I_{leakage}}$$

$$= \frac{1000}{4 \times 10^{-3}}$$

$$= 250 \times 10^{6}$$

$$= 250M\Omega$$

To maintain accurate performance in a system under these conditions the threshold becomes:

$$\boldsymbol{\frac{200V}{1.5mm} = 133\left(\frac{V}{mm}\right)}$$

And above this threshold a leakage of:

$$impedance\ per\ mm = \frac{measure\ impedance - source\ impedance}{distance}$$

$$= \frac{250 \times 10^{3} - 50 \times 10^{3}}{1.5}$$

$$= 133\ \frac{M\Omega}{mm}$$

The parallel conductors exhibited a similar performance but with a threshold of 1.8KV and a similar resistance within its leakage region. The normalized threshold becomes:

1800V/1.5mm

=1200V/mm

This does match up with the rule of thumb threshold given for the beginning of glow discharge. As this is the glow discharge region it also indicates that glow discharge was below 200nA, so negligible for most practical purposes.

The IV curve of the clean PCB ostensibly looks like that of the cylindrical conductors, with a lower threshold of:

1.5KV/1.5mm=1KV/mm.

The differentiator is that the glow discharge region does not reach its threshold until 1.7KV. There is a slight hump around the threshold which corresponds to the dark discharge region in figure 5.3. The actual mechanism of this is largely immaterial beyond that of curiosity as the single rule of thumb previously has been confirmed with a further two for best- and worst-case real world scenarios.

It is not uncommon for the PCB designer to introduce cut-outs between high and low voltage elements of mixed circuit boards. As machining techniques become more advanced this is now no longer limited to blocks of circuitry and could potentially be used to introduce cut-outs beneath surface mount components. Not only does this potentially reduce residual flux trapped under components not entirely removed by the wash process, but also the previously demonstrated FR4 surface leakage.

The major application for this is surface mount high voltage supply capacitors which give several mm between supply and ground (e.g. 3mm in 1812 package). High value resistors in the order of hundreds of mega ohms or giga ohms (used to isolate high voltage supplies from low voltage control circuits) could also become sources of error under such conditions. For constructing prototypes, the developed discharge coefficients need to be applied to all components used in high voltage circuits as it cannot be assumed dark discharge will be negligible at a component's rated value.

Table 2: *Summary of breakdown behaviour under tested condition. This updated rules of thumb for high voltage PCB design:*

Material	Threshold (V/mm)	Leakage (MΩ/mm)
Bare conductors	1200	130
Contaminated PCB	130	130
Clean PCB	1000	130

It was observed during these measurements that air breakdown creates varying artefacts in the time domain which could be severely problematic in high performance systems. Characterizing this was beyond the scope and limitations of the equipment for these measurements but could provide further reductions in clearance if accurately documented.

Finally, the effect of adding glass or ceramic inserts through PCB slots over air gapping the PCB alone would be of potential interest. Hamamatsu have included a similar process in recent products in the form of ceramic coatings; however limited information is available at this time

6 Preliminary Simulations

6.1 Divider simulations

As covered in section 2.2, the purpose of this block of electronics is to develop the individual dynode accelerating voltages from a single main supply. The problematic issue is that the dynodes have increasing current requirements further along the circuit (figure 2.4-2.5). The traditional method for achieving this is to use a long potential divider chain (figure 2.6) with sufficient current flowing through it that any dynamic elements are insignificant. The disadvantage of this approach is that the dynodes still see significant supply impedance whilst the static current will typically be an order of magnitude above the peak dynode current, resulting in poor economy. The problem can be simplified into one of reducing the required offset current of a passive divider whilst maintaining its performance.

An active divider (figure 6.1), Cockcroft Walton based supply (figure 6.2) and resistive divider (figure 6.3) were all simulated, with 3 variants of each circuit with results shown in table 3. Measurements of droop were taken at all 5 nodes along with the total supply current at quiescent. Figure 6.4 highlights underdamped effects associated with the active divider circuit.

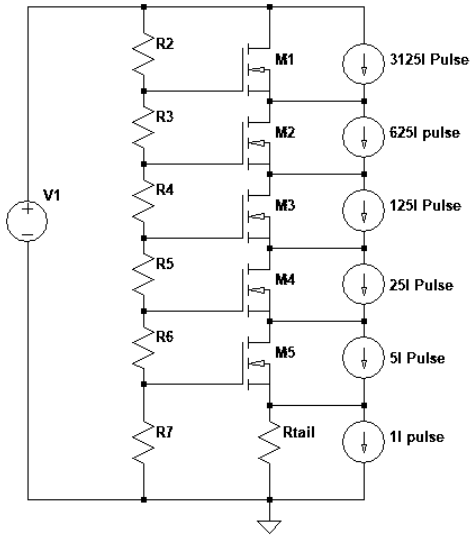

Figure 6.1: Active divider simulation

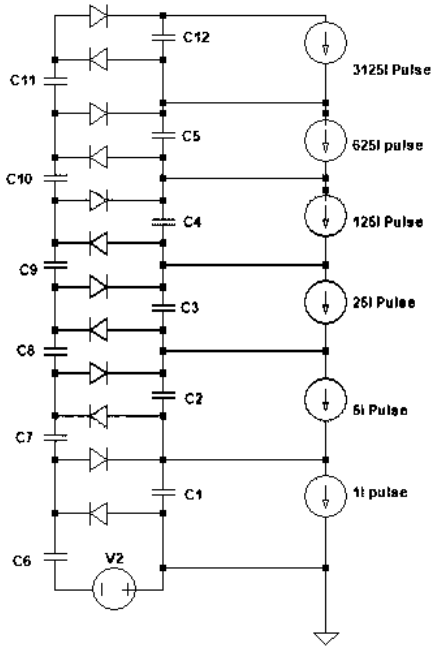

Figure 6.2: *Voltage Multiplier based divider simulation*

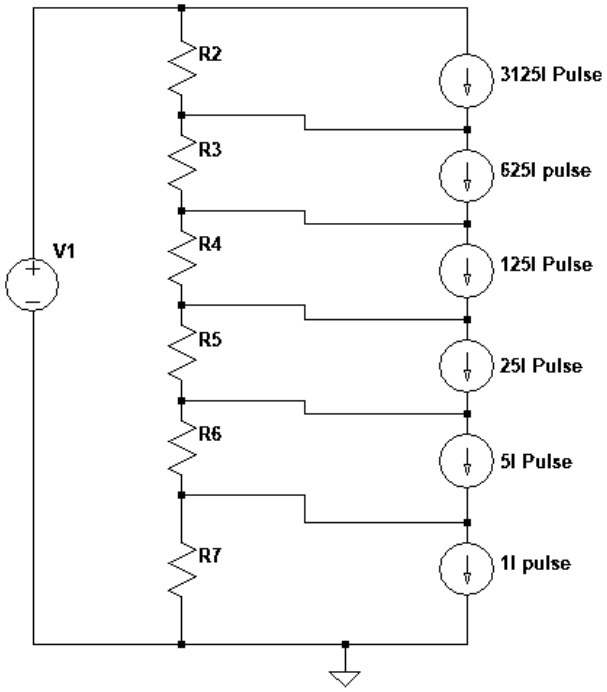

Figure 6.3: *Resistive divider simulation*

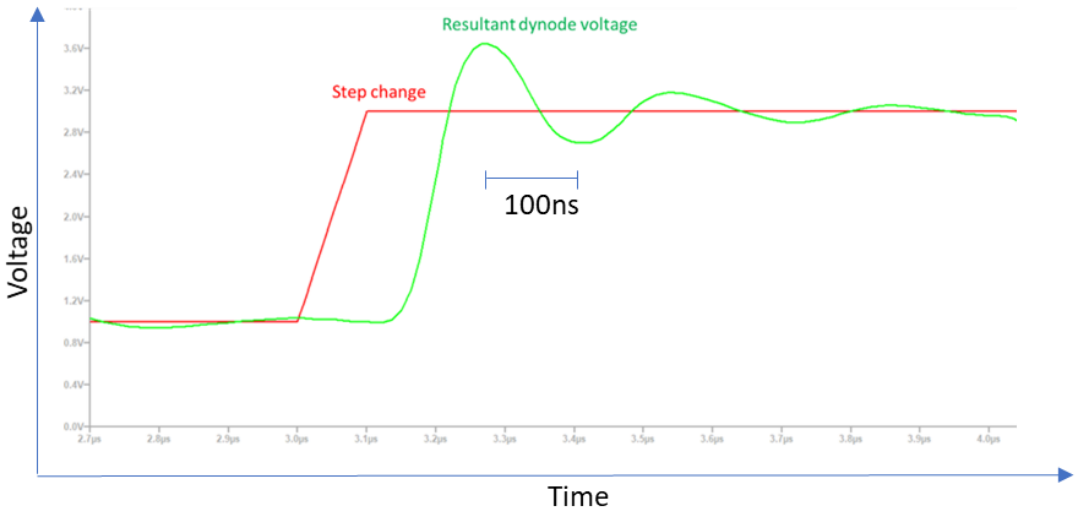

Figure 6.4: *Simulated overshoot related underdamping effects under a capacitive load (100nF)*

Table 3: Comparison table of divider methods (600V supply)

Circuit	Supply current	Droop1	Droop2	Droop3	Droop4	Droop5
Resistive1 (R=200K)	500uA	5V	5V	3.8V	2.6V	1.3V
Resistive2 (R=40K)	2.5mA	1V	1V	0.8V	0.5V	0.25V
Resistive3 (R=8K)	12.5mA	200mV	200mV	150mV	100mV	50mV
CW1 (C1=10p)	20uA approx.	14V	10V	6V	3V	1.2V
CW2 (C1=100p)	20uA approx.	600mV	800mV	600mV	300mV	130mV
CW3(C1=1n)	20uA approx.	140mV	90mV	55mV	32mV	12mV
Active 1 (Rtail=10M)	15uA	1V	300mV	50mV	13mV	1.8V
Active 2 (Rtail=5 M)	25uA	1V	200mV	50mV	10mV	1mV
Active 3 (Rtail=2 M)	102uA	500mV	180mV	20mV	3mV	0.9mV

6.2 Hardware confirmation

In order to quantify the variables discussed above and verify the simulations conceptually, a basic circuit was constructed to test the most severe effects introduced under high rate conditions.

In order to create conditions for this, a 500mm*100mm*50mm caesium iodide (doped with Thallium) scintillator coupled to an *Electron Tubes* PMT [22] was used. This was used in conjunction with a Multi-Channel Analyser (MCA) capable of 100,000 counts per second (CPS). The circuit was powered with a lab-type high voltage power supply coupled to a fully active dynode chain and AC coupled to the MCA. The chain was set up using Infineon BSS127 N-channel Mosfets biased to 26uA quiescent current (drain), 8uA reference current (bias divider) with 330nF bypass capacitors across each cascode stage. The intent was to replicate both the droop and ringing (figure 6.4 and table 2) and quantify the effect on a full detector system.

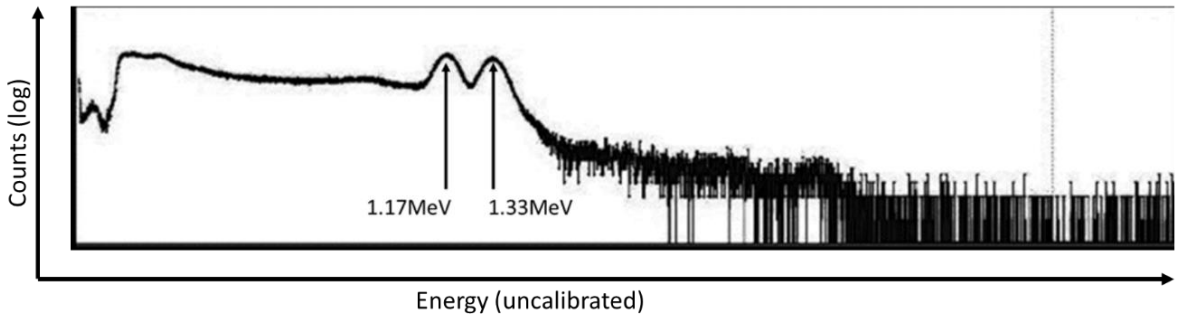

Figure 6.5: Cobalt-60 spectrum taken on proof of concept jig

Figure 6.5 shows a Cobalt-60 spectrum at 13,000 CPS. It retains its distinctive twin peak emission with a little less separation than would be optimal.

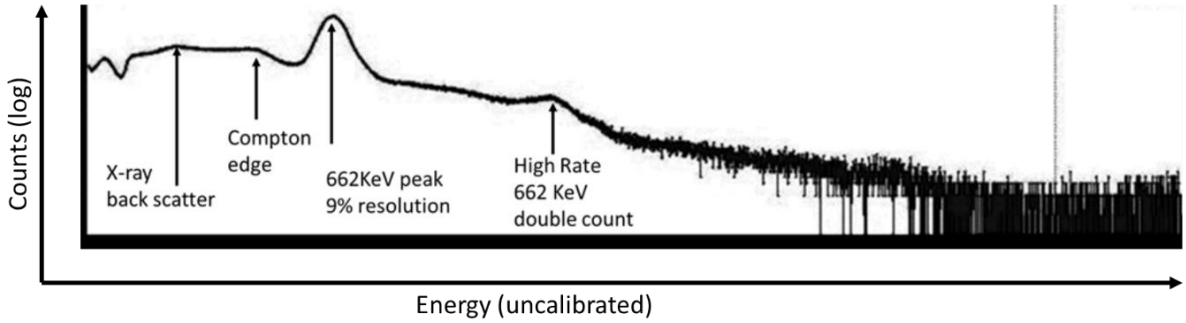

Figure 6.6: Caesium-137 spectrum taken on proof of concept jig

Figure 6.6 shows a Caesium 137 spectrum maintaining both its peak and Compton edge at 45,000CPS. Resolution is around 9%. This scintillator/MCA combination should be capable of below 8% but this is still acceptable at this very high rate with no baseline restoration.

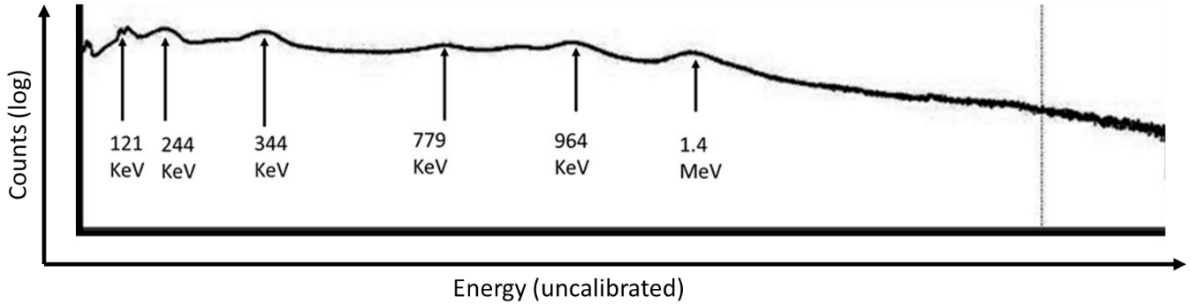

Figure 6.7: EU152 spectrum taken on proof of concept jig

Figure 6.7 shows a europium-152 spectrum at 80,000CPS. At this very high rate the spectrum has lost most of its energy information; however peaks are still in existence and very close to the correct position.

Although this was a very brief test, it was intended to ascertain whether peak broadening or peak movement would be more of an issue for the dynode circuitry. It demonstrated that peaks maintained correct positioning at far higher count rates than a hand-held detector would be likely to experience or would be expected to accurately record, and peak broadening would be the issue to hinder the design process.

6.3 Critical component evaluation: MOSFETS

To further understand the underdamped nature of the active divider (figure 6.4) and understand the resolution/peak broadening problem with the circuit, the MOSFETs were measure within the cut off region:

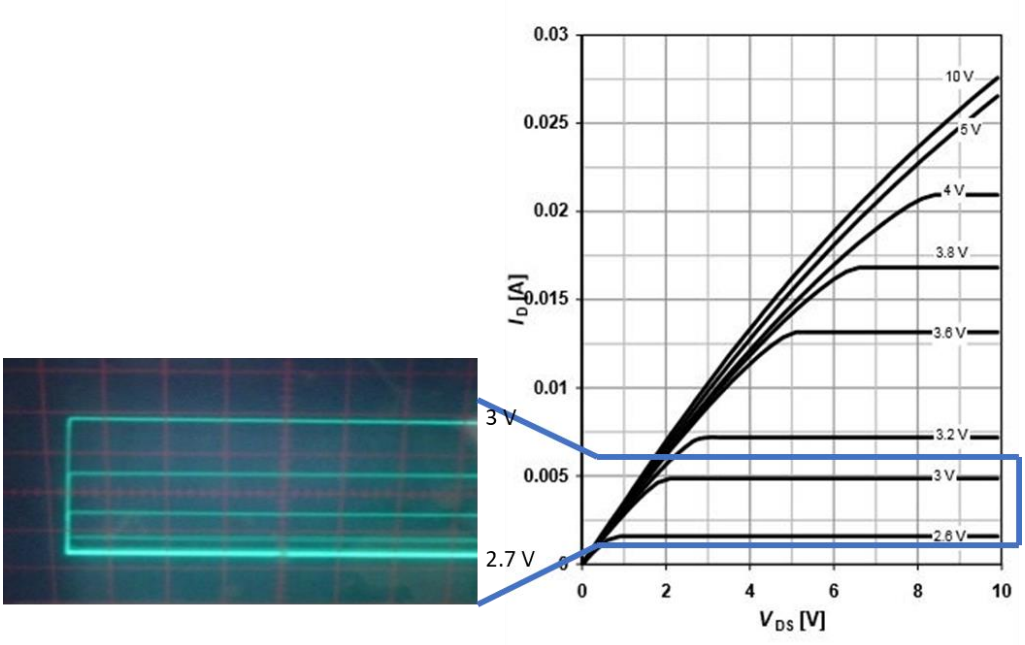

Figure 6.8: *Infineon BSS127(VT=2V published) MOSFET transition region transfer curve* [23]

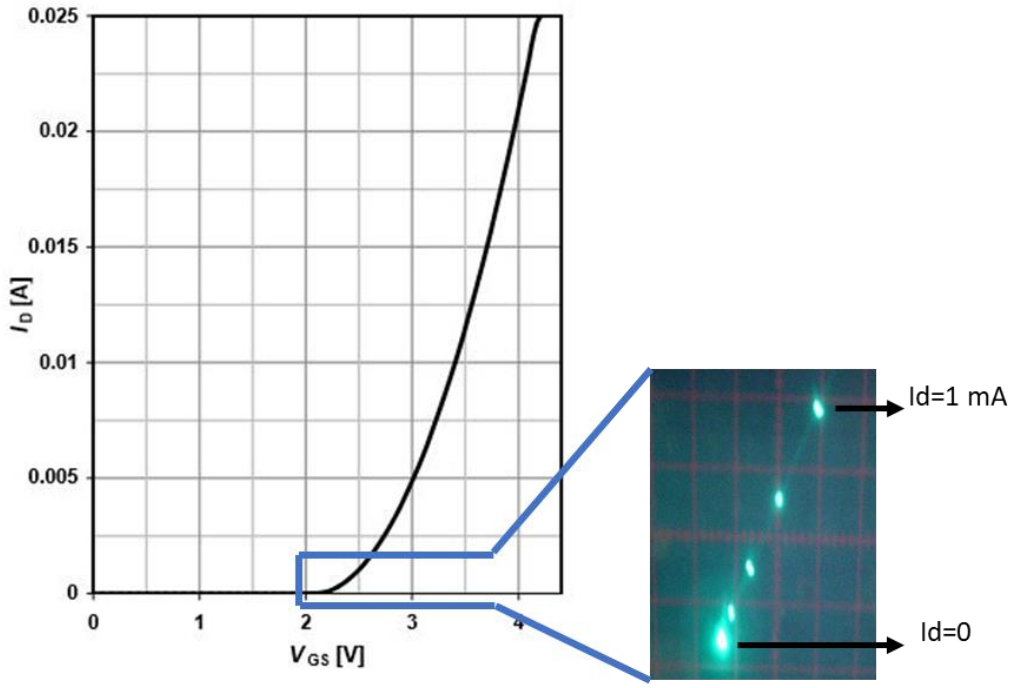

Figure 6.9: *BSS127 linearity* [23]

In reference to figures 6.8- 6.9 we see the cut-off transition region of the BSS127 Mosfet used for initial testing. This is not shown in any detail in the datasheet but is critical for the dynode systems speed as the feedback system will compensate more quickly in the MOSFETS linear region.

7 Design

7.1 High voltage DC-DC converter concept build

In designing the electronics for a project of this nature at a modular level the order of design can be as important as the design itself. The decision was made to build a supply capable of powering an existing dynode/PMT circuit (used for simulation proving in section 6.2), then design a suitable alternative dynode circuit. Once this was completed the power module was to be refined based on updated dynode circuit requirements. This also served as the base for the voltage multiplier-based divider circuits.

From the review in section 3 a flyback supply driving a Cockcroft Walton ladder was specified for the basis of the power supply board. Although this is a simple, relatively compact concept the trade-off is the choice of switching frequency as it will be common to both elements. Figure 7.1 illustrates the principle via a block diagram.

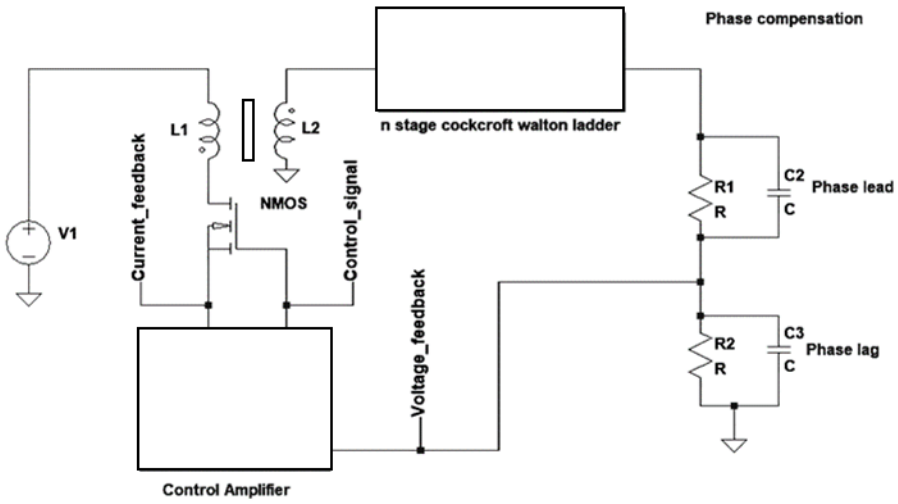

Figure 7.1: Basic block diagram of circuit

High ratio transformers tend to have higher intrinsic capacitance, so have reduced high frequency response. Analysis of available parts found many flyback transformers designed for space conscious circuits have severe attenuation when switching at an ideal frequency for the primary inductance. This caused a large offset current due to forced discontinuous mode operation.

When the subsequent Cockcroft Walton ladder is considered there are also trade-offs with selection of switching frequency. The capacitor droop is reduced at higher frequency; however recovery time losses in the diodes become more significant at higher frequencies.

This does raise the difficult decision amongst all the potential compromises of where to start the design process. This was done based on component availability; in this instance the most limited was the flyback transformer. The losses for the transformer and switching

diodes were measured and overlaid with an ideal (lossless) voltage multiplier. These are shown in figure 7.2.

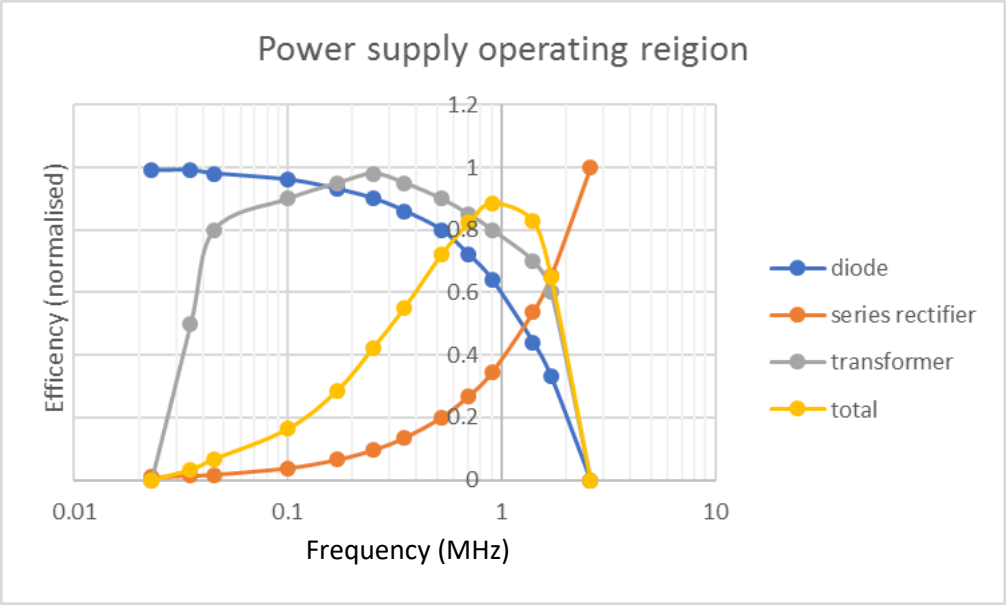

Figure 7.2: Overlaid efficiencies of all 3 power supply components.

When using a commercially available monolithic switching amplifier for reduced footprint, cost, or supply offset current, a drawback is that there is often little provision for adjustment of phase margin or time constants of the system, so external components need to be designed accordingly. The system shown in figure 7.3 was used when evaluating prospective components for suitability. It functions by modulating the feedback at a threshold just surpassing the hysteresis of the internal comparator and measuring the superimposed modulation of the output rail. This was found to be most successful with a modulation frequency a decade below the amplifier's switching frequency. The phase lag can then be calculated by viewing both waveforms on an oscilloscope. This also serves to measure the hysteresis level of the amplifier, as this will dictate the accuracy of the final system. This single point measurement does assume a simple phase margin, dictated predominantly by a single circuit element and should be developed further to be of swept frequency if results are found to be inadequate.

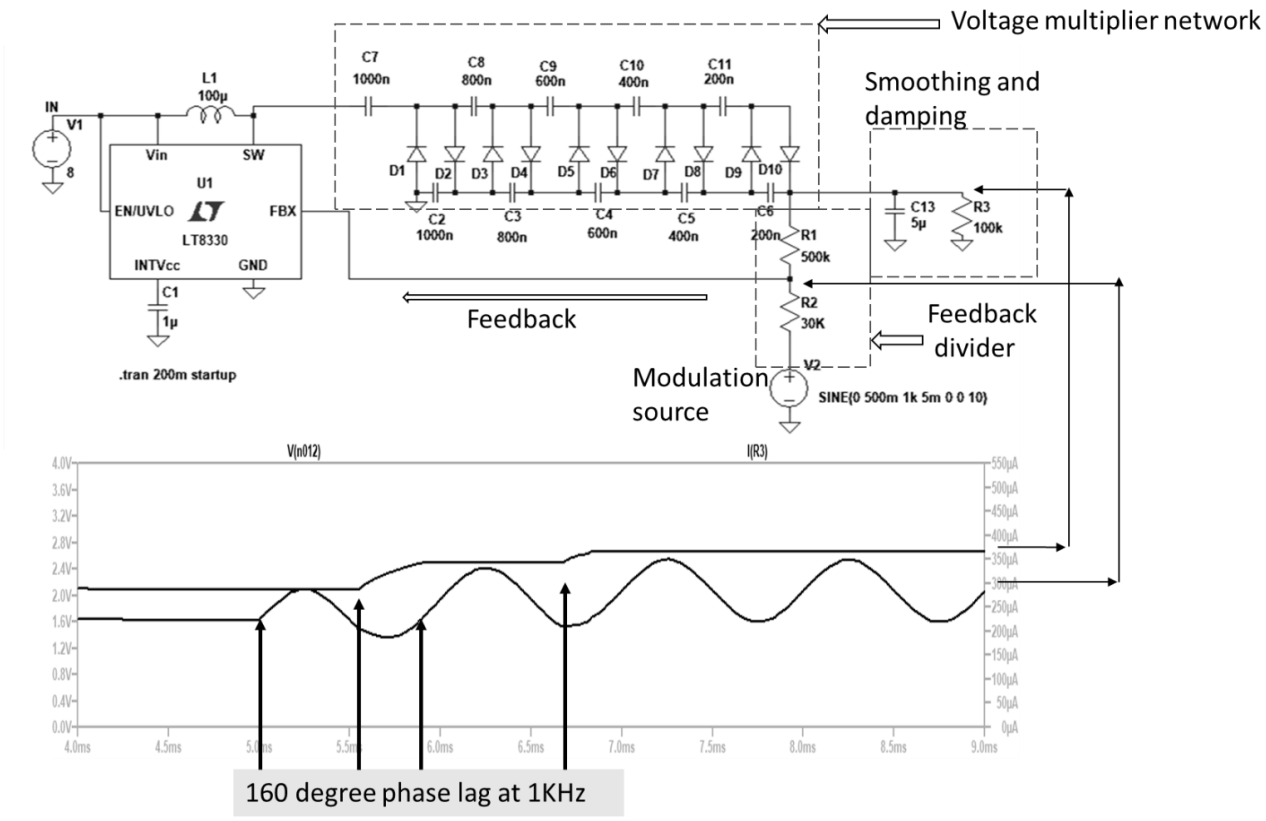

Figure 7.3: Simulated phase lag technique diagram

As previously stated, the starting point for the design was the switching transformer since the least flexibility was available from off the shelf parts. After measurement of available items, the *Wurth 750311691* transformer was selected based on physical volume, power rating and primary inductance. The primary inductance of 80uH, with a 1:5 ratio (2mH secondary) with low leakage (1µH peak quoted, 0.1µH measured) demonstrated advantage over other devices of this form factor. It was quoted as maintaining its inductance to 90% on a 1mA secondary draw which was confirmed on test and provided a comfortable amount of headroom for the supply. The secondary was rated to 150V but on testing the point of breakdown was found to be the gap between the pins of the device at 4KV.

Although many suitable switching amplifiers were evaluated the MAX669 [24]was selected based on measurement of hardware. Both this and the LT3757 [25] had the

required variable switching frequency and external switch capability whereas the Maxim required around half the current of the LT part for the control circuit (250µA).

It was found that the other differentiator between switching amplifiers was the threshold at which they switched modes; be they burst, pulse skipping or steady PWM. The Maxim was found to have a lower threshold of moving from various power saving modes so was potentially more stable, although it did lack the post input comparator compensation of the *Linear Technologies* equivalent.

When selecting the diodes for the Cockcroft Walton ladder, the requirements were a small form factor due to the number required, and to be robust enough to handle transients and errors during testing. The BAS21-03W [27] switching diode was rated for 250V peak, exceeding the voltage rating of the switching transformer of 250V. Its recovery time of 50ns was adequate for the 250KHz/4µs switching. Its reverse leakage current was 0.1µA (measured) under steady state; however the peak reverse leakage when transitioning between forward and reverse bias was not published.

Nine multiplier stages were set as based on preliminary testing based on minimum acceptable recovery time. This number can be mathematically optimised for a simple sinusoidal source [15] but combining these calculations with the efficiency variation of the switching amplifier proved counterproductive. The limit of the supply was found to be 1425V under normal load which maintained diode headroom but exceeded the transformer rating.

As the range of switching amplifiers was reduced to those requiring an external switch, a suitable Mosfet had to be selected. An Infineon IRLML0060 NMOS was selected as it offered a good deal of headroom for switching transients (60Vds and 100mA). It was also capable of switching from the relatively low voltage from a switching amplifier on a 5V supply with a V_t of 1 to 2.5V (based on measurement of 25 parts) . Gate-source capacitance (290pf at 25V) was not found to cause any significant issues with the selected switching frequency of 250KHz.

To maximise efficiency, far less current was assigned to the feedback potential divider than any of Maxims example circuits so, to prevent any impedance mismatch losses, a

buffer amplifier was included between the feedback derivation and the switching amplifier. Upon testing it was found this was superfluous from an ideal electronics perspective but added a great deal of flexibility to the PCB layout as the unbuffered signal was particularly prone to pick up from the switching circuits. A MAX4130 was chosen for this due to its low power consumption (800 µA) and 10MHz unity gain bandwidth, high enough not to add a significant pole with the operating region of the phase margin.

As the MAX669 had continually variable switching frequency, several factors had to be considered, as demonstrated in figure 7.2. 250KHz was chosen to maximize the ladder's efficiency and reduce the time constant, along with cost and size of any output filtering. This was above the rated 220kHz of the flyback transformer. However this was offset by its poor transient response making a snubber circuit unnecessary. This did add a further pole in the phase margin but this was not found to be an issue.

As discussed in the literature review, to maintain a linear transfer function the capacitors in the CW ladder need to be on a linear taper; however capacitors are not available off the shelf in these denominations. An approximation was made, as shown in table 3, to achieve similar results. In this example, the voltage drop across each individual stage is irrelevant if the phase lag can be compensated for with a single RC stage.

***Table 4**: Capacitor multiplier simplified taper*

Required multiplier	Approximated multiplier
1	1
2	1
3	2.7
4	2.7
5	2.7
6	4.7
7	4.7
8	4.7
9	10

Paralleling identical values of capacitors is the only method of avoiding this tapering error but was too bulky to use with this initial build.

Using this ratio, a C value of 10nf was chosen to correspond to a droop of 40mV/mA per stage. This made the losses insignificant when compensated for at some expense of recovery time. At this operating point MLCC droop is not significant enough to warrant any compensation. However it should not be ignored in further modification in which capacitor sizes are reduced.

Through simulation the compensation required to maintain the phase margin was a single capacitor phase lead filter at the divider stage. This is confirmed by the technique set out in section 3.4. Assuming the device internally compensates for flyback phase contributions the phase margin will be:

$$Phase\ margin = n(multipler\ margin) + compensation$$

$$= 9(90) + 90$$

$$= 720° = 0°\ equivalent\ (+2\ cycle\ recovery\ delay)$$

Experiments with more multiplier stages proved unstable as the phase margin of the control circuit caused underdamped effects on full load transients. Reducing the number of stages to as low as 5 still produced the required output voltage but problems were encountered with transformer saturation and reduced overall efficiency as the limitations of the MAX668 switching amplifiers current mode operation proved problematic. It would have been possible to address this by using a transformer with a higher primary inductance, but this would have resulted in a larger physical size, a lower switching frequency due to increased parasitic capacitance in the transformer, and larger capacitors required in the multipliers due to the lower switching frequency.

The full circuit is shown below in figure 7.4 along with the bill of materials in Table 4.

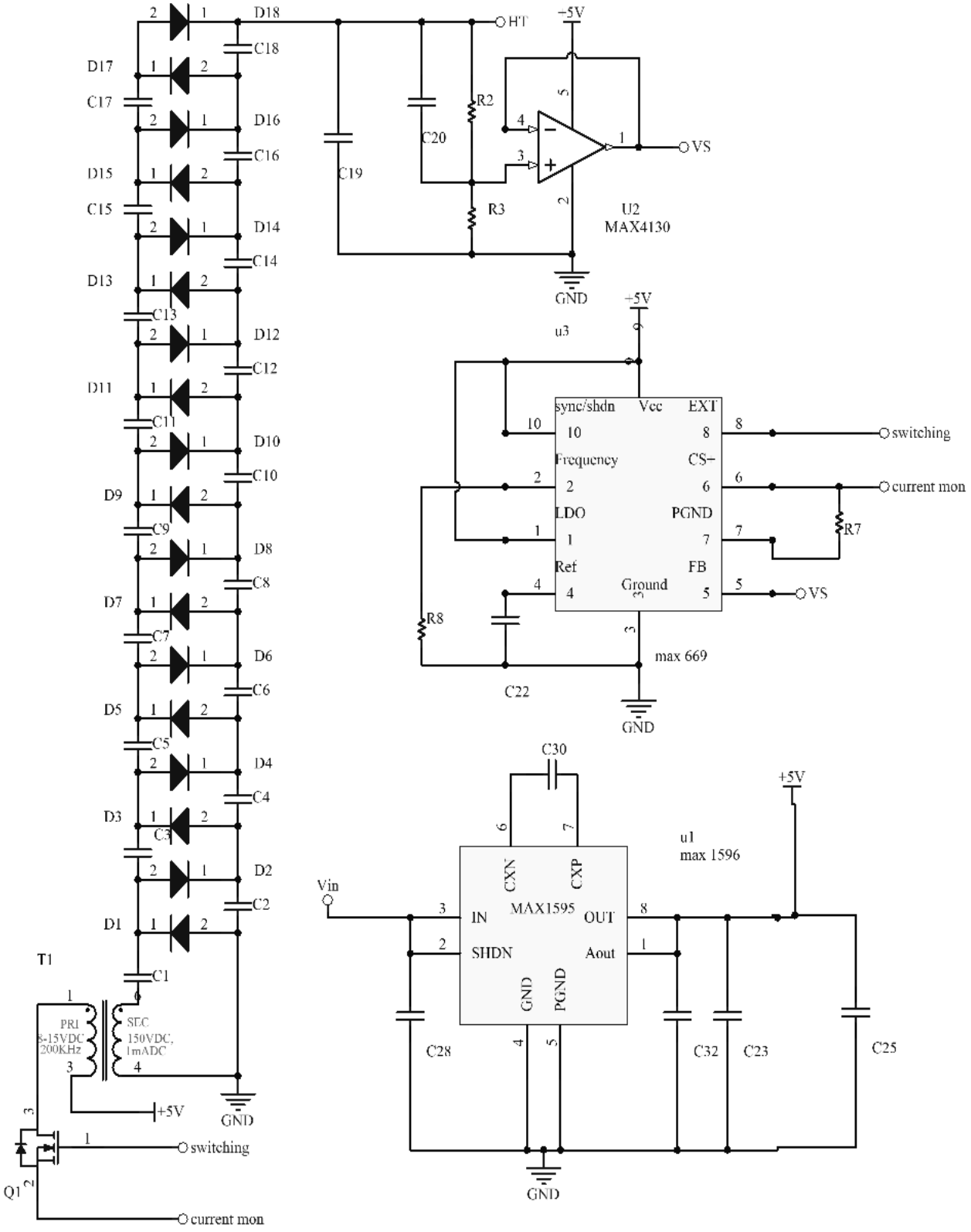

Figure 7.4 *High voltage module circuit diagram*

(Bill of materials shown in Appendix table 6)

Table 5: *Bill of materials.*

Part	brand	Details	Quantity	unit price	total price
Transformer	Wurth	750311691	1	5.21	5.21
Mosfet	Infineon	IRLML0060	1	0.23	0.23
diode	infineon	BAS21-03W	18	0.031	0.558
Linear Regulator	Microchip	MCP1700T-330	1	0.3	0.3
Switching regulator	MAXIM	MAX669	1	4.11	4.11
Charge pump	MAXIM	MAX1595	1	3.44	3.44
Charge pump	MAXIM	MAX1719	1	2.64	2.64
Opamp	MAXIM	MAX4130	1	2.3	2.3
10n capacitor	Murata	XR7 2Kv	1	1.26	1.26
1G resistor	Vishay	CRHV	1	1.64	1.64
150p capacitor	TDK	COG 3Kv	1	0.616	0.616
100n capacitor	KEMET	XR7 600V	2	0.224	0.228
47n capacitor	KEMET	XR7 600V	6	0.463	2.778
22n capacitor	KEMET	XR7 600V	6	0.234	1.404
10n capacitor	KEMET	XR7 600V	4	0.086	0.344
					27.058

As can be seen in table 3 the total price for the design is £27.05. assuming £1 each for the PCB and similar for all the passives (resistors, non-critical capacitors) which gives a materials estimate of £29. Although high for consumer equipment, for lab equipment this is very competitive and under volume manufacturing (above price is for individual parts) could easily fall below £20. Where possible, brands have been unified across components to access lower bulk prices direct from manufacturer.

7.2 Active divider prototype

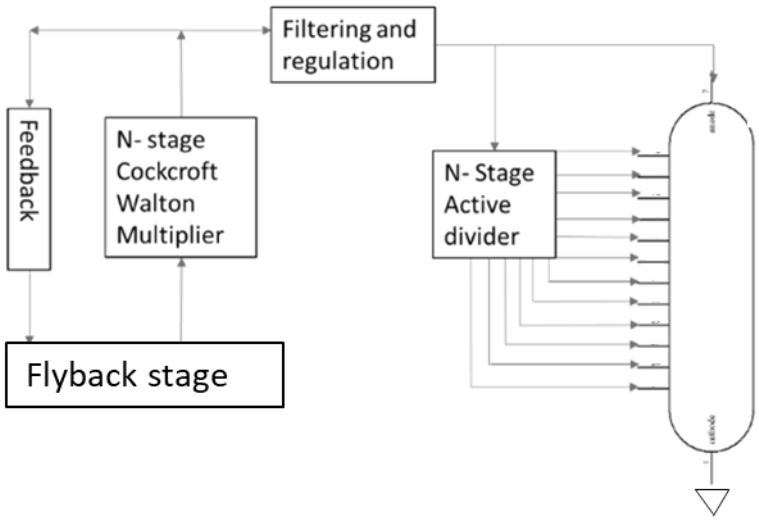

Figure 7.5: *Active divider system level concept.*

As previously discussed and illustrated in figure 2.9, the active divider principle has been used since silicon technology was available for redressing the balance between power

consumption and performance within the photomultiplier circuit. The block diagram in figure 7.5 illustrates the overall concept of the system.

Based on the BSS127 NMOS curves taken (section 6.3) the supply ladder was biased to 50uA quiescent current as determined in Section 6.1. Initial tests revealed the circuit was particularly fragile when encountering overshoot from the parallel reservoir capacitors (C6,7 figure 7.6). The solution was to fit protection diodes to stop the gate going negative with respect to the source. Although a simple problem, reverse leakage had the potential to disable the independence of the reference chain from the supply chain. The solution was found to be using Infineon's BAS-416 with single figure pA leakage. Although reverse leakage is published as 3pA measured units were found to be higher, but still below 10pA.

For this early prototype a resistive load was used as a low risk option over more complex coupling techniques. This was coupled to a single inverting stage based around an ADA4805 or MAX4452 operational amplifier. Both consumed only 600µA and had a 200MHz small signal gain bandwidth product. The risk was that both had a much slower large signal response and so could cause non-linearities.

From the early testing in section 9.2 it became apparent that the active stages had the potential to become unstable if parallel reservoir capacitors were excessively large (150nF+), so a large footprint was left for these with values set on test once the DC operating point had been established. The full circuit is shown in figure 7.6 and was used with the power supply circuit shown in figure 7.4.

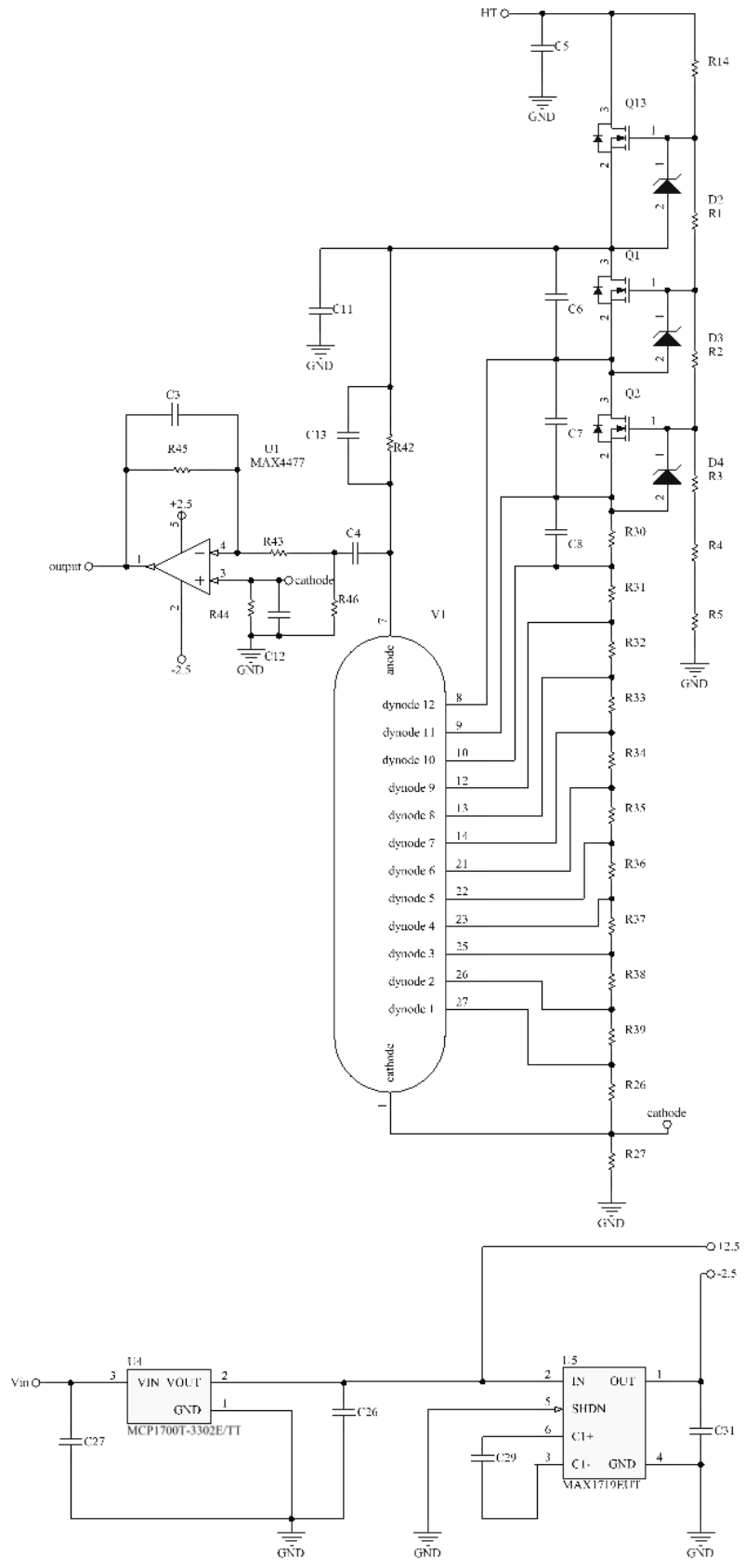

Figure 7.6: *Active divider-based circuit diagram (BOM shown in Appendix table 7)*

7.3 Voltage multiplier prototype

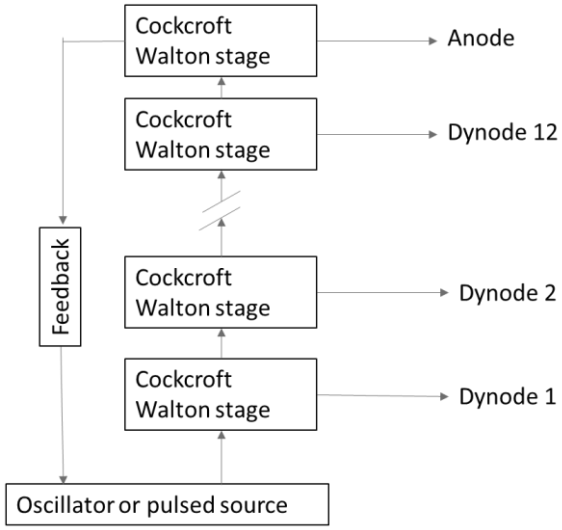

Fig.7.7: *Dynode circuits directly driven by CW ladder concept*

The second prototype build was a CW direct to dynode circuit as conceptually illustrated in figure 7.7. As the additional divider stage acting as a regulator (Q1, figure 7.6) was unavailable in this configuration the prototype was based around a negative high voltage supply. This allowed DC of the PMT's anode to a charge amplifier powered from the battery with no offset. In addition to complexity the large disadvantage of this negative HT from a purely practical perspective is that like most metal clad PMTs the outer case is connected to the cathode for screening purposes and would require insulation for use, which potentially adds a great deal of size to a SiP module requiring UL or CE certification. Coupling an inverting boost converter to a voltage multiplier was unconventional, with the implemented system (L2 and L3 figure 7.8), requiring further optimization.

Because of the 15 stages required for a 12 Dynode PMT, a benefit was that a boost converter could be used in place of the flyback converter. An LT8330 was used which contained an integral 60V switching transistor, extremely low control amplifier current consumption (sub 100uA) and a 2MHz switching frequency for high voltage multiplier efficiency. As no flyback transformer was used, this allowed a decade higher switching frequency to be used to minimize CW losses by the same order. This also allowed a much smaller 0805 inductor to be used, saving PCB space. The device also included both positive and negative references to the feedback comparator, so no inversion was required for

negative feedback signals. In the meta-supply (figure 7.4) the flyback converter kept the supply within its linear region when boosting from a 5V supply. To keep the switching converter within this same region, two LT8330 converters were cascaded rather than using the charge pump from the meta supply. This maintained the same PWM operating point of the converter by using a 1:5 input converter ratio rather than the 1:5 transformer ratio of the meta supply.

Because of this increase in switching frequency (from 200KHz to 2MHz), 0402 capacitors could be considered over the bulkier 0805-1812 capacitors used in the flyback supplies. Examples with a published 10nF 100V rating had a measured actual capacitance of 2nF at 55V DC bias which was still an equivalent doubling of base capacitor value over previous prototypes with the increase in frequency.

With this reduction in part count and capacitor package the entire assembly could be condensed onto a single PCB. For this prototype the 3-12V converter, rail splitter and amplifier were excluded to be placed on an external PCB although there was ample room for them on a single PCB.

Flexibility was built in to take the feedback to the supply from any of the nodes along the CW ladder. This was expected to be a compromise between noise (as the phase margin moves further out as the node number increase) and linearity as voltage errors increase further up the ladder due to tapering oversimplification.

In addition to the noise rejection from the negative HT supply variant, a lower specification for the first stage amplifier is required. For this purpose, a LTC6261 200µA, 30MHz Opamp was included, configured as a charge amplifier, DC coupled at both its input and output. This was set to a 0.65µs time constant, critically damped to give a Gaussian approximation of the energy of each event, potentially excluding some circuitry from any subsequent MCA.

An alternate option for this would be a current mirror with a high-density ratio (eg. 1:20) to discard all the operation amplifiers in the circuit (reference fig.1.2.7). This would be particularly applicable to a full ASIC solution.

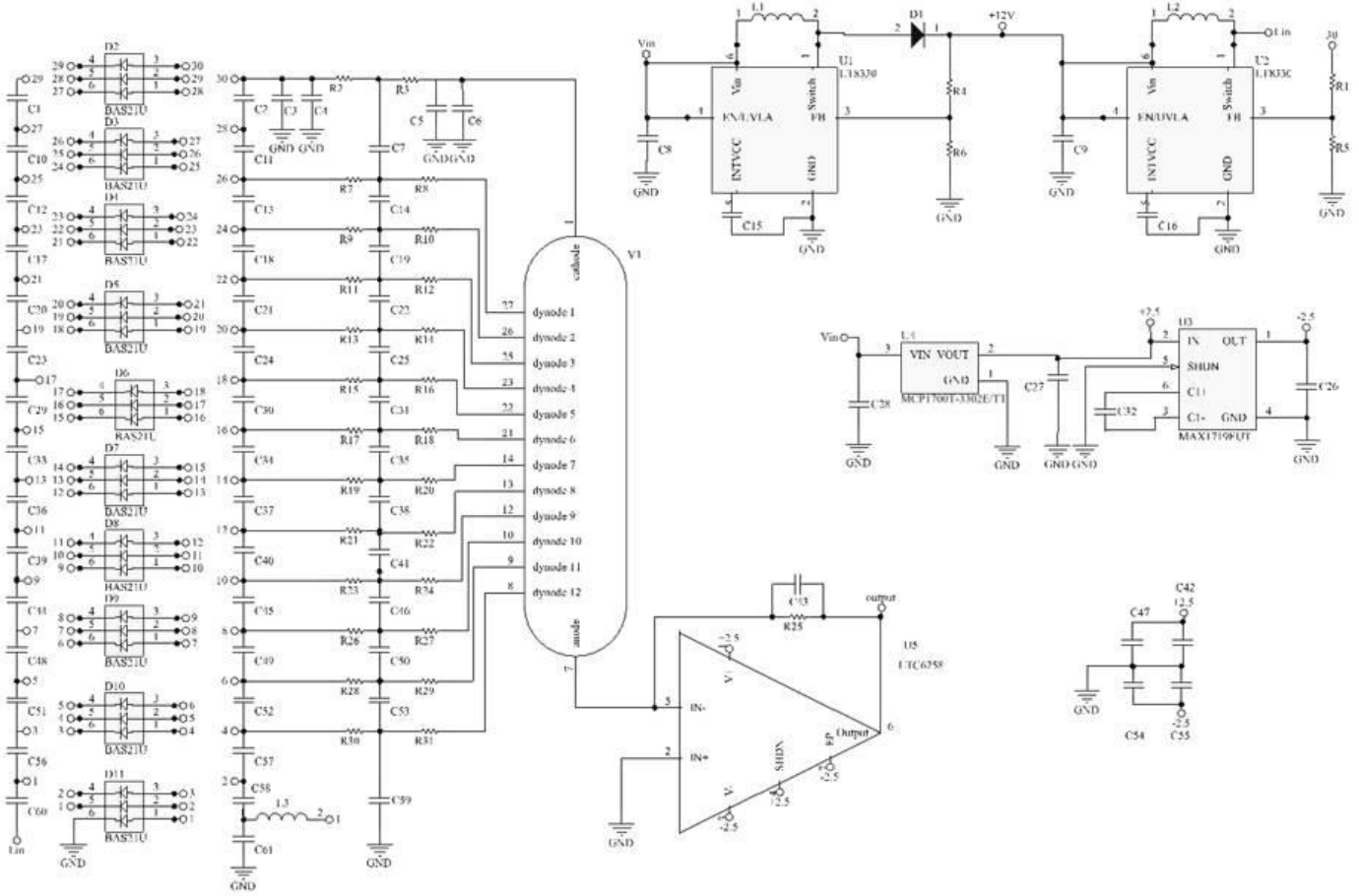

Fig.7.8: *Direct coupled negative HT prototype (BOM shown in Appendix table 8)*

7.4 Clamped active divider

As illustrated in figure 7.9 and 7.10 the concept of this synthesis was to address the cascode and flyback errors detailed in the active divider simulation results (Chapter 6). This used push-pull blocks in place of the constant voltage single ended blocks of the previous design.

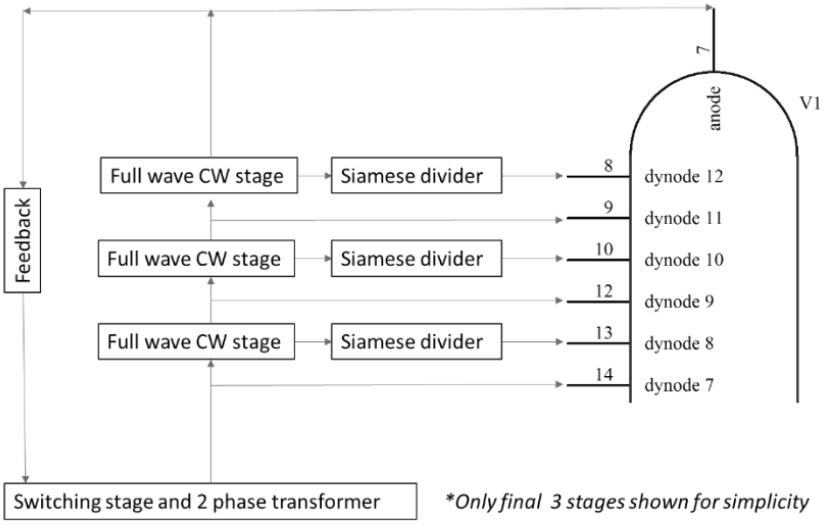

Fig.7.9: *Active division of Cockcroft Walton stages*

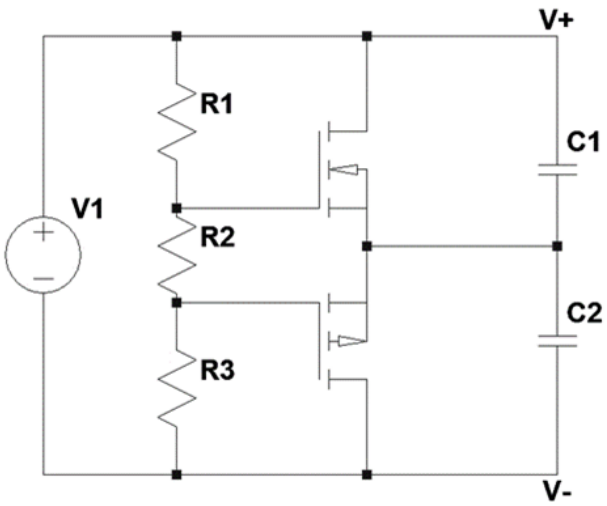

Fig.7.10: *Siamese divider block.*

These are clamped by the stages of the Cockcroft Walton ladder in the supply. This attempted to minimise the linearity errors of the Cockcroft Walton based supply by reducing the number of stages to 8, thus reducing the n^2 error term by a factor of 2.6 over the 14 stage ladder used in the direct prototype. This would further reduce errors in a more conventional 10-dynode PMT.

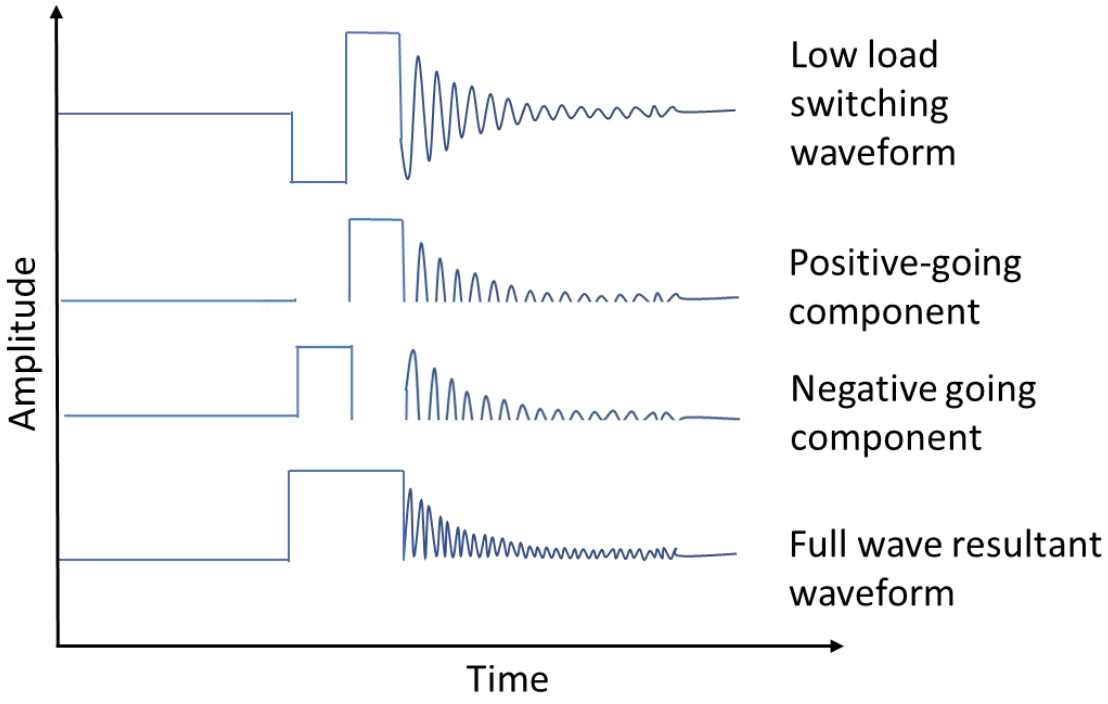

Figure 7.11: *Light load switching waveform (MAXIM 17222* [26]

As shown in figure 7.11 the typical light load switching waveform used by many manufacturers of PWM switching amplifiers (MAXIM, LT, TI etc) features a short pulse followed by a section of decaying oscillation to minimize inductance requirement's offload. With pulsed operation a full wave rectifier serves little purpose but during this operational mode the decaying oscillation can be full wave rectified to minimize CW capacitor values, droop and noise. The provision for full wave multiplier was added to the circuit to investigate this. In contrast to the other developments this provision dictated that the PCB build was much larger than could be used for a hand-held detector, but this was felt worthwhile to investigate the technique. The PHC2300 NMOS, PMOS pairs used in the dividers were very bulky in a SOIC package, overrated for the application, and should be

replaced with a more suitable part should this design prove suitable for further development

As previously discussed, the CW ladder needs to be tapered in order to maintain equal voltage across each stage under load. In the active divider design this was to simplify its transfer function to maintain a cleaner phase margin. However as this design sets the dynode voltages directly with the CW stages it has a more direct effect on performance. The capacitive taper used in the meta supply (table 3) was used in this supply for accurate comparison. The same resistive loading was used as the active divider build for accurate comparison and for the possibility of matching anode drop with CW droop for a predictable non-linearity. The full circuit is shown in figure 7.12.

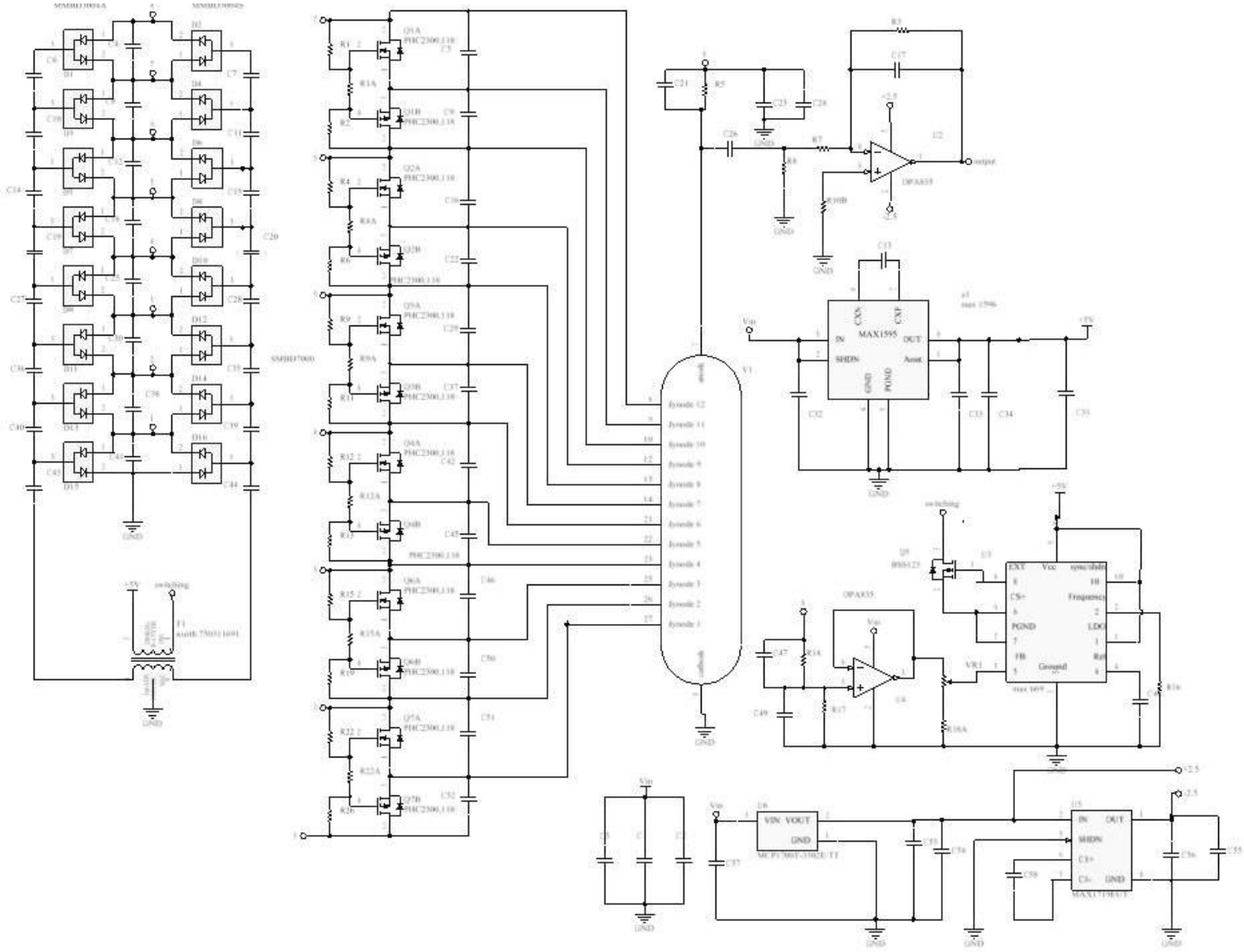

***Fig.7.12**: Clamped active divider circuit diagram. (BOM shown in Appendix table 9)*

7.5 High density PCB layout

As section 5.2 and 5.3 demonstrated it is not as much the complexity of the electronic design that will limit any competitive size reduction, nor the bulk of components used, but the physical clearances involved. Using the design rules outlined in section 5.3 for both air gaps and FR4 the following process was carried out for all 3 prototypes. However only the active divider system will be described, being the most complex.

Component choice was not as straightforward as selecting the part that fulfilled the various criteria in the smallest possible form factor; for delicate designs of this nature selecting a part that appears small and to fulfil, for example, absolute voltage rating may be small enough that dark discharge between its terminals is significant even if the device continues to function.

As these boards were required for development they had to be slightly enlarged to accommodate mounting holes and signal/power connectors. In a product the sub assembly would be potted in epoxy but these required frequent disassembly for optimization of component values. This also required that components not required for the final design were also included. Figure 7.13 illustrates how these boards were assembled into a SiP detector module.

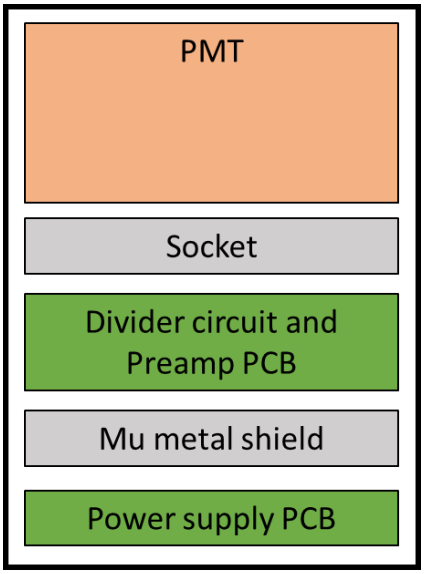

Fig 7.13: *Full detector sub assembly*

As the active divider was the most complex design this required 2 PCBs back to back; however the simplest of the 3 designs only require a single board. These required 5 wire links between the boards.

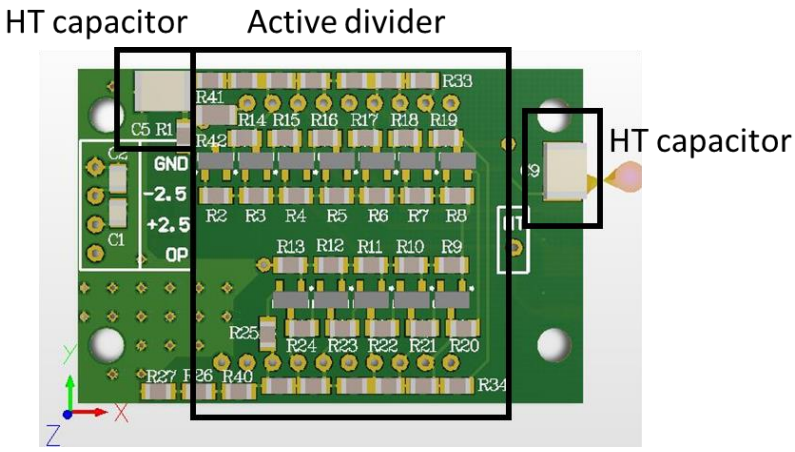

***Figure.7.14**: Upper board dynode cascode circuit.*

Figure 7.14 shows the underside of the top board (beneath the PMT socket). This side consists of the cascode dynode circuit (active and passive dividers), a HT bypass capacitor and decoupling capacitors for the +/- 2.5V rails. As no elements of the cascode circuit have a particularly high voltage (55V in the test circuit) across it, spacing between dynode components can be relatively small as long as the entire chain is kept clear of the ground planes. The only component with a high voltage across it is C5 which decouples the HT after the link wire between boards and a relatively long PCB trace. An 1812 capacitor with a 3mm gap between pads was selected. An air gap was not required as any leakage across this component simply corresponds to an increase in supply current. As the ground plane is comparatively small it is decoupled with vias (interconnections between the layers) every 2mm between sides.

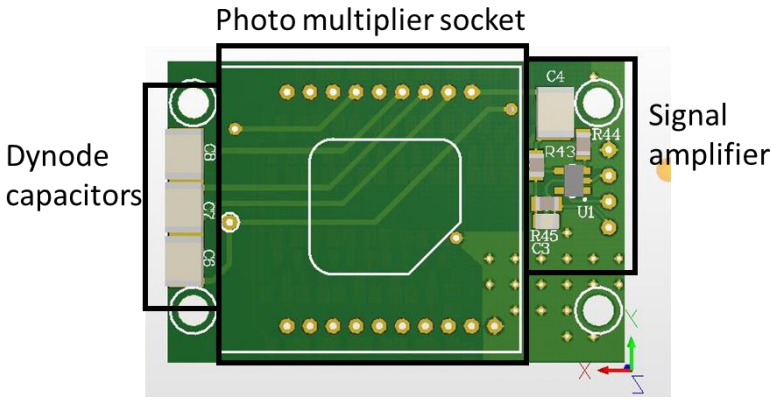

Figure 7.15: *Upper board showing PMT mounting and 1st stage amplifier.*

Figure 7.15 shows the upper side of the top board containing the PMT socket, 1st stage amplifier, and bypass capacitors for the first 3 dynodes.

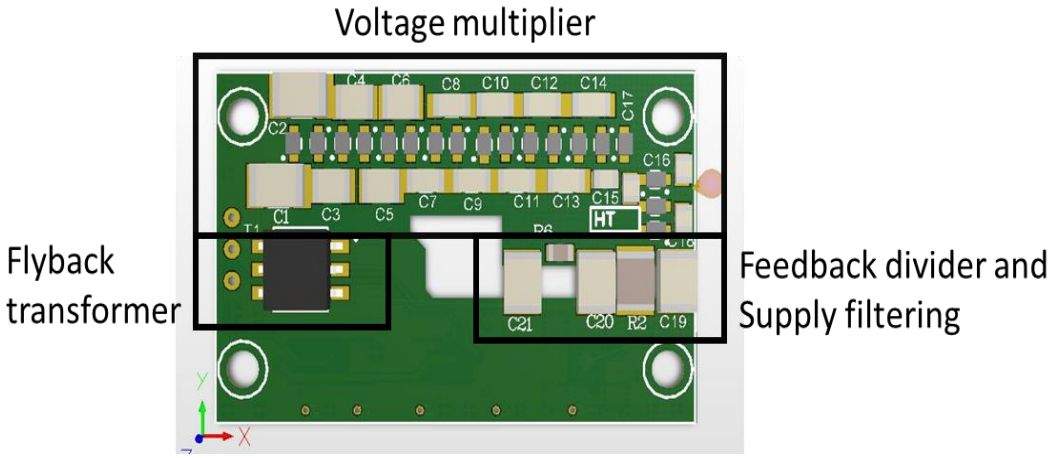

Figure 7.16: *Lower board high voltage generation.*

Figure 7.16 demonstrates the initial concept for the lower board. The board includes the flyback transformer, Cockcroft Walton multiplier, high voltage feedback, and final smoothing capacitors. These are all the components to which clearance is critical to performance and are arranged in a clockwise manner around a board cut out which also separated the pads on the feedback resistor, phase compensation, and smoothing capacitors. This leaves space for a clean signal path between the derivation of the feedback signal and the switching circuits.

On earlier prototypes it was found that the switching diodes tended to cause artefacts in the victim components in the feedback loop beyond that of the transformer or Mosfet

switching. The element that makes this problematic is that as commercial switching amplifiers rely on a comparator rather than steady state control for efficiency this pickup represents an error term which is inversely proportional to load. This makes load regulation especially poor and creates an equivalent supply impedance.

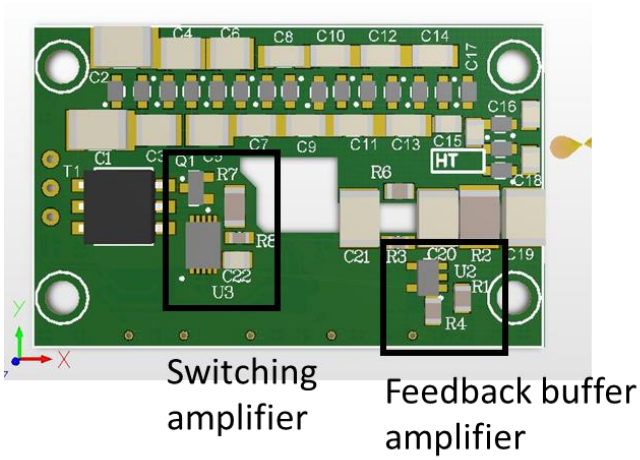

Figure 7.17: *Lower board high voltage generation and control amplifiers.*

In reference to figure 7.17 the following addition to the layout is to add both the feedback buffer amplifier (U2), switching amplifier(U1) and switching transistor(Q1). The two critical tracks are the high impedance feedback line (R2-U1 which has a high susceptibility to pick-up) and the switching line (T1-Q1). A buffered low impedance line runs between U2 and U3.

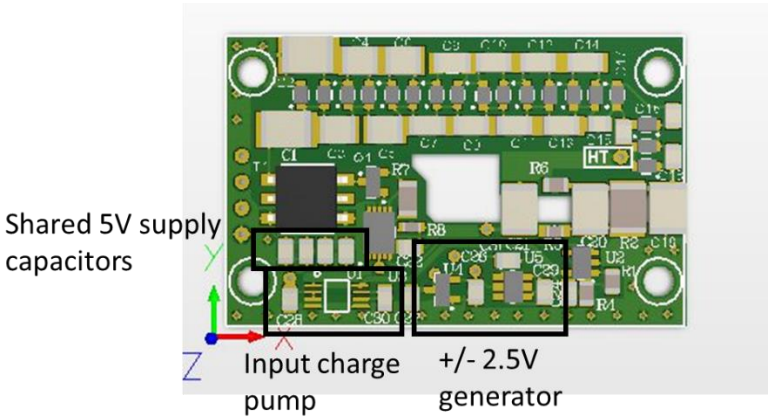

Figure 7.18: *Full power supply board including pre-regulation and differential power rail low voltage circuitry.*

Figure 7.18 shows the completed board with the addition of input power supply conditioning circuits. A clear ground rail is maintained along the lower edge of the board.

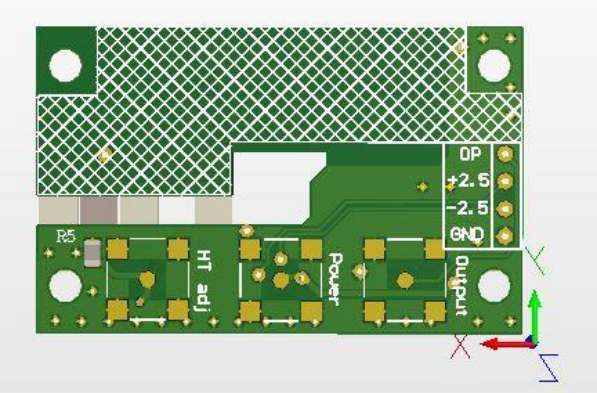

Figure 7.19: *Power supply board underside detailing connectivity.*

The reverse side of the power supply board is shown with test *Subminiature Version A* connectors in figure 7.19. Although these were only included for ease of repeated testing it was found that the output contained an element of pickup from the switching circuits, so a screened cable had to be directly soldered to the output of the 1st stage amplifier and tracks cut accordingly. The white hatched area is a reminder of a *keep out area* beneath the series rectifiers to exclude sensitive signals.

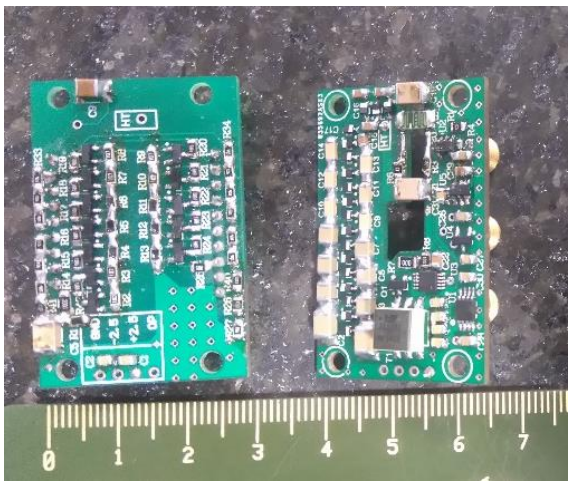

Figure 7.20: *populated board demonstrating manufacturability of the concept*

Figure 7.20 shows the built-up prototype as a demonstration of the feasibility of manufacturing devices of this size. The board used no advanced technology, using only

0.3mm vias and structures greater than 0.154mm. In quantities of 1000, price per unit can be brought as low as £0.10 per board, with these prototypes costing £1 each.

Layout process summary:

- As previously demonstrated, clearance across FR should be maintained at 130V/mm and 200V/mm across board cutouts. If these cannot be avoided dark discharge can be predicted using the formulae in section 2.1.
- On such a small board with numerous cutouts, creep clearance around un-plated edges must also maintain these clearances. PCB layout packages will typically not check these within the *design rule check* function so need to be maintained manually, or ideally not run any tracks under high voltage sections.
- A circular layout forming the control loop with a board notch, with bridging components to couple high and low voltage sections was found to be the optimal layout for signal integrity.
- A ground plane running around the outside of the low voltage sections was found to be optimal for maintaining signal integrity whilst avoiding leakage from the high voltage elements.
- With the size, complexity, and voltages involved pickup or leakage is inevitable so needs to be treated as intrinsic to the design. Larger development boards are of some use but cannot be assumed to be transferred to a smaller board and function in the same manner.

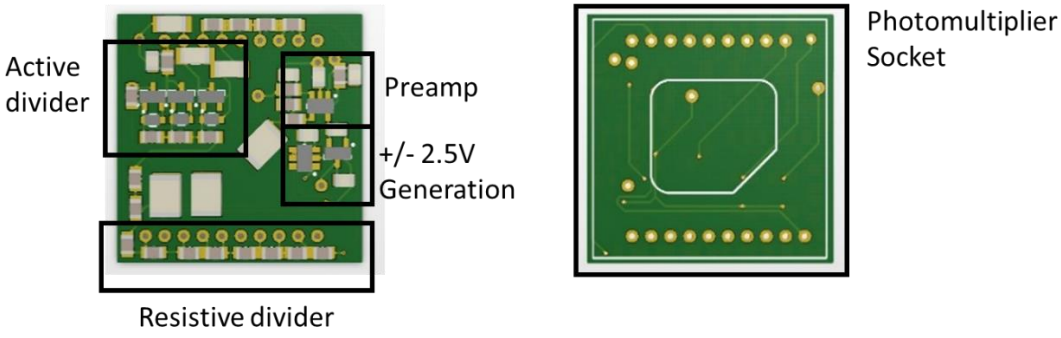

Figure 7.21: Final active divider circuit

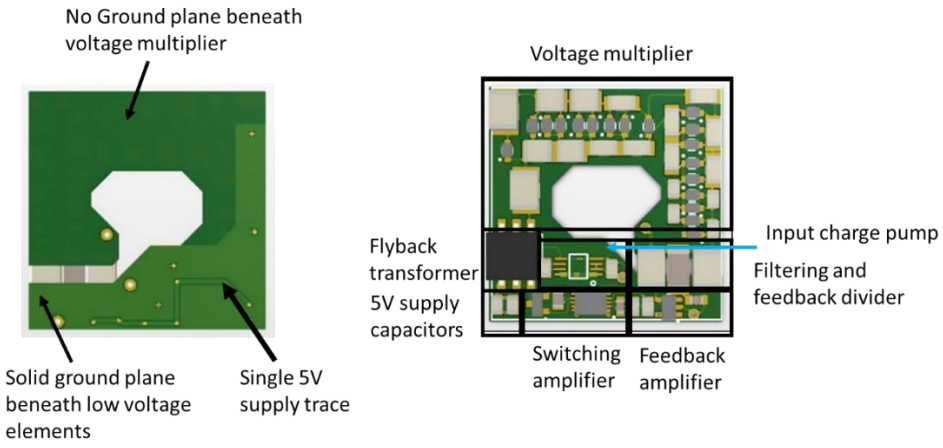

Figure 7.22: *Final power supply board*

Figures 7.21-2 shows a proposed production-ready layout of the above circuit. Any components included for development purposes have been removed and the overall board dimensions reduced to sit within the footprint of the PMT. The large cut out in the centre is oversized for isolation but is intended to aid epoxy potting of the module.

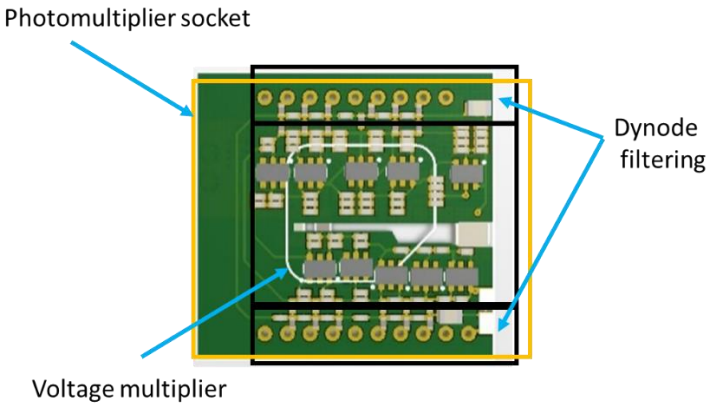

Figure 7.23*: Single board layout following the same design principals (Cockcroft Walton direct circuit) socket side*

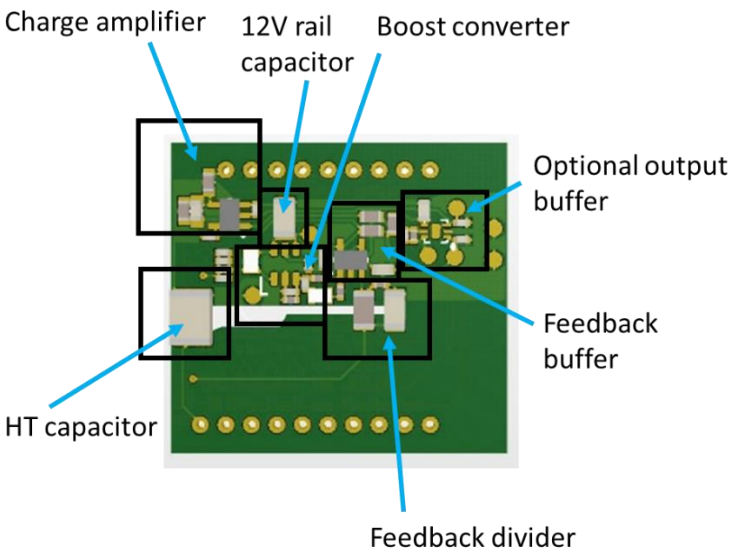

Figure 7.24: *Single board layout following the same design principals (Cockcroft Walton direct circuit) under side*

Figures 7.23-24 show both sides of the voltage multiplier prototype. This was the only one of the three prototypes that was able to be built at this early stage on a single PCB. The design philosophy was to place all the voltage multipliers under the PMT socket with all the buffering and power supplies on the underside. The bulky feedback divider and HT capacitors were isolated via a cut-out.

8 Results and Discussion

In order to critically assess the standard radiometric criterion of resolution, linearity, and pulse width the following detectors were measured:

1. A solid state detector consisting of 16 (4X4 array) SiPMs providing a comparable active area to that of the PMT. These were SenSL TJ sipms designed to aim to reach the speed of a PMT at the expense of power consumption. These were powered from a Tektronix lab-type power supply set to a proven operating point (28.5V). It would have been a more effective comparison to construct a low power hand held type power supply but this was felt to be an additional variable that might unnecessarily create doubt in results.

2. Hamamatsu example PMT circuit (R11265U-M4 as other prototypes) with datasheet values for a resistive divider. Hamamatsu's temperature compensation (un-bypassed cathode resistor) was removed as it was found to add significant non-linearities. This setup was used to derive an operating point at which resolution was acceptable but the shot noise associated with setting the supply too high was not encountered. This was found to be 700V.
3. A separate low power high voltage power supply and active divider circuit designed to be operated directly from a Li-Ion battery.
4. Integrated high voltage power supply with active divider clamped to the voltage multiplier to minimize cascode errors designed for direct battery operation.
5. Integrated PMT and power supply with voltage multiplier directly driving dynode circuits for further reduction in supply current and form factor

All PMT measurements used the same scintillator, PMT, and radiation sources. Initially 3 prototypes were brought up on the bench with idle power consumption, noise, load regulation cut off, and signal integrity being measured.

All 5 devices were then coupled to a scintillator with a Cs137 spectrum and a combined Cs137/Eu152 spectrum taken for each device. Using software created by Dr Alan Bell [27] the resolution and linearity of the detectors could be evaluated in line with industry standards.

Linearity was measured on one unit (Active divider) using a curve tracer and light source to confirm that any non-linearities were optical detector or electronics based rather than scintillator based.

8.1 Electronic testing

Of the two key supply parameters, supply offset current and stability, initial estimates can be made before the PMT is introduced to the system. The results from the 3 test boards are shown below in table 4. +/-2.5V supplies and signal amplifiers are excluded from these measurements.

To characterise both the power supply step change performance and the input amplifier the completed module was tested with a Horiba Nanoled laser system using a 1ns 450nm LED head, rather than moving straight to testing the system with a scintillator crystal which can present complex signals due to optical issues.

As with the PCB design summary, only one of the three concepts is described in detail. There is significant overlap between all designs, so any solutions are applied globally.

Table 6: Power supply performance of all prototypes.

Circuit	Noise peak	Consumption (supply only)	Consumption (dividers included)	Load regulation cut-off (1%)
Active divider	4mV	12mW (4mA)	30mW(10mA)	380µA
Hybrid	23mV	9mW (3mA)	18mW(6mA)	450µA
Cockcroft Walton	8mV	3mW (900µA)	N/A	210µA

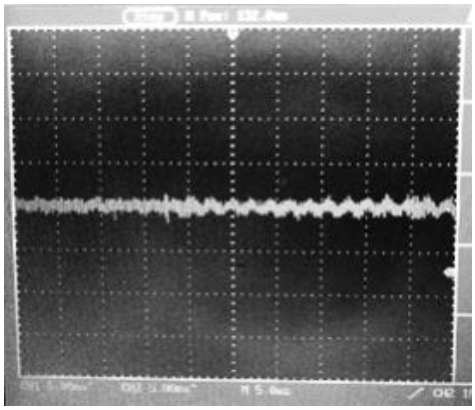

Figure 8.1: *Post regulator ripple (2mV 500KHZ)*

Ripple in the signal band (figure 8.1) was 2mV predominantly at 500KHz, the first harmonic of the switching frequency. Low frequency noise after the cascode active filter was 4mV (500Hz control loop noise). This was calculated to cause less than 0.01% increase in resolution with signal band noise in line or better than commercial products using linear oscillator-based systems.

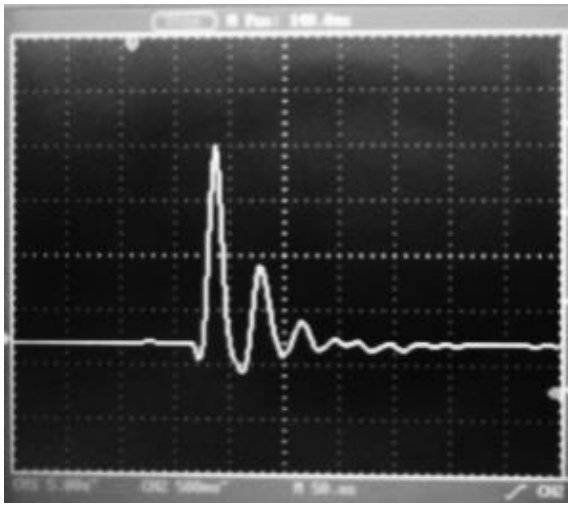

Fig 8.2: *Ringing due to inadequate dynode termination*

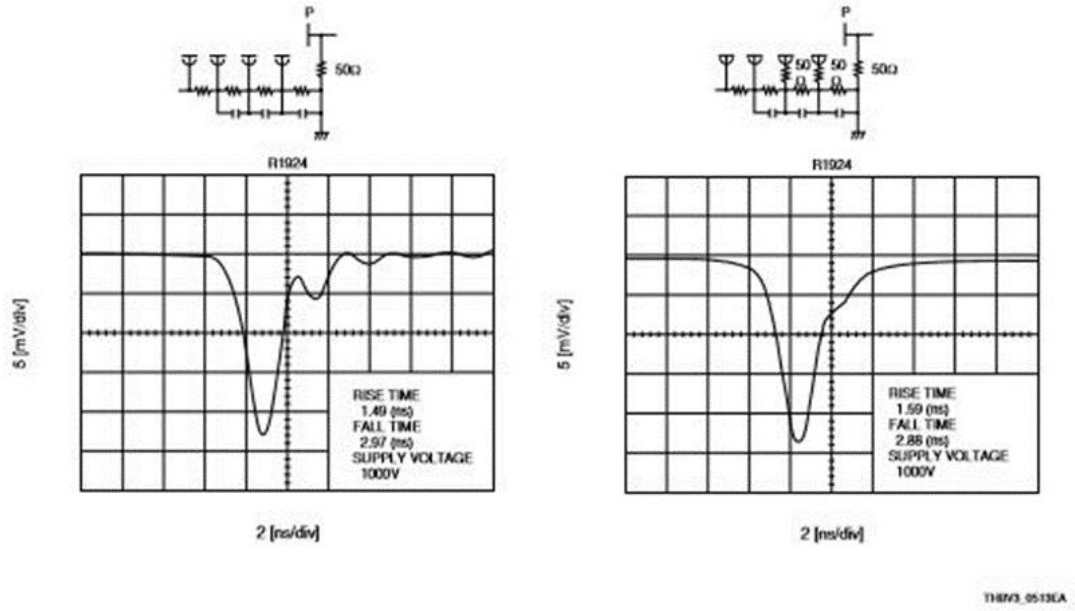

Figure 5-13: Effect of damping resistors on ringing

Figure 8.3: *Hamamatsu's illustration of typical lack of dynode termination ringing* [6]

Figure 8.2 shows the signal at the PMT anode RC coupled in to 50 ohms with no amplifier. As can be seen there is a significant ringing in the signal. This was briefly tested with a scintillator and found to be proportional to energy. This was hypothesized to be an artefact from ceramic capacitors; however substituting the value had no effect on the time constant of this ringing. The bandwidth of the first stage amplifier was then reduced to remove any resonance-based ringing (at a higher frequency). Figure 8.3 shows Hamamatsu's

example of inadequately bypassed dynodes causing comparable ringing. Bypassing these to ground rather than just using the capacitors as a reservoir for large events greatly reduced these artefacts. This ringing was not present on the example resistive circuit, so the small amount of ringing remaining was likely to be caused by an underdamped element of the action of the active divider.

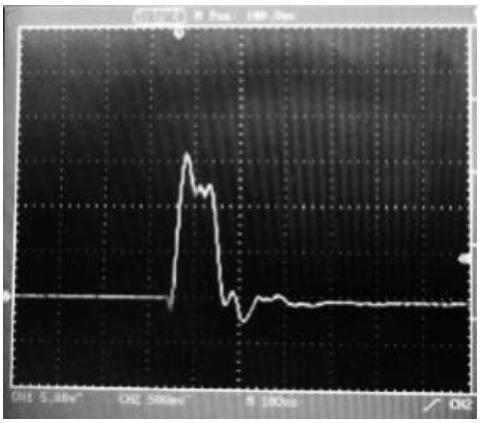

Figure 8.4: *MAX4452 non-linearity of transition from small to large signals.*

The Opamp originally chosen for the first stage amplifier was a MAX4452, noted for its 200MHz gain bandwidth, modest 600uA supply current requirement and negative rail input. A degree of uncertainty was present in its differing small signal and large signal response, although the decision was made to proceed and evaluate this component in more detail. Had this change from small signal been progressive in nature this is potentially an advantage providing a reverse logarithmic response that allocates more of the available ADC bins to low energy information offsetting any noise flaw issues. On measurement this was a hard step as illustrated in figure 8.4, rendering the signal range to less than 1V. Even within this region the amplifier generated severe error for fast transients, and no usable energy information before the damping capacitor was added.

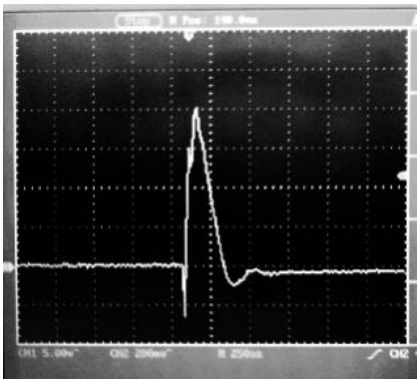

Figure 8.5: *MAX 4130 demonstrating distortions introduced with fast signals.*

With the required bandwidth being significantly reduced due to damping (around 5MHz) a MAX4130 previously used in the power supply was substituted for the MAX4452. The current consumption was slightly higher (800µA) and bandwidth significantly lower (10MHz) but it served to demonstrate the performance of a less temperamental amplifier. Figure 8.5 demonstrates a typical event with this amplifier with the underdamped elements artefacts of the divider still being clearly visible.

The damping introduced does preclude the detector for pulse shape discrimination applications. If it was to be developed for this application solutions would either be to decouple all the dynodes to ground or use a more comprehensive multi stage integrating amplifier.

8.2 Reference circuits

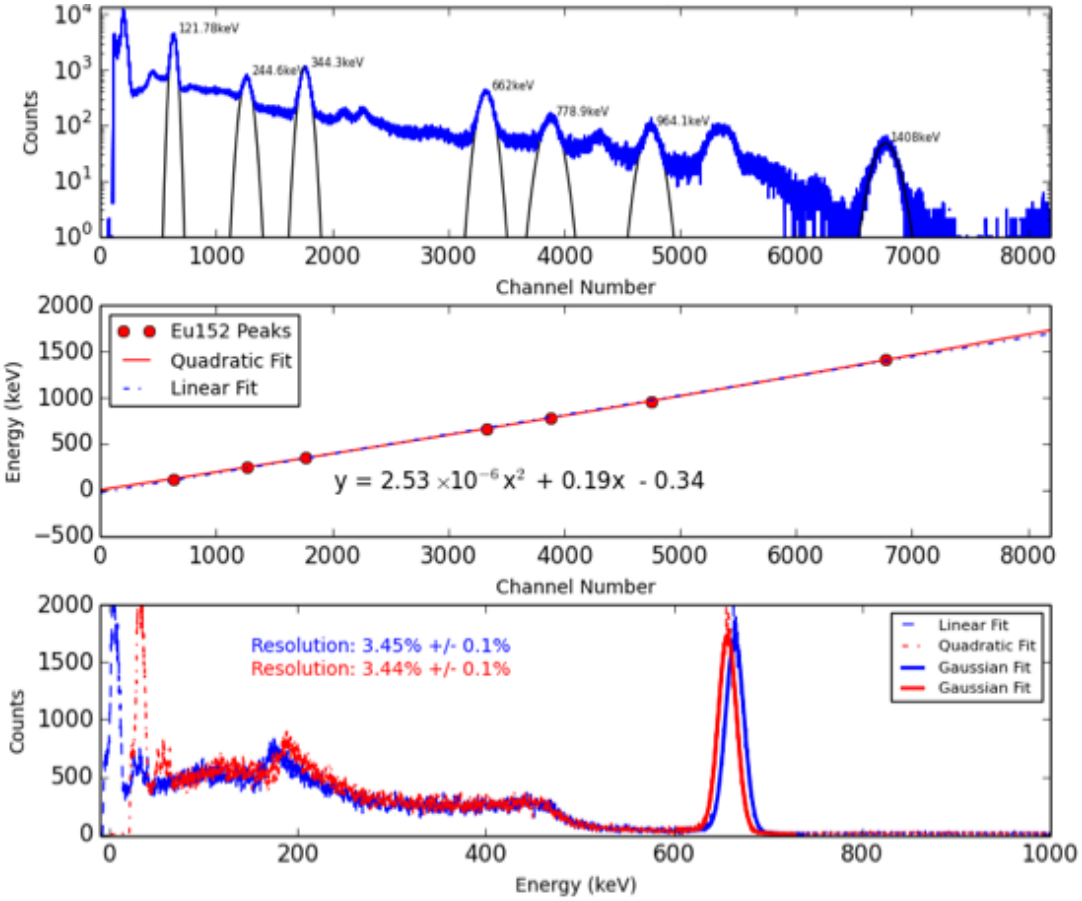

Figure 8.6: *Hamamatsu example circuit (resistive divider) linearity with europium and caesium spectrum.*

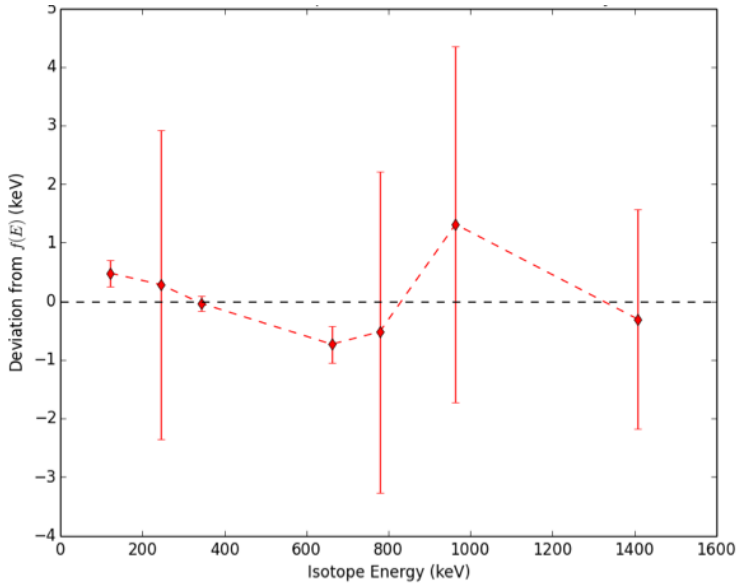

Figure 8.7: *Hamamatsu example circuit deviation from polynomial fit.*

Hamamatsu quoted the PMT of producing a 3.3% resolution at 662KeV [4] with lanthanum bromide. An off-brand scintillator was used so the 3.45% resolution shown in Figure 8.6 was consistent with expectations of the lab PMT setup. The operating point was also lowered from 900V to 700V to reduce noise (eliminate shot noise) and reproduce the low energy Europium peaks required for linearity evaluation. The linearity was +/- 1.5KeV throughout the range of operation (fig.8.7).

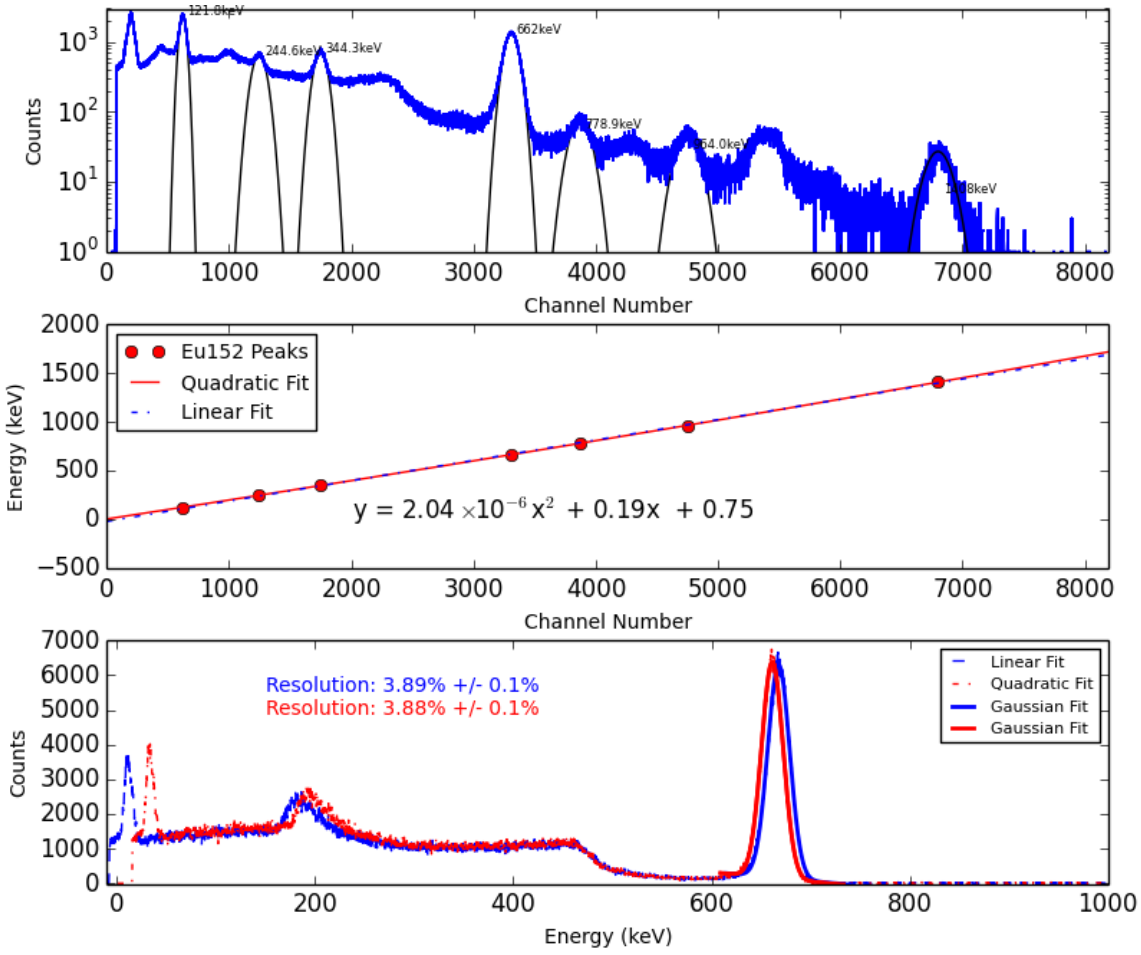

Figure 8.8: *4x4 6mm SiPM array linearity with europium and caesium spectrum*

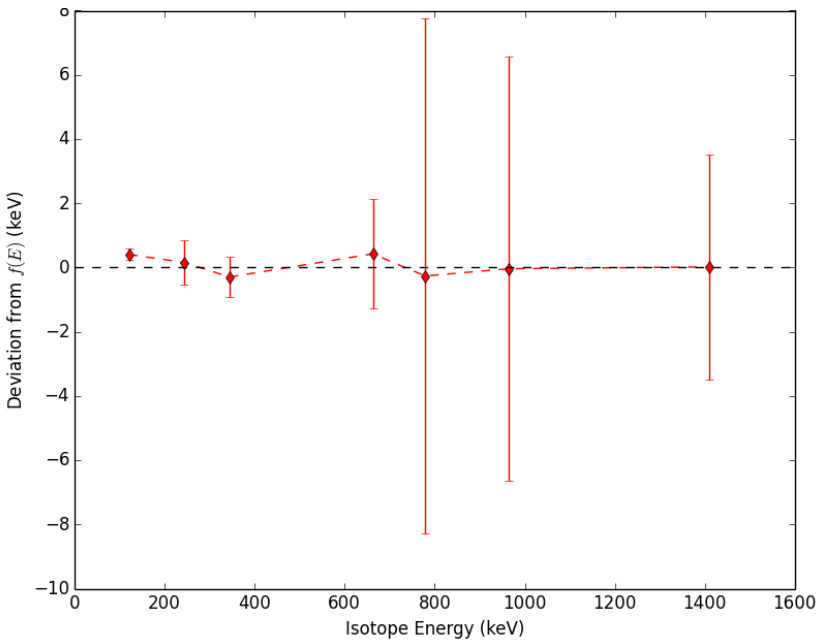

Figure 8.9: *4x4 6mm SiPM array deviation from polynomial fit*

The solid-state detector array coupled to the same scintillator array produced a 662KeV resolution of 3.9% in line with expectations (figure 8.8). It did outperform the PMT on linearity although the difference is negligible (0.7KeV) in terms of experimental error.

8.3 Active divider

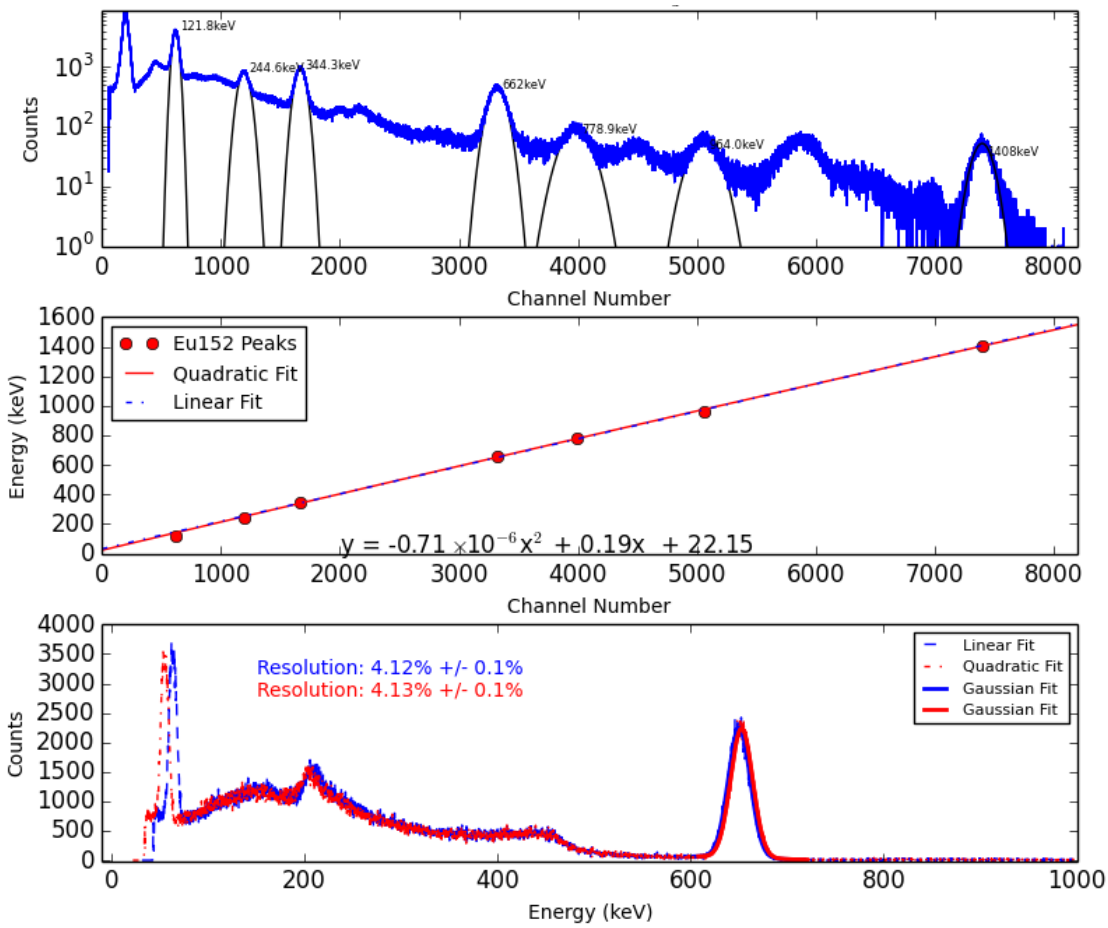

Figure 8.10: *Active divider PMT linearity with europium and caesium spectrum*

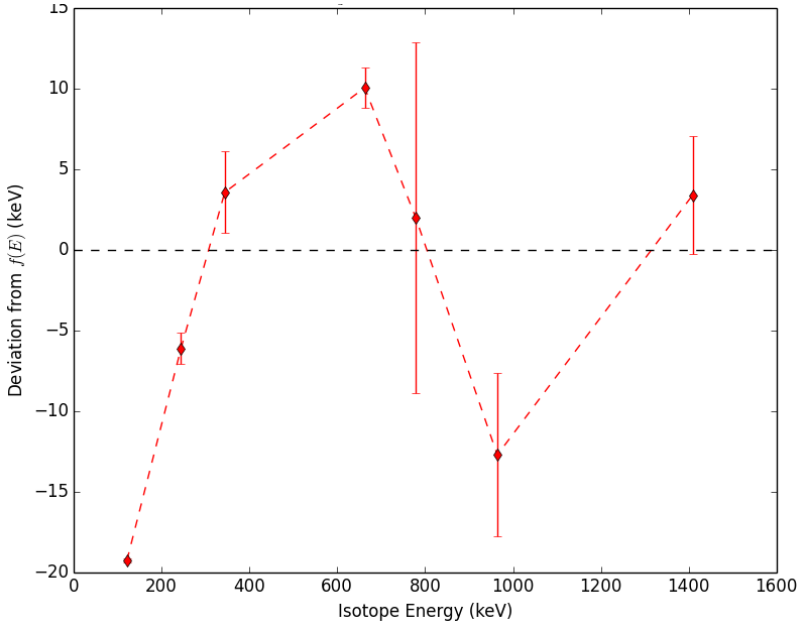

Figure 8.11: *Active divider PMT deviation from polynomial fit*

The active divider circuit (figure 8.1) produced worse 662KeV resolution (4.1%) than both the lab PMT setup (3.45%) and the SiPM circuit (3.9%). When the lower dark noise contribution and shorted integration time are factored in (0.5µS vs 2µS) it becomes clear there is stability issue causing gain to vary and create the 0.65% resolution over lab conditions. In reference to section 2.1 this would only be in the order of 500mV variations in accelerating voltage cumulatively to cause effects of this magnitude. As demonstrated in the hardware testing and the negative artefacts introduced into the signal the most likely solution is that more damping is required around the active divider and its reference chain. It is likely that careful PCB layout to include large capacitors would address this to a certain extent. It was also found that the cut off region on these MOSFETS used varied even more than the active regions so biasing them accordingly would limit these variations.

The strong point of this device were the efficiency and headroom of the supply stage and the range of adjustment. 4mV of noise and 4mA offload current draw are unachievable in comparable commercial designs. Even with the above shortcomings there would still be strong reason to use this if high rates, temperature stability or harsh environments prohibit SiPM usage.

The most noteworthy points are in relation to linearity (figure 8.11); The peak deviations (600KeV and 1MeV) corresponded to a mirror of those in the lab-PMT setup (figure 8.7). This is theorised to be a gain error in the active divider mechanism and the overdamped response (figure 6.4). Secondly the sub 300KeV linearity error which is calculated to be the point at which the MOSFETs reach threshold and start supplying current to the dynode beyond that of their leakage resistance.

8.4 Cockcroft Walton

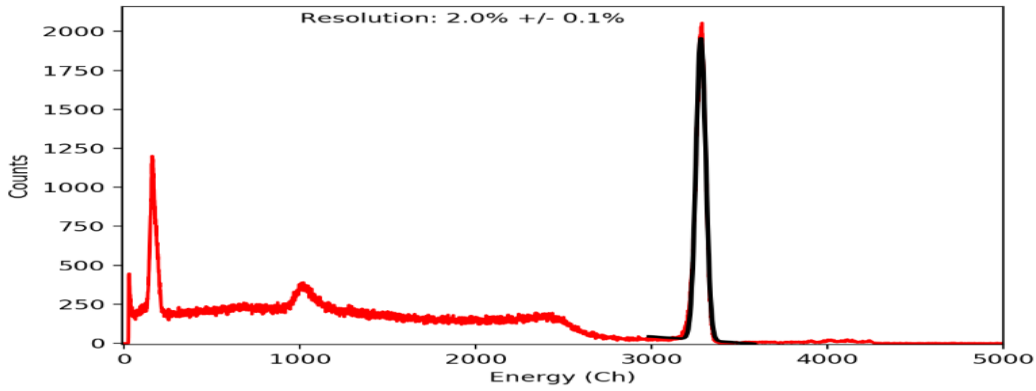

Figure 8.12: *Cockcroft Walton based PMT caesium spectrum*

This detector was based around a negative HT supply which was extremely efficient in reducing power supply noise contribution to below an equivalent of 5KeV.The overextension of this concept was to use only a boost converter to drive the multiplier rather than a flyback stage as there was found to be deficiency in the supply to deliver larger transient currents. This manifested itself in a severe non-linearity above 550KeV yielding a false 2% resolution at 662KeV (figure 8.12). The detector had excellent performance at low energy, in contrast to the active divider circuit, so would be particularly useful even in its current form as an X-ray detector. Unfortunately, the non-linearity evident on the Cs137 spectrum prevented a full linearity test as it was beyond the range of the program previously used.

The power consumption drew 1.1mA for the full system from a 3.3V supply. The high voltage supply consumption was 700µA with the charge amplifier drawing 300µA.

8.5 Clamped active divider

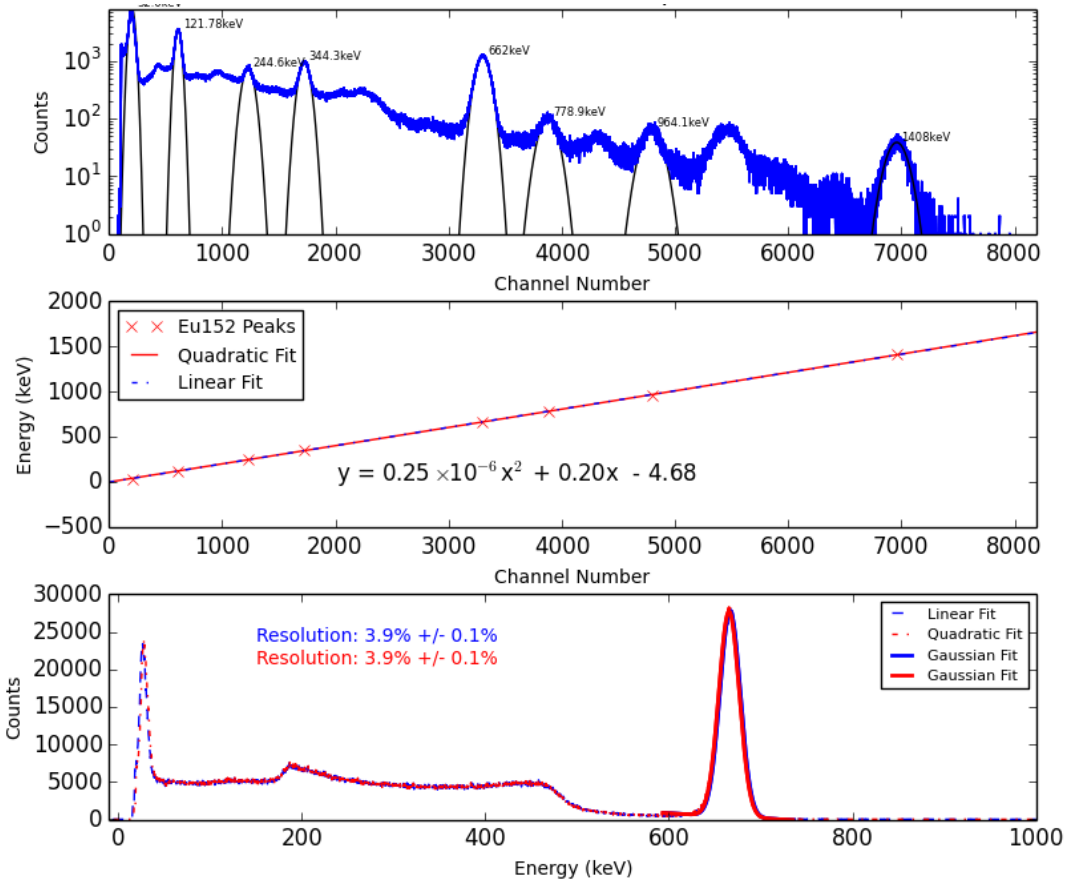

***Figure 8.13**: Hybrid divider PMT linearity with europium and caesium spectrum*

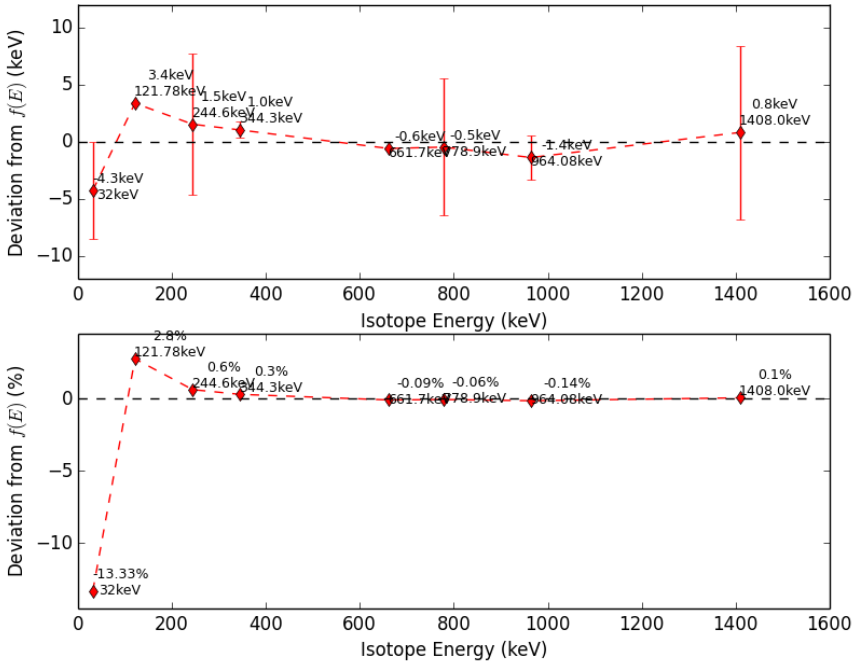

***Figure 8.14:** Hybrid divider PMT deviation from polynomial fit*

The hybrid design equalled the solid-state detector's resolution (3.9%, figure 8.13) and provided excellent power consumption. Its failing was that it produced excessive noise, so gain had to be increased to compensate as periodic elements of the supplies burst mode operation caused peaks in the spectrum. With the lower gain of the other detectors it produced 3.3% resolution at 662KeV but with noise peaks at 50KeV and 170KeV. This is an increase in performance over the Lab PMT so should be investigated further.

The linearity was also the best of the three prototypes (figure 8.14) with performance above both the lab PMT circuits above 300KeV. It did suffer with the same low energy gain error as the active divider circuit but with less severity, and presumably the same mechanism. The differentiator however is that, as the active blocks are push-pull, the biasing can be adjusted to compensate for this.

If this MOSFET bias issue was refined to a matched diode system rather than resistor and the device was converted to negative HT this prototype has the potential to exceed the LAB-PMT performance at close to solid state power consumption.

8.6 Optical linearity

As has been stated previously the system was tested as a whole as irregularities in either the power supply, divider or amplifier could adversely affect the results taken. In order to confirm whether artefacts were caused by the modules, and not by the scintillator, a semiconductor analyser was modified to trace the linearity of the full module. The active divider was the only suitable circuit for this application but still served to eliminate scintillator errors from any conclusions drawn.

A Telequipment Curve trace was set up to drive a 450nm LED from its step generator, with the complete module between the current sense terminals as shown in figure 8.15. The results are shown in figure 8.16, which, although not a substitute for the software europium analysis conducted previously, confirm the peak and minimum non-linearity points of the circuit. An inverted form of these points is also present in the resistive divider, using a lab-type power supply suggesting an anomaly within the PMT itself for which the active divider is overcompensating. The MCA used can be eliminated as the points of deviation (600KeV and 1MeV) are not present on the SiPM or Clamped divider measurements.

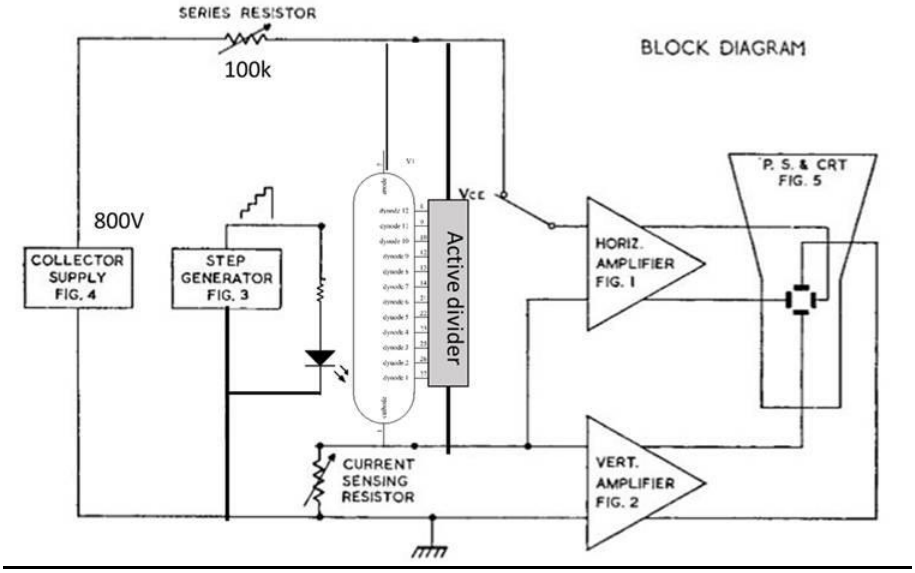

***Figure 8.15**: Modified CT71 curve tracer used to confirm linearity measurements.* [28]

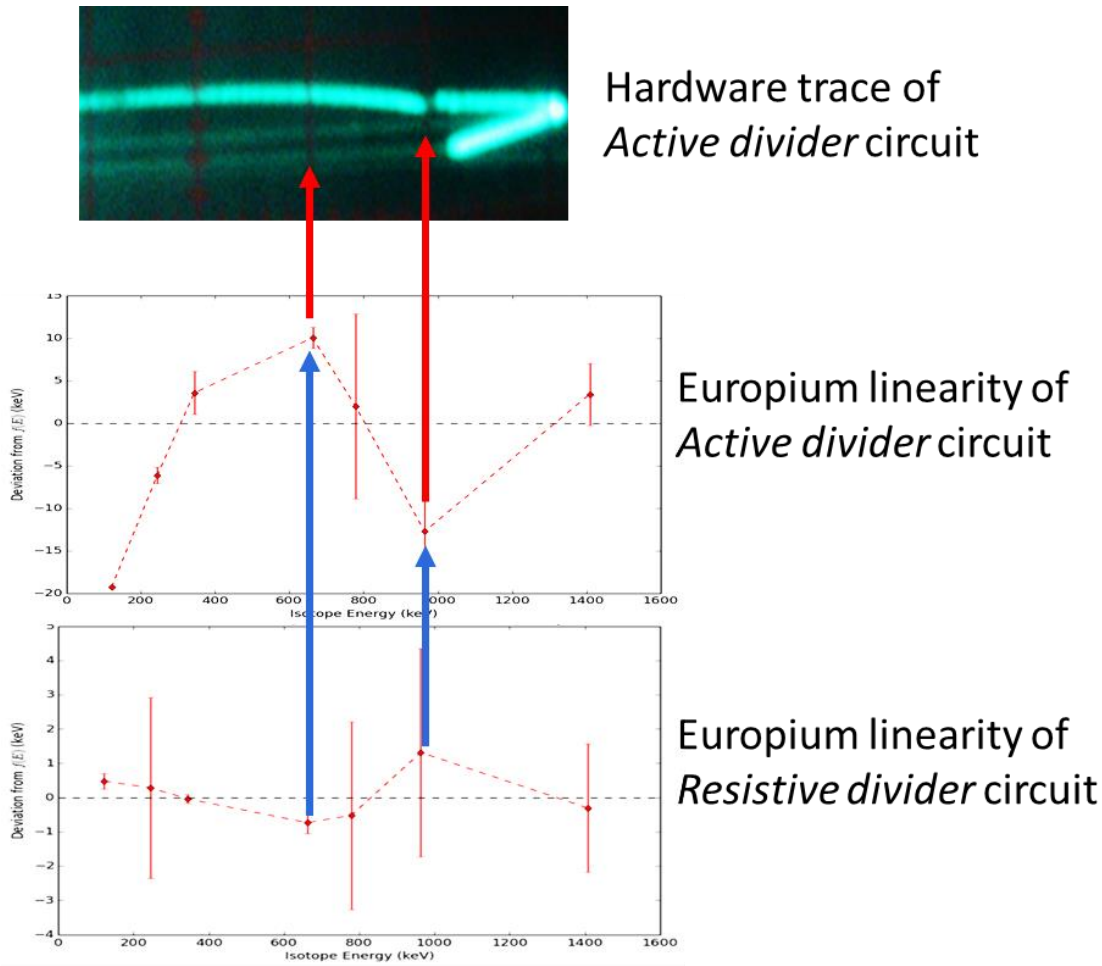

***Figure 8.16:** Linearity of the active divider PMT circuit taken on a semiconductor tester.*

8.7 Results summary

Table 7: *Summary of testing*

Circuit topology	power consumption (full front end)	Pulse width	662KeV resolution	Peak non-linearity (KeV)
Lab PMT	200mW (approx.)	<0.5µS	3.45%	1.5
1" SiPM array	24mW	2µS	3.90%	1
Active divider	38mW	<0.5µS	4.10%	12
Hybrid	30mW	<0.5µS	3.90%	3.4
Cockcroft Walton	5mW	0.65µS	Non-linear	Non-linear

9 Conclusions and Further Work

9.1 Analysis against performance criteria

Footprint equal to that of an equivalent area solid-state module.

The PCB footprint of the completed module was comparable to that of the solid-state equivalent, although deeper. Should MEMs PMTs become commercially available this module would be of similar dimensions to that of a solid-state module.

This is only applicable to 1” detectors as the circuitry does not scale down infinitely. If a smaller detector is required, the secondary electronics are likely to be prohibitively large, independent of any future reduction in PMT/electron multiplier size. As the further development of the concept is to implement a refined version of the findings here to a µPMT, further work will be required to fit these circuits to a 10mmx10mm PCB.

Power supply requirements equal to that of a solid-state module with the inclusion of buffer amplifier.

In reference to table 4, power requirements of the example circuits varied from 5-38mW in comparison with 24mW for the solid-state example. It has been identified that with bespoke Mosfets this could be reduced to the same amount as the solid-state detector. The

TJ SiPMs used are not the lowest power devices available so should not be seen as the limit of solid state detectors.

To provide positive going pulses to be retrofittable in the place of a solid-state detector

As previously highlighted the footprint of the device matched that of a solid-state device. With the Hamamatsu R series used for these proof of concept builds a shorter scintillator would be required. It is anticipated when MEMs PMT technology reach maturity that the module could be a drop-in replacement. The simplified, single stage decoupling amplifier did require careful setup when used with the AC coupled circuits, so the DC coupled charge amplifier is recommended for any developments.

Power to be 3-5V typical of lithium battery system voltage

The charge pump front end (U1 figure 7.4) to the power supply handled these requirements. When a boost converter was used in its place for flexibility and efficiency (U1 figure 7.8) efficiencies were improved but some non-linearities were introduced into the system. With the optimisation of phase margin and careful selection of supply capacitors the inrush current on 'power up' was suitable for battery powered operation.

Performance to be as close as possible to that of available photomultipliers datasheet values and/or factors causing loss of performance to be documented.

None of the prototypes outperformed the Hamamatsu published example PMT circuit in all respects, though the Cockcroft Walton coupled prototype required 2.5% of the power to operate. It also had the lowest noise flaw of any of the detectors but suffered from non-linear high energy performance.

The active divider circuit lost resolution and linearity to underdamped MOSFETS but the closest to lab performance was the synthesised clamped active divider circuit. It suffered from signal band noise, and the same low end non-linearity as the active divider to a reduced extent. It did demonstrate that it could meet the resolution if noise was reduced by developing a negative HT variant.

9.2 Achievements

- Characterisation of high voltage multi-layer ceramic capacitors' behaviour under DC bias.
- Modelling of non-linearity of Cockcroft Walton multipliers including these capacitors.
- discharge modelled in free air and across FR4 dielectric for accurate prediction high voltage compact PCB design.
- Full detector front end developed suitable for replacing solid state detectors for special applications.
- Novel DC coupling hybrid direct/active divider method concept proven and highlighted for development.
- Phase margin measurement technique was powerful and will be developed further.

9.3 Compromises

- Multistage phase margin compensation/variable compensation omitted.
- Dynode circuit speed not measured at a bench level. This was problematic as it was theorised to be the source of many errors but tools to measure this were only constructed toward the end of the project, as off the shelf test equipment was found unsuitable.
- Current mirror coupling omitted. Although the performance of DC coupled circuits were evaluated, further research should be carried out, especially if silicon elements are incorporated into the tube itself.
- Hybrid design did perform as well as the lab type circuit at 662kev with 1k load resistor but needed this to be increased because of supply noise sub 100keV. An active filter circuit may have remedied this but a negative HT variant should have been built for comparison after the sub 5KeV noise flaw of the Cockcroft Walton direct coupled was measured.
- The Cockcroft Walton direct coupled circuit showed excellent promise but needed further development which was unavailable during the research period. A stage was skipped in proving the unorthodox coupling of the inverting converter to the CW ladder which would need further development.

- Should more suitable semiconductors for the dynode chain become available there is potential for this circuit to track changes in current through this circuit rather than relying on reservoir capacitors.
- There is still dead space on the PMT base board, along with power supply capacity to spare, so other elements such as pulse shaping, and baseline restoration could be integrated into this for a true 'straight to ADC' System in Package.

9.4 Further development for SOC solution.

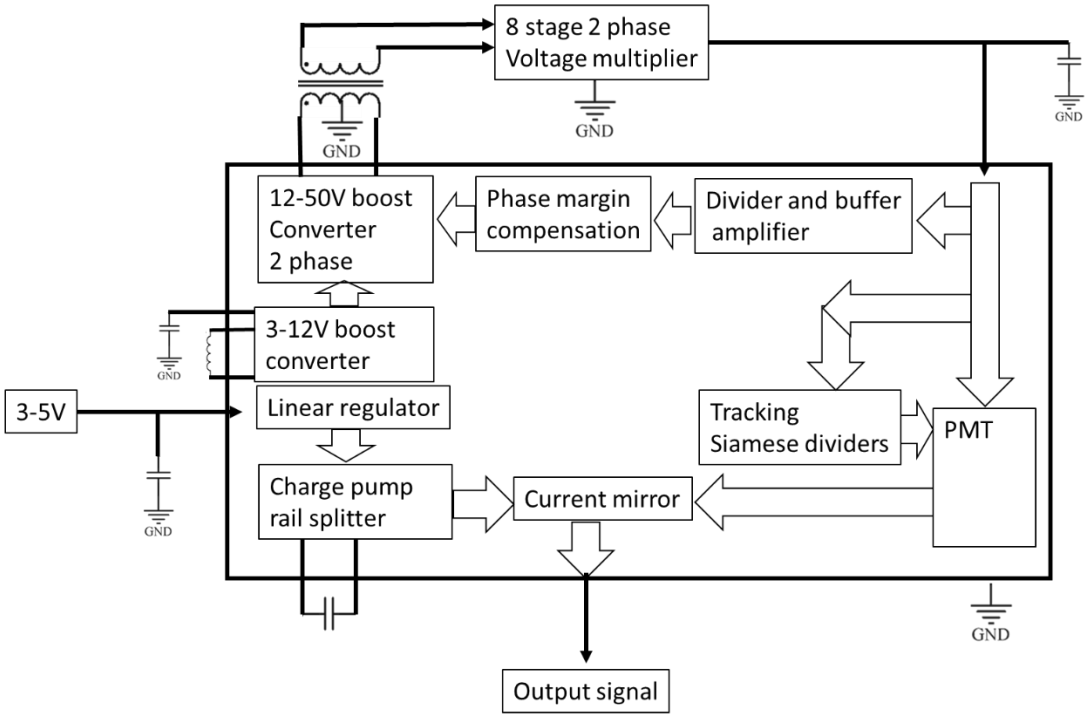

Fig 9.1: *Suggested ASIC implementation for SOC*

In reference to section 9.4 the system shown in figure 9.1 is recommended for a system on chip solution. The modifications are highlighted in Table 5.

This is based on the clamped active divider method synthesised for this project, although it combines successful elements from the other 2 prototypes. As stated in the result section the two issues that caused problems in this detector were the noise associated with the positive HT supply and the oversimplified MOSFET biasing method. It also maintains the 2-phase voltage multiplier. It is thought that capacitor sizes can be reduced for quick recovery time and reduced form factor with the negative HT supply.

It is recommended that the 2-stage boost converter is used (from the Cockcroft Walton direct prototype) but driving a 1:1 transformer and the inverting converter previously used had limitations. This serves to eliminate the 1:5 transformer used in both the flyback prototypes, so a higher frequency is attainable.

It is anticipated that at a silicon level a current mirror can be used for coupling although this will require further investigation. Alternatively the 200µA charge amp (used in the Cockcroft Walton direct circuit) could be reduced to a slower amplifier without any performance reduction and further power reduction.

Finally a more sophisticated continuously variable phase margin correction system would benefit the system and development process greatly. Table 5 summarises the modifications to the clamped active divider circuit to either allow a well refined SiP solution or the starting point for a SoC solution.

Table 8: Propose changes to implement a high performance SOC solution

Modification	Intended result	potential shortcoming.
2 stage boost-converter as CW prototype	Improved line regulation	complexity
2 phase transformer drivers	faster switching regulator transient response	switching losses increase, complexity
1:1 transformer driving CW ladder at 1 MHz (fixed)	eliminate non-linearities from CW prototype	bulky
Negative High voltage supply	lower signal noise contribution from power supply	additional insulation required around PMT
Siamese dividers as the hybrid prototype	Eliminate capacitive overshoot errors.	bulkier with more power consumption than CW direct coupled
Current mirror signal decoupling	Simplicity	difficult to prove with discreet parts at high ratios
Dedicated variable phase margin compensation block	Supply accuracy	complexity
Small CW caps, linearity compensation externally	faster recovery	amplitude errors over time domain errors
Single mode boost converter PWM (no burst or pulse skip)	Supply noise	narrower operational range
Non-comparator feedback input stage, PI only.	Supply accuracy eliminate 300*20mV hysteresis error.	narrower operational range

The steps to achieve this are anticipated to be as follows:

- Refine push-pull divider biasing arrangement without sacrificing power consumption. Confirm negative HT operating point.
- Develop boost, phase correction, and current mirror at discreet transistor level.
- Build full discreet transistor prototype to evaluate concept.

10 Bibliography

[1] J. Sharpe, Nuclear Radiation Detectors, London: Methuen & Co, 1955, p. 179.

[2] Hamamatsu Photonics, Kengo Watase , “What is the Micro PMT?,” 2013. [Online]. Available: https://www.laserfocusworld.com/articles/print/volume-49/issue-05/features/photomultiplier-tubes--upmt-is-key-to-high-performance-portable-.html. [Accessed 4 February 2019].

[3] L. AGGER, “Electron Multipliers,” in *Principals of electronics*, McMillan and company limited, 1963, pp. 311-325.

[4] Hamatsu Photonics, “PHOTOMULTIPLIER TUBES AND PHOTOMULTIPLIER TUBE ASSEMBLIES.; R11265U-M4 series and H13226A Series,” 2017. [Online]. Available: http://www.hamamatsu.com/resources/pdf/etd/R11265U-M4_H13226A_TPMH1359E.pdf. [Accessed 4 February 2019].

[5] H. Bruining, Physics and applications of secondary electron emissions, London: Pergamon, 1954.

[6] Hamamatsu Photonics, “PHOTOMULTIPLIER TUBES: Basics and Applications, Third edition,” 2007. [Online]. Available: https://www.hamamatsu.com/resources/pdf/etd/PMT_handbook_v3aE.pdf.

[7] Hamamatsu Photonics, “Photocathode technology:Elemental technology,” [Online]. Available: https://www.hamamatsu.com/us/en/technology/innovation/photocathode/index.html. [Accessed 7 December 2016].

[8] Saint Gobain Crystals, “BrilLanCe(TM) Scintillators Performance Summary,” 2009. [Online]. Available: http://www.gammadata.se/assets/Uploads/SGC-BrilLanCe-Scintillators-Performance-Summary.pdf. [Accessed 2019 February 4].

[9] Telefunken Electronics, “S82 stereo amplifier manual,” 1961.

[10] NASA, W. T. Harrigill, Jr.; I. T. Myers, “High performance DC-DC conversion with voltage multipliers,” 1974. [Online]. Available: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/19740018624.pdf. [Accessed 4 February 2019].

[11] NASA, J. J. Kisch; R. M. Martinelli, “HIGH FREQUENCY CAPACITOR-DIODE VOLTAGE MULTIPLIER,” 1977. [Online]. Available:

https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/19780007457.pdf. [Accessed 4 February 2019].

[12] J. D. Cockcroft and E. T. S. Walton, "Experiments with High Velocity Positive Ions.—(I) Further Developments in the method of obtaining High Velocity Positive Ions.," 2017. [Online]. Available: https://royalsocietypublishing.org/doi/abs/10.1098/rspa.1932.0107. [Accessed 4 February 2019].

[13] J. D. Cockcroft and E. T. S. Walton, "Experiments with High Velocity Positive Ions. II.— The Disintegration of Elements by High Velocity Protons.," 1932. [Online]. Available: https://royalsocietypublishing.org/doi/abs/10.1098/rspa.1932.0133. [Accessed 4 February 2019].

[14] E. Ioannia and K. Tatakis, "Optimal Design of a half wave cockcroft walton voltage multiplier with minimum total capacitance," 2010. [Online]. Available: https://ieeexplore.ieee.org/document/5456136. [Accessed 4 February 2019].

[15] P. M. Lin and L. Chua, "Topological generation and analysis of voltage multiplier circuits," October 1977. [Online]. Available: https://ieeexplore.ieee.org/document/1084273. [Accessed 4 February 2019].

[16] X. L. Polozec, "Input Impedance and Transfer Function of N-Stage Cockcroft-Walton Voltage Multiplier," 2016. [Online]. Available: https://www.researchgate.net/publication/309736327. [Accessed 4 February 2019].

[17] EMCO HIGH VOLTAGE, "A-Series Datasheet," [Online]. Available: https://www.xppower.com/Portals/0/pdfs/SF_A_Series.pdf. [Accessed 4 February 2019].

[18] CDE Cornell Dubilier, "Multilayer Ceramic Capacitors - Performance Characteristics," [Online]. Available: http://www.cde.com/resources/catalogs/ceramperf.pdf. [Accessed 4 February 2019].

[19] M. Fortunato, "Temperature and Voltage Variation of Ceramic Capacitors, or Why Your 4.7µF Capacitor Becomes a 0.33µF Capacitor," 2012. [Online]. Available: https://www.maximintegrated.com/en/app-notes/index.mvp/id/5527. [Accessed 4 February 2019].

[20] J. Fielding, RF design basics, Radio Society of Great Britain, 2007, p. 192.

[21] N. S. Kopeika, J. Rosenenbaum and R. Kastner, "Abnormal glow discharge detection of visible radiation," *Applied Optics,* vol. 15, no. 6, pp. 1610-1615, 1976.

[22] Electron tubes, J C Barton, “Basic physics & statistics of photomultipliers R/P063,” 2011. [Online]. Available: http://et-enterprises.com/images/technical_papers/rp063_basic_physics_statistics_of_PMTS.pdf. [Accessed 4 February 2019].

[23] Infineon Semiconductor, “Bss127 datasheet,” [Online]. Available: https://www.infineon.com/dgdl/Infineon-BSS127-DS-v02_01-EN.pdf?fileId=db3a304330f686060131049ef4883edb. [Accessed 4 February 2019].

[24] Maxim Integrated, “MAX668/669 Datasheet,” [Online]. Available: https://datasheets.maximintegrated.com/en/ds/MAX668-MAX669.pdf. [Accessed 4 February 2019].

[25] Linear technology, “LT3757 datasheet,” [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/3757afe.pdf. [Accessed 4 February 2019].

[26] Maxim Integrated, “MAX1722/MAX1723/ MAX1724 datasheet,” 2017. [Online]. Available: https://datasheets.maximintegrated.com/en/ds/MAX1722-MAX1724.pdf. [Accessed 4 February 2019].

[27] D. A. J. Bell, *Bazinga.PY spectrum processing,* castleford, 2016.

[28] Telequipment, Curve Tracer Type CT71, 1974.

Appendix

Table 6: *Component values for high voltage supply build.*

Identifier	Value	Function
C1,2	100n, 500V, XR7	Multiplier Capacitor
C3-8	47n,500V, XR7	Multiplier Capacitor
C9-14	27n, 500V, XR7	Multiplier Capacitor
C15-18	10n, 500V, XR7	Multiplier Capacitor
C19	10n, 2000V, XR7	Multiplier Capacitor
C20	140pF, 3000V C0G	Phase Lead
C22	1u	Intvcc bypass
C23,25,28,38	10u	Low voltage supply decoupling
R2	1gig-vishay high voltage	High voltage feedback
R3	2.2meg	High voltage feedback
R7	0.001R	Current feedback
R8	43K	Frequency set
D1-D18	BAS21-03W	Multiplier diode
U1	MAX1596	3-5V Charge pump
U2	MAX4130	Opamp
U3	MAX669	Switching regulator
Q1	IRLMA0060	Switching MOSFET
T1	Wurth 750311691	Flyback transformer

***Table 7**: Active divider component values*

Identifier	Value	Function
C4,5,11	10n, 2000V	Supply Bypass/decoupling
R1,2,3,14	50meg	Reference chain
R4	500meg	Reference chain
R5,27,44	0R	
R30-39,26	2meg	Dynode divider
R42	1k	load resistor
C13	2.2pF	Load HF bypass
R46	5K	Coupling termination
R43,45	20k	Inverting amplifier gain set
C3	200p	Inverting amplifier feedback bypass
C12	DNF	
27,26,29,31	10u	Low voltage supply decoupling
U1	LTC6241	Opamp
U4	MCP1700T	linear regulator
U5	MAX1719	inverting charge pump
Q1,2,13	BSS127	MOSFET
D2,3,4	BAS416	protection diode
V1	Hamamatsu R11265u	Photomultiplier

***Table 8**: Multiplier direct component values*

Identifier	Value	Function
U1,2	LT8330	Switching regulator
D1	BAS21-03W	Diode
R1	1gig	feedback resistor
R5	2meg	feedback resistor
R4	900k	feedback resistor
R6	100k	feedback resistor
C15,16	1u	INTVC bypass
C8,9	10u	Low Voltage supply bypass
C47,42,54,55	10u	Low Voltage supply bypass
U5	LTC6261	Opamp
R25	1k	Charge amp feedback
C42	200p	Charge amp feedback
C28,32,27,26	10u	Low Voltage supply bypass
U4	MCP1700T	Linear regulator
U3	MAX1719	Inverting charge pump
V1	R11265u	Photomultiplier
L1-3	82u	Inductor
R3,8,10,12,14,16,18,20,22,24,27,29,31	50R	Dynode damping resistor
R2,7,9,11,13,15,17,19,21,23,26,28,30	1k	Filter resistor
C3,4,5,6	10n, 2000V	High voltage decoupling
d2-11	BAS21U	Multiplier diode
C60,56,51,61,56,57,52	8*10n, 100V	Multiplier Capacitor
C48,44,39,49,45,40	6*10n, 100V	Multiplier Capacitor
C36,33,29,37,34,30	4*10n 100V	Multiplier Capacitor
C23,20,17,24,21,18	2*10n 100V	Multiplier Capacitor
C12,10,1,13,11,2	10n, 100V	Multiplier Capacitor
C51,53,46,41,38,35,31,25,22,19,14,7	10n, 100V	Filter Capacitor

Table 9: *Hybrid concept component values*

Identifier	Value	Function
U2	LTC6240	Opamp
U1	MAX1595	charge pump
U4	MAX4130	Opamp
U3	MAX669	Switching regulator
U6	MCP1700T	Linear regulator
U5	MAX1719	Inverting charge pump
V1	R11265U	Photomultiplier
R5	1K	Load resistor
C21	2.2p	Load HF bypass
C26	10n,2000V	Coupling capacitor
R8	10k	Terminating resistor
R10B	0R	
R7	20k	Rin, inverting amplifier
R3	20k	Rfb, inverting amplifier
C17	100p	Cfb, Inverting amplifier
Q5	Bss123	Switching transistor
D1-16	MMBD3004S	Multiplier diode
C32,33,34,31,43,1,2,3,57,53,54,58,56,55	10u	Low voltage supply decoupling
R14	1gig	Feedback resistor
R17	2meg	Feedback resistor
C19	DNF	
C47	140p	Phase lead feedback capacitor
T1	Wurth 750311691 (modified)	Flyback transformer
Q1-7	PHC2300	PMOS/NMOS pair
C43,40,38,41,39,44	100n	Multiplier capacitor
C36,37,25,30,28,35	47n	Multiplier capacitor
C19,14,12,18,15,20	27n	Multiplier capacitor
C6,10,4,8,7,11	10n	Multiplier capacitor
R1,2,4,9,11,12,13,15,19,22,26	50meg	Reference chain resistor
R1A,4A,9A,12A,22A	2meg	Reference chain resistor