Technology Enhancements for Next Generation Radiation Detectors

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Abstract

Portable radiation detectors are becoming widely used across various industries, particularly the security industry to roll out networks of portable detectors for illicit nuclear material detection. The capabilities of modern detectors have rapidly increased in recent years, largely with the use of advancements in photonics technology. This research program demonstrates two versatile methods of maximising the use of state of the art solid state photo multiplier technology and dual gamma neutron scintillation material, by using low power digital and analogue methods where low power consumption in portable devices is essential for longer operation times between battery charges.

A 25 million sample per second analogue to digital converter system is developed and its performance analysed for methods of gamma event energy capture using a basis of well-established principles used in radiation detection. Its architecture flexibility allows the embedding of different applications, where firstly using it similar to a traditional peak capture circuit is evaluated for gamma energy capture. Secondly, the system is evaluated when using continuous or triggered sampling of a silicon photo multiplier array output both with and without prior stages of analogue signal processing, in order to accurately capture the radiation event signal for digital processing of gamma radiation events. The results show 8-bit peak capture accuracy using generated semi – Gaussian input signals simulating scintillation requirements as fast as using a 1 µS shaping time at 250,000 events per second. The results also show that the ADC system is able to continuously sample a scintillation event, where the captured data is re-plotted for evaluation, where further on device digital processing methods can yield radiometric information.

A low power analogue based circuit is also developed and evaluated for use with the dual gamma neutron scintillator CLLB. Current pulse shape discrimination methods rely on offline processing of pulse datasets to distinguish between a gamma and a neutron event, where the common method used relies on integration windows. This method when implemented in electronic circuitry as a timer controlled gated integrator can prove challenging to design efficiently and can consume excessive amounts of power which is a disadvantage for a battery powered product. The method used in the implemented analogue circuit relies on a combination of amplitude ratio windowing and pulse height discrimination, where successful discrimination between gamma and neutron events was achieved, and where the circuit depending on configuration and application consumes as low as 14 mW of power.

Extract Works and Attendances

A summary paper published in the 2017 XXXIInd General Assembly and Scientific Symposium of the International Union of Radio Science (URSI GASS) and presented as part of the URSI 32nd GASS conference 19th – 25th August 2017 was written on works regarding the development of the 25 MSps ADC System and its use in radiation detection methods researched. The paper titled 'Low Power Embedded Processing of Scintillation Events with Silicon Photo Multipliers' explains the benefits of using the developed folding ADC prototype, with the high data conversion benefits and field upgradable firmware for continuous optimal processing of radiation events in a low power solution, intended for battery operated devices and custom applications.

A conference paper accepted for presentation at the 2nd URSI AT-RASC, Gran Canaria, 28 May – 1 June 2018 by D. W. Upton was contributed to as second author. The paper titled 'Low Power High-Speed Folding ADC based Partial Discharge Sensor for Wireless Fault Detection in Substations' explains the analogue architecture and operation of the 25 MSps ADC system in detail, and how the digital control designed and described in this research is implemented in the ADC prototype with the use of the FPGA application written in VHDL. The paper describes how the originally intended application for the ADC was for monitoring potential discharge radio emission occurrences in power grid substations, where the application is similar to that of the ADCs use in a radiation detection application.

The 1st International SPAD Sensor Workshop ISSW 26th - 28th February 2018 was attended, gaining knowledge of the current and future state of the art in single photon avalanche diode technology, the crucial technology in recent developments in photon capture applications such as in radiation detection and LiDAR imaging.

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1 Introduction

In the environment around us, radiation is emitted from many radioactive sources both natural and manmade. Natural sources such as granite rock, natural radon in the ground, and cosmic radiation largely make up the background radiation levels, varying by geometric location. Manmade sources, consisting of laboratory synthesised radioactive material, and processed material from natural sources also contribute to background levels, largely from use in medical practices.

Radiation sources have uses in everyday life, not only for medical treatments, but for example are also used in industrial instruments for material thickness measurements, tinned food processing and household smoke alarm detectors. Radioactive waste products are also produced in the nuclear power industry, and although usually sealed and safely disposed of, accidental leakage or escape of radioactive materials have contributed to hazardous radiation levels in some places such as Chernobyl and Fukushima.

The manufacture and use of manmade sources and the uses of them are strictly controlled due to the health hazards of excessive radiation exposure to individuals and to the public. Radiation detection devices are essential for discovering and monitoring the potential impacts of radiation exposure, whether it's from an unsafe natural increase in radiation levels, the effects of a nuclear accident or illicit movement and use of a radiation source or radioactive material.

1.1 Radiation Monitoring and Radioactive Source Control

The use and manufacture of radioactive material is increasing as demand of it for its uses increases in society, therefore the control of the increasing amount of radioactive source material is seen as an ever increasing challenge for security services. Some radioactive sources are more controlled than others, typically due to the health hazard the material presents from its type, strength and energy of emitted radiation.

The main radiation types are alpha, beta, gamma and neutron, where gamma and neutron radiation are also categorised as uncharged radiation. Uncharged radiation can travel large distances compared to alpha and beta radiation due to its higher penetration energy, therefore its detection can also be achieved from a distance. Gamma radioactive sources will emit gamma radiation with specific gamma energies depending on the decay of the radioactive isotopes in the material. When using gamma spectroscopy, these energies can be identified in the yielded gamma spectrum and matched to the known gamma emissions of radioactive isotopes, where the isotope can then be identified. Figure 1-1 shows a typical collected spectrum showing energies consistent with the identification of the isotope caesium 137 (Cs137).

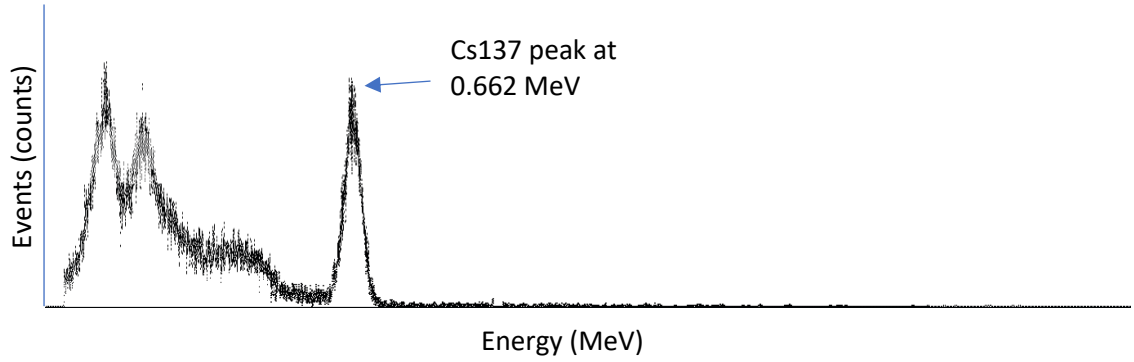

Figure 1-1 A typical Cs137 spectrum showing energy peak of 0.662 MeV for the Cs137 radioactive isotope.

Source control is therefore made more complex by not only having to monitor for unsafe radiation levels but also to identify the radiation sources detected to evaluate the safety of the immediate environment. An example of this would be a medical patient that has undergone recent treatment with the use of a medical radioactive material, would then be emitting radiation with the energies of the associated isotope used in the medical treatment. As a public safety concern, medical sources and the radiation exposure is strictly controlled so a prolonged exposure would not increase any risk to health. The detection of radioactive waste in a city centre however would cause a safety concern if detected with any exposure level, and the necessary security actions can then be taken.

The development of technology in radiation detection devices, and the increased requirement for detection devices is pushing development of mass market, particularly pocket sized, hand held portable radiation detection and monitoring devices in the security industry.

1.2 Radiation Safety and Monitoring Systems

Currently, a large amount of radiation detection for security is used at transportation hubs, particularly for goods scanning to detect any radioactive contaminates, or undocumented transportation of radioactive material that could be used for illicit purposes if its intended destination is reached. Often called portal screening, large installations built to scan shipping containers or lorries in bulk whilst moving through, where an example is shown in Figure 1-2.

Figure 1-2 Example of a lorry radiation screening portal (Shanghai Eastimage Equipment Co Ltd, 2016).

Whilst these solutions are suitable for large scale detection, the technology is impractical for densely populated city centres for example and is far from a portable solution.

Traditional portable detection devices are often heavy and do not meet in the industry demands of the pocket sized, hand held device. This is largely due to the radiation detection method employed in the device, where the use of Geiger Muller tubes or the use of photo multiplier tubes (PMTs) with scintillator material restricted how small such a device could be. Another issue is that the traditional detectors used require the generation of high voltage, particularly for PMTs where the operation voltage required can be over 1000 V, thus the power demands often dictated larger batteries.

Scintillation is the process of photon emission upon radiation interaction in specified scintillator material where it can then be used to detect a chosen type of radiation. Portable devices already typically use a Caesium Iodide crystal as a gamma scintillator, and Boron can be used as a neutron scintillator, both then implemented as two discrete gamma and neutron detector modules. Radiation devices that use the method of scintillation have benefited from recent advances in silicon photomultiplier (SiPM) technology which achieves single photon detection from a component as small as 1x1 mm and only requiring a relatively low operation bias voltage of between 30 V and 60 V. The SiPM technology removes both the requirement of the use of large PMT detectors and the associated power consuming electronics. This then has allowed the use of smaller batteries, in turn leading to smaller, more power efficient portable radiation detector devices where the latest portable detectors can achieve operating power consumptions as low as 300 mW, such as the Kromek D3S, shown in Figure 1-3.

Figure 1-3 The Kromek hand held D3S gamma and neutron detector (Kromek Ltd, 2016).

The Defence Advanced Research Projects Agency (DARPA) aims to use a wide network of portable radiation detection devices carried by already mobile people such as police officers and fire crews to monitor radiation, particularly in the city centres. By processing the accumulated spectra data from all the detector devices through internet based cloud computing methods, DARPA aims to use a live heat map as shown in Figure 1-4, to visually identify the radiation level, where the system can send the necessary alerts depending on the automated detection and identification of a potentially illicit radioactive material (DARPA, 2015).

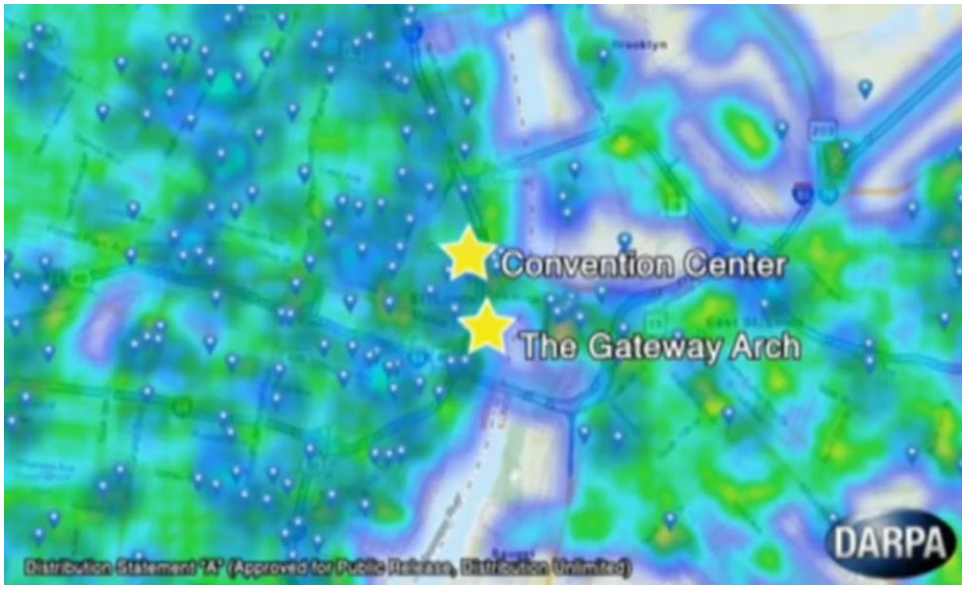

Figure 1-4 Simulated heat map showing radiation levels monitored by a network of portable detectors in a city (DARPA, 2015).

1.3 Research Aims and Objectives

The requirements from industry applications is for the next generation of uncharged radiation detection devices to be smaller in size and have a longer operational time between battery replacement or charge. By exploiting the latest advances in SiPM technology and new state of the art scintillation material, which scintillates upon gamma and neutron interaction, detector sizes can

potentially be reduced by a factor of two, as currently separate gamma and neutron modules can be combined. To be able to exploit this however, the electronic circuitry must not only be able to accurately process the gamma spectroscopy information, but accurately distinguish between a gamma and neutron event whilst achieving a high operational power efficiency. The developed circuitry must also be scalable to match the specified scintillator capability, where some applications require the processing of up to 100,000 detected radiation events per second for extreme emergency situations.

The research objectives were as follows:

- Evaluate the existing technology available for radiation detection using scintillators and SiPM technology for gamma and neutron detection.
- Determine key technology requirements for the use of scintillators and SiPMs, as well as gamma spectroscopy and gamma neutron discrimination.
- Design and implement detection circuitry and relevant processing techniques that can then allow the implementation of low power, compact size gamma spectroscopy applications and provide gamma neutron discrimination.
- Deliver and evaluate prototype systems using the developed circuitry that can provide accurate detection of radiation events through the use of scintillators and the use of test radiation sources.

1.4 Research Structure and Methodology

The following method was used to achieve the objectives set out in section 1.3, where each point then has a summary of the work undertaken and the key research contributions made to the research aims.

- Complete a literature review, covering the principals of radiation detection via the scintillation method. Further include an investigation of existing pulse shape discrimination methods based on the current state of the art scintillation technology. Add to the literature review an investigation on the latest SiPM technology, and commonly used electronic processing circuitry for radiation event detection devices.

Chapter two in this research establishes the foundation technology that is commonly used for radiation detection, including for use in modern portable devices. The chapter evaluates how the radiation events are detected and the importance of capturing the event signal characteristics, of which the subsequent circuit design proposed by this research uses as the basis for the novel enhancements that allow low power gamma neutron discrimination and gamma spectroscopy.

- Propose, design and test a flexible and power efficient electronics processing circuitry solution for use with a scintillator given the 100,000 event rate requirement, including the ability to be able to use the latest combined gamma neutron scintillators.

Chapter three in this research explains how using a state of the art analogue to digital converter (ADC) and the developed novel digital processing through the use of a Field Programmable Gate Array (FPGA) can eliminate the use of some of the traditional radiation event signal processing circuitry. The implementation of the designed system, including the constructed VHDL processing methods shows that the radiation event signal can be accurately reconstructed digitally such as to acquire the characteristics required for gamma spectroscopy and gamma neutron discrimination, with an efficient power consumption vs circuit performance advantage over traditional systems.

- Further propose, design and test an optimised solution for dual gamma neutron scintillators, where the emphasis is on size reduction and power efficiency.

Chapter four in this research details a novel method of gamma neutron discrimination whilst achieving low power operation, drawing particular reference to the innovative window generation circuit. This is developed and implemented in circuitry for the system gamma neutron discrimination performance to be evaluated, yielding a system figure of merit (FOM) of 1.68 whilst consuming less than 15 mW of power using the first prototype. Through further system optimisations and further adding low power optimised traditional circuitry for gamma spectroscopy, the final circuit design achieves the objectives with the FOM of 1.68 whilst consuming as lower power as 14 mW.

- Conclude information on the design methods and the tested solution’s performance for use in portable radiation detection devices, also providing a future technology outlook.

The conclusion in chapter five highlights the key detection technology enhancements of the research and concludes on the designed systems effectiveness for their use in portable radiation detectors. A future outlook on radiation detector technology is also summarised.

2 Literature Review

For the purposes of radiation detection in portable devices, it is important to understand the front-end detection process, to determine the existing analogue signal processing methods are employed, and how the scintillation event characteristics translate to gamma energy information for gamma isotope identification, and neutron detection. This will provide a written overview of radiation detection from first principals.

2.1 Scintillation overview

Using scintillation as a method of detecting ionizing radiation is a well-established process used in many applications, where different scintillating material is selected depending on the type of radiation that is to be detected, and the photon to electrical signal conversion method that is intended for use in the application. (Knoll G. F., Scintillation Detector Principles, 1999). A simplified diagram of the process is shown in Figure 2-1.

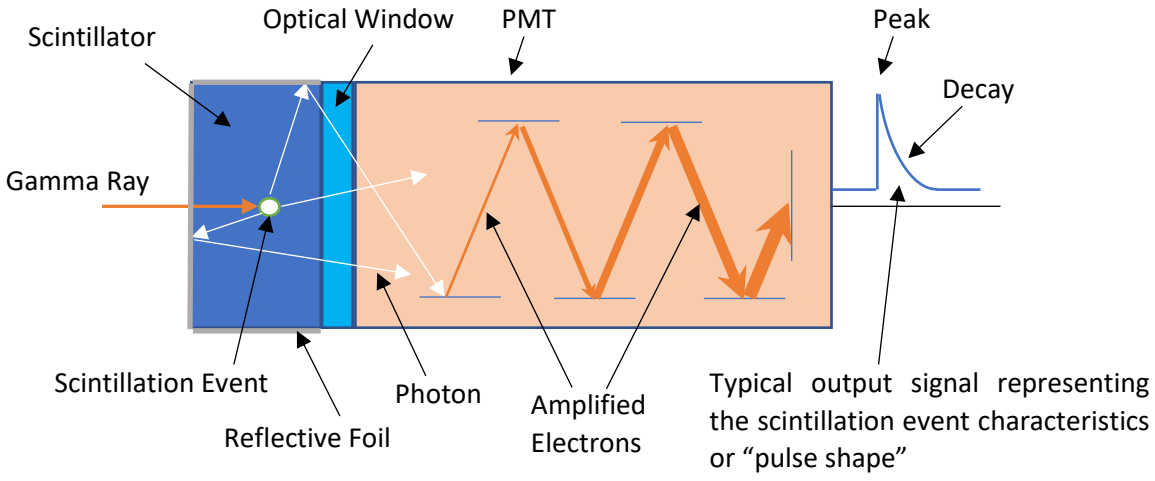

Figure 2-1 Diagram to show a gamma ray interaction with a scintillator and the photon detection method used.

The selection of the scintillation material is normally based on the efficiency of it converting the kinetic energy of the radiation particle in to photons, linearly over the energy range of interest; typically measured in keV or MeV. The material must also have suitable luminescence and optical properties, where the wavelength and the pulse shape of the emitted photons matches the detection capabilities of the sensor in the application, typically a photo multiplier tube (PMT) or photodiode based component. (Knoll G. F., Scintillation Detector Principles, 1999). The use of the photon sensor allows the allows conversion of the emitted photons from the scintillation event to be converted into an electrical current output, which can then be processed by the detector electronics.

Focusing on gamma radiation detection; in the year 1948 Robert Hofstadter showed that an inorganic scintillator composed of sodium iodide, with a trace of thallium iodide used as an activator yielded a significant quantity of emitted photons upon radiation interaction. The process of scintillation with most inorganic materials is the same, ionising radiation interacts with the scintillator crystal material and excites electrons, causing them to rise from the valance band in the material atomic structure, to the conduction band. As this leaves behind an electron hole, the return of the electron causes the emission of a photon. Since the gap width between the valance band and the conduction band in a pure crystal material such as sodium iodide on its own is too great, the resulting photon emission has a high energy that is not easily detected. (Knoll G. F., 1999).

The use the activator, thallium iodide in this case allows for an increased probability of photon emission with a lower energy and hence a wavelength that is easier to detect. This process can be seen in Figure 2-2. Efficiencies and decay characteristics of these electron interactions, and therefore the photon yield and photon emission pulse shapes upon scintillation are different for each material. Gamma radiation passing through the crystal will excite many electrons proportional to the kinetic energy of the radiation absorbed, and since different radioactive isotopes emit gamma energies that can identify the isotope, this process forms the basis of gamma spectroscopy applications (Pursley, J & Michigan State University, 2001).

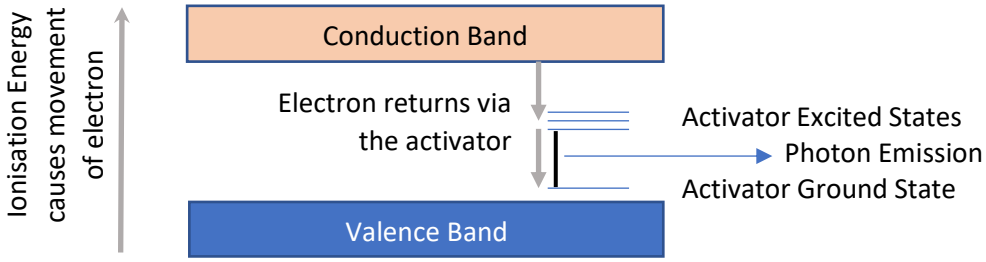

Figure 2-2 Diagram showing electron movement upon ionization event in an activator doped scintillator.

As well as a large photon yield, sodium iodide with thallium activator, NaI(Tl), exhibits low non-linearity for photon output versus the gamma radiation absorbed, at 38000 photons per MeV. The wavelength of the emitted photons upon scintillation for NaI(Ti) is 415 nm, and is compatible with common detector sensitivities and also, has a decay time characteristic of 230 nS. Additionally, NaI(Ti) is relatively easy to produce, compared to that of organic scintillator alternatives, and can be scaled to different shapes and sizes. Considerations must be made when using NaI(Tl) however, as the crystal is hydroscopic, where atmosphere moisture can destroy the crystal and hence must be sealed in a protective encapsulation with a window often referred to as being canned. NaI(Tl) crystals also considered to be brittle and therefore must be handled with care, making it unsuitable for some harsh

applications where exposure to forceful impacts could damage the crystal. (Knoll G. F., Scintillation Detector Principles, 1999).

Although NaI(Tl), is still commonly used in applications, Caesium Iodide with thallium activator, CsI(Tl), is also commonly used in application where crystal robustness is needed as it is less brittle than NaI(Tl), and where performance to volume is important. CsI(Tl) yields 65000 photons per MeV, higher than that of NaI(Tl), however the wavelength of the photon emissions is at nominally 550 nm and is therefore further away from the peak sensitivity of some detector devices such as PMTs, compared to that of NAI(Tl). The photon emission wavelength of a selection of inorganic scintillators showing spectral sensitivity and wavelength can be seen in Figure 2-3. The total time of the pulse generated upon a scintillon event in CsI(TI) is also longer than NaI(Ti) with two time components to its scintillation decay process at 680 nS and 3340 nS, making the scintillation event time longer and CsI(Tl) less suitable to higher radiation count rate applications (Saint-Gobain Crystals, 2017). The entirety of the pulse generated form the scintillation event represents the total energy deposited into the scintillator crystal from the gamma radiation, and therefore the detector system must be capable of capturing the pulse output height and shape accurately to accurately process the energy deposited from the radiation in the scintillation event (Knoll G. F., 1999).

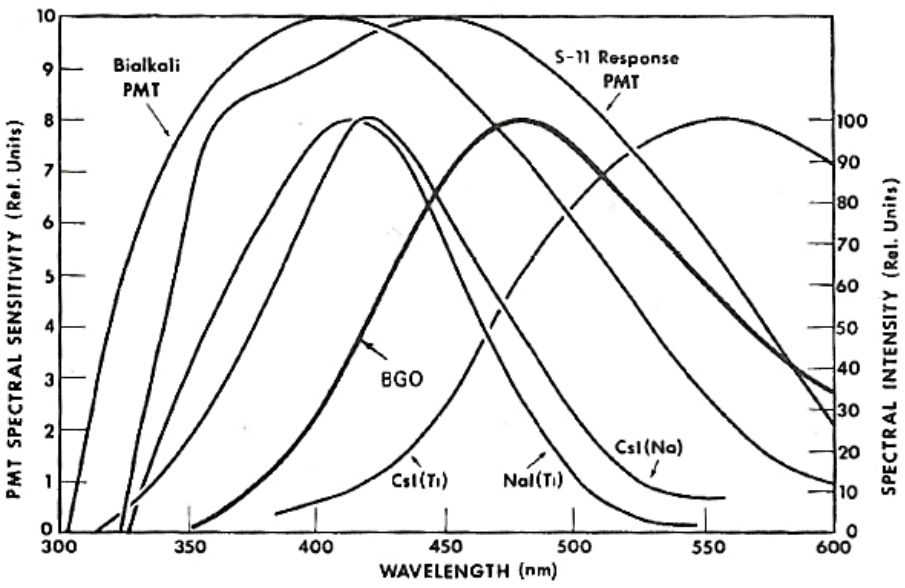

Figure 2-3 Emission wavelength of selected inorganic scintillators plotted with the response sensitivities of two PMT examples. (Knoll G. F., Scintillation Detector Principles, 1999).

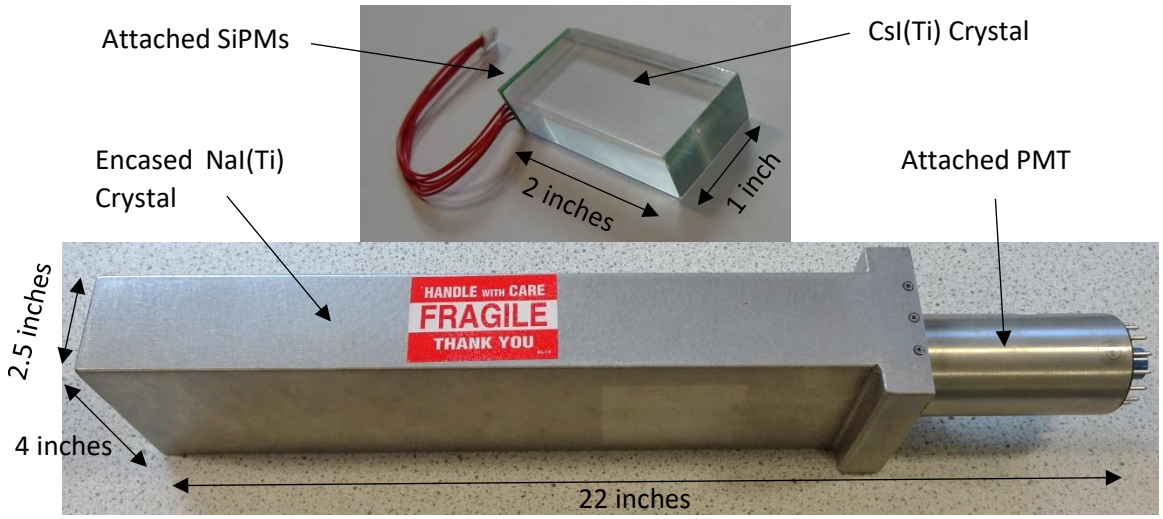

Figure 2-4 CsI(Tl) Crystal with bonded SiPMs on a PCB (Top), Metal encased NaI(Tl) Crystal with attached PMT (Bottom).

2.2 Scintillation for Neutron Detection

Research into neutron detection has increased since a recent global shortage of Helium 3, which was traditionally used for neutron detection. Helium 3 is a by-product of the radioactive decay of tritium of which the United States, a previous supplier of this has ceased production of, as tritium is only made as part of specific nuclear weapons manufacturing methods that are no longer used. (United States Government Accountability Office, 2011).

An alternative method for neutron detection with Helium 3, currently deployed in some portable detectors is to use a lithium-6 fluoride and zinc sulphide phosphor compound, where as part of the thermal neutron interaction with the lithium-6 fluoride an alpha particle is produced. This alpha particle then reacts with the zinc sulphide phosphor compound to emit photons with a wavelength in the region of 450 nm. Zinc sulphide alone can also be used for alpha particle detection (Saint-Gobain Crystals and Detectors, 2002). The photons produced can then be detected using a PMT for example. As these compounds tend to be absorbing to the wavelength of the emitted photons, they are often applied in thin layers to maximise surface area available for interaction with minimal material photon absorption, and a waveguide is then used to channel the photons to the detector. (Southern Scientific Ltd, 2012).

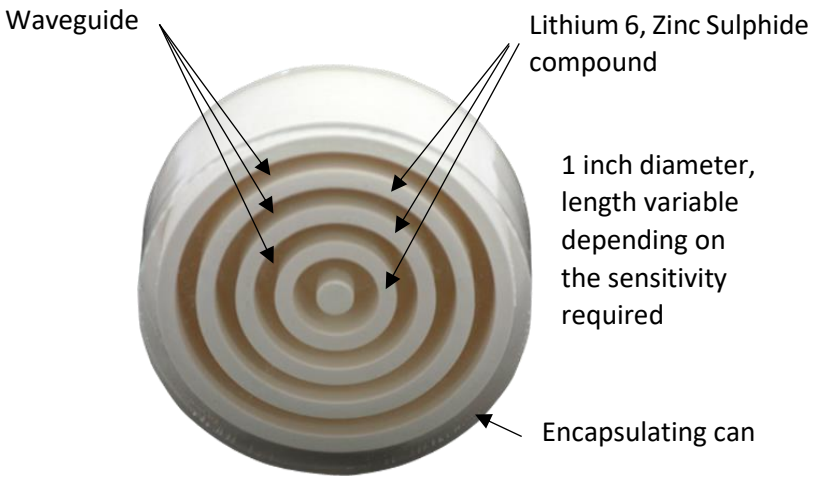

Figure 2-5 Neutron detector, showing thin Lithium Zinc Sulphide layers and wave guide layers example. (Southern Scientific Ltd, 2012).

Neutrons are primarily categorised in to thermal (or slow) neutrons, or fast neutrons depending on the neutron kinetic energy. Thermal neutrons typically possess energies of fractions of, or a few eV, where fast neutrons can possess energies in to the MeV range. Since the energy spectrum of thermal neutrons is so narrow, many detectors count thermal neutrons using the basis of the method described above, rather than capture the associated energy. Fast neutron detection can be achieved by typically employing hydrogenous or carbon based neutron moderators to reduce the kinetic energy to that of a thermal neutron (Saint-Gobain, 2017).

Spectroscopic fast neutron detection can be achieved by employing extra physical processes including elastic or inelastic scattering (Saint-Gobain, 2017). Applications for neutron spectroscopy include spent nuclear reactor fuel identification (Akyurek & Usman, 2015). Spectroscopic alpha particle detection can also be used to identify the source material, however can be challenging as alpha particles are easily absorbed in air and do not penetrate very far through matter. (arpansa, 2017). The detection of a high rate of neutrons would be classed as a hazard for security applications, hence most portable products use a moderator, typically water based, or some plastic based materials to decrease the energy of fast neutrons in to thermal neutrons, and only count the number of neutron interactions, rather than employ more complex spectroscopic processing for neutrons (Knoll G. F., 1999).

2.3 Dual Gamma Neutron Detection Capable Materials

Using the similar scintillation principles as with gamma detection and neutron detection, crystals are emerging onto the market that can scintillate upon both gamma and neutron radiation interaction. Such a material would allow the use of a single detector system yielding both power and size benefits for portable detector products. (Saint-Gobain Crystals, 2017).

One particular crystal material of interest is Cs2LiLaBr6 (CLLB) due to its high scintillation photon output of up to 60000 photons per MeV of radiation energy absorbed, good energy resolution figure relative to other scintillator materials, and photon emission wavelengths that are still compatible with common detection systems. (Mesick, Coupland, & Stonehill, 2016) (Shirwadkar, et al., 2010).

The properties of CLLB that are useful in dual gamma neutron detection is that the scintillation characteristics are different for gamma and neutron events, as well as alpha particle interactions. (Mesick, Coupland, & Stonehill, 2016). The differences can be seen in Figure 2-6.

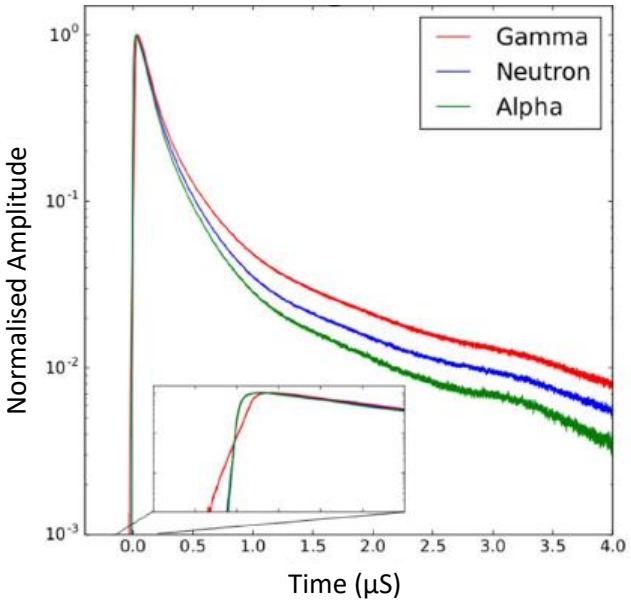

Figure 2-6 Normalised CLLB scintillation average output waveforms for gamma, thermal neutron and alpha particles. (Mesick, Coupland, & Stonehill, 2016).

Another property of CLLB is the photons emitted upon neutron scintillation yield an electron equivalent energy of between 3.03 MeV and 3.2 MeV. Given that the energy ranges of interest in this project is for the identification of sources, with isotope emissions ranging between 60 keV and 3 MeV, there is another possible method of discrimination between gamma and neutron events. This can be seen when comparing gamma and neutron energy information spectroscopically, where Figure 2-7 shows gamma isotopes and neutron energy appearing in a sample spectrum. Both this energy range and the decay time of the photon output pulse are the key discrimination properties that factor in implementing gamma neutron discrimination methods. (Mesick, Coupland, & Stonehill, 2016).

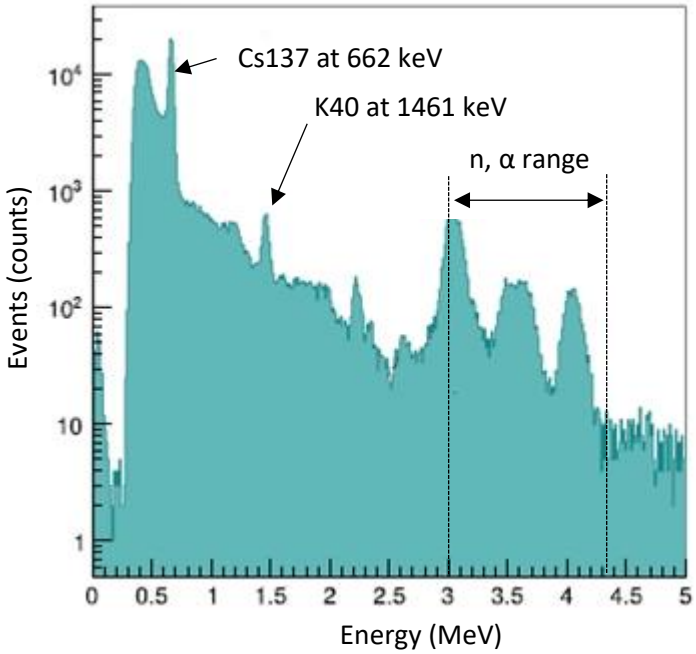

Figure 2-7 An energy spectrum acquired using CLLB exposed to gamma, thermal neutrons and alpha radiation. (Mesick, Coupland, & Stonehill, 2016).

2.4 Discrimination methods

There are multiple methods of discriminating gamma events from neutron events when using dual scintillators such as CLLB. Two main methods of gamma neutron discrimination that are commonly applied are pulse height discrimination (PHD) and pulse shape discrimination (PSD), where PSD methods often yield more distinguishable gamma neutron separation (Glodo, Hawrami, Loef, Shirwadkar, & Shah, 2012). These are applied to the electrical pulse output from the detection of the photons from the scintillation event through a device such as a PMT or photodiode component such as a SiPM.

2.4.1 Pulse Height Discrimination

The method of PHD applied to CLLB is achieved based on identifying the neutron scintillation events where the emitted photons yield an electron equivalent energy of 3.03 MeV to 3.2 MeV, therefore by setting a threshold for any event that occurs over 3 MeV for example, will be deemed as a neutron event assuming no alpha particle detection. This method is however limited in accuracy as photon coupling to the detector is not perfect, and some gamma events can also register above 3 MeV such as cosmic gamma rays. (Mesick, Coupland, & Stonehill, 2016) (Glodo, Hawrami, Loef, Shirwadkar, & Shah, 2012).

2.4.2 Pulse Shape Discrimination

Pulse shape discrimination relies primarily on identifying the difference in the decay characteristic between a gamma and neutron interaction, as shown previously in Figure 2-6. Integral windows are set at two time places where the decay difference is greatest between a gamma and neutron event. The signal present in these windows is then integrated and compared to each other and in some cases, the total length of the pulse. Figure 2-8 shows an example of this for another dual gamma neutron scintillator Cs2LiYBr6:Ce (CLYB). The integration result, which is the discrimination parameter in this method is accumulated over the total number of events in a histogram, used to show the separation of gamma and neutron events. (Glodo, Hawrami, Loef, Shirwadkar, & Shah, 2012).

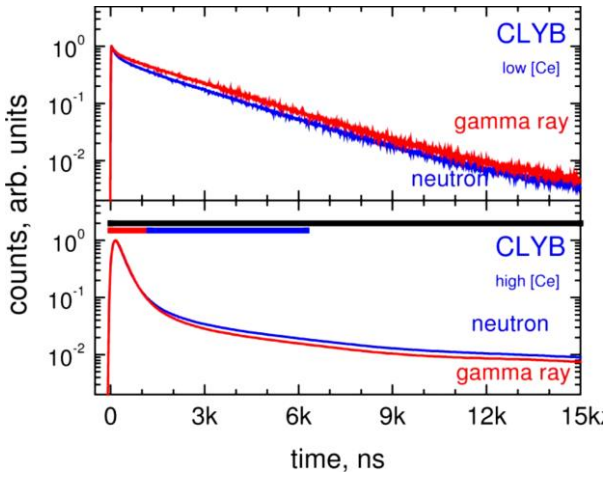

Figure 2-8 Smoothed gamma and neutron scintillation output showing window bars for the window integration periods (Glodo, Hawrami, Loef, Shirwadkar, & Shah, 2012).

Both pulse height and pulse shape discrimination currently rely on digital conversion and processing of continuously sampled input pulses and so typically have to rely on high power components such as fast Analogue to Digital converters or laboratory oscilloscopes capturing the pulse waveforms, for offline pulse shape discrimination processing. Hand held detector products therefore do not yet implement these methods. (Cester, et al., 2014).

2.4.3 Pulse Gradient Detection

A less commonly used method is pulse gradient measurement, where the peak of the scintillation signal is detected, and its amplitude is then measured. The time measured between this and the event signal decay crossing lower threshold voltage, where typically the event detection threshold voltage is used. As both axis parameters are then known, a gradient can be found and is used as the discrimination parameter in this method. In the same way as pulse shape discrimination, these gradient figures accumulated over multiple events are plotted on a histogram, and an FOM calculated

(Saldana & Stemen, 2014). The method is less commonly applied in CLLB applications as the peak to tail differences are minimal, so the discrimination result is poor.

2.4.4 Evaluating Discrimination Methods and Systems

The main calculation used to evaluate the effectiveness of a discrimination system is its figure of merit (FOM), where the greater the figure of merit result, the greater the effectiveness of the system of correctly identifying the occurrence of a gamma or neutron scintillation interaction (Knoll G. F., Radiation Detection and Measurement, 2010). A figure of merit that is greater than 1.5 is generally considered as good in application. Scatter plots as suggested for use with pulse shape discrimination can be used to realise the FOM by gaussian fitting the accumulated gamma and neutron discrimination parameters and applying the FOM calculation. The equation for calculating the FOM when using this method is shown in Equation 2-1.

$$FOM = \frac{Centriod_{gamma} - Centriod_{neutron}}{FWHM_{gamma} + FWHM_{neutron}}$$

Equation 2-1 Figure of Merit Equation used to evaluate the effectiveness of a discrimination system.

A figure of merit of 1 would indicate that a decision threshold between determining whether an event was caused by a gamma or neutron would be hard to implement, as the gamma event and neutron event result regions would be next to each other in a histogram. Less than 1 would indicate discrimination was only partially, or not achieved as the regions overlap.

2.5 Radiation Detection Utilising Silicon Photo Multipliers

Detecting the photons from scintillation caused by ionizing radiation interactions is currently achieved by the well-established use of photon detection components such as PMTs, positive – intrinsic – negative (PIN) photodiodes and standalone avalanche photodiodes (APD). Each of these detection components have advantages, such as single photon sensitive PMT performance, and the low relative operating voltage, cost and size of PIN diodes and APDs. Silicon photo multipliers (SiPM) have been developed with the aim of achieving these characteristics, where the performance of a PMT is achieved using the same size component as many PIN diodes and APDs, ideal for portable devices. (Jackson, O'Neill, Wall, & McGarvey, 2016).

SiPMs are constructed using avalanche photodiodes (APD) that have been specifically fabricated so when biased into Geiger mode become single photon sensitive and referred to as a single photon avalanche diode (SPAD). As well as a SPAD, a quench resistor is connected to the SPAD anode as shown in Figure 2-9(a) to limit the current flow upon photon interaction, and with SensL manufactured SiPMs a fast output capacitor is also connected to the anode to form a microcell. (SensL Technologies Ltd,

2017). The SPAD is operating in Geiger mode when a reverse voltage that is in excess of the breakdown voltage is applied, known as overvoltage. A typical breakdown voltage depends on the fabrication process used when manufacturing the SiPM so varies between manufacturers however, 25 V is a typical breakdown voltage for a SensL SiPM, and an overvoltage of typically between 1 V and 5 V is applied. (Jackson, O'Neill, Wall, & McGarvey, 2016).

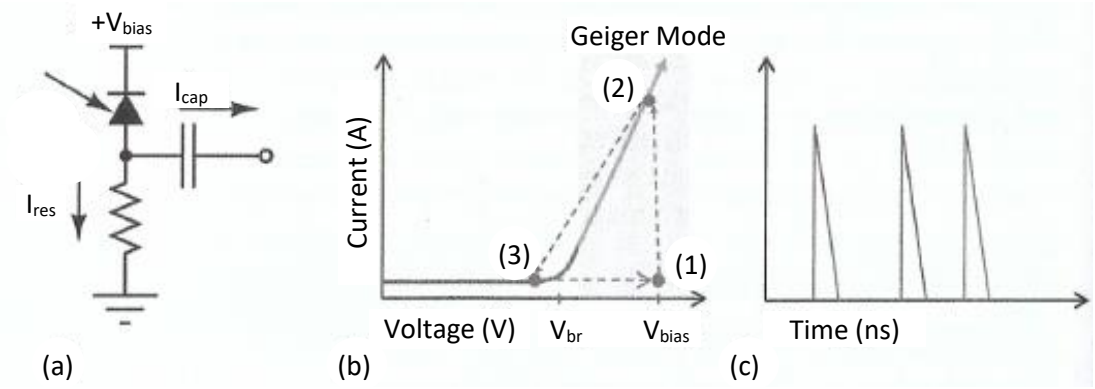

Figure 2-9 APD operation overview showing (a) A single microcell configuration, (b) states of a microcell upon photon interaction shown on a current vs voltage graph, (c) Output voltage pulses using a load resistor (Jackson, O'Neill, Wall, & McGarvey, 2016).

For comparison, Hamamatsu SiPMs typically have a breakdown voltage of between 50 V and 70 V, and a 10 V overvoltage range can then be applied. The amount of overvoltage applied determines how much gain is achieved from the SiPM, which is typically a magnitude of between 10^5 and 10^7 charge carriers generated in the gain region of each SPAD, for the charge carrier created by the initial photon interaction. (Hamamatsu Photonics, 2017).

The simplified operation of a single microcell upon photon interaction can be seen in Figure 2-9(b), where biased using an external voltage source in overvoltage operation with no current flow, the breakdown of the SPAD and generation of charge carriers causes current to immediately flow and after the step change reactance through the capacitor, which is the desired event signal, the voltage over the quench resistor starts to rise, seen at point 2 in Figure 2-9(b). This allows the microcell to recover by causing the voltage over the SPAD to lower to below the SPAD breakdown voltage. at which point the current no longer flows and can be seen at point 3 in Figure 2-9(b). The overvoltage is then restored over the SPAD given there is no longer a voltage drop caused by current flow through the quench resistor, returning to point 1 in Figure 2-9(b), and the microcell is ready for the next photon interaction. Using a load resistor to convert current to voltage, a typical output voltage from a microcell (from cathode to anode) upon photon interaction can be seen in Figure 2-9(c), where this faster initial current flow causes the faster rising edge, and the slower recovery resulting in a slower falling edge of the voltage output pulse. (Jackson, O'Neill, Wall, & McGarvey, 2016).

Arrays of tightly packed microcells are then fabricated onto a single SiPM component to allow the detection of multiple photons, demonstrated by the schematic shown in Figure 2-10, where the outputs of many microcells are arranged in parallel to sum the outputs together. Manufactured SiPMs however, will typically have high hundreds or thousands of microcells depending on manufacturer and size variant. Microcell sizes again depend on variant but are typically selectable from arrays populated with 10 µm microcells, to arrays populated with 50 µm microcells. (SensL Technologies Ltd, 2017).

The array of microcells enables the detection of multiple photons arriving at the same time within the SiPM surface area. As each microcell is single photon sensitive it will breakdown regardless of how many photons interact with it, however other microcells on the SiPM will still be ready for photon interaction. Given there is also a recovery time for each microcell, photon interaction may also be missed by a microcell as it had not yet recovered, and this is known as deadtime. (Hamamatsu Photonics, 2017).

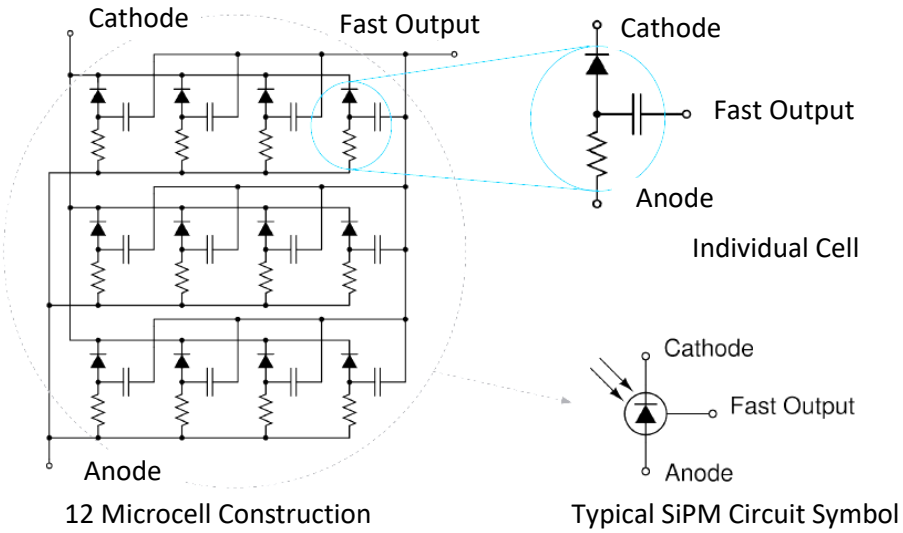

Figure 2-10 SiPM construction example using 12 microcells (SensL Technologies Ltd, 2017).

To capture the scintillation photon output using a SiPM, the photon emission wavelength must fall into the optimal sensitivity region of the SiPM, where ideally the peak wavelength of the emitted photons should match the peak sensitivity wavelength of the SiPM. This sensitivity can be selected from variants of SiPMs from different manufactures, to match for the intended scintillation crystal, or other photon source to be used in the application. The sensitivity for a SensL 30035 SiPM can be seen in Figure 2-11, where the peak sensitivity at a wavelength of 420 nm can be seen quoted in terms of Photon Detection Efficiency (PDE). The difference in gain that can be achieved by adjusting the level of overvoltage applied to the SiPM bias voltage can also be seen. (Jackson, O'Neill, Wall, & McGarvey, 2016). PDE is also affected by the fill factor of a microcell array, as only the silicon area containing the

SPAD is photon sensitive, leaving non photon sensitive area used for the quench resistor, array connections, and the fast output capacitor where applicable. Given that microcells are available in different geometrical sizes each with a proportion of sensitive area, the more microcells in an array, a lower fill factor is achieved. (Hamamatsu Photonics, 2017).

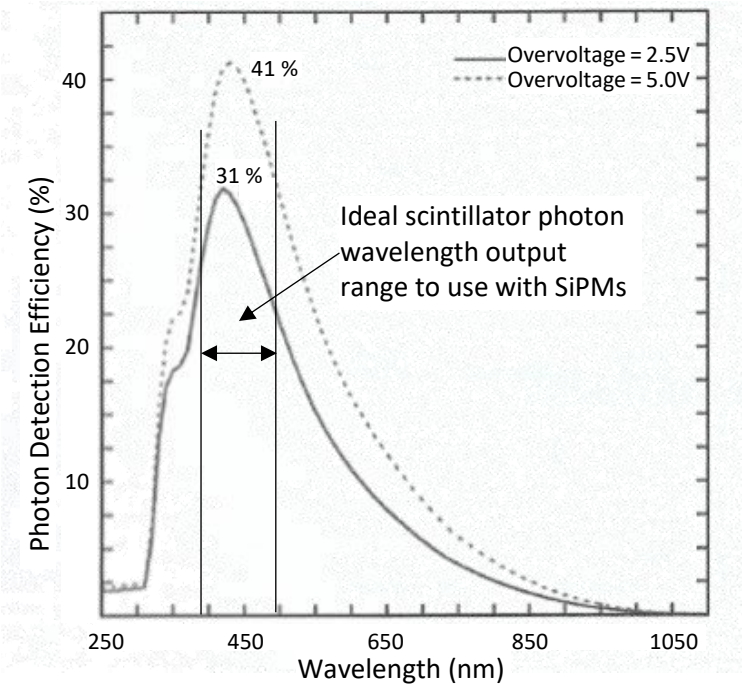

Figure 2-11 Graph showing optimal wavelength for photon detection efficiency at over-voltages of 2.5 V and 5.0 V (Jackson, O'Neill, Wall, & McGarvey, 2016).

When using SiPMs for scintillation detection, it is common to tile individual SiPM components, connecting them in parallel, in order to maximise photon collection from a larger scintillation crystal. Care must be taken when tiling SiPMs to minimise the gap between them, in order to reduce the probability of missing a photon. Packages for SiPMs vary between manufacturer, where the package used may have an effect on the total sensitive area of the SiPM, and the refractive index of the package material selected will also influence the total system efficiency of detecting photon emissions. Matching this refractive index of the SiPM packaging is often considered along with refractive index of the scintillator crystal, and any optical coupling required to bond the SiPM array to the crystal, such as epoxy. It is also common to wrap or encapsulate crystals in reflective coating, with the aim of eventually reflecting the photons towards the SiPM array. Encapsulation is also necessary in some cases due to the hydroscopic properties of the crystal, such as with an NaI(Ti) crystal. (Jackson, O'Neill, Wall, & McGarvey, 2016).

2.6 Scintillation Event Processing Circuitry using SiPMs

Processing the electrical pulse output from a SiPM upon a scintillation event can be implemented using both analogue and digital circuitry based techniques, whilst implementing varying methods of digitising the data for user readout applications. The complexity of the system that is implemented largely relies on the amount, and type of information that is required from the scintillation process, for example pulse height, pulse shape or both. The system shown in Figure 2-12 is a typical detector system to process electrical signals generated from the SiPM output upon a photon detection from a scintillator.

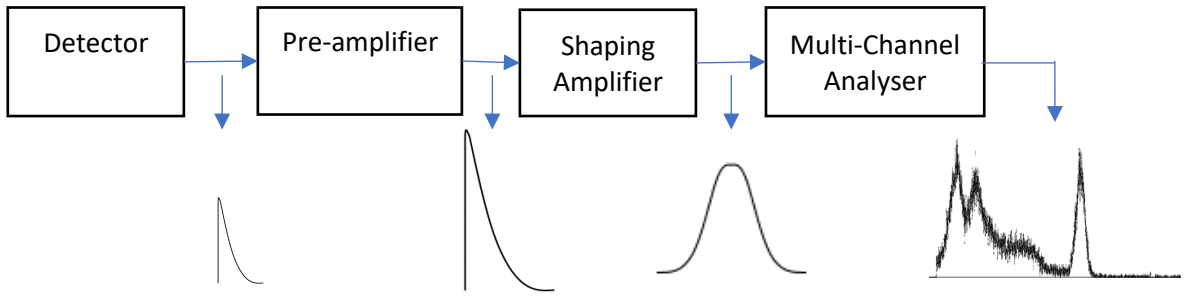

Figure 2-12 Diagram of a typical detector system, showing the typical electrical signal output at each stage.

The detector output signal in Figure 2-12 is a typical SiPM output signal upon photon detection from scintillation. The characteristics of the signal are largely delectated by the scintillator used as discussed in section 2.1, with some impact from parasitic capacitance and inductance in the SiPM and connections to it. Low parasitic capacitance is desired for use with faster scintillators applicable for processing of high event rates. Since the typical SiPM output is of the order of 100 mV, a pre-amplifier is used, with a gain set to achieve the scaling of the radiation energy range within the shaper input voltage limits. (Knoll G. F., 1999).

The function of the shaper in a typical detector system is to provide two functions, to integrate the input pulse coming from the amplified SiPM signal, and to define the event within the set shaping time. Since the SiPM pulse shape, with the fast rise time and slower decay tail represents the total energy deposited in the scintillation event, by integrating this signal the scintillation event can be represented by the maximum amplitude of the resulting integration using the shaped pulse. (Noulis, 2016).

An option for signal shaping is to use low pass, passive resistor – capacitor networks (RC) filters provide an integration function, forming the basis of the implemented shaping filter. The required filter response is referred to as the required shaping time, where the time at which the peak amplitude of the shaped signal is achieved is the end time of the input signal, and hence the end time of the required integration of the scintillation event. This can be achieved as an RC filter preforms as an integrator

within the limits of the time constant set by the resistor and capacitor components. (Knoll G. F., Pulse Shape, 1999). In practice, the shaping time is adjusted to that the maximum signal to noise ratio is achieved, as integrating to the end of the event pulse results in integrating further in to the smaller tail signal where signal noise is more dominant. (Abbene, Gerardi, & Principato, 2016). The shaping time of the implemented RC filter, assuming the same RC stages are repeated, is given by Equation 2-2, where τ_s is the shaping time, *n* is the number of RC networks or the order of the combined filter, R is the resistance value of each resistor, and C is the capacitance value for each capacitor. (Noulis, 2016).

$$\tau_s = n\mathrm{RC}$$

Equation 2-2 - Shaping time equation (Noulis, 2016).

An issue for pulse detection applications is that utilising a single RC filter stage yields undesirably long fall time which results in a system that has a limited maximum count rate throughput. As further RC networks are added to the shaping filter, where the time constants are optimised the output response of the filter tends further towards that of a Gaussian shaped output, with close to symmetrical rise and fall shaping times, ideal for improving the ability of a system to process a higher count rate, as the long fall time of the RC filter is reduced. (Knoll G. F., Pulse Shape, 1999).

A further issue when using passive RC networks in pulse detection is the loss of signal amplitude at the output of the filter of each filter stage, resulting in a reduced signal to noise ratio (SNR) and ultimately a degradation in spectrum data. Active filter topologies that implement operational amplifiers to add gain after each RC stage, as shown in Figure 2-13, reduces the loss of signal amplitude, and allows an improved SNR when capturing the peak amplitude of the shaped pulse. (Noulis, 2016).

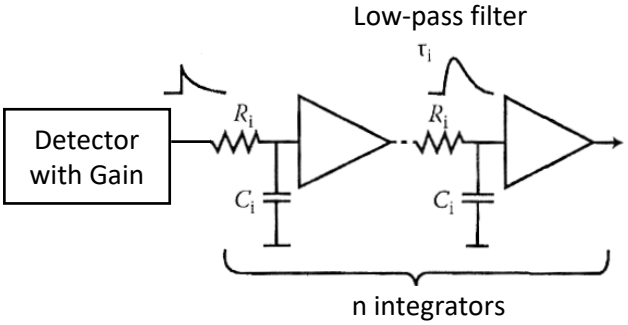

Figure 2-13 - Diagram showing basic structure of an $(RC)^n$ second order shaping filter with gain stages (Noulis, 2016).

A more efficient solution over many RC filter and amplifier networks is to use a Sallen and Key topology filter to implement a semi-gaussian shaping element, as a higher order of filter can still be achieved to yield a near ideal gaussian response, with only using 1 amplifier for every 2 filter orders. (Jianbin, Wei, Fang, Yi , & Xing , 2011).

The function of the Multi-Channel Analyser (MCA) is to measure the amplitude of the shaped pulse converting this to digital data used to form the spectroscopic information. For the MCA to operate, a trigger using a threshold voltage comparator is typically employed to detect the rising edge of the incoming event signal. The voltage threshold is set above any signal noise, thus not to trigger when events are not present, as shown in Figure 2-14. The comparator logic output then triggers the internal analogue to digital conversion of the shaped pulse height. (Abbene, Gerardi, & Principato, 2016).

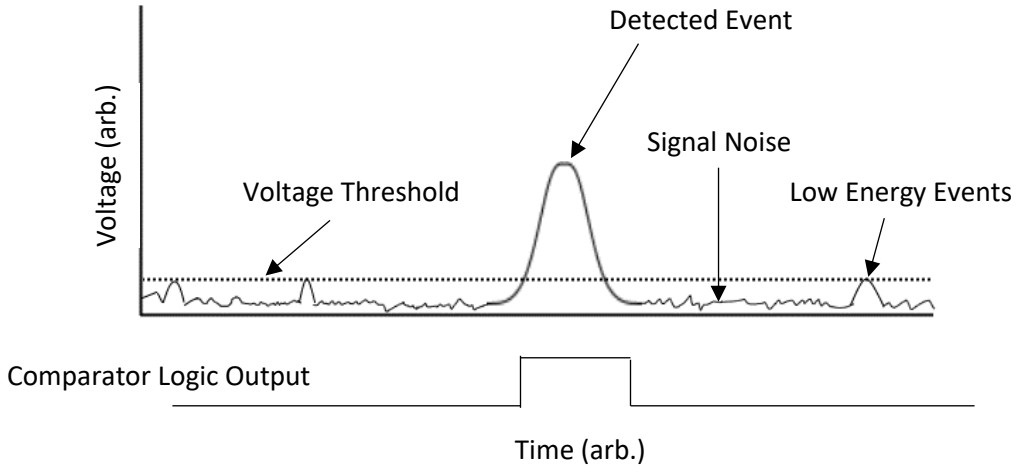

Figure 2-14 Operation of a threshold comparator used to detect events.

An MCA typically has customisable user settings that enable the use of many shaping times, adjust trigger thresholds and select conversion methods for testing many pulsed signal applications including radiation detection. Since an MCA is typically a bench top device, for portable devices the use of an MCA would not be a practical solution however, an electronic circuitry method exists that is used to capture the peak amplitude of a signal.

2.7 Circuitry used for Peak Amplitude Capture

A peak capture circuit in a basic form, a diode and capacitor connected as shown in Figure 2-15 can be used to hold the highest amplitude of a signal presented at the anode of the diode. As voltage at Vin rises, the voltage over the capacitor also rises, matching the voltage of the input signal less the forward voltage drop over the diode. As the diode prevents the discharge of the capacitor, and hence in an ideal case no current path for the capacitor to discharge, in an ideal case with no circuit losses the largest amplitude applied at Vin is held at Vout. (Harowitz & Hill, 2015).

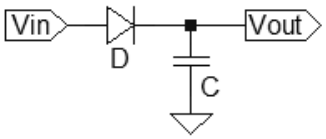

Figure 2-15 Basic peak detector using passive components.

Since the voltage drop of the diode and any current leakage through the capacitor would lower the held voltage relative to the input, as well as the difficulty of digitising the voltage held on the capacitor without discharging the capacitor, as current into an ADC for example, the diode – capacitor circuit is only an ideal case circuit. (Harowitz & Hill, 2015).

A practical implementation of the peak capture circuit that overcomes these diode and output issues is shown in Figure 2-16. The operation of the circuit is as such that the Vout will always update to the peak amplitude voltage at the Vin, until switch SW is closed to reset the held peak voltage. The function of the second amplifier is to buffer the voltage held over the peak hold capacitor C1, and as such its output will always equal this voltage. Given the issues described with acquiring the peak voltage from the hold capacitor in Figure 2-15, the input to this amplifier must be of high enough impedance as to not discharge the hold capacitor. The function of the first amplifier is compare the voltage at Vin to the voltage that is held over C1. If the voltage at Vin is larger than the held voltage over C1, obtained through feedback resistor R1 from the output amplifier, the input amplifier drives D2 until the voltage at Vin is equal to the voltage over C1, and hence Vout. The voltage output of the input amplifier is always a forward diode voltage drop due to D2, above that of the voltage over C1, and since the amplifier aims to match the voltage of its negative input with its positive input, D1 remains reversed biased. When the voltage at Vin is lower than the held voltage, D2 prevents the modification of the held voltage by the input amplifier, however the input amplifier output voltage is now a diode forward voltage drop below Vin to allow feedback through D1, which becomes forward biased, and a voltage drop over R1 forms from the held voltage at Vout. Closing switch SW then discharges C1, allowing the detection of further peak voltages in the incoming signal, and in practice can be implemented using a MOSFET or analogue switch component, using the switch enable signal for its control. (Pallas-Areny & Webster, 1999).

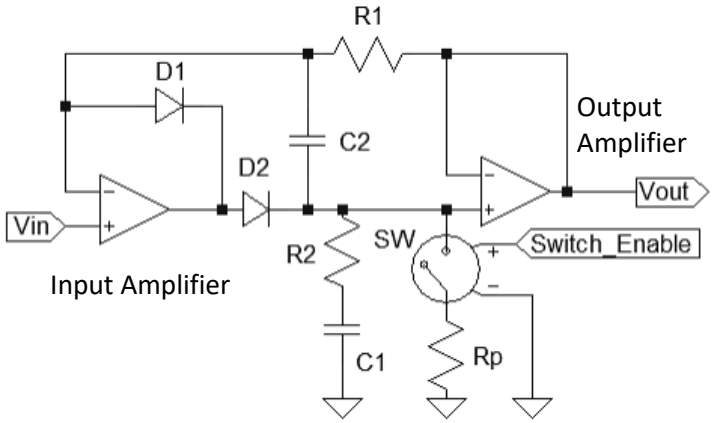

Figure 2-16 Practical implantation of a peak detector circuit based on op-amps and diodes (Pallas-Areny & Webster, 1999).

With this peak capture circuit, issues with current surges when charging the hold capacitor are prevented by the use of resistor R2 and capacitor C2 as in Figure 2-16, where current surge in to the hold capacitor and the response of the diodes are optimised for peak detect accuracy based on the properties, such as slew rate of the amplifiers used, and properties of the diodes used. Resistor Rp is to protect against a current surge through the switch when the hold capacitor is discharged upon reset. (Pallas-Areny & Webster, 1999). The operation of the circuit is not perfect however, due to the input bias current of the output amplifier and the diode leakage and capacitor leakage causing the peak hold voltage to decrease over time. The longer the peak value is to be held in 'hold' mode, the more these factors must be considered when designing the peak detect circuit. (Harowitz & Hill, 2015).

The oscilloscope trace in Figure 2-17 shows the instantaneous signals present from a typical gamma radiation detector, relating to the process shown in Figure 2-12.

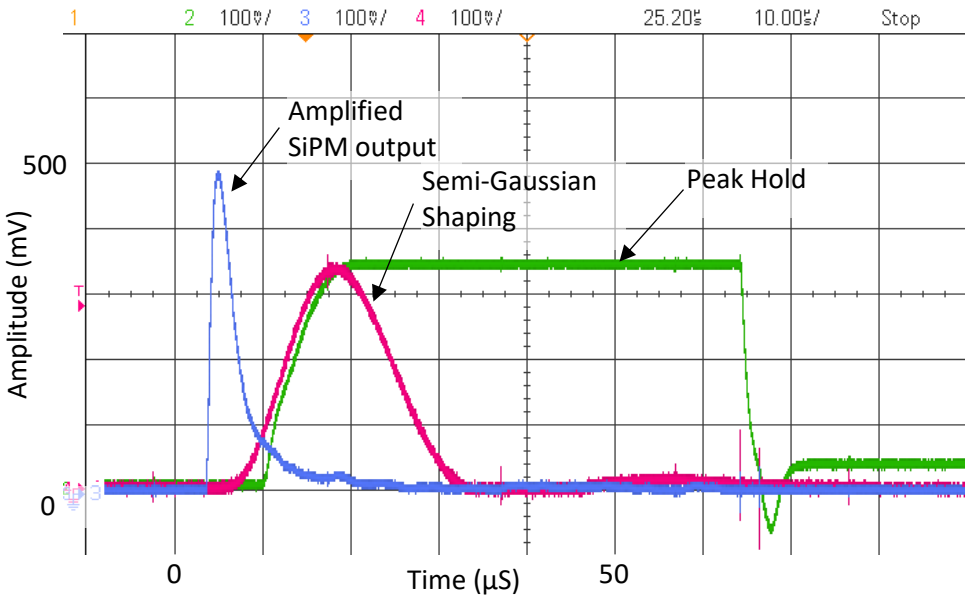

Figure 2-17 Oscilloscope trace of the analogue signals in a gamma detector, showing the amplified SiPM output (blue), the shaping stage output (pink) and the peak capture and hold (green).

An ADC is typically used to sample the peak hold voltage, where the peak capture circuit is required to hold the peak voltage accurately for the duration of the conversion time of the ADC used. The issues already mentioned which reduce the accuracy of the peak voltage will often contribute to specifying an ADC with a faster conversion time than when the peak hold voltage droop becomes too significant, however these often compromise on factors such as resolution, conversion time, power consumption and component cost. The conversion time of the ADC selected also directly impacts the system 'dead time', being the time that the system is busy processing the current radiation event, as the longer the time taken for the ADC conversion the more likely another radiation event will occur, thus compromising both events. (Knoll G. F., Multichannel Pulse Analysis, 1999). An example of the ADC properties compromise would be that a flash ADC would yield fast conversion times, however with increasing resolution a flash ADC typically has higher power consumption and have a higher component cost. A further example is the use of a Successive Approximation ADC which typically yield faster conversion times over a Sigma Delta ADC and low power converters are available from integrated circuit manufacturers, however factors such as missing ADC conversion codes and parameters such as integrated non-linearity (INL) have an impact on the accuracy, typically showing as repeated glitches in the generated spectra. (Lenero-Bardallo & Rodriguez-Vazquez, 2016).

2.8 Spectrum Creation

The spectroscopic information is typically represented as a histogram, showing the number of times a processed radiation event has yielded the digital conversion value. Each conversion value, typically called a channel, represents a bin (x-axis) in the histogram, where each bin also represents a radiation energy value in MeV. The accumulation of events in the histogram ultimately shows the spectrum of the radiation detected, yielding the ability to identify a radioactive isotope if present, as suggested in section 1.1. (Abbene, Gerardi, & Principato, 2016).

The resolution requirements for the spectrum, or the channel size of the histogram, depends on the isotope gamma energy emissions that are to be distinguished from the spectrum. Figure 2-18 shows a 12 bit spectrum, enabling the identification of isotopes from a mixed radiation source. The lower channels in Figure 2-18 between 0 and 500 show the identification of 3 isotopes within close proximity to each other.

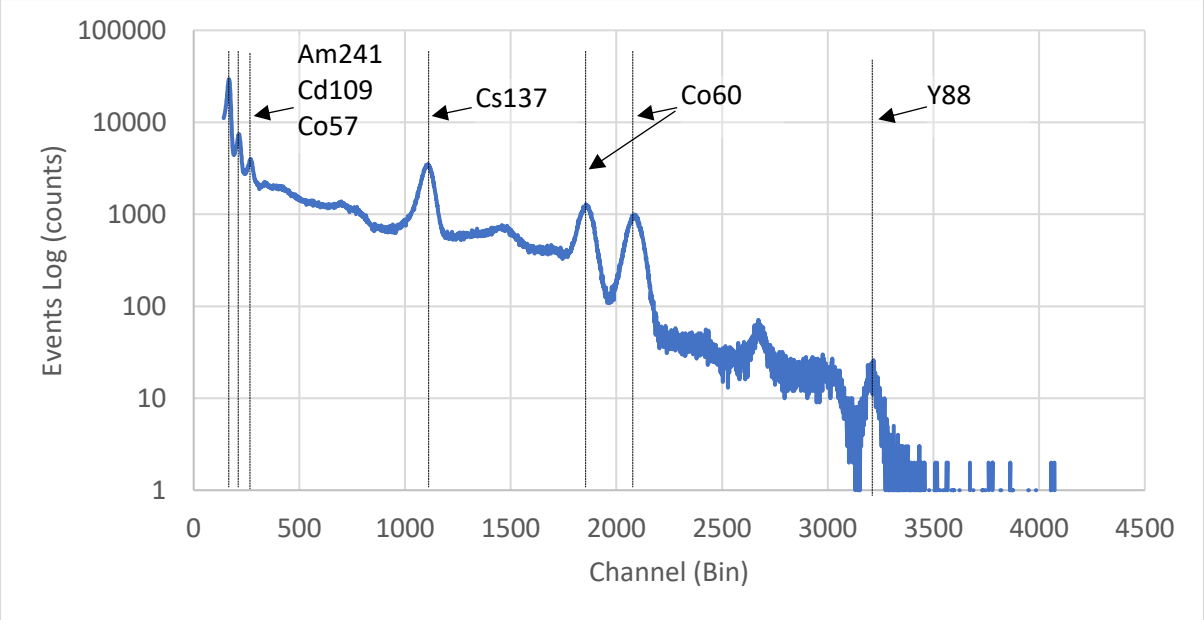

Figure 2-18 Annotated 12 bit resolution spectrum showing identified isotope peak positions from a mixed radiation source.

Figure 2-19 shows the same accumulated spectrum reduced to 7 bit resolution, where the 3 isotopes identified between channels 0 and 500 in Figure 2-18 can no longer be identified.

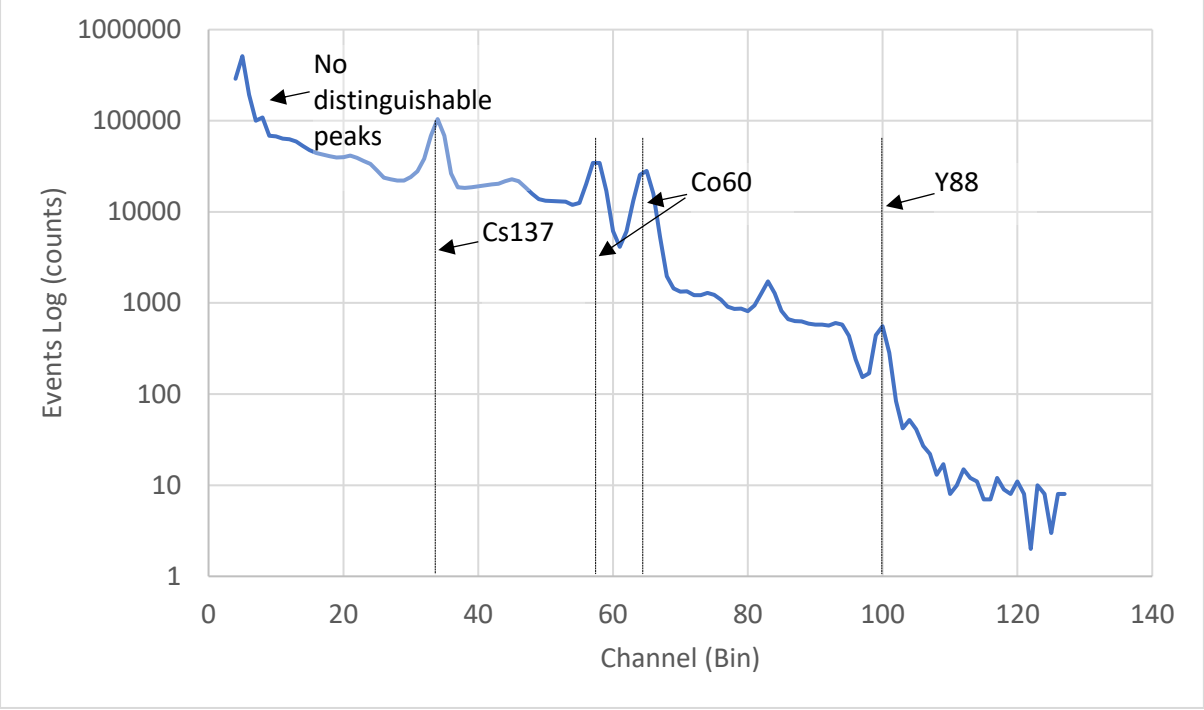

Figure 2-19 Annotated 7 bit resolution spectrum showing identified isotope peak positions from a mixed radiation source.

The channel resolution of the spectrum generated is dependent on the characteristics of the ADC, where the combined inaccuracies of an ADC are often quoted in terms of effective number of bits (ENOB). With electrical noise considerations as well as the ADC specifications, if a 12 bit spectrum

resolution is required, a higher resolution 16 bit ADC is typically used to guarantee 12 ENOB. (Knoll G. F., Multichannel Pulse Analysis, 1999).

When converting the channel to an energy step value, the spectrum energy range is divided by the spectrum resolution. Equation 2-3 shows the channel energy steps in a 12 bit system, with a 3 MeV spectrum range.

$$\frac{3\ MeV}{4096} = 0.732\ keV$$

Equation 2-3 - Calculated Resolution capability of the gamma detector circuitry in the D3S using reported 12 bit resolution.

To convert the channel to an actual reported energy value, the calibration of the detector is achieved by exposing the detector to known isotopes with well-spaced energy emissions, where the channels can be mapped to the known energy peaks in the generated spectrum. In practice, the energy conversion not perfect, where factors such as signal to noise ratios, and energy resolutions of the crystal contribute to a degradation in the spectrum gathered. (Knoll G. F., 1999).

2.9 Literature Review Conclusion

The development of scintillation detection technologies and the required electronics for processing radiation events for gamma and neutron detection has a solid foundation in portable radiation detector products. The importance of accurately capturing the scintillation characteristics, i.e. the pulse shape using the processing electronics is paramount for determining the energy deposited in the crystal or distinguishing the difference between a gamma or neutron. It is clear that the next generation of research on dual gamma neutron scintillators will prove a viable solution for future enhancements to portable detector products exploiting SiPM technology. There exists a requirement to develop the next generation of electronic circuitry to enable the low power processing of events from upcoming dual gamma neutron scintillators, applying the discrimination methods that have so far only existed in laboratory based environments. Although the scintillator CLLB currently yields high application performance, newer scintillators could surpass the performance of CLLB in the future and as research in to dual gamma neutron scintillators continues to evolve, any electronics would need to be upgradable to yield the continuous high performance of the detector product.

3 Low Power Digital Solution for Radiation Detection

Lowering power consumption and maximising flexibility of processing electronics for the use of multiple scintillators in uncharged radiation detector products is addressed with the proposed digital processing solution. By converting the associated electrical signal of the detected gamma or neutron event, to digital information earlier in the event signal processing chain, performance and power efficiency improvements, as well as a firmware modifiable system configuration is achieved.

3.1 High Rate Peak Capture

Traditionally, as discussed in section 2.6 the energy information of the gamma radiation event will be converted to a digital value typically by the ADC sampling a peak hold voltage. It can be seen from Figure 3-1 that the peak detect and hold circuitry adds 46 µS after the peak of the output from the shaping circuitry stage, where the total event lasts 60 µS. As the peak detect function is a substantial proportion of the total event time, by reducing the hold time the maximum event rate can be increased. The hold time however, is dictated by the speed of the implemented ADC and reset procedure programmed in the microcontroller. Circuitry improvements must be made to improve the ADC sample time, and reduce peak hold time, to improve detector capability with and enhance high count rate processing.

In an ideal case, the peak hold function should be reset upon the output of the shaping stage returning to the baseline of the output signal, where the radiation event has then passed. This can be seen in Figure 3-1.

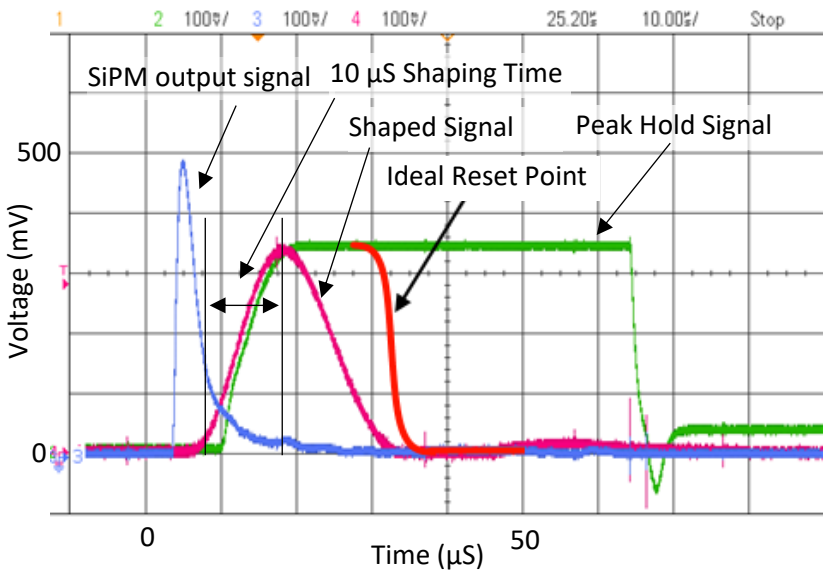

Figure 3-1 Oscilloscope trace with overlaid trace showing the ideal peak hold reset point.

For a caesium iodide scintillator with an applied 10 µS shaping time, a symmetrical shaped decay time of 10 µS is ideally the required time to complete an ADC conversion and reset. This is not demanding for most commercially available ADC components or microcontroller ADC modules however, as the requirement for the number samples per second increases, the power consumption and cost of the ADC component tends to rise. This must be considered for applications where fast scintillators such as NaI(Ti) are used that require a faster 2 µS shaping time.

3.2 Analogue to Digital Conversion Requirements

Given that the energy information is represented by the amplitude of the shaped pulse, if a radiation event with same energy was to occur again it is important when generating a spectrum that the same pulse amplitude sampled by the ADC yields the same digital result in each event. The parameters that are most important for the accuracy of this is the INL of the ADC, where these parameters represent bit accuracy error from the ideal transfer function of the ADC, and the accuracy of the bin width per output code. (Maxim Integrated Products, Inc, 2001).

Some ADC architectures a yield higher level of INL with two commonly used ADC architectures in detectors being the Wilkinson linear ramp converter and the Successive Approximation (SAR). The Wilkinson ADC can offer improved INL performance at the cost of conversion speed, where the greater the resolution, the more output codes the ramp generator must cycle through, limiting the detector event processing rate. SAR ADCs offer fast conversion speeds of around 1 Million samples per second (MSps) however INL figures vary, where cost is often a factor in the performance. (Knoll G. F., Multichannel Pulse Analysis, 1999).

3.3 Increasing the Sample Rate for Digital Peak Detection

The use of digital peak detection for this application allows the removal of the peak detect circuitry, and hence the additional processing time used in its functionality. The shaped pulse amplitude however still must be acquired to determine the radiation event energy information. The method used in this application is where upon an event threshold trigger, continuously sample the shaped pulse signal to digitally determine the maximum amplitude.

The ADC used for digitizing the signal for this application utilised a pipelined folding architecture currently under development in research led by David Upton at the University of Huddersfield leading to collaboration of its development for a use in this radiation detection application. The ADC architecture allows conversion rates of up to 25 MSps, whilst maintaining sample accuracy. The implemented detector system is shown in the diagram in Figure 3-2.

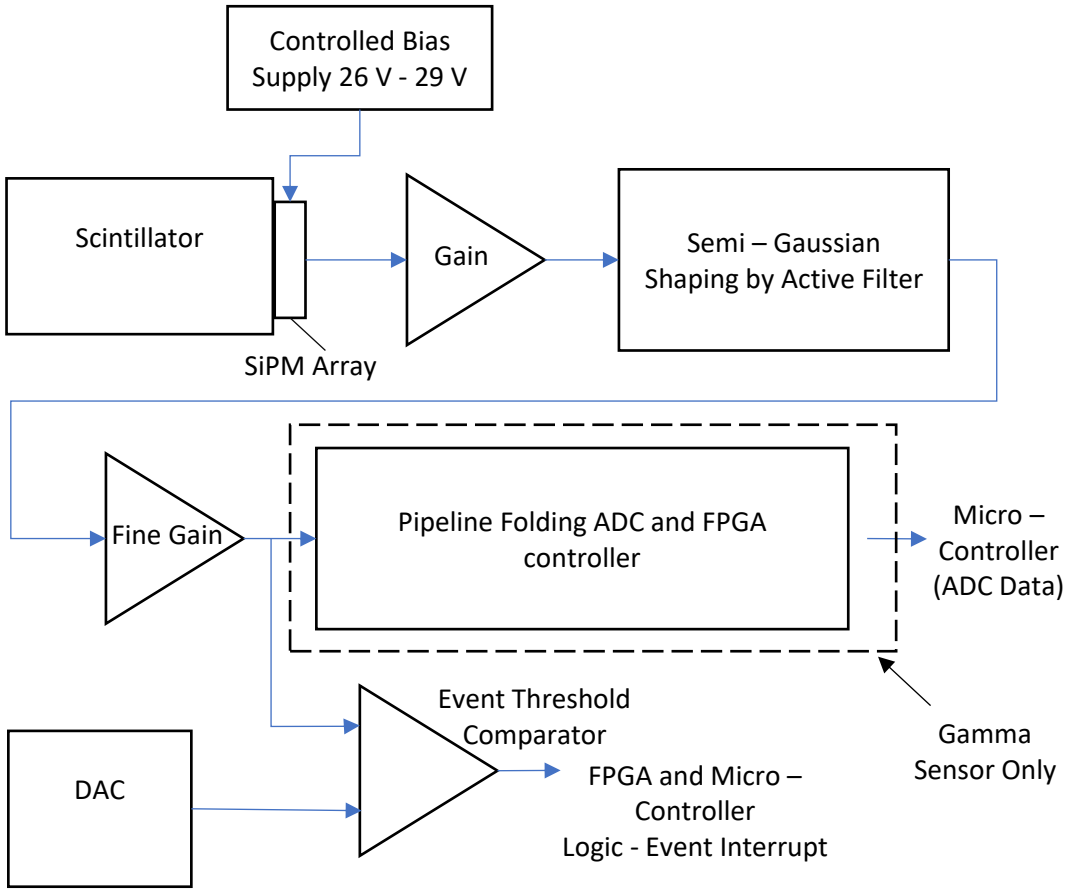

Figure 3-2 Gamma Detector System using the Pipelined Folding ADC for pulse amplitude capture.

3.4 The High-Speed Pipelined Folding ADC System

There are two main parts to the Pipelined Folding ADC, the analogue signal comparison circuit, and the data control logic implemented in this application using a Field Programable Gate Array (FPGA). The analogue signal comparison section of the ADC system was already well developed and was based on works completed by (Moreland C. W., 1995), (Moreland, et al., 2000) and (Dine & Maloberti, 2003). The ADC architecture then required the control logic to be designed and implemented in the FPGA.

The analogue section of the ADC system consists of seven folding stages, an input sample and hold (S&H) circuit, and an additional comparator making up eight digital outputs for an eight-bit ADC architecture. Each stage consists of an amplifier with a gain of two based on the Tent Map function applied, where non-inverting or inverting functionality is controlled by the output status of a preceding comparator. A reference voltage V_{ref} that is half of $V_{max,}$ is compared to the input of the previous stage output, where if the signal is over V_{ref} then the amplifier output in the stage is inverted. This essentially represents the V_{min} to V_{max} output of a preceding stage as V_{min} to V_{max} and back to V_{min} on the output. The comparator output, logic zero or logic one, from each stage also represents a bit in the ADC output code where the total result code output is of Gray code representation. (Moreland,

et al., 2000). This functionality is demonstrated with typical signals for a four-bit folding ADC shown in Figure 3-3.

The addition of a S&H circuit in each folding stage was shown in works (Dine & Maloberti, 2003), and shown in Figure 3-3, allows the pipelining of each of the stages in the folding ADC. This functionality requires a non-overlapping clock (NOLC) as each stage relies on a stable output from the previous stage, therefore showing that each can be in sample or hold mode, as the signal sample ripples through each stage. As each stage is then processing successive samples in the incoming sequence, reconstruction of the Gray code result from each of the pipelined stages is required. The pipelining increases the maximum sample rate of the original folding architecture, where the maximum sample rate was limited by each ADC input sample rippling through all the stages for a valid output result code. This reconstruction was implemented in the FPGA, where the logic program for the FPGA was designed and written in VHDL.

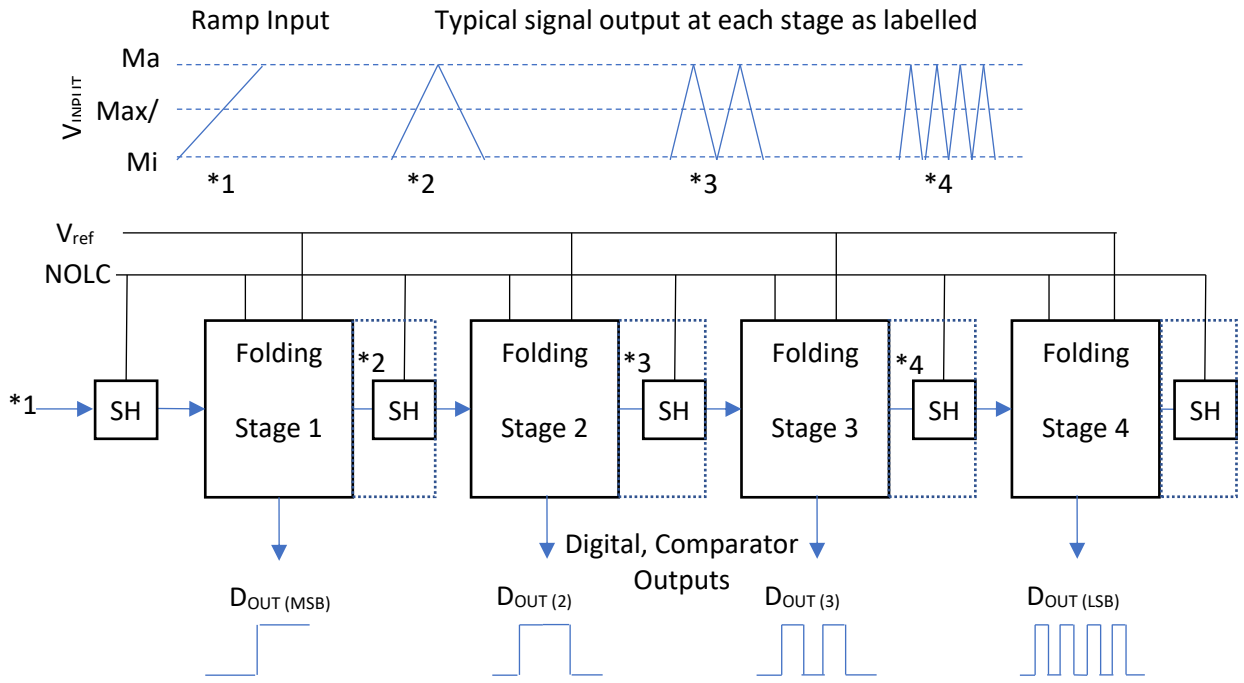

Figure 3-3 Block level diagram of a 4bit Sample and Hold, Folding ADC, with ramp input and associated typical output signals (over multiple samples).

3.5 Designing the ADC Data Control Logic using FPGA Technology

The block elements required in the data control logic for control over the pipeline folding ADC architecture are shown in Figure 3-4 where the non-overlapping clock generator, the data assembly logic and a communication interface combined to form the overall processing application required in the design.

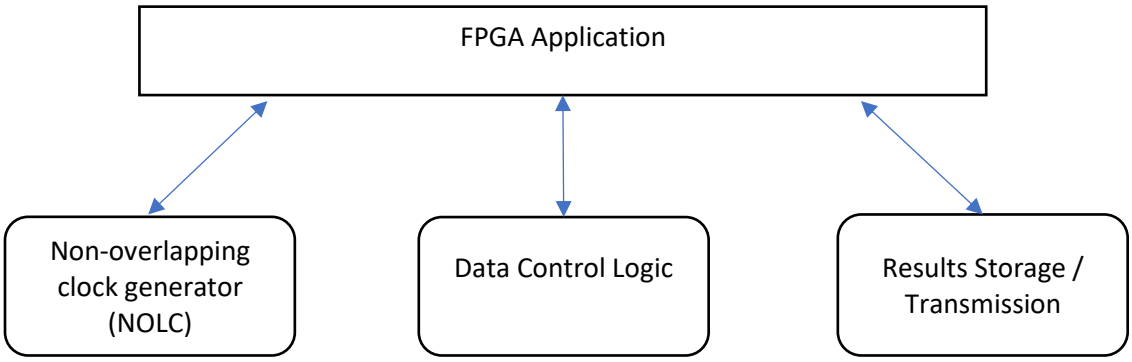

Figure 3-4 FPGA Application diagram showing the required components in the design and written VHDL outline.

Figure 3-4 also outlines the operational sections of the written VHDL code which was written to the FPGA for system operation. The VHDL written can be found in Appendix B, where each subsequent logic design section in this research details the operation of the logic written in the VHDL.

3.5.1 Clock Control

The NOLC component implemented is a bi-phase, 2 output clocks, where the non-overlapping requirement uses two time points where both outputs have a logic 0 output. The Pipeline Folding ADC architecture requires the NOLC to guarantee isolation between each folding and, S&H stage. Loss of this isolation would result in adjacent ADC sample cross talk, where the amplifier outputs of each stage start to affect the adjacent stage amplifier, yielding sample results that are contaminated with each other. A diagram of the NOLC output is shown in Figure 3-5, where τ_{clk} is the sample rate, Clk_p and Clk_n are the outputs signals, and T_{nol1} and T_{nol2} are the non-overlapping time points.

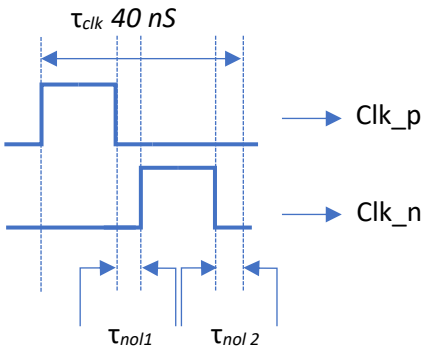

Figure 3-5 Waveform diagram showing the Non Overlapping Clock generation and output.

The NOLC component was implemented using the available FPGA logic and the onboard Phase Locked Loop (PLL) clock source by setting the PLL output frequency to 250 MHz, ten times that of the intended sample rate of the ADC. Due to the non-overlapping requirement, this high frequency was required to be able to implement the two non-overlap logic 0 output points with the required time length optimal for maintaining accurate operation of the ADC and providing the stage to stage isolation.

3.5.2 Pipeline Gray Code Data Handling

The Pipelined Folding ADC's digital Gray code output is generated by a comparator in each stage, where its input signal changes the state of the comparator if its greater than that of the reference voltage. For the pipeline operation to function, the S&H stages preceding each stage require time to charge the S&H capacitor. When these are charged to match the stage input, so the voltage output is stable, the comparator output which could have changed state many times during charging, will also now be stable. This is then the ideal point at which the FPGA can sample the state of the logic outputs, however in case of any occurrence of capturing the comparator outputs on a point of logic transition, input protection was implemented to minimise glitch conditions from entering the data conversion logic. By using synchronisation logic on the data inputs as shown in Figure 3-6, glitches because of metastability can be prevented (Altera Corporation, 2009).

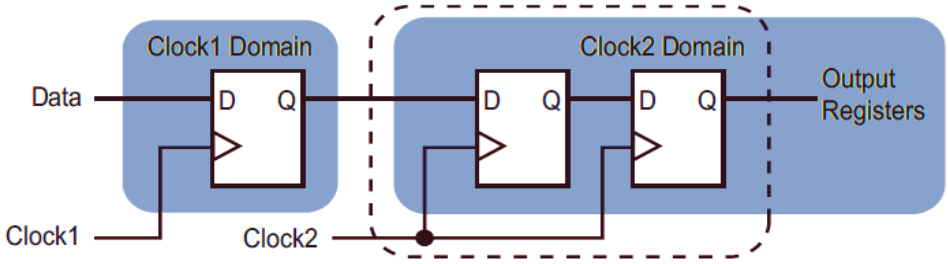

Figure 3-6 FPGA Input Synchronisation Logic for Metastability Protection (Altera Corporation, 2009).

The ADC NOLC although generated by the FPGA in this case, is still treated as an external clock domain, where if an external NOLC was used instead, this would be the case anyway. The data inputs to the conversion logic are synchronised to the fast PLL clock, as the synchronisation occurs using the state sequence driven by the fast PLL clock. From a design view both the sample, and the hold states each occur once in a sample clock cycle, and therefore the results are only available at the end of each hold state, in an alternating pattern as the input sample ripples through each stage. Categorising the stages in to odd and even stages allows for the array logic to be designed with both this two point availability of results and the pipeline logic, allocated as shown in Figure 3-7.

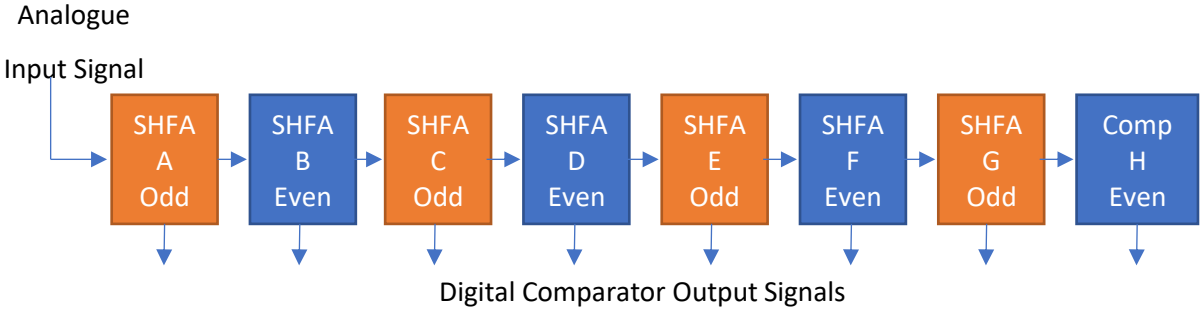

Figure 3-7 ADC sample and hold stages showing the ADC stage odd and even output categories.

For multiple samples and the pipeline control, a series of 4 aligned registers allow for the input of data according to the stage of the ADC the Gray code sample bit has come from, in order to re-construct the single sample result from the ADC pipeline. Registers A0 to A3 in Figure 3-8 represent an array, where each register is filled with data from the preceding part of the pipeline, and the new input data from each successive folding stage of the ADC in sequence. This sequence is shown in the data construction table in Figure 3-8, showing the first 4 samples of the ADC in operation and the converted data output from Gray code to binary. The operation of the data construction table is also expanded in Appendix A, where the construction of the results and the state of the data control logic through the first eight clock edges is detailed using individual construction tables. The detailed view also shows clearly how the latency of a standard pipeline method is halved, due to the acquisition of two bits in a single clock cycle instead of a single bit of the full ADC result code.

Group	C(x)	Array (Gray Code)					
		A0	A1	A2	A3	Binary Result	
Even	CA	SA3	SA2	SA1	SA0	Bit7	MSB
Odd	CB	SB3	SB2	SB1	SB0	Bit6	
Even	CC	n	SC2	SC1	SC0	Bit5	
Odd	CD	n	SD2	SD1	SD0	Bit4	
Even	CE	n	n	SE1	SE0	Bit3	
Odd	CF	n	n	SF1	SF0	Bit2	
Even	CG	n	n	n	SG0	Bit1	
Odd	CH	n	n	n	SH0	Bit0	LSB
Key: x = Don't Care, n = not used Data format example S Sample A Comparator 0 Sample Number							

Figure 3-8 ADC Data Control Logic Table showing the first 4 conversions ripple through the control logic of the ADC as in operation at the time of the 4th sample + 1 PLL clock.

When the binary conversion result is available, it has incurred 4 sample clock cycles and an additional 3 PLL clock cycles latency from the original sample of the input signal as detailed in Appendix A. The 172 nS latency of the results is of no issue to the application, as any radiation detection results would still be processed in a sufficient time for spectrum reporting to a human operator of a detector device. The pipeline latency is improved over what would be an 8-sample cycle latency due to the use of the NOLC, and the ADC architecture converting two bits in one sample clock cycle. The 3 PLL clock cycle latency is due to the input synchronisation logic and the Gray code to binary conversion, where the input synchronisation happens before the acquisitions enter the data control logic and therefore is not shown in the data construction tables.

This ADC data control logic was used in the test application, initially written to test the performance of the ADC, before adding the functionality for the gamma detector requirements with the peak capture improvements. The VHDL code uses in this design can be found in Appendix B.

3.6 Application of the FPGA for ADC Architecture Control

The application control layer for testing the ADC for bulk sample data processing is shown in the flow diagram in Figure 3-9, and the VHDL implementation can be seen in Appendix B.

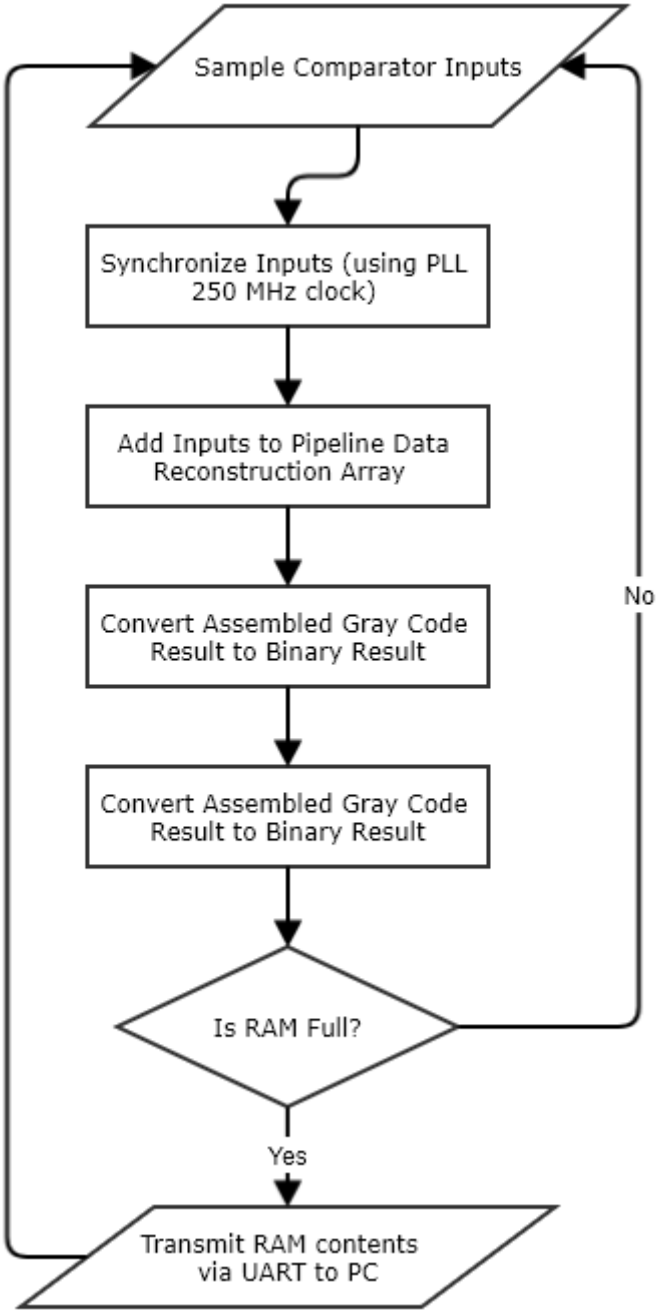

Figure 3-9 Flow diagram showing the data processing system implemented in the FPGA for result reconstruction and transmission.

The application designed brought together the ADC data control logic, uses a 32 kB Random Access Memory (RAM) implemented as an array in the FPGA logic to store the sample results ready for transmission to a computer for offline analysis via the transmit only design based on a Universal Asynchronous Receive and Transmit (UART) module.

3.6.1 Design of the UART Transmission

UART modules are used in many electronic devices as a communications method as the hardware required to implement a UART communication mode is commonly supported by many devices and computer communication ports. The UART module written in VHDL for the FPGA was used because of this combability however, only allowed communication data rates of up to 1 MBaud due to hardware limitations of the computer.

UART transceivers can be configured with different settings for flow control, data parity and frame sizes. The configuration settings chosen in the design are shown in Table 3-1, where the 800 kbps data transfer rate is due to the required UART frame packing for communication synchronisation, shown in Figure 3-10.

Parameter	Configuration
Baud Rate	1 MBaud
Parity	None
Flow Control	None
Stop bits	1
Data Rate	800 kbps (Based on configuration)
Data bits	8

Table 3-1 UART configuration used in the application.

Whilst other communication interfaces exist, such as Universal Serial Bus (USB) which can handle increased data rates of over 200 MBps, the UART communication does not limit the operation of the ADC as the results are stored in the RAM first, and then transmitted. The RAM availability is based on the logic available in the FPGA, where the 32 KB RAM and the application fills 90% of the available logic onboard.

The construction of a data frame in a UART module when using the configuration in Table 3-1 is shown in Figure 3-10. The start (St) and stop (Sp) bits are the mandatory packing required for UART, where D(n) is the data bit for the data payload. The design was based around the transmission operation of an Atmel (now Microchip) UART module (Atmel Corporation, 2016) and then written in VHDL, as in Appendix B.

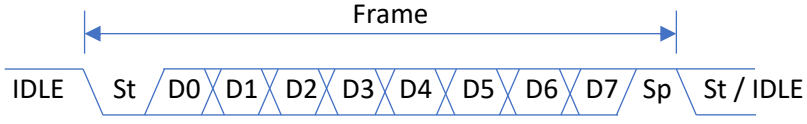

Figure 3-10 Logic diagram showing a single UART frame at configured in the design.

3.7 Initial Test Results and Analysis

Initial results were collected by first using a 200 Hz ramp input, where the S&H Folding stage outputs were verified, as shown in Figure 3-11. A Gray code representation of the ramp input was observed, closely matching the expected output signals as shown in Figure 3-3.

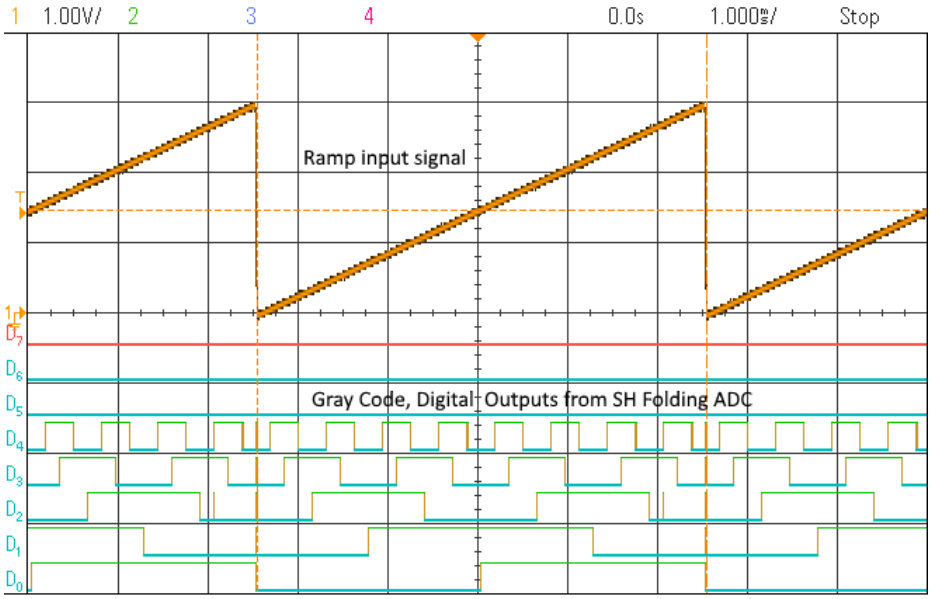

Figure 3-11 Oscilloscope trace showing the verification of the Gray code outputs from the S&H Folding ADC.

Multiple frequencies were then used to test the ADC, where a sine wave of 100 kHz collected from the ADC system is shown in Figure 3-12. The results for this were transmitted to the computer through the UART to enable the replotting of the data.

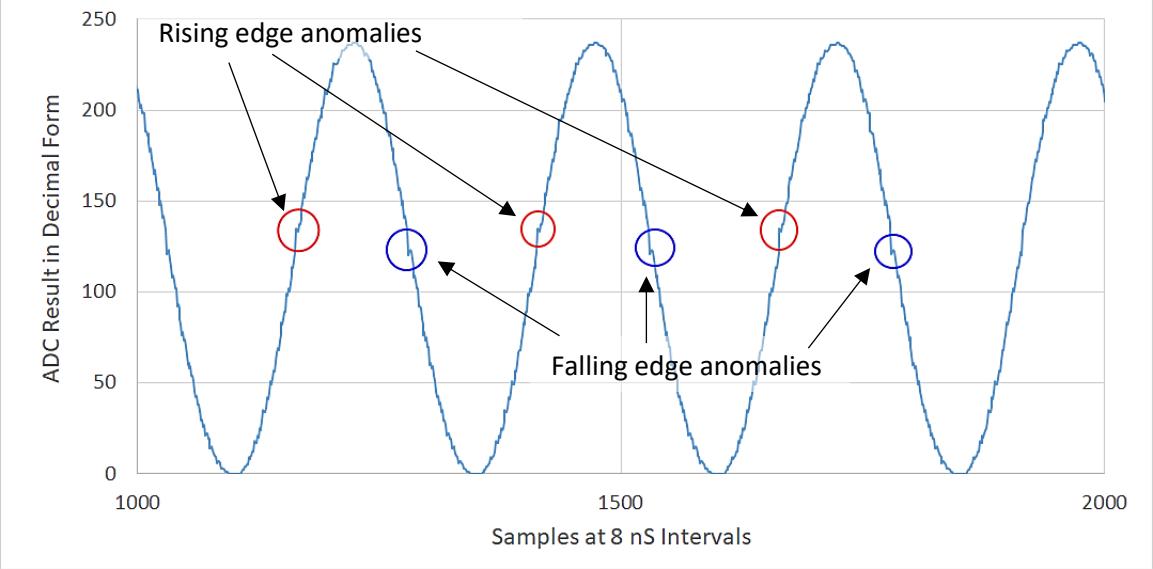

Figure 3-12 Results obtained by using the ADC system with a 100 kHz sine wave input, re-plotted from the captured data, with circled anomalies.

Since the input sine wave is re-constructed in Figure 3-12, this verifies that the functionality of the logic implemented in the VHDL application accurately handles the pipeline data reconstruction and the Gray Code to Binary conversion. Analysing the re-plotted data closely however does show repeating anomalies, where these are likely to be errors in the folding ADC conversion process. The anomalies, shown by the red and blue rings in Figure 3-12 are likely to be a more significant gain error in the MSB folding stage, making the accuracy of that bit output lower than the other outputs.

Due to the anomalies, the prototype system is not achieving the maximum 8 bit accuracy, however it is rare that a commercially available ADC would have an ENOB that is the same as the total resolution of the ADC. As the resolution can be increase by adding further stages however, the Folding ADC system accuracy can be improved using the knowledge gained from testing the folding ADC system. A further source of inaccuracy is the potential for noise, or inaccuracies from the sine wave generator. Further testing when using the ADC system for peak detection shows how these anomalies affect the peak detection accuracy.

3.8 Peak Detection Application

The advantage of the designed ADC system for peak detection and capture is the high-speed conversion rate of 25 MSps allows for accurate capture of the peak amplitude, at the position of peak. A slower sample rate would result in an increased probability of missing the true peak between samples. The application was modified from that in section 3.6 to implement the peak detect functionality, by comparing current and previous samples within the FPGA.

The peak detection state is a condition attached to the storage of the result, hence only the results of the peak values are loaded to the RAM array for later transmission through the UART. This allows the capture of more peaks in the signal and improved the testing for peak accuracy. The condition on storage also does not add any further latency to the output of the result.

The peak detection method used consists of the FPGA comparing the newly acquired sample result to the previous sample results to determine which is of higher value. The FPGA holds this higher value for comparison with the next sample result. Noise prevents the use of the first lower sample result determining the peak, therefore the higher sample result is held for 10 samples before confirming the peak value. If a higher sample result is acquired within the 10-sample period, the confirmation period restarts with the higher value. A peak confirmation pulse with the 10-sample delay can be seen on logic line D8 in Figure 3-13.

3.9 Peak Detection Results and Analysis

Using the Gaussian function signal generator in an Agilent MSO-X 3054A, simulated shaped input signals were used to test the accuracy of the peak capture, since the amplitude of the peaks in the simulated signal can be set to a known value. A limitation of the function generator however is that the shaping time is linked to the event rate, however as faster scintillators would be used in high count rate applications anyway, the peak detection accuracy still must be maintained, where any loss of accuracy would determine the limits of the system.

Since a system using a sodium iodide based scintillator would typically employ shaping times of 2 µS to 3 µS, generating a 2.5 µS gaussian pulse using the signal generator for 10000 events, at a rate of 100,000 events per second was used to test the peak capture accuracy. To then test the system limits for peak capture accuracy, 10000, 1 µS shaping time gaussian pulse events at a rate of 250,00 events per second were generated and captured. A low, mid and high amplitude input of the generated gaussian signal were used with each shaping time, to validate performance across the input range of the ADC system and the results are shown in Figure 3-14.

To validate the peak capture system functionality, test signal outputs were used and shown on the annotated oscilloscope trace in Figure 3-13, showing a single pulse event, where the reconstructed binary representation is shown in the logic traces D7 – D0, MSB to LSB respectively. The black centre line annotation shown is time position of the peak, however the latency of the ADC system can also be seen where the first time the peak value of 77 as represented by D7 – D0, is less than 80 nS as shown in the trace. This parallels with the calculations in section 3.5.2.

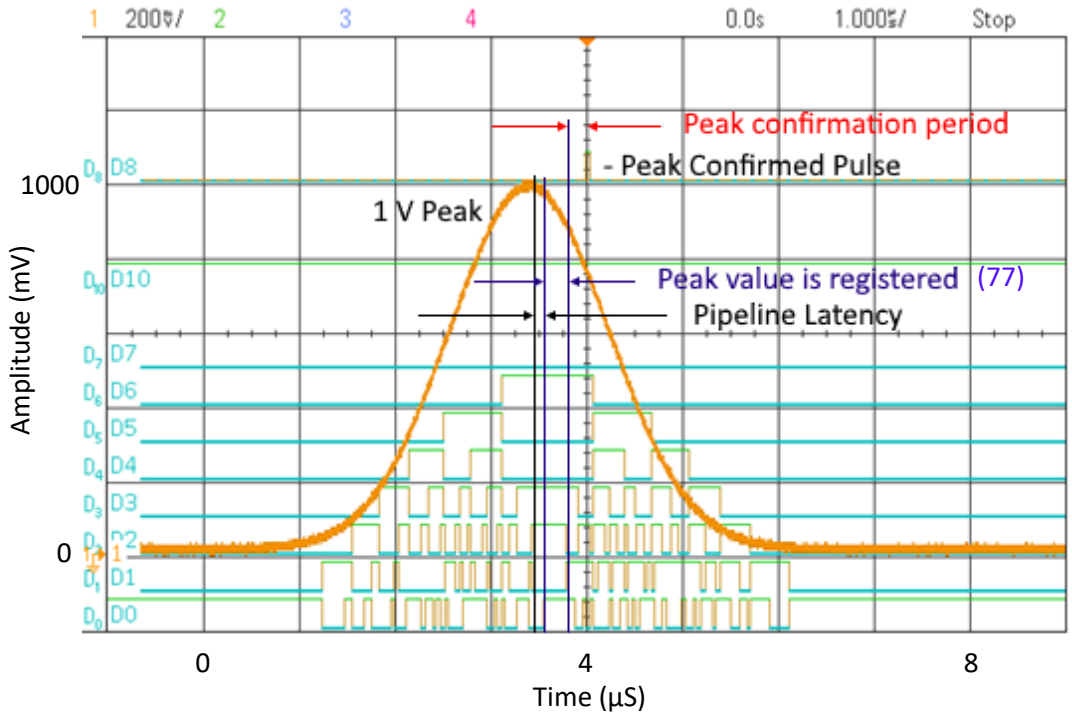

Figure 3-13 Annotated oscilloscope trace showing a generated shaped pulse with a 2.5 µS shaping time, and binary logic representation from the ADC system.

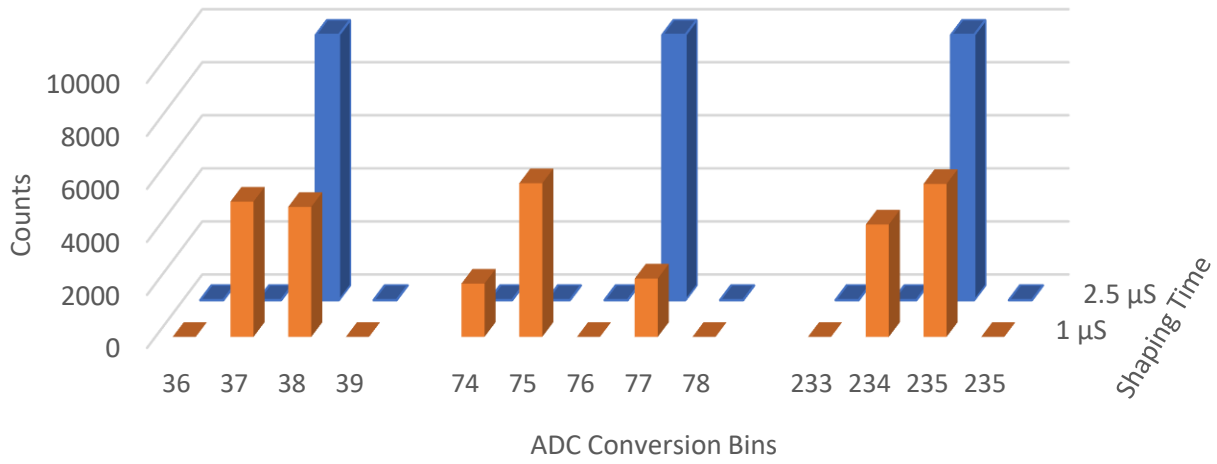

Figure 3-14 Graph showing 10,000 acquired peak values using the generated 2.5 µS and 1 µS shaping time inputs for 3 discrete amplitudes.

The comparison of the shaping times in Figure 3-14 show that the system performance accuracy with the 2.5 µS shaping time achieves the full 8 bit accuracy with the three test amplitudes. With the 1 µS shaping time tests, after consideration of the generator noise, and that the generator output is of 8 bit resolution its self, the folding ADC system performance may degrade to 7 bit accuracy at the mid test amplitude with the 1 µS shaping time. At the low and high test amplitude for the 1 µS shaping

time, the generated shaped signal amplitude could be falling between two discrete bins upon conversion, therefore not representing resolution degradation.

For the application of radiation detection using a sodium iodide based scintillator with a 16 by 4 inch size, a count rate of 100,000 counts would represent a considerable radiation source present, and since the ADC system can maintain the 8 bit accuracy for shaping times used with NaI(Ti) scintillators, respectable spectrum information can be gained for use with the source identification.

For testing the absolute accuracy, the voltage represented by the peak result as shown in Figure 3-13 is 1 V. The result code of 77 translates to a voltage of 905.9 mV, a difference of 94.5 mV from the oscilloscope measurement, where the reference is 3 V.

Although the peak conversion result is consistent over the 10000 peak samples, the voltage difference between the oscilloscope measurement and the ADC system result is likely the result of the 50 Ω BNC cable used between the oscilloscope and the low input impedance of the ADC, where the input impedance of the ADC circuit reduces the apparent amplitude of the input signal. Using design information of the analogue ADC section, the input impedance is determined by R_{in} in the inverting sample and hold circuit at the input of the ADC, which is 490 Ω.

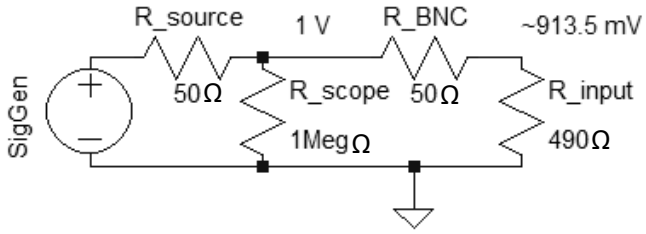

Figure 3-15 Circuit representation of the measurement and test setup.

The equivalent measurement setup circuit is shown above in Figure 3-15, where a potential divider is formed between the scope reading of a 1 V peak, the BNC cable and the ADC input impedance, resulting in the attenuation of the 1 V peak signal as seen by the scope to 913.5 mV, closer to the result obtained by the ADC system. This could be improved using a buffer amplifier with a high input impedance at the input to the ADC system, which is typical in the application of many ADCs in practice. Secondly, each bit in the 8 bit ADC system represents a voltage step of 11.8 mV, therefore the decimal result of 77 has a tolerance of ± 5.9 mV.

As shown by the results, the functionality of ADC for the peak capture application will provide accurate 8 bit gamma spectra information for the use in radiation source identification with scintillators requiring as faster shaping time of 2.5 µS, such as sodium iodide.

3.9.1 Digital Design and FPGA use improvements

The use of the FPGA for the ADC architecture control could be changed and implemented in dedicated logic, potentially in an ASIC for example to achieve a dedicated ADC integrated circuit. Using an FPGA for this task however, provides the advantage of allowing customisable applications to be 'added on top' on the functionality of controlling the ADC architecture. Such a method was used to implement the peak capture application into the FPGA process, allowing the ADC to function as both the peak capture and ADC requirements in the detector system.

Digital correction logic could also be added to the FPGA application subject to further research at the University of Huddersfield, to compensate for the gain stage to stage, and total gain offsets as seen in with the difference between the measured peak on the oscilloscope traces and the ADC result output in the results. Further reduction of these offsets would be gained with the use of precision resistors in the Folding ADC prototype circuit, or fabricating the analogue circuitry, or both digital and analogue circuitry on silicon with an ASIC implementation.

3.10 Further Implementing Digital Event Processing

Given the ADC systems high sample rate, its ability to directly sample the amplified SiPM pulse was tested, where given the flexibility of the FPGA, any spectra processing can be achieved using the FPGA and appropriate additions to the processing logic. The system diagram can be seen in Figure 3-16, where the requirement for pulse shaping and peak capture can be implemented digitally in the FPGA. Also, by removing the electronic circuitry used for providing the pulse shaping function, further power savings can be gained, on top of the power savings gained by removing the peak capture circuitry previously.

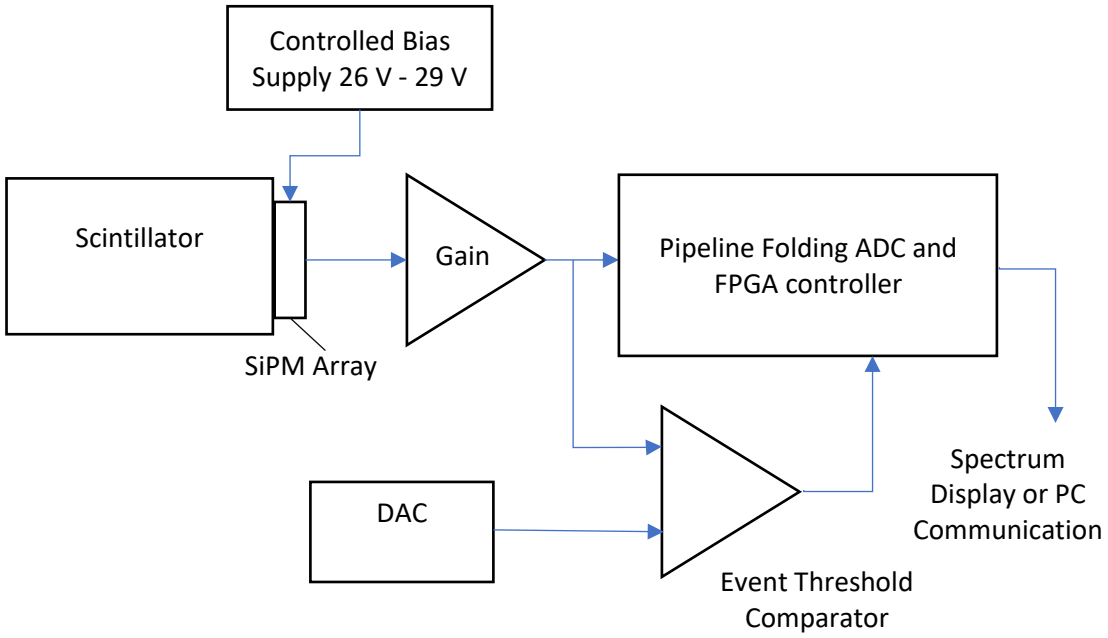

Figure 3-16 Folding ADC System applied to sample an amplified SiPM signal directly.

To evaluate the system accuracy, sample radiation pulses were captured using the ADC system, by continuously sampling at 25 MSps, an amplified SiPM output, coupled to a CsI(Ti) crystal, capturing background gamma radiation events. The results are shown in Figure 3-17 and Figure 3-18, and show the re-plotted samples from the ADC data, and a five data point moving average example trace that could be applied in the FPGA logic to improve event re-construction.

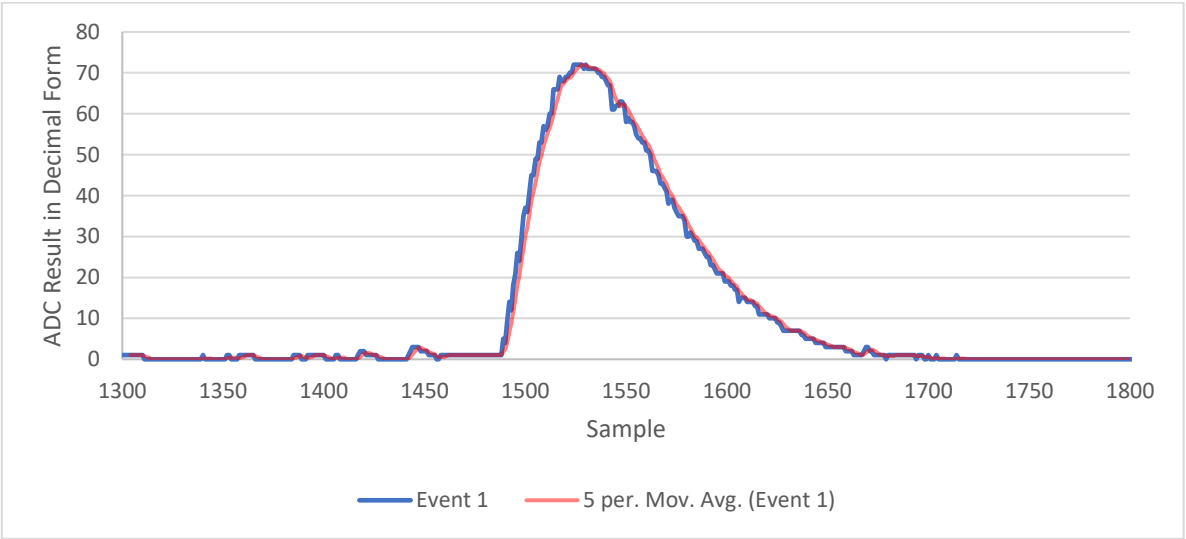

Figure 3-17 Mid ADC input range captured gamma radiation event extracted from continuous sampling an amplified SiPM output coupled to a CsI(Ti) crystal using the ADC system and applied moving average.

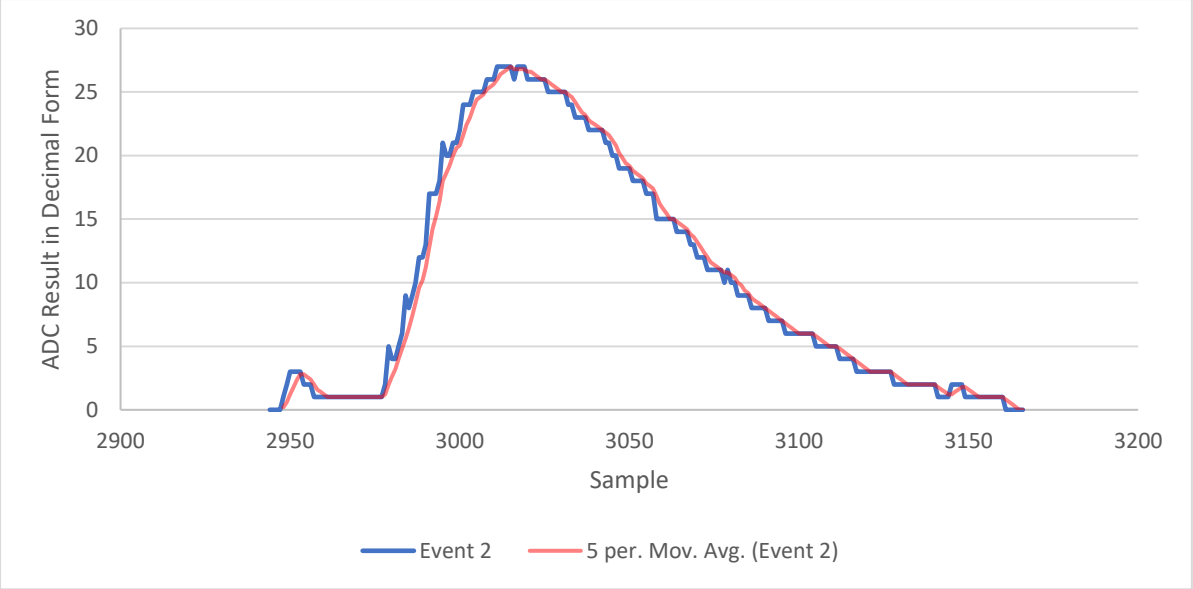

Figure 3-18 Low-end ADC input range captured gamma radiation event extracted from continuous sampling an amplified SiPM output coupled to a CsI(Ti) crystal using the ADC system and applied moving average.

As the FPGA uses a RAM array to store sample data before transmitting the contents, it is possible to apply live processing in the FPGA for the desired data output in the application, such as spectrum generation. Since the sample rate of 25 MSps is known, both the time and amplitude information are available, where digital pulse analysis methods can be implemented in the FPGA logic.

The system, when collecting the results in Figure 3-17 and Figure 3-18, is running continuously, therefore sampling even when no events are present. It can be implemented in the FPGA application that the storage of events only occurs when the signal crosses a threshold, similar to a digital low level discriminator, replacing the DAC and comparator. Such usage where continuous sampling at 25 MSps was required achieved a power consumption of 160 mW. For maximum power efficiency however, if the DAC and comparator remained in the system as in Figure 3-16, the ADC system can be triggered by the comparator output and therefore stop sampling when no events are present. Such operation was tested by starting and pausing the NOLC, where the ADC system consumed 100 mW, a power saving of 60 mW over continuous sampling operation.

3.10.1 Application for Dual Gamma Neutron Scintillators.

As mentioned in section 2.4, the use of dual gamma neutron scintillators has relied on post processing results collected from laboratory acquisition systems, to obtain gamma neutron separation data. Using the system proposed in Figure 3-16 with a dual gamma neutron scintillator such as CLLB, application logic can be added to the FPGA to apply a pulse shape discrimination method as mentioned in section 2.4.2 to the captured events from the lower power ADC system, implemented in a portable detector product. The advantage of the upgradable firmware of the FPGA can also be used to apply

the latest pulse shape discrimination method or be changed to use with any of the next generation scintillation detection crystals.

3.11 Conclusion

The proposed use of the folding ADC architecture and the flexibility of the application of the FPGA improves on the technology typically implemented in the current generation of hand held gamma and neutron detectors. Although the peak capture application improves on spectrum linearity by removing the slight nonlinearity contribution of the peak hold circuit, the ADC system allows the high sample rate benefits of raw output event processing from a relatively low power acquisition system capable of implementation in a hand-held gamma neutron detector. The total digital system explored allows for on device event processing, application flexibility and lower power system to fully exploit the use of next generation scintillators such as CLLB and providing the ability to process high radiation event rates.

4 Low Power Analogue Solution for Utilising Advanced Dual Gamma Neutron Detection Scintillators

The emergence of scintillators capable of gamma and neutron detection promises further compacting of hand held detection. The technology required to process the scintillation event information however, has again previously relied upon laboratory MCAs and offline processing of the acquired event data to determine the gamma and neutron events. The crystal of interest for use with the analogue discrimination technique designed is current state of the art gamma neutron scintillator CLLB, due to its optimal scintillation properties, where SiPMs are then used to detect the emitted photons form the scintillation event.

4.1 Analogue Discrimination Method in Principal

The discrimination technique designed makes use of analysing the scintillation event output at pre-set amplitude percentages, therefore making the variable of interest a time measurement between these pre-set points. The technique also combines benefits of existing discrimination techniques as in section 2.4, where a combination of pulse height and pulse gradient discrimination provides the same benefits of pulse shape discrimination without the requirement of reconstruction the pulse by either digital or analogue integration.

By analysing CLLB scintillation outputs as shown earlier in Figure 2-6, there are maximum points of difference in the output signal that can be exploited as the most appropriate comparison points for pre-set amplitude percentages, where for this technique two points will be used being the upper and lower percentages of the peak amplitude of the event. The use of amplitude percentages allows for any amplitude of scintillation event pulse to be analysed for discrimination between gamma and neutron events, as even though neutron events appear to have a fixed gamma equivalent energy output in a spectrum, factors such as variations in the photon collection and other high energy gamma events occurring results in neutron scintillation events with a range of amplitudes, as suggested in Figure 2-7.

A diagram of the discrimination technique explored is shown in Figure 4-1, where the addition of an upper level discriminator (ULD) adds the capability of pulse height discrimination, as reviewed in section 2.4.1 and therefore, enhance the capability of accurate discrimination further.

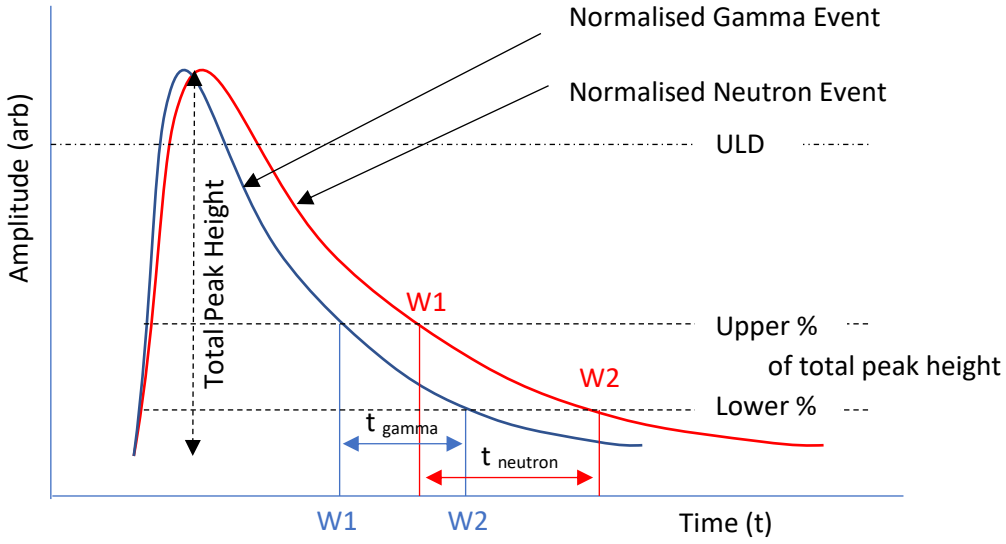

Figure 4-1 Implemented method for pulse shape discrimination of normalised typical CLLB scintillation outputs for a gamma and neutron event.

For the discrimination decision between a gamma and neutron event, the time measured between the set level thresholds will be compared to a pre-set window length, where lengths less than the pre-set will be determined as neutron events, and greater than will be determined as a gamma event. This window length would be programmed to adjust in environments with changing temperatures, as the quantity of emitted photons form the scintillation event, and performance of the SiPMs in a device would change over a temperature range.

4.2 Analogue Discrimination System Design

The designed analogue system takes the approach optimising existing analogue event processing circuitry for low power operation and then incorporating the designed discrimination circuitry which, uses efficient time to digital conversion methods that generates instantly comparable conversion results for use in the discrimination technique applied. The circuit functionality used to implement the designed discrimination method in section 4.1 is explored.

4.2.1 Peak Finding

The gamma neutron discrimination methods explored in section 2.4 require a known peak position time to then process the discrimination operation. In systems that post process acquired data, the peak can be easily determined by processing the data with peak finding algorithms. Also, as the peak to be determined changes amplitude event by event, comparing the signal amplitude to a set voltage threshold will not yield the true peak position. The method designed determines the peak live in operation and is implemented by comparing a delayed repeat of the event with its self. The system is shown in Figure 4-2.

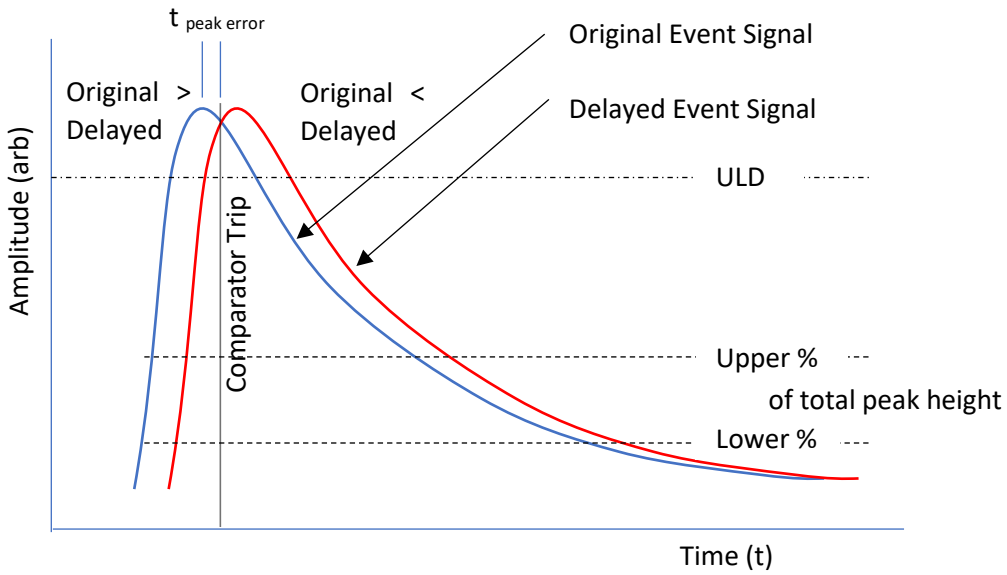

Figure 4-2 Diagram of the peak finding method using a delayed repeat of the scintillation event signal using a comparator to compare both signals.

In the design, the comparator compares both signals, and when the original event signal falls below that of the delay event, the output changes. Internal hysteresis in the selected comparator, the Texas Instruments LMV7219, prevents the output from changing state upon any introduced noise, or short event signal imperfections that may occur within the defined internal hysteresis. Although hysteresis can be added to a comparator using external resistors, the internal hysteresis implemented in the comparator offers improved accuracy over using external passive components and uses less components in total which is again advantageous for portable design.

Another property of the selected comparator is the propagation time, where the time taken from the signal comparison to output change is 7 nS. Since the output of the comparator represents the position of the peak in time, any propagation delay introduces an error in determining the true position of the peak.

Correcting for the peak error time is achieved by attenuating the original event signal by introducing a potential divider on the comparator input. The effect of this can be seen in Figure 4-3. By using the traditional low level discriminator (LLD) as shown in Figure 2-14, however triggering on the original event signal, as well as using the ULD, the logic signals available for use in the time measurements are the LLD, ULD and peak comparator output edges.

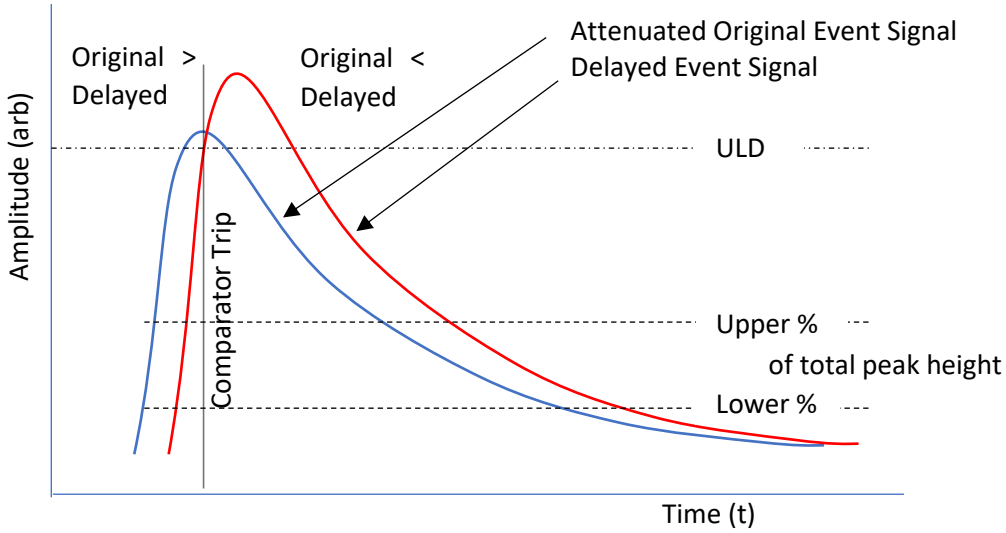

Figure 4-3 Diagram showing peak error correction by attenuation of the original event signal.

4.2.2 Event Signal Delay Generation

Introducing a delay in the signal can be achieved by using various circuit modules, such as by using passive filter components or imitating a transmission line by using large size inductor components that are not ideal for portable devices where space is often a constraint and are also limited to achieving short single Nano-second signal delays.

The design implements an active all pass filter based signal delay, making use of an op-amp to achieve larger delay times with minimal signal distortion. The circuit module can be seen in Figure 4-6, and makes use of a passive filter to introduce a phase shift, where the amplifier compensates for the loss of amplitude relative to the input signal (Harowitz & Hill, 2015).

Since the delay caused by the phase shift is frequency dependant, the all pass circuit required tuning for the frequency characteristics of scintillation event signal. The comparator hysteresis and propagation delay also bound the minimum delay required as to trigger accurately, there must be enough of a difference in signal amplitude at the peak position as generated by the signal delay, greater than the comparator hysteresis. This delay must then also be greater than the propagation delay of the comparator, as if the signal delay is not long enough at all points of the event signal, the time position accuracy of the comparator triggering on the peak will be reduced.

The required components of the all pass filter are calculated using Equation 4-1.

$$T_{delay} = \frac{2RC}{1 + \left(\frac{f}{f_0}\right)^2}$$

Equation 4-1 Finding the time delay generated from an all pass filter based on known signal frequencies (Pallas-Areny & Webster, 1999).

The target delay chosen was 100 nS based on the rising edge component of the scintillation event signal typical of CLLB, and since Equation 4-1 has an input frequency term, the delay generated will change dependent upon the frequency construction of the scintillation event signal. During the decay of the scintillation event signal, the delay generated for the event decay would be less than the faster rising edge due to its frequency content and therefore having a compression effect on the delayed event signal compared to the original. A 100 nS delay allows these constraints to be met across the majority of the event signal.

The all pass filter provides a phase lag or phase lead dependant on filter C-R or R-C configuration, where the phase variation due to the use of the op-amp is doubled to between -180° or 180° and 0, centring on the f_0 cut off frequency at 90°of the filter stage. (Pallas-Areny & Webster, 1999). Since minimal attenuation is required for use with the comparators for peak detection, the f_0 frequency is set above the fastest frequency component in the scintillation event signal.

By selecting C as 470 pF and R as 100 Ω at the first instance, f_0 is calculated as 3.39 MHz by using Equation 4-2. (Analog Devices, Inc, 2012).

$$f_0 = \frac{1}{2\pi RC}$$

Equation 4-2 Finding f_0 in Equation 4-1 where f_0 is equal to 3.39 MHz.

By approximating the event rising edge frequency, the maximum delay achieved on the event signal can be calculated. Figure 4-4 shows a typical gamma event output from using a CLLB scintillator with SiPMs, using a Cs137 radiation source. Figure 4-5 shows an annotated measurement of the leading-edge rise time of the event.

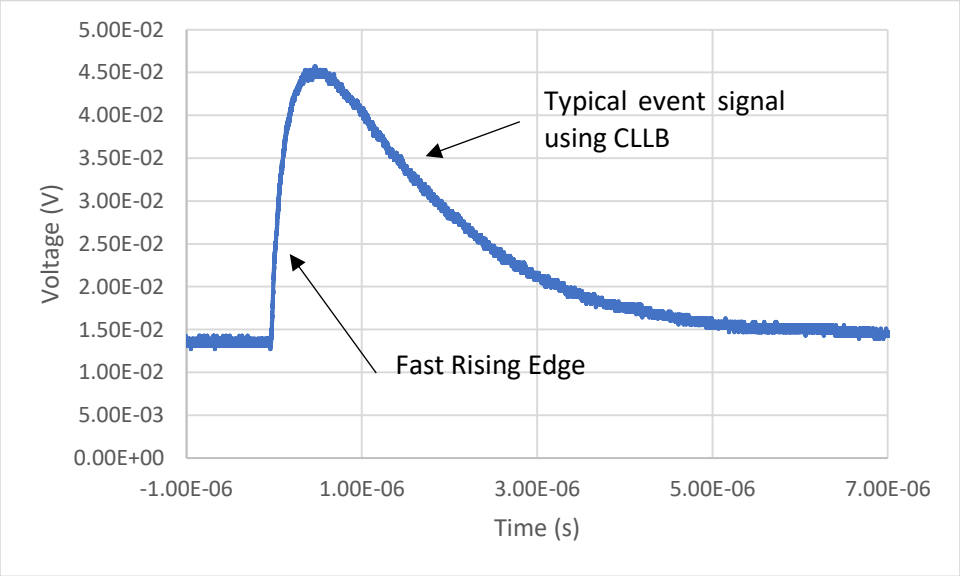

Figure 4-4 Event signal output of a Cs137 scintillation event using CLLB and a 4x4 array of SensL J-Series SiPMs.

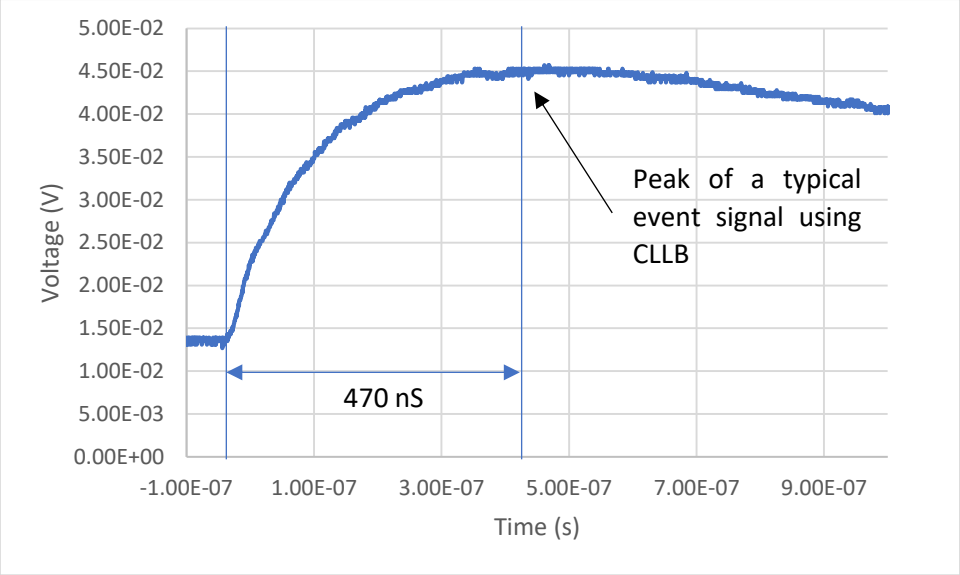

Figure 4-5 Leading edge rise time measurement of 470 nS based on the event in Figure 4-4.

The sine wave fit, frequency approximation using the measurement in Figure 4-5 is shown below in Equation 4-3, as assumes the completion of a full sine wave period, where the measurement shown represents $\frac{\pi}{2}$.

$$\frac{1}{4 \times 470_{ns}} = 532\ kHz$$

Equation 4-3 Calculating a sine wave fit approximation using the measurement in Figure 4-5.

Using 532 kHz as f in Equation 4-1, the time delay using the selected components is calculated as 91.7 nS.

4.2.3 Simulating the delay circuit

The selected amplifier used in the all pass filter to generate the delay is the LTC6261, based on its low current consumption of 240 µA and a bandwidth of 30 MHz, well inclusive of the f_0 frequency.

The simulated circuit is shown in Figure 4-6, where the calculated 532 kHz rising edge approximation frequency is used as a simulated voltage source to check the desired delayed response output, where the simulated output waveforms are shown in Figure 4-7.

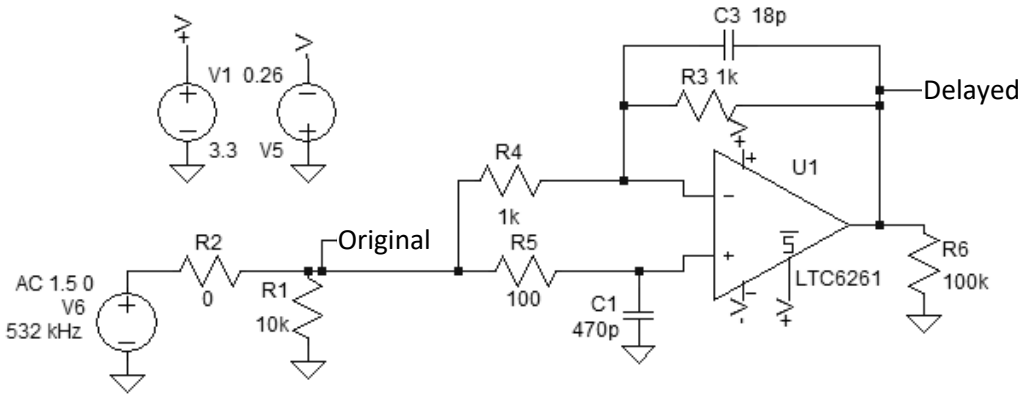

Figure 4-6 Simulated All Pass circuit used to generate the signal time delay.

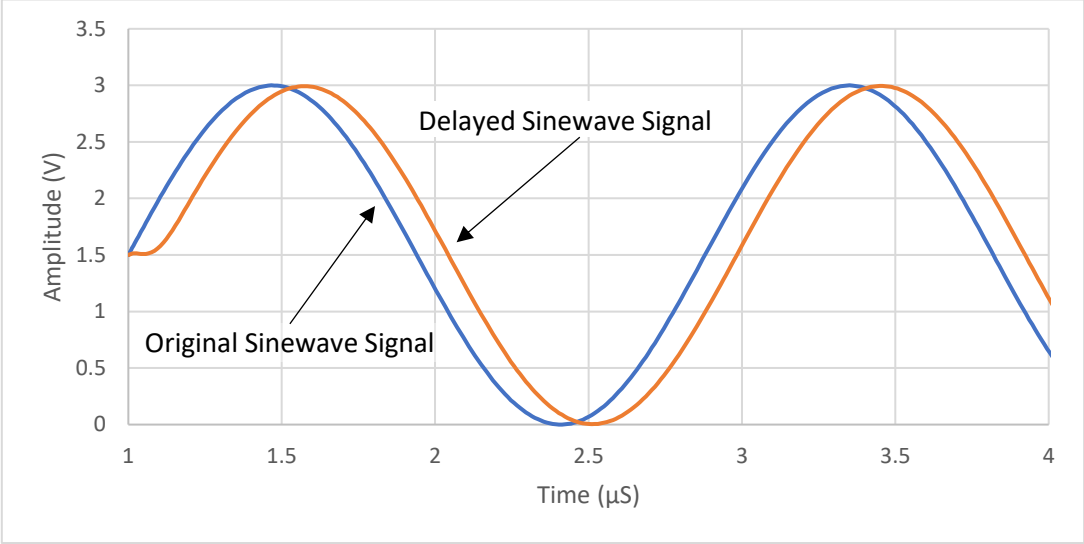

Figure 4-7 Simulated results of using the circuit in Figure 4-6, showing a delayed output of the input waveform of 99 nS.

The simulated delay of 99 nS is close to the calculated delay of the all pass circuit, where the difference is can be explained by properties of the amplifier that the simulator is using in its calculations. Simulating the same circuit with different op-amps in place yields different delays, for example if an LT6220 or an LTC6240 amplifier is used, a delay of 96 nS and 110 nS is simulated respectively.

Simulating the all pass delay circuit with a typical, amplified scintillation event pulse can be seen in Figure 4-8.

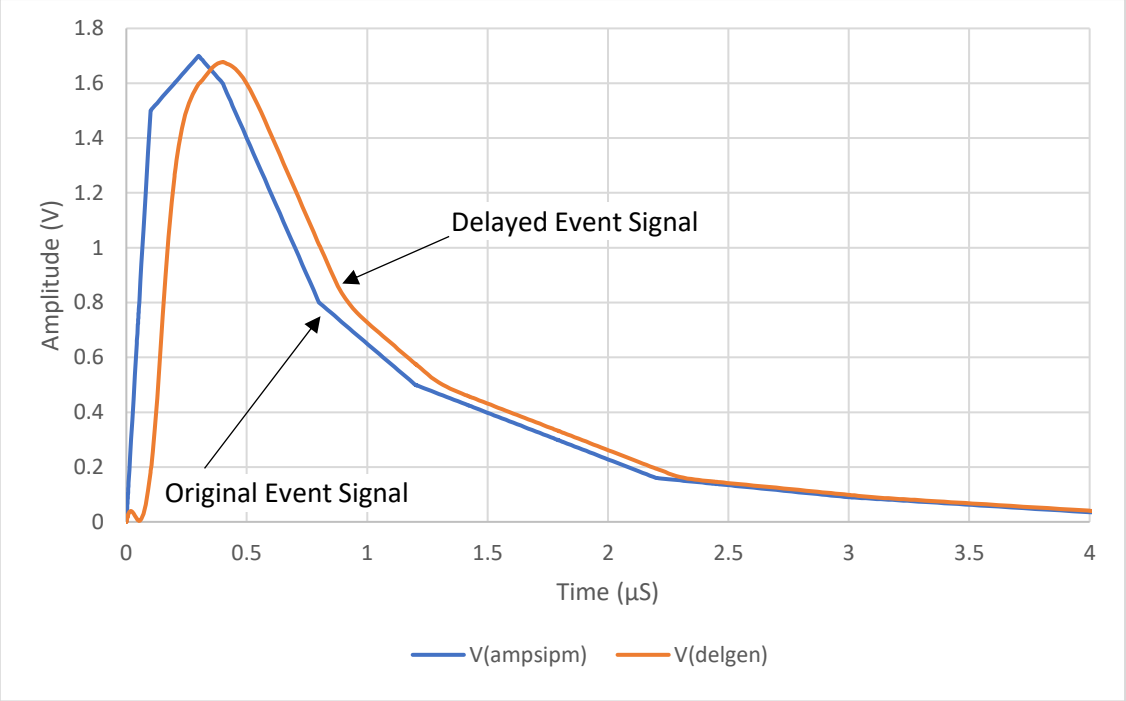

Figure 4-8 Simulating the All Pass delay circuit with a typical scintillation event signal.

The compression effect can be seen on the delayed signal in Figure 4-8, as discussed in section 4.2.2. This was simulated and tested for use with the windowing discrimination method.

4.2.4 Window Generation

Similar to the peak time error correction method in section 4.2.1, adjusting the amplitude of the delayed or original scintillation event signal relative to each other changes the time at which the signals intersect each other, at which point the comparator can change state. By using 2 comparators 1 for the upper % window, and 1 the lower % window intersect point, the time between the two comparator output changes can be measured using a timer circuit element. The timer in this design is an FPGA counter, however could be an adjustable logic pulse comparison. Figure 4-9 shows the generation of the start of the time window W1, where Equation 4-4 shows the calculation for the intersect time, with 'A' referring to the associated comparator designation.

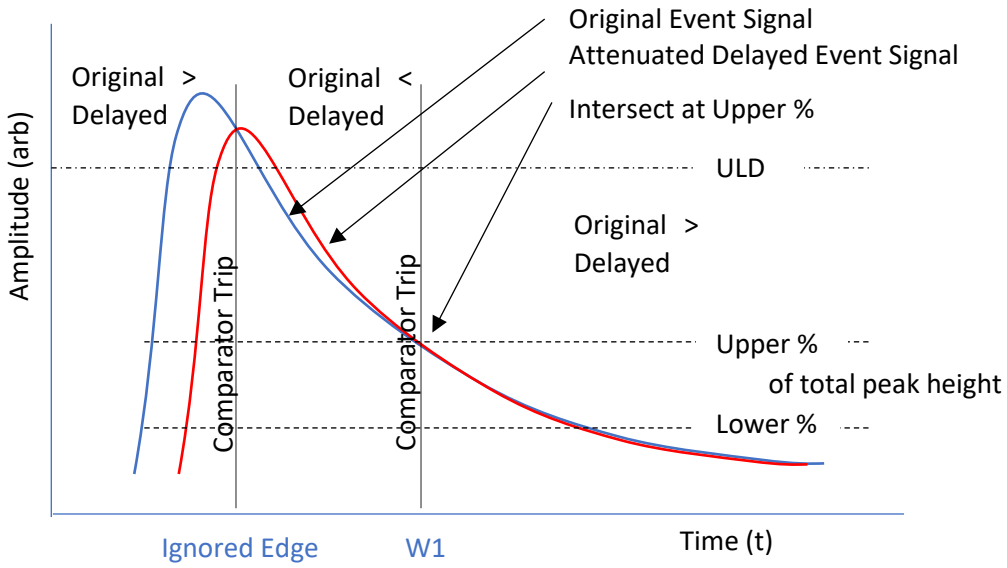

Figure 4-9 Diagram showing the adjustment of the original and delayed event signals to adjust the intersect time point to generate W1.

$$t_{W1} = t_{original}\ \frac{R2_{A-}}{R1_{A-} + R2_{A-}} + t_{delay}\ \frac{R2_{A+}}{R1_{A+} + R2_{A+}}$$

Equation 4-4 Calculating the relative amplitude intersect time point for W1.

R1 and R2 are the potential divider resistors placed on both the positive and negative signal input of the comparator for the delayed and original event signal amplitude adjustment. The potential divider ratios, relative to each input determine the % threshold. W1 and W2 are both points in time relative to the original event signal at which the comparator changes, where the delay is not fixed due to the frequency dependency of the all pass and the frequency content of the scintillation event signal. Figure 4-10 shows the generation of the end of the time window W2, where Equation 4-5 shows the calculation for the intersect time, with 'B' referring to the associated comparator designation. The time between W1 and W2 is then measured and used for the discrimination decision.

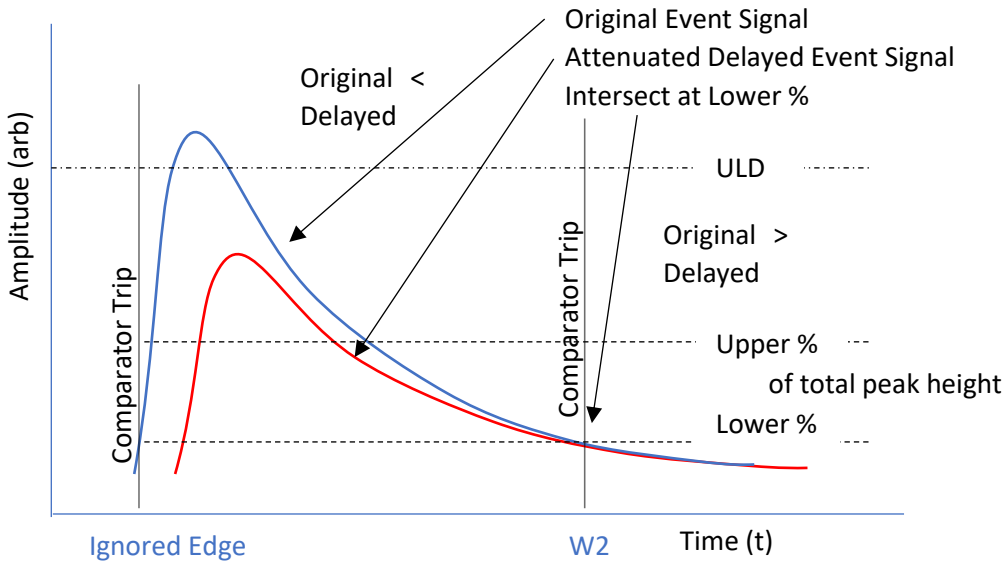

Figure 4-10 Diagram showing the adjustment of the original and delayed event signals to adjust the intersect point to generate W2.

$$t_{W2} = t_{original}\ \frac{R2_{B-}}{R1_{B-} + R2_{B-}} + t_{delay}\ \frac{R2_{B+}}{R1_{B+} + R2_{B+}}$$

Equation 4-5 Calculating the relative amplitude intersect time point for W2.

Figure 4-11 shows the comparator configuration to generate the discrimination window, where the LT1720 has been used for simulation part availability purposes, where its performance closely matches the LMV7219 part. The resistor values represent upper and lower percentage window values of 52% and 25% respectively, values found using a simulation of the circuit.

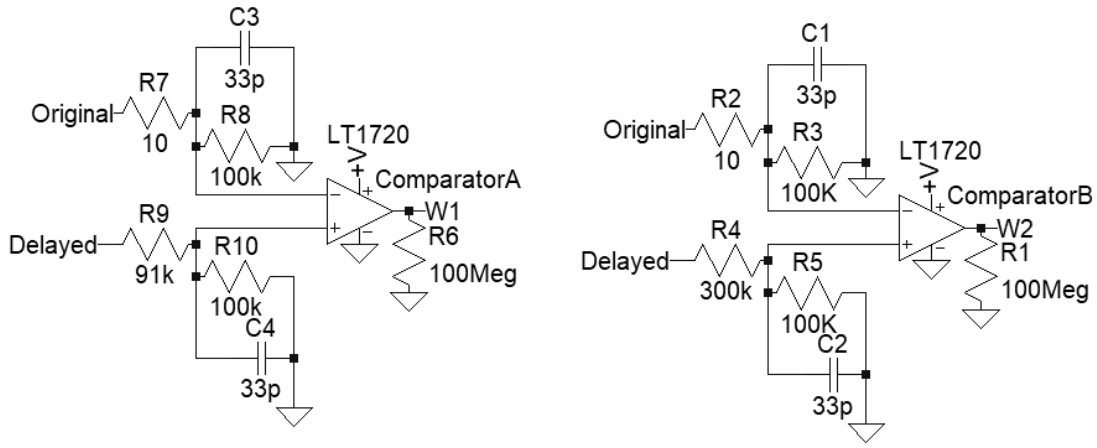

Figure 4-11 Discrimination window generation using two comparators.

4.3 Discrimination System Design

The analogue system designed for gamma neutron discrimination is shown in Figure 4-12, where similar to the previous FPGA ADC system, SiPMs biased into the Geiger mode operation were used to capture the photon emissions from the CLLB dual gamma neutron scintillator, and the SiPM electrical signal is then amplified before entering the discrimination circuitry. An adjustable potential divider was used for the prototype design however, a DAC can also be used for digital adjustment of the LLD and ULD.

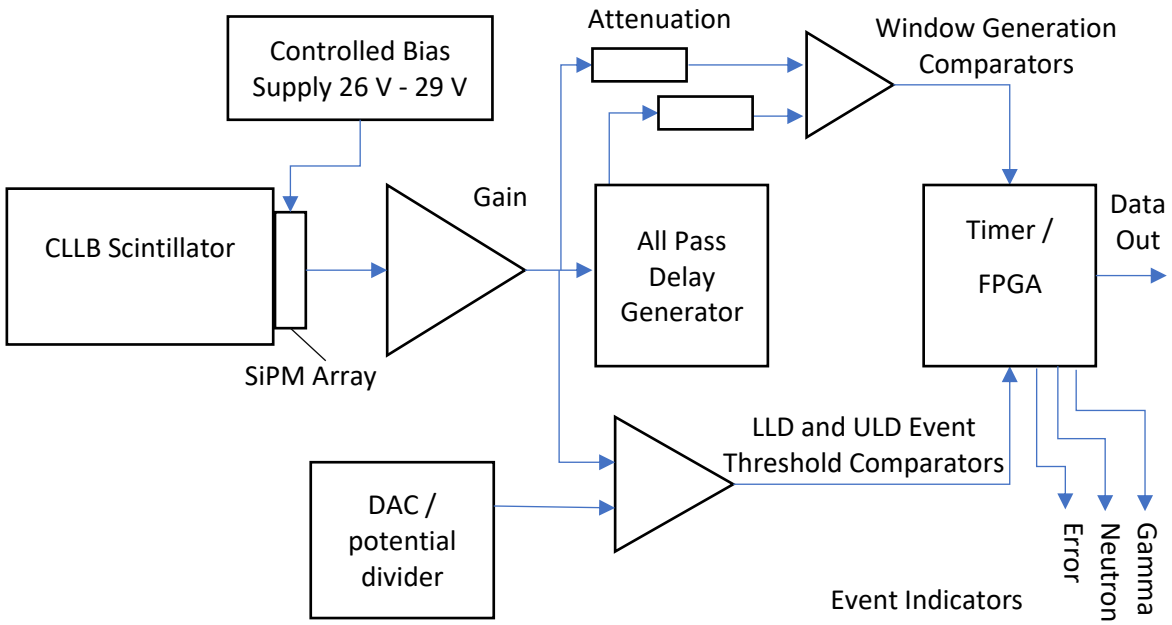

Figure 4-12 Designed gamma neutron discrimination system.

4.3.1 FPGA Window Timer and Program Design

The diagram in Figure 4-13 shows the timer unit implemented in the FPGA. As mentioned, the discrimination decision is only required for events that are greater than the ULD, therefore the timer unit is only enabled after a ULD trigger output. The timer result output data is then ready upon the W2 stop signal, and then can be reset and disabled, ready for the next event.

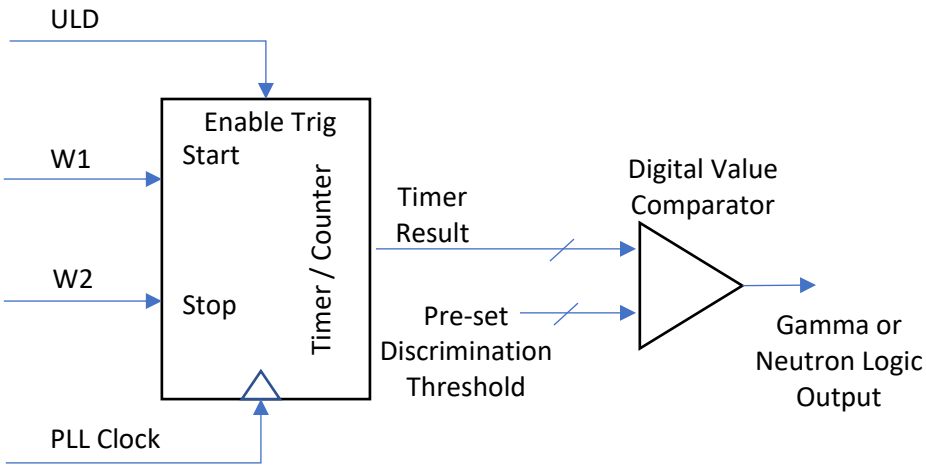

Figure 4-13 Timer unit diagram implemented in the FPGA for window time measurement.

For the prototype, an RGB LED was used to visually check the discrimination outcome of each radiation event above the ULD. The timer result data was compared with a digital value adjustable in the VHDL code, where the gamma or neutron outcome was used to drive an assigned colour of the RGB LED. An error colour was also used for any over range events, where the timer unit overflowed.

4.3.2 Simulation of the Discrimination System

Combining the circuit elements discussed in section 4.2, a full system was simulated in order to determine the best upper and lower percentage threshold for gamma neutron discrimination. By using the simulation circuit in Appendix C to step through different values for the window percentages, a maximum window time difference between the simulated gamma and neutron events was found. The results for simulated schematic in Appendix C are shown in Figure 4-14.

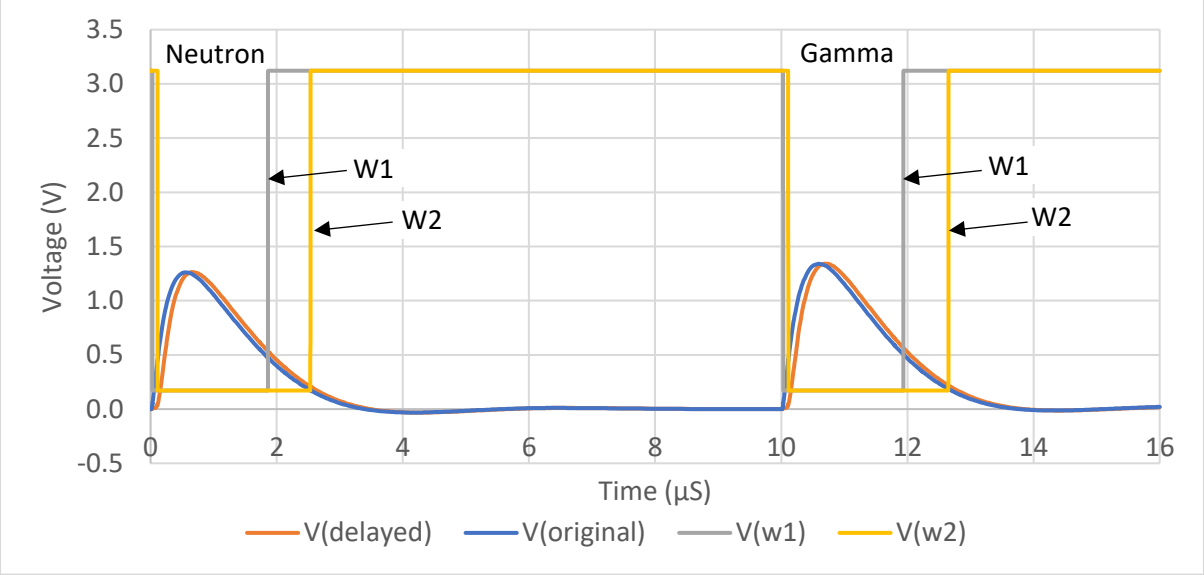

Figure 4-14 Simulated discrimination circuit results, showing window for neutron (1st event) and a gamma (2nd event).

Looking at each event closely, the time measurement between the two comparator rising edges are measured as 670 nS for the neutron event, and 710 nS for the gamma event, as shown in Figure 4-15 and Figure 4-16.

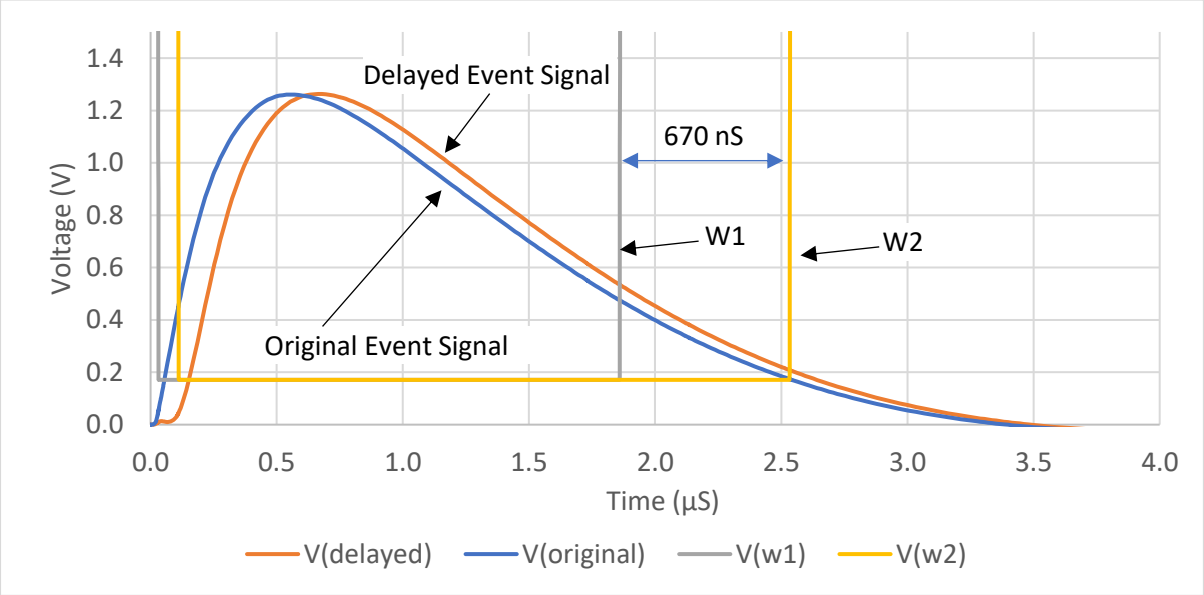

Figure 4-15 Simulated neutron event window measurement.

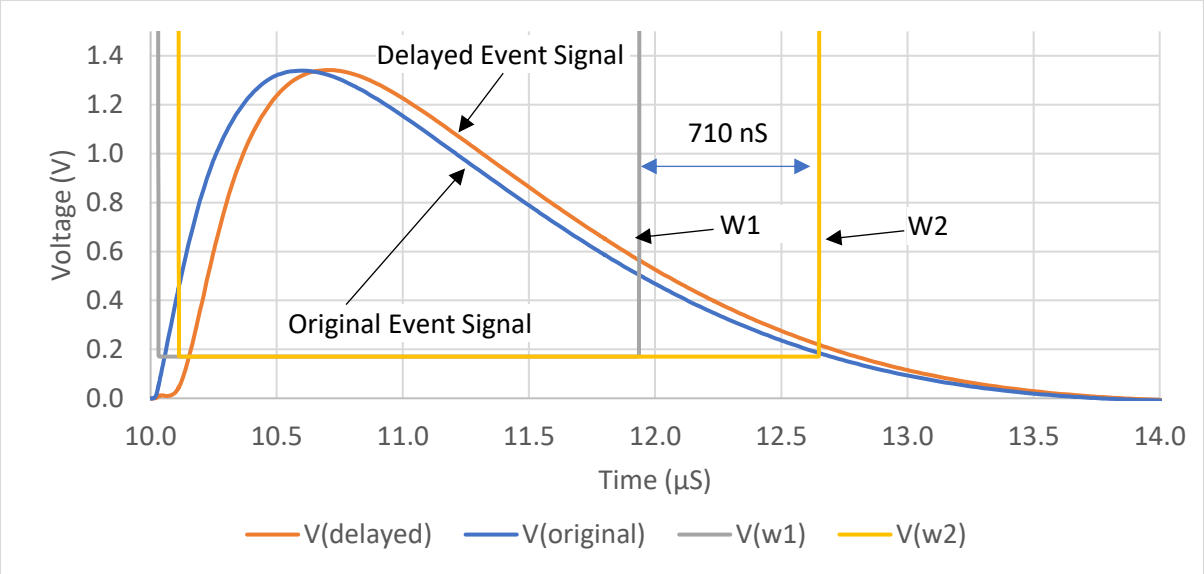

Figure 4-16 Simulated gamma event window measurement.

Although the simulation shows that a discrimination can be made, a difference of 40nS between a gamma and neutron event would require a fast timer of greater than at least two times the time period difference, therefore greater than 500 MHz. This is not ideal for power consumption, as Phase Locked Loops (PLLs) consume more power as the output frequency increases. The FPGA on the DE0 Nano development board used for the ADC system is capable of generating clock of up to 570 MHz using the onboard PLL, which can be used for a counter.

4.4 Testing the Prototype Discrimination Circuit

A prototype discrimination circuit was built, implementing the all pass delay and windowing circuits, and bringing the comparator outputs to the FPGA also used in section 3, where the difference between the W1 and W2 window markers were measured, and sent to a computer via the designed UART terminal explained in section 3.6.1. The SiPM array attached to the CLLB crystal was a 4x4 array of J-Series SensL SiPMs biased at 27.8V. The created schematic that implements the circuit design from each of the system elements and can be seen in Appendix D. A rendering of the designed, outsourced manufactured and populated PCB used for testing the circuit can also be seen in Appendix D.

4.4.1 Measuring the Delay Generated

The delay generated by the designed all pass circuit, using the LTC6261 amplifier was measured, where the results are shown in Figure 4-17.

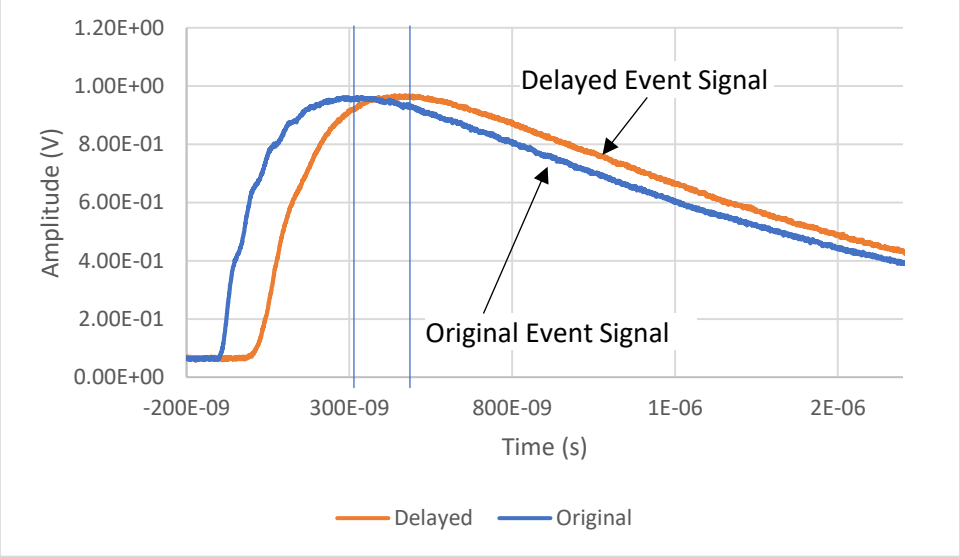

Figure 4-17 Measuring the generated signal delay in the prototype circuit, showing a delay of 173 nS.

The delay generated was longer than simulated and calculated, however is only beneficial for circuit performance, as longer delay improves the comparators triggering accuracy over relying on the hysteresis.

4.4.2 Setting the ULD

By using a Cs137 radiation source, its 662 keV energy emission can be used to map the amplitude of the scintillation event signal to its corresponding energy, to then establish energy ranges. CLLB has good linear scintillation properties, where a reasonably linearly proportional number of photons is emitted per keV in the radiation interaction. Since a neutron interaction will cause a scintillation event equivalent to approximately 3.2MeV, the calculation in Equation 4-6 can be used to determine the expected amplitude of the neutron scintillation event signal from the SiPM output. The Cs137 event

amplitude of 32.125 mV in Figure 4-4 will be used for the 662 keV reference, where using an oscilloscope with display persistence, the most common event amplitude (with exception of the low level 30 keV emission) will be the 662 keV energy emission. The oscilloscope trace used can be seen in Appendix E.

$$32.125\ mV\ \times \frac{3.2\ MeV}{0.662\ MeV} = 155.3\ mV$$

Equation 4-6 Calculating the expected amplitude of neutron scintillation events using a Cs137 event amplitude reference.

Given the neutron range as suggested by Figure 2-7 of 3 MeV to 3.4 MeV the ULD can therefore be set to approximately 145 mV as any event below this will be determined automatically as a gamma event, and any events with an amplitude greater than the ULD threshold will be determined as gamma or neutron based on the discrimination circuit result. These amplitudes are based on SiPM output amplitudes and can be scaled when setting the thresholds according to the gain on the SiPM amplifier.

4.5 Results and Analysis

The discrimination circuit prototype was firstly tested by using individual gamma and neutron sources, to establish a known readout expectation of the system with each source. A Californium 252 neutron source (Cf 252) that can be seen in Appendix E, was used to show the typical system performance using an oscilloscope to monitor the SiPM event signal, and the W1 and W2 comparator outputs. This can be seen in Figure 4-18.

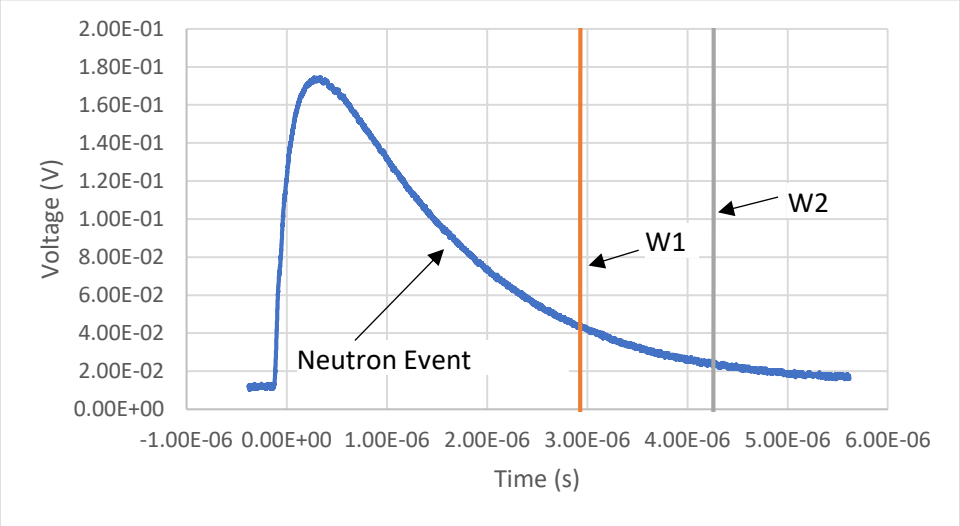

Figure 4-18 Oscilloscope trace showing a neutron event with the discrimination window.

A directional (by lead case) Cs137 source that can be seen in Appendix E, was used as the gamma radiation source to identify a distinguishable pulse shape difference for gamma events. A high energy gamma event likely to be cosmic radiation was then captured, as this would be an event with equivalent energy to that of a neutron event that the would require a discrimination result. The typical

system performance can be seen in Figure 4-19, with the same test setup as used for capturing the neutron event with the system.

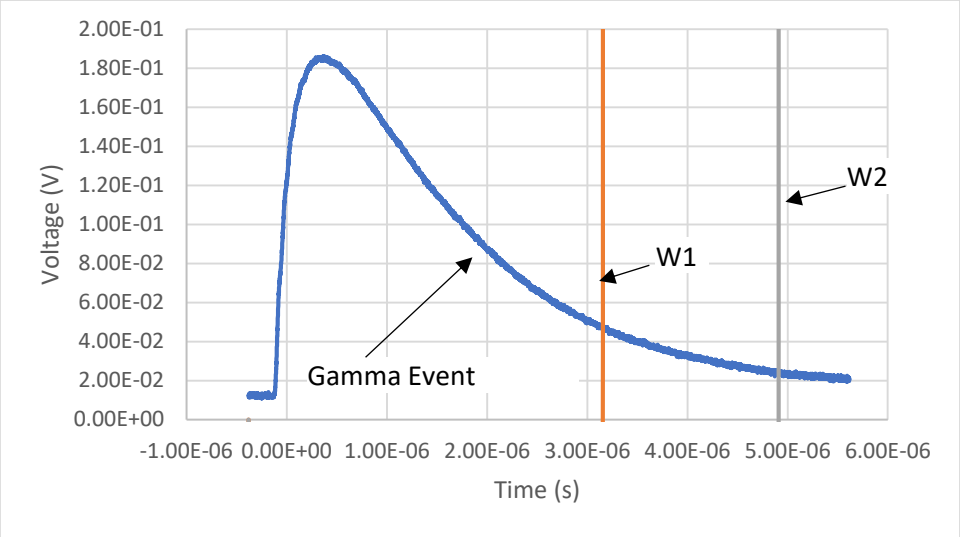

Figure 4-19 Oscilloscope trace showing a gamma event with the discrimination window.

When comparing the two events and the associated comparator outputs for the windowing discrimination system, the window movement and lengthening can be seen for the gamma event compared to the neutron event. This is shown in Figure 4-20, where the counter measurement result from the FPGA application for each window is also shown. The calculations for converting the counter result to a window time is shown in Equation 4-7, where the window times calculated match with the oscilloscope trace in Figure 4-20.

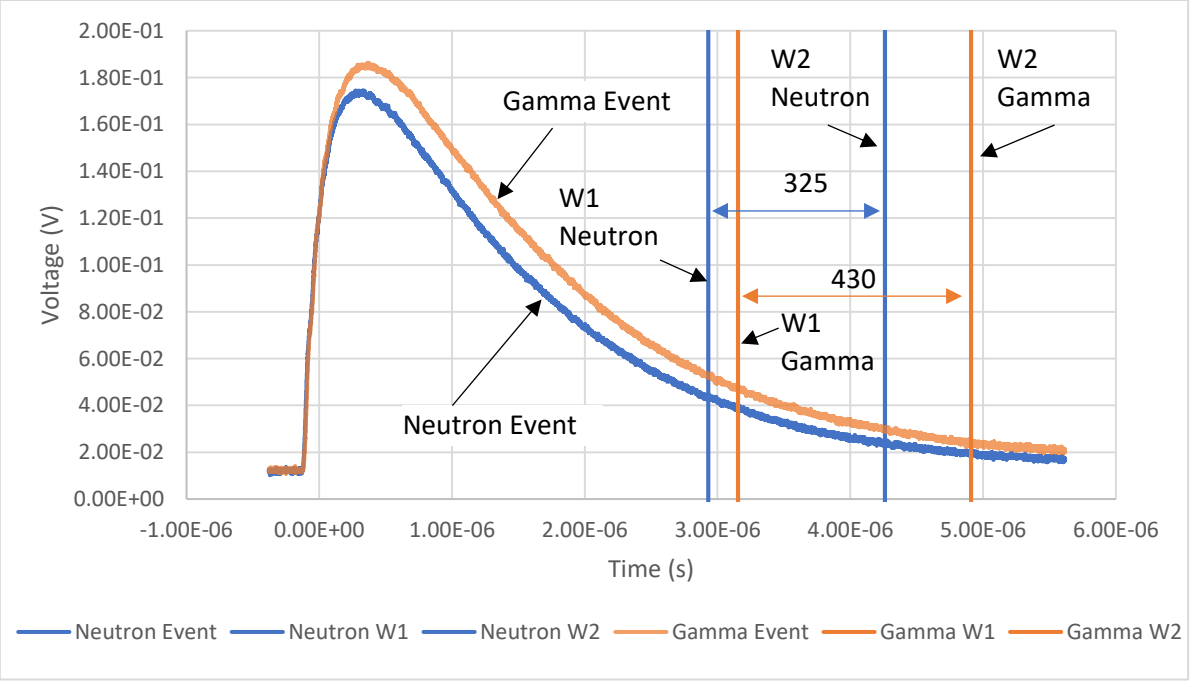

Figure 4-20 Oscilloscope trace showing a neutron and gamma event with the discrimination windows.

$$\frac{1}{250\ MHz} \times 325 = 1.3\ \mu S$$

$$\frac{1}{250\ MHz} \times 430 = 1.72\ \mu S$$

Equation 4-7 Calculations showing the conversion of the counter result to a discrimination window time for a neutron event (top) and gamma event (bottom).

The 420 nS difference between the gamma and neutron window results shows a good indication that the system is able to discriminate, where the window lengths are also longer than simulated. This is beneficial to the system and is likely the result of the increased signal delay introduced by the all pass filter configuration. By collecting a batch of random events and plotting the window times on the histogram in Figure 4-21, two distinct regions of window times can be seen, where neutron event window times fall approximately between counter results of 310 to 390, and 450 to 550 for gamma events. The histogram can then be used to calculate the system performance.

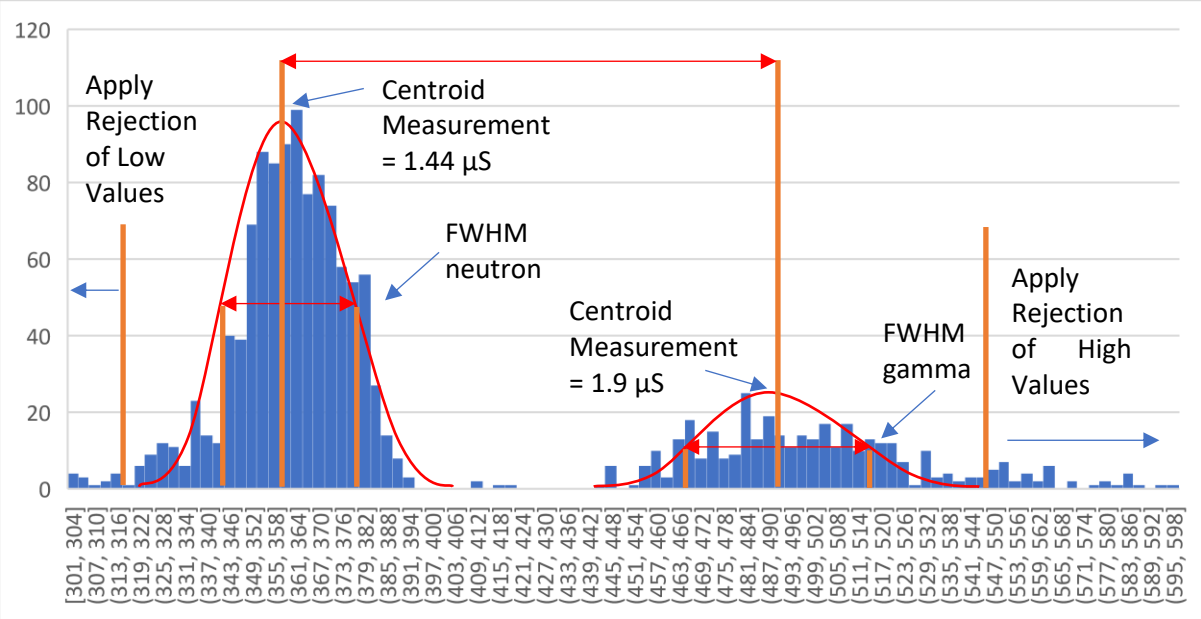

Figure 4-21 Histogram of window times using the discrimination system with gamma and neutron radiation sources, with FOM measurement annotations using a 250 MHz counter clock.

4.5.1 System Figure of Merit

As explored in section 2.4, the FOM is used to gauge the system's discrimination effectiveness. Gaussian fitting has been added to the histogram, with the aim of defining the distinct neutron and gamma event results. The centroid of each gaussian fit can then be seen, where the centroid measurement for neutron events is 1.44 µS, and 1.9 µS for gamma events, having converted the counter results to window times. The full width, half maximum (FWHM) measurement is taken by using the width of the gaussian shape, at half its maximum amplitude, and is also shown in Figure

4-21. The values for these can be seen in Equation 4-8, where the system FOM is shown using Equation 2-1.

$$\frac{492 - 357}{(517 - 467) + (376 - 346)} = 1.68$$

Equation 4-8 Worked figure of merit calculation based on the discrimination histogram results in Figure 4-21.

The FOM shows that discrimination between gamma and neutron events has been achieved, where a decision threshold can be set to a window counter result between 409 and 440, thereby categorising the events live in operation. If an event with window counters is greater than the decision threshold, the event can be determined as a gamma event, and subsequently energy information of the event can be captured, using traditional analogue methods of pulse shaping and peak capture for example. If the event is below the set window counter value, the event can be determined as a neutron and no further energy processing is then required for the event capture.

4.5.2 Power Consumption

The total power consumption of the prototype system, excluding the FPGA as this can be application specific, is shown in Table 4-1. The table also includes an in system SiPM bias supply, replacing the use of the external power supply used for the prototype.

Component	Current Consumption
Pre-Amplifier (LTC6161)	240 µA
Delay Amplifier (LTC6161)	240 µA
Window, LLD and ULD comparators 4x (LMV7219)	4 mA
In system bias supply (LT8410) and SiPMs	50 µA
Total Current	**4.530 mA**
System Voltage	3.3 V
Total Power	**14.949 mW**

Table 4-1 Power consumption properties of the proposed prototype discrimination system.

Since the circuit is intended for portable products requiring low power consumption further improvements to the discrimination were found.

4.6 System Improvements

Whilst a FOM of 1.68 indicates discrimination is achievable, some events cause counter results greater than the gamma events gaussian fit shown in Figure 4-21. Extremely high window values are caused by radiation events likely cosmic again, with higher energy than the desired monitoring range of the detector. This then causes the pre-amplifier after the SiPM event signal output to saturate where an

example of this can be seen in Appendix E. By identifying these events and categorising them as erroneous events, they can be rejected in the FPGA application.

Window counter results below the neutron gaussian fit have also being captured and can be rejected also now the system characteristics can be seen in the generated histogram. Detection and rejection of pulse pile up events captured, and the potential to further optimise the amplitude threshold of the ULD, would decrease the low counter results. Optimising both the over range erroneous events and the ULD threshold can then yield further improvements in the discrimination system and FOM.

The use of the FPGA with the PLL running at 250 MHz contributes to a sizeable proportion of power usage in the discrimination system. Whilst the FPGA selection would be optimised in a designed product for low power, such as selecting a low power Lattice ICE family FPGA or combining applications onto the FPGA for other product functions, at the discrimination system level the PLL clock can be reduced to save power. Whilst halving the PLL clock to 125 MHz would halve the window counter precision, the gap of 31 counts between the neutron and gamma gaussian fits in Figure 4-21 can be halved to 15 counts with minimal error introduction. Using a system clock of 125 MHz would also allow a range of microcontrollers with timer or counter units available to industry, to perform the same discrimination application in a detector product.

Another solution to ease hardware requirements, particularly if working with microcontroller timer modules, that typically have a pulse width counter, would be to use logic to form single digital pulse for the window, rather than relying on the separate W1 and W2 signals. The addition of an exclusive or (XOR) gate combines the W1 and W2 signals, whilst only providing a true output during the difference between the W1 and W2 rising edges, as shown in Figure 4-22.

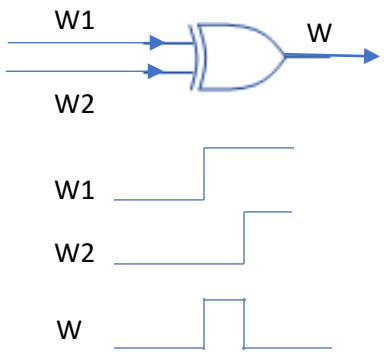

Figure 4-22 XOR gate used to create a logic pulse with the length matching the difference between W1 and W2 rising edges.

Alternatively, the timer requirement can be removed from the system, and a programable monostable stable element and a further XOR gate can be added, where the monostable pulse is programmed to be the decision threshold length, similar to the counter value with the FPGA. The example in Figure

4-23 shows a scenario where if the W pulse exceeds that of the non-re-triggerable monostable output, the XOR gate output will be true for the difference, where the pulse would then indicate a gamma event. If no pulse was produced at output D, and an event was detected by the ULD threshold comparator, then the event detected was caused by a neutron.

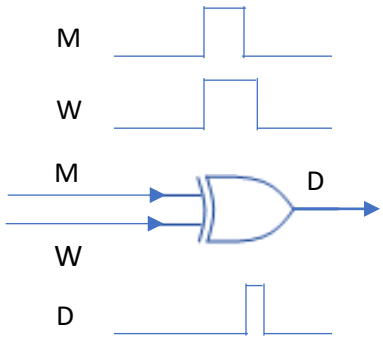

Figure 4-23 Using a monostable and XOR logic as the decision threshold in the discrimination system.

For both window pulse methods, whether by pulse measurement or monostable comparison, logic would also need to be added so that the difference in W1 and W2 falling edges is ignored by the system. This could be achieved by only counting the first window pulse after the ULD trigger.

Removing the window counter requirement, the requirement for a fast PLL clock also is removed, therefore saving power in the chosen microcontroller or FPGA selected for the remaining product application as a lower processing clock can be used. A further power saving can be made by optimising the comparators selected for the windowing and ULD, LLD thresholds. The TLV3201 comparator consumes only 40 µA compared to the 1 mA of the LMV7219 comparator. A compromise is made with the increase from 7 nS to 40 nS of the comparator output propagation time, however so long as this remains constant through operation, the only effect of this will be the 33 nS time latency of the same window pulse, where the pulse window width at the comparator output will not be affected. This represents a total saving of 3.84 mA, or 12.67 mW over the 4 comparators required in the system.

4.7 Spectroscopic System Design with Gamma Neutron Discrimination

By using the analogue gamma neutron discrimination developed, a traditional detector circuit can be enhanced to provide a system cable of gamma spectroscopy and neutron detection. Taking further advantage of new signals available, an issue where the LLD trigger changes time position relative to the shaped signal rising edge at different amplitudes, further causing variable ADC sample points in time causes degradation in the linearity of the gamma spectrum. This effect is called amplitude, or rise time walk (Knoll G. F., Radiation Detection and Measurement, 2010). Designing the circuit so the LLD is triggered on the amplified SiPM event signal rather than the semi-gaussian shaped signal, the

peak position of the shaped signals remains at a reasonably constant time difference to the faster event rising edge for the LLD trigger. By using a second monostable to generate a logic pulse for this time difference, this monostable can then be used to directly trigger the ADC conversion on the AD7980.

The AD7980 can be used as a track and hold ADC, where its input sample capacitor is held on the input signal, in this case the shaped signal (Analog Devices, 2017). Upon the end of the monostable, the peak of the semi-gaussian shaped signal can be sampled. This eliminates the peak capture requirement, and any digital control over event sample timing and peak hold resetting.

The proposed spectroscopic gamma and neutron radiation detection system shown in Figure 4-24 brings together technology reviewed in section 2 such as the analogue pulse processing methods, the designed analogue gamma discrimination system and the associated improvements to fully exploit the dual gamma neutron scintillator CLLB and SiPM technology. System control elements, such as the bias control is also shown, and the proposed circuit components and power calculations are shown in Table 4-2, with a total power consumption of 14.4 mW for a product system.

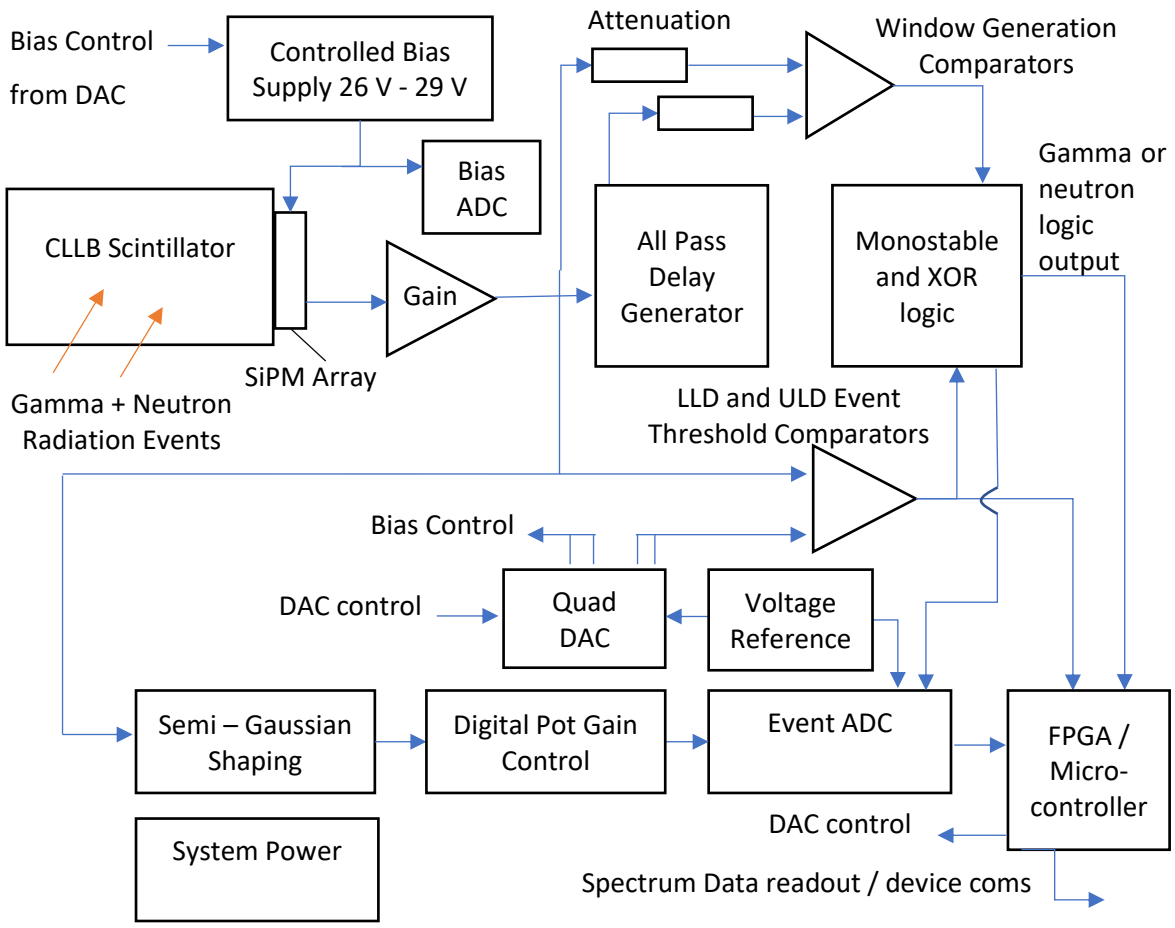

Figure 4-24 Proposed spectroscopic gamma and neutron radiation detection system for portable, low power devices.

Component	Current Consumption
Pre-Amplifier (LTC6261)	240 µA
Delay Amplifier (LTC6261)	240 µA
Shaping Amplifier 2x(LTC6261)	480 µA
Window, LLD and ULD comparators 4x (TLV3201)	160 µA
In system bias supply (LT8410) and 3x SensL J-Series SiPMs	50 µA
Event ADC (AD7980)	212 µA (based on background radiation activity of 100 events per second)
LLD, ULD Thresholds and Bias Control Quad DAC (AD5667)	900 µA
ADC / DAC voltage reference (REF3425)	95 µA
Bias Readback ADC (MCP3422)	135 µA
Dual Monostable (SN74LV221A)	200 µA (based on background radiation activity)
Dual XOR logic (SN74LVC2G86)	20 µA
Gain Control Digital Potentiometer MCP4551	2.5 µA
Proposed System Current	**2.1845 mA**
Lattice ice40LM series FPGA	111 µA Static 1.7 mA Basic spectrum accumulation application
Circuit Losses + Power Regulator I.C. estimate	370 µA
Total Proposed System Current	**4.3655 mA**
System Voltage	3.3 V
Total Power	**14.4 mW**

Table 4-2 Complete gamma spectroscopic and neutron detection system components proposed using the improvements suggested to the discrimination system.

4.8 Section Conclusion

The gamma neutron discrimination method in the prototype achieved successful gamma neutron discrimination as indicated by the FOM achieved and was successfully implemented with electronic circuitry in the prototype system. The designed discrimination circuitry and proposed product ready system provides a low power and portable gamma neutron detection solution. The gamma neutron discrimination capability for the designed discrimination method and circuit implementation yielded a good FOM of 1.68 for a proposed system power cost of as low as 14.4 mW. Using only a single scintillation crystal not only saves space, but also the cost in using two scintillators, and two sets of SiPMs and associated processing circuitry. The discrimination methods could also be used for other applications such as radar, where pulse analysis plays a key role in interpreting the radar information feedback.

5 Conclusion

For applications that wish to continuously improve the performance and efficiency of the radiation detection capability by applying the latest processing knowledge and scintillator characterisations or be first to market with an emerging scintillation detector, the ability to modify and add digital processing methods to a low power continuous sampling acquisition system allows for this in utilising the folding ADC and FPGA system. Continuous learning and research findings into existing scintillators, and new dual scintillators can be added to a product via firmware over the air update to the FPGA application, allowing a detector product to remain state of the art for longer whilst in service.

Whilst some of the latest portable radiation detectors already achieve power consumptions of 300 mW as mentioned in section 1.2, the use of the Folding ADC in portable detectors with its power consumption of 100 mW, leaves 200 mW for the remaining detector system electronics. As mentioned in section 3.11, if the remaining application processing requirements was handled by the FPGA, the power consumption increase upon the 100 mW would be minimal, therefore achieving the research aim of developing low power, high count rate capable, and flexible technology for radiation detectors.

Systems using now well characterised scintillations such as CLLB for increasingly smaller portable products desiring extended operating times or tight battery requirements, a product utilising the low power analogue gamma neutron discrimination system provides a solution that achieves low power operation with the advantage of providing both gamma and neutron radiation detection with the use of only one scintillation crystal. The proposed solution, only requiring as low as 14.4 mW of power is substantially lower than the 300 mW power consumption of the current detector device technology, allowing substantial device operational time improvements to what is currently achievable from a single battery charge.

Both methods enhance the capabilities of existing detector systems by bringing traditionally bench top applications and capabilities to a portable product, and allowing a smaller, more power efficient product. Both methods allow for the use of spectroscopic gamma and neutron processing, where accurate spectrum resolutions can be achieved due to the accurate capture of the scintillation characteristics and pulse shape, thereby being able to locate and identify any illicit or hazardous radioactive material and boosting security in society.

5.1 Achieving the Research Objectives

The following points summarise the achievements made towards the objectives in section 1.3.

- The background and latest innovations in scintillation based radiation detection were evaluated, where the improvements in scintillator and SiPM technology has already proved useful to achieving compact gamma spectroscopic devices.
- The key focus on the event characteristics gained from the literature review, and the appreciation of the background detection physics including the use of SiPM technology and pulse shape discrimination methods that already sets the foundation for the novel detection systems designed in this research.
- Two detection systems are designed, prototyped and tested in this research. The first is an efficient power vs performance system that focus on providing the ability to capture the radiation event signal digitally, with the required accuracy to allow for gamma spectroscopy and gamma neutron discrimination. The configurability of digital logic in the FPGA used in the system ensures flexibility for different applications, where different scintillators can then be used. The second detection system utilises a novel windowing system, using the state of the art gamma neutron scintillator CLLB, an all pass filter, and timings between comparator thresholds to achieve gamma neutron discrimination with a FOM of 1.68. Further to this, it is shown that by enhancing the traditional circuitry used in gamma spectroscopic for low power consumption, a detection system can be implemented with a power consumption figure as low as 14.4 mW.
- Results were taken with both detection systems, and their suitability for compact, longer operation time hand held radiation detection devices was evaluated, where the innovations in this research prove to enhance the capability of portable radiation detectors.

5.2 Future Work

With the commercial release of the CLLB product from the manufacturer Saint-Gobain in late 2018, the technology developed provides a solid platform for which it can be rolled out in mass produced products (Saint-Gobain, 2017). The circuits and technology developed could also be utilised in ASICs, of which the drive for developing these as an alternative to standard circuitry based systems' is being realised by the industry, given the drive for mass produced radiation detectors for wide scale deployments, for instance with the DARPA sigma program.

One such ASIC development is the Kromek Apollo ASIC, aimed at entering the market with a balance of high performance, flexible processing and low power operation where it is due for release in the roll out of new portable, separate gamma neutron detectors also in late 2018. The ASIC features 16 sensor input channels, each with customisable analogue processing methods including variable pulse shaping, and adjustable integration windowing. The 16 inputs can be used as separate sensor inputs or tied together from fewer sensor modules to allow multiple processing methods to be performed on the same sensor signal, useful in some methods of gamma neutron pulse shape discrimination. Although not directly part of this research, two development phase circuit boards were designed and manufactured to breakout the ASIC inputs and test its performance for future development, where the designs can be seen in Appendix F.

Using the test PCBs in Appendix F, the ASIC minimum power consumption was found to be 70 mW, where this accounts for the analogue processing circuitry, 3 ADC cores and a 128 MHz PLL for integration timing windows, digital conversion results storage and Serial Peripheral Interface (SPI) communications. Exploiting the flexibility of the development boards in Appendix F allows for spectroscopic testing and gamma neutron testing to be carried out, yielding optimistic resolution results and a discrimination FOM of greater than 1.8, all be it with the higher power consumption.

Where the use of the scintillation detection principals has benefited with the development of SiPM technology in recent years, further development in photon detection technology has allowed for processing circuitry to be added to the same integrated circuit as the SPAD cell. Leading manufactures such as ST and Tower Jazz, and technology developments at the University of Edinburgh and the Politechnico di Milano have pushed the technology forward, where an example developed by the Politechnico di Milano features a 32x32 SPAD array of macropixels, with each macropixel containing 10-bit time to digital converter (TDC) (Villa, Portaluppi, Sanzaro, Conca, & Zappa, 2018). Although the drive in the technology is from LiDAR applications for 3D imagery, it is hoped that the technology can be used to further increase gamma spectrum resolution by both enhanced individual pixel control and gating, as well as gain further power and space savings in scintillation based radiation detection devices.

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Appendix

A. Data Construction Table for the Folding ADC System

1st Sample Odds

Grp	Cx	Array					
		A0	A1	A2	A3	Bin	
E	CA	SA0	x	x	x	x	MSB
O	CB	x	x	x	x	x	
E	CC	n	x	x	x	x	
O	CD	n	x	x	x	x	
E	CE	n	n	x	x	x	
O	CF	n	n	x	x	x	
E	CG	n	n	n	x	x	
O	CH	n	n	n	x	x	LSB

2nd Sample

Grp	Cx	Array					
		A0	A1	A2	A3	Bin	
E	CA	SA0	x	x	x	x	MSB
O	CB	SB0	x	x	x	x	
E	CC	n	x	x	x	x	
O	CD	n	x	x	x	x	
E	CE	n	n	x	x	x	
O	CF	n	n	x	x	x	
E	CG	n	n	n	x	x	
O	CH	n	n	n	x	x	LSB

3rd Sample

Grp	Cx	Array					
		A0	A1	A2	A3	Bin	
E	CA	SA1	SA0	x	x	x	MSB
O	CB	x	SB0	x	x	x	
E	CC	n	SC0	x	x	x	
O	CD	n	x	x	x	x	
E	CE	n	n	x	x	x	
O	CF	n	n	x	x	x	
E	CG	n	n	n	x	x	
O	CH	n	n	n	x	x	LSB

4th Sample

Grp	Cx	Array					
		A0	A1	A2	A3	Bin	
E	CA	SA1	SA0	x	x	x	MSB
O	CB	SB1	SB0	x	x	x	
E	CC	n	SC0	x	x	x	
O	CD	n	SD0	x	x	x	
E	CE	n	n	x	x	x	
O	CF	n	n	x	x	x	
E	CG	n	n	n	x	x	
O	CH	n	n	n	x	x	LSB

5th Sample

Grp	Cx	Array					
		A0	A1	A2	A3	Bin	
E	CA	SA2	SA1	SA0	x	x	MSB
O	CB	x	SB1	SB0	x	x	
E	CC	n	SC1	SC0	x	x	
O	CD	n	x	SD0	x	x	
E	CE	n	n	SE0	x	x	
O	CF	n	n	x	x	x	
E	CG	n	n	n	x	x	
O	CH	n	n	n	x	x	LSB

6th Sample

Grp	Cx	Array					
		A0	A1	A2	A3	Bin	
E	CA	SA2	SA1	SA0	x	x	MSB
O	CB	SB2	SB1	SB0	x	x	
E	CC	n	SC1	SC0	x	x	
O	CD	n	SD1	SD0	x	x	
E	CE	n	n	SE0	x	x	
O	CF	n	n	SF0	x	x	
E	CG	n	n	n	x	x	
O	CH	n	n	n	x	x	LSB

7th Sample

8th Sample

Grp	Cx	Array					
		A0	A1	A2	A3	Bin	
E	CA	SA3	SA2	SA1	SA0	x	MSB
O	CB	x	SB2	SB1	SB0	x	
E	CC	n	SC2	SC1	SC0	x	
O	CD	n	x	SD1	SD0	x	
E	CE	n	n	SE1	SE0	x	
O	CF	n	n	x	SF0	x	
E	CG	n	n	n	SG0	x	
O	CH	n	n	n	x	x	LSB

Grp	Cx	Array					
		A0	A1	A2	A3	Bin	
E	CA	SA3	SA2	SA1	SA0	x	MSB
O	CB	SB3	SB2	SB1	SB0	x	
E	CC	n	SC2	SC1	SC0	x	
O	CD	n	SD2	SD1	SD0	x	
E	CE	n	n	SE1	SE0	x	
O	CF	n	n	SF1	SF0	x	
E	CG	n	n	n	SG0	x	
O	CH	n	n	n	SH0	x	LSB

8th Sample + 1 PLL clock

Grp	Cx	Array					
		A0	A1	A2	A3	Bin	
E	CA	SA3	SA2	SA1	SA0	Bit7	MSB
O	CB	SB3	SB2	SB1	SB0	Bit6	
E	CC	n	SC2	SC1	SC0	Bit5	
O	CD	n	SD2	SD1	SD0	Bit4	
E	CE	n	n	SE1	SE0	Bit3	
O	CF	n	n	SF1	SF0	Bit2	
E	CG	n	n	n	SG0	Bit1	
O	CH	n	n	n	SH0	Bit0	LSB

Key

x = Don't Care

n = not used

Data format example S A 0

Sample Comparator Sample Number

B. VHDL

The VHDL used in the Folding ADC operation. Code text may wrap round with the line formatting, where the colour coding scheme can then be used to identify different terms.

```
-- Folding ADC Operation Control
--Richard Haigh
--12/03/17

-- Uncomment code sections for continuous sample mode
--LLD mode or peak capture mode. sections are encased with
-- _____________________________ and a number marking its
--start and end
-- signal name may not reflect use, check comments.

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

--define external signals
ENTITY FA_CLOCK IS

      PORT  (
                  --clk      :     in std_logic; -- only for using direct
clock, not pll
                  clkp1 , clkp2 , clkp3 , clkp4      :     out std_logic;
                  clkn1 , clkn2 , clkn3  :     out std_logic;
                  PLL_IN : in std_logic;
                  PLL_RST: in std_logic;
                  --PLL_OUT : out std_logic;
                  PLL_LOCK : OUT std_logic;
```

```
                    data_out : out std_logic_vector (7 downto 0);
                    CA0 , CB0 , CC0, CD0 , CE0 , CF0 , CG0 , CH0 : in
std_logic;
                    --O    E     O    E     O     E     O  E  Comparator Grp

                    uart_clock_out : OUT std_logic;


                    utxA : out std_logic;
                    utxB : out std_logic;
                    GorB : in  std_logic;

                    SPI_MOSI , SPI_CS_n , SPI_CLK : out std_logic;

                    just_3V3 : out std_logic;

                   data_gout : out std_logic_vector (7 downto 0);
                   data_ubout : out std_logic_vector (7 downto 0);
                   data_cvalueout : out std_logic_vector (3 downto 0)

                    );

END ENTITY;

ARCHITECTURE behav OF FA_CLOCK IS

component PLLTEST1 is
      PORT
      (
            areset            : IN STD_LOGIC  := '0';
            inclk0            : IN STD_LOGIC  := '0';
            c0          : OUT STD_LOGIC ;
            locked            : OUT STD_LOGIC
      );
END component PLLTEST1;

component codecorrection is -- Experiential code correction unit under
development at UOH
      PORT  (
                    PLL_IN                  : in std_logic;  -- PLL clock
(feb 17: 250 MHz)
                    Clk                           : in std_logic;  -- clock
used for sample and hold (feb 17: 25MHz )
                    res                     : in std_logic;  -- resets all
Difference registers
                    Input_Gray                    : in std_logic_vector (7
downto 0);
                    UncorrectedBINARY       : out std_logic_vector (7 downto
0);
                    CalcDiffValue                       : out
std_logic_vector (3 downto 0);
                    CorrectedBINARY         : out std_logic_vector (7 downto
0)
                    );
END component codecorrection;


-- define internal signals
SIGNAL count      :     integer := 0;
signal valid      : integer :=0;
signal peak       : std_logic_vector (7 downto 0);
```

```
signal clk        : std_logic;

signal A0 : std_logic_vector (1 downto 0);
signal A1 : std_logic_vector (3 downto 0);
signal A2 : std_logic_vector (5 downto 0);
signal A3 : std_logic_vector (7 downto 0);
signal CA1 , CA2 , CB1 , CB2 , CC1 , CC2 , CD1 , CD2 , CE1 , CE2 , CF1 ,
CF2 , CG1, CG2, CH1, CH2 : std_logic;
signal bin_out : Std_logic_vector(7 downto 0);
signal gray_out: std_logic_vector(7 downto 0);

signal frame : std_logic_vector (7 downto 0);
signal baud_diva : integer :=0;
signal baud_divb : integer :=0;
signal tx_en : integer := 0 ;
signal uart1_clk : std_logic;
signal uart1_state : integer :=0;
signal uart1_databuf : std_logic_vector (7 downto 0);
signal uart1_tx_complete : integer :=0;
signal cor_res :std_logic;
signal cor_gray_in : std_logic_vector (7 downto 0);
signal cor_bin_out : std_logic_vector (7 downto 0);
signal cor_ubin_out : std_logic_vector (7 downto 0);
signal cor_diff_value : std_logic_vector (3 downto 0);
signal clkp , clkn : std_logic;
signal sample_en : std_logic;

--define RAM for conversion results storage
type RAM is array (32768 downto 1) of std_logic_vector (7 downto 0);
signal MEM8x4 : RAM; -- MEM is not 8x4 anymore, its 8x32768
signal mem_counter : integer :=0;
signal uart_mem_counter : integer :=1;
--
--Begin the operation of ADC
BEGIN
--PLL is internal predefined hardware accessed by the portmap to it
PLL0: PLLTEST1 port map ( areset=> PLL_RST , inclk0 => PLL_IN , c0 => clk ,
locked => PLL_LOCK); -- portmap PLL
-- Port map the external module, using code under development at the UOH
behav: codecorrection port map ( PLL_IN=> clk ,
                                                                clk=>
clkn ,
                                                                res =>
cor_res ,

      Input_Gray => cor_gray_in ,

      UncorrectedBINARY => cor_ubin_out ,

      CalcDiffValue => cor_diff_value ,

      CorrectedBINARY => cor_bin_out); -- portmap codecorrection


just_3V3 <= '1'; -- for jump GorB connector


-- Uncomment the data out vectors to enable parallel data output for
testing
-- Select Gray or Bin parallel output using GorB jumper
```

```
--data_out(7) <= ((gray_out(7) and GorB) or (bin_out(7) and (not GorB)));
--data_out(6) <= ((gray_out(6) and GorB) or (bin_out(6) and (not GorB)));
--data_out(5) <= ((gray_out(5) and GorB) or (bin_out(5) and (not GorB)));
--data_out(4) <= ((gray_out(4) and GorB) or (bin_out(4) and (not GorB)));
--data_out(3) <= ((gray_out(3) and GorB) or (bin_out(3) and (not GorB)));
--data_out(2) <= ((gray_out(2) and GorB) or (bin_out(2) and (not GorB)));
--data_out(1) <= ((gray_out(1) and GorB) or (bin_out(1) and (not GorB)));
--data_out(0) <= ((gray_out(0) and GorB) or (bin_out(0) and (not GorB)));

--data_out (7 downto 0) <= gray_out (7 downto 0);--Gray Code
data_out (7 downto 0) <= bin_out (7 downto 0);--BIN Code

--Constant assign data logic in and out of code correction unit
--data_out (7 downto 0) <= cor_bin_out (7 downto 0);-- corrected BIN Code
data_ubout (7 downto 0) <= cor_ubin_out (7 downto 0); -- uncorrected bin
code
data_cvalueout (3 downto 0) <= cor_diff_value (3 downto 0); -- gray cor
code
data_gout (7 downto 0 ) <= gray_out (7 downto 0);
cor_res <= GorB;

--devide up clocks used in prototype signal distribution
clkp1 <= clkp;
clkp2 <= clkp;
clkp3 <= clkp;
clkp4 <= clkp;

clkn1 <= clkn;
clkn2 <= clkn;
clkn3 <= clkn;

--data_out (7 downto 0) <= MEM8x4(count);

--uart_clock_out <= uart1_clk; -- pin 40 Pin_J14 D8 scope

--SPI_CLK <= clk;

-- Process starts the clocked operation
      ADC_OPERATION: PROCESS

      BEGIN

            WAIT UNTIL RISING_EDGE(clk);

            -- Non over lapping clock generation statements
            IF count < 4 THEN

                  --MEM8X4 <= ("01111111", "01111111" );

                  clkp <= '0';


                  clkn <= '1';


                  count <= count + 1;

            ELSIF count = 4 THEN
            --non overlap
                  clkp <= '0';
```

```
                clkn <= '0';


                count <= count + 1;

            ELSIF count > 4 AND count < 9 THEN

                clkp <= '1';

                clkn <= '0';

                count <= count + 1;

            ELSIF count = 9 THEN
            --non overlap
                clkp <= '0';


                clkn <= '0';


                count <= 0 ;


            END IF;


            --data control and Syncro

            IF count = 0 THEN-----------------------------------------------
-----------------------------------0
            --sync odds
            CA2 <= CA1;
            CC2 <= CC1;
            CE2 <= CE1;
            CG2 <= CG1;


            ELSIF count = 1 THEN-------------------------------------------
-----------------------------------1
            --load odds in array
            A0(1) <= CA2;
            A1(1) <= CC2;
            A2(1) <= CE2;
            A3(1) <= CG2;


            ELSIF count = 2 THEN-------------------------------------------
-----------------------------------2
            --na



            ELSIF count = 3 THEN-------------------------------------------
-----------------------------------3

--do peak capture here ??
--
--          END IF;
```

```
            ELSIF count = 4 THEN----------------------------------------
----------------------------------4

                  --sample_evens <= '1';
                  CB1 <= CB0;
                  CD1 <= CD0;
                  CF1 <= CF0;
                  CH1 <= CH0;


            ELSIF count = 5 THEN----------------------------------------
----------------------------------5
            -- sync evens 1
                  CB2 <= CB1;
                  CD2 <= CD1;
                  CF2 <= CF1;
                  CH2 <= CH1;


            ELSIF count = 6 THEN----------------------------------------
----------------------------------6
            --load evens in array
            A0(0) <= CB2;
            A1(0) <= CD2;
            A2(0) <= CF2;
            A3(0) <= CH2;


            ELSIF count = 7 THEN----------------------------------------
----------------------------------7
            --shift array, combination logic
            A3(7 downto 2) <= A2 (5 downto 0);
            A2(5 downto 2) <= A1 (3 downto 0);
            A1(3 downto 2) <= A0 (1 downto 0);


            ELSIF count = 8 THEN----------------------------------------
----------------------------------8
            -- convert Gray code to bin on a single clock edge
            bin_out (7) <= A3(7);
            bin_out (6) <= A3(7) xor A3(6);
            bin_out (5) <= (A3(7) xor A3(6)) xor A3(5);
            bin_out (4) <= ((A3(7) xor A3(6)) xor A3(5)) xor A3(4);
            bin_out (3) <= (((A3(7) xor A3(6)) xor A3(5)) xor A3(4))xor
A3(3);
            bin_out (2) <= ((((A3(7) xor A3(6)) xor A3(5)) xor A3(4))xor
A3(3)) xor A3(2);
            bin_out (1) <= (((((A3(7) xor A3(6)) xor A3(5)) xor A3(4))xor
A3(3)) xor A3(2)) xor A3(1);
            bin_out (0) <= ((((((A3(7) xor A3(6)) xor A3(5)) xor A3(4))xor
A3(3)) xor A3(2)) xor A3(1))xor A3(0);

            --load complete parallel gray code to test output or code
correction unit
            gray_out(7 downto 0 ) <= A3(7 downto 0);
            cor_gray_in (7 downto 0 ) <= A3(7 downto 0);


            ELSIF count = 9 THEN----------------------------------------
----------------------------------9
```

```
            --sample odds

                  CA1 <= CA0;
                  CC1 <= CC0;
                  CE1 <= CE0;
                  CG1 <= CG0;

            -- Peak Detect -----------------

                  if peak > bin_out then -- if the held peak value is
greater than the current sample
                        valid <= valid +1;            --add a valid peak
reading

                        if valid = 5 then -- noise suppresion figue  -- 1
is instant, 5 is good 40 used for testing peak out only without trigger
logic
                        uart_clock_out <='1'; -- peak detect confirmed

                        --
_____________________________________________________*1
                        -- Uncomment section for Peak capture

--                if mem_counter < 32768 THEN
--                MEM8X4 (mem_counter) <= peak;
--                mem_counter <= mem_counter+1;
--                SPI_CS_n <= '1';
--                tx_en <= 0;  -- this stops uart transmitting whilst
sampling
--
--          ELSE
--                SPI_CS_n <= '0';
--          --send to uart and reset when uart_mem_counter = 0
--
--                IF tx_en = 0 and uart1_tx_complete = 1 THEN --IF valid >9
and tx_en = 0 and uart1_tx_complete = 1 THEN
----                        --uart out peak if uart is free
--
--                        uart1_databuf <= MEM8X4 (uart_mem_counter);
--                        tx_en <= 1;
--                        uart_mem_counter <= uart_mem_counter +1;
--                        if uart_mem_counter > 32769 then
--                              uart_mem_counter <= 1;
--                              mem_counter <=1;
--                        END IF; -- end uart / mem counter reset
--
--                elsif tx_en = 1 and uart1_tx_complete = 0 then  --states
01 is ready, 10 is reset tx_en, 00 is busy, 11 is ambig
--
--                        tx_en <= 0;
--
--
--                END IF;     --end uart transmission routine
--
--          END IF; -- end memory record and transmit routine

                        --
_____________________________________________________*1
```

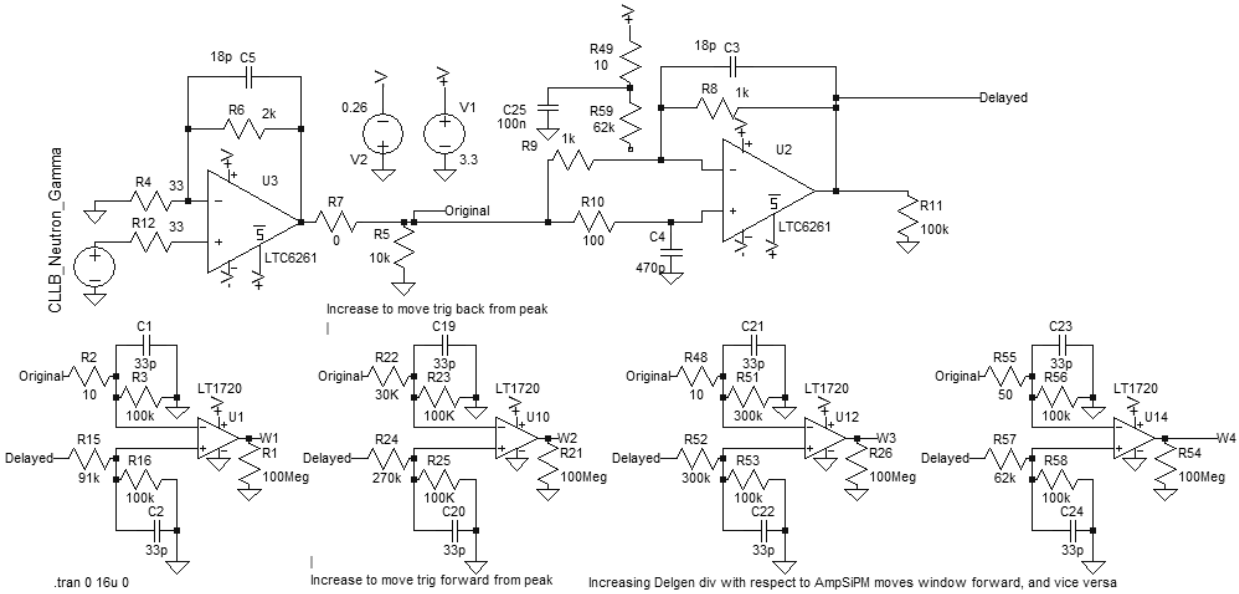
```
                        --valid <= 0;                                   --reset
the valid counter   ***!!!!*** make sure to put back in if contin output is
required    *********
                        --peak <= (others => '0'); -- ( 0 => '1', others =>
'0');--reset for the next peak
                                              ********
                        elsif valid = 70 then  -- delay until peak find
resumes

      *********
                        valid <= 0;                             --reset the
valid counter   ***!!!!*** make sure to put back in if contin output is
required                ********
                        peak <= (others => '0'); -- ( 0 => '1', others =>
'0');--reset for the next peak
                                                 *******

                        else
                        uart_clock_out <='0'; -- sample is lower than peak
but awaiting confirmed
                        end if;

                  else   -- tracking the signal looking for peak
                        uart_clock_out <= '0';  -- peak not confirmed
                        peak <= bin_out;              --track the signal
                        valid <= 0;                   -- no valid peak
                  end if;

            -- send to memory / uart out-----------------

--                if  bin_out > 10 then --software lld  -- ch128 in 8 bit
*3
--
            --if sample_en = '1' then
            --_____________________________________
            --Only leave in for continuous sampling*2 or LLD triggered
sampling
            if mem_counter < 32768 THEN
                  MEM8X4 (mem_counter) <= bin_out;
                  --MEM8X4 (mem_counter+16385) <= cor_ubin_out;
                  mem_counter <= mem_counter+1;
                  SPI_CS_n <= '1';
                  tx_en <= 0;

            ELSE
                  --sample_en <= '0';
                  SPI_CS_n <= '0';
            --send to uart and reset when uart_mem_counter = 0

                  IF tx_en = 0 and uart1_tx_complete = 1 THEN --IF valid >9
and tx_en = 0 and uart1_tx_complete = 1 THEN
--                      --uart out peak if uart is free

                        uart1_databuf <= MEM8X4 (uart_mem_counter);
                        tx_en <= 1;
                        uart_mem_counter <= uart_mem_counter +1;
                        if uart_mem_counter > 32769 then
                              uart_mem_counter <= 1;
                              mem_counter <=1;
                        END IF; -- end uart / mem counter reset
```

```
                  elsif tx_en = 1 and uart1_tx_complete = 0 then  --states
01 is ready, 10 is reset tx_en, 00 is busy, 11 is ambig

                        tx_en <= 0;


                  END IF;     --end uart transmission routine

            END IF; -- end memory record and transmit routine
            --_____________________________________*2
            --END IF; -- End if sample requested
--
--          else
--          end if; -- end lld *3

      END IF;

      END PROCESS ADC_OPERATION;

      ---------------------------------------------------------------------
-------------------------------------------------------------
      -- Generate the clocks for UART
      UART_CLK_GEN: process

      BEGIN

            wait until rising_edge (clk);

            if baud_diva = 250 THEN --     for 39 for 3MBaud@120MHz 6249
for 19200Baud@120MHZ
            baud_diva <=0;

            else
            baud_diva <= baud_diva +1;

            end if;

            if baud_diva < 100 then       -- divide divider by 2
            uart1_clk <= '1';


            elsif baud_diva > 100 AND baud_diva < 200 THEN
            uart1_clk <= '0';


            end if;


      END PROCESS UART_CLK_GEN;

---------------------------------------------------------------------------
-----------------------------------------------------
      -- The UART Module - Raw data output
      UART1: PROCESS (uart1_clk, tx_en, uart1_state)

      BEGIN

if rising_edge(uart1_clk) then
    --if I_reset = '1' then
      --uart1_state <= 0;
      --frame <= X"00";
```

```
      --uart1_tx_complete <= '1';
      --tx <= '1';
    --else
      if uart1_state = 0 and tx_en = 1 then
        uart1_state <= 1;
        frame <= uart1_databuf;
        uart1_tx_complete <= 0;
        utxA <= '0'; -- start bit
              utxB <= '0';
      elsif uart1_state < 9 and uart1_tx_complete = 0 then
       utxA <= frame(0);
             utxB <= frame(0);
        frame <= '0' & frame (7 downto 1);
        uart1_state <= uart1_state + 1;
      elsif uart1_state = 9 and uart1_tx_complete = 0 then
       utxA <= '1'; -- stop bit
             utxB <= '1';
        uart1_tx_complete <= 1;
        uart1_state <= 0;
      end if;
    end if;
  --end if;
end process;


END behav;
```

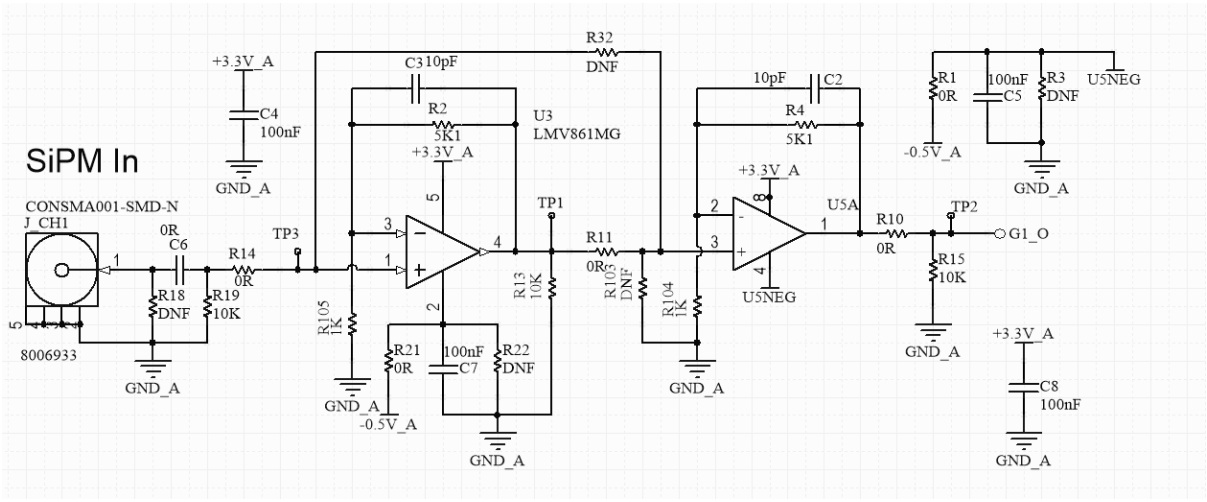
C. Simulated Discrimination Circuit

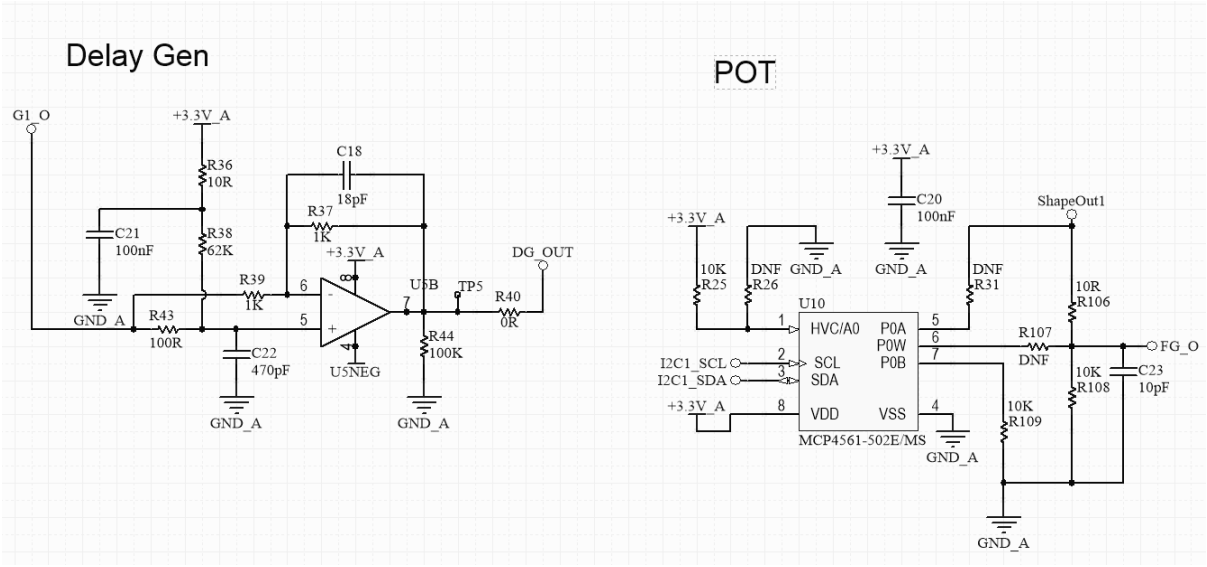
The circuit used for the window discrimination is shown in the schematic below. Four window generation circuits were simulated at once to reduce the need for multiple simulation compilations.

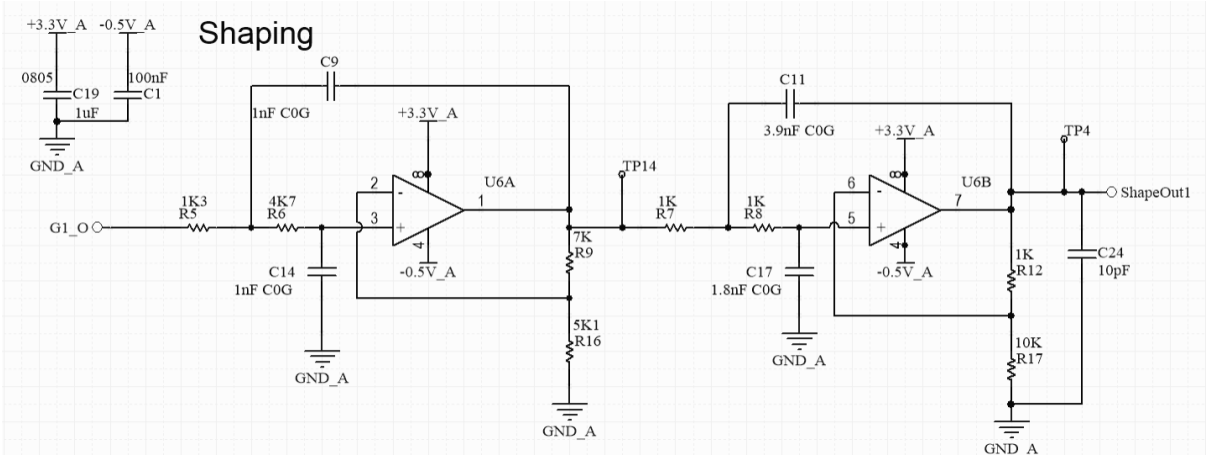


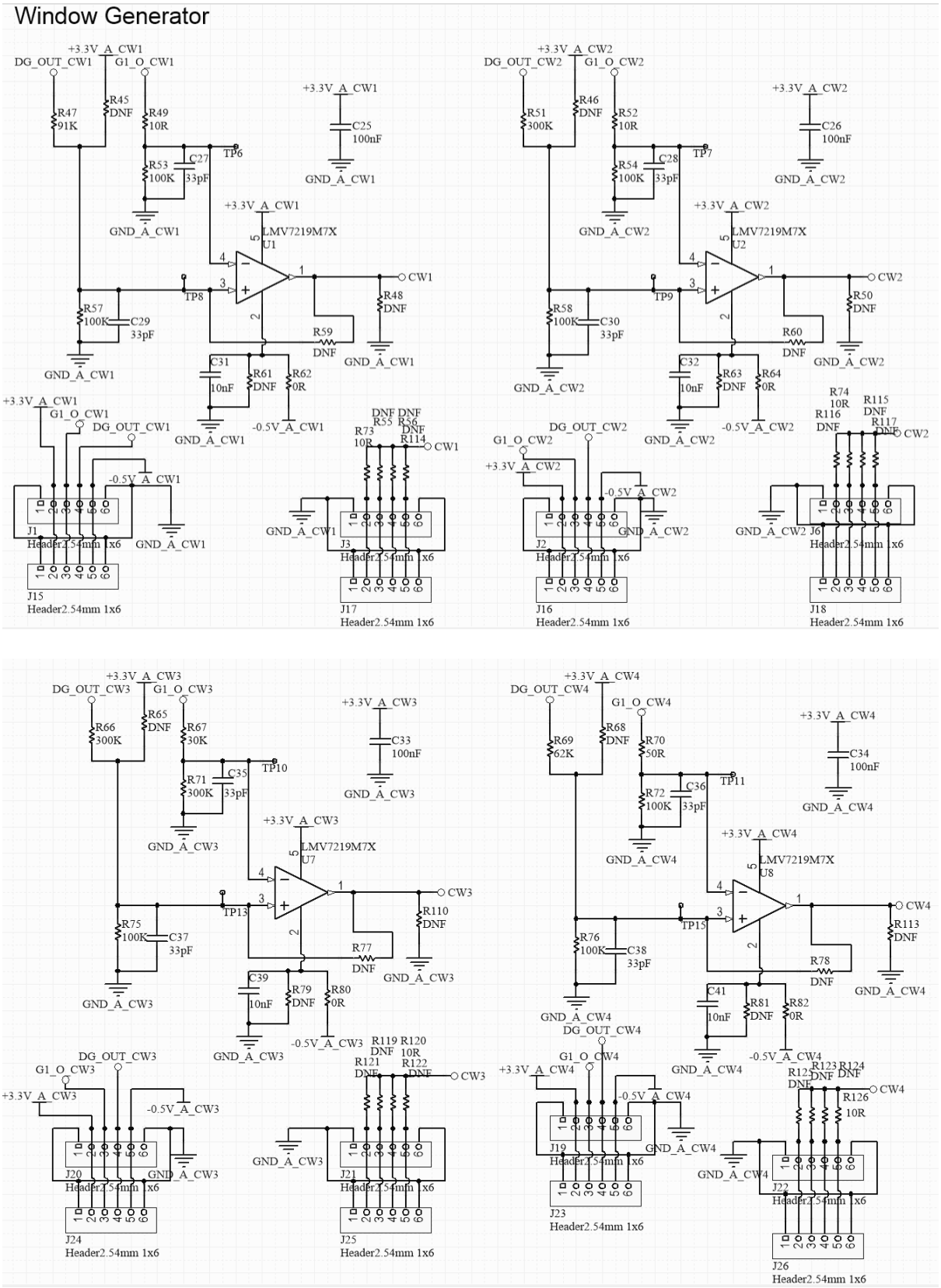
D. Prototype Discrimination Circuit Schematic and Manufactured PCB

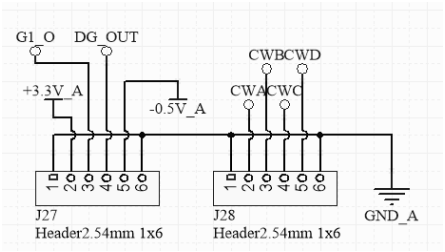
The schematic shows the circuitry designed to implement the gamma neutron discrimination method, used with the 4x4 SiPM array mounted to the CLLB scintillator.

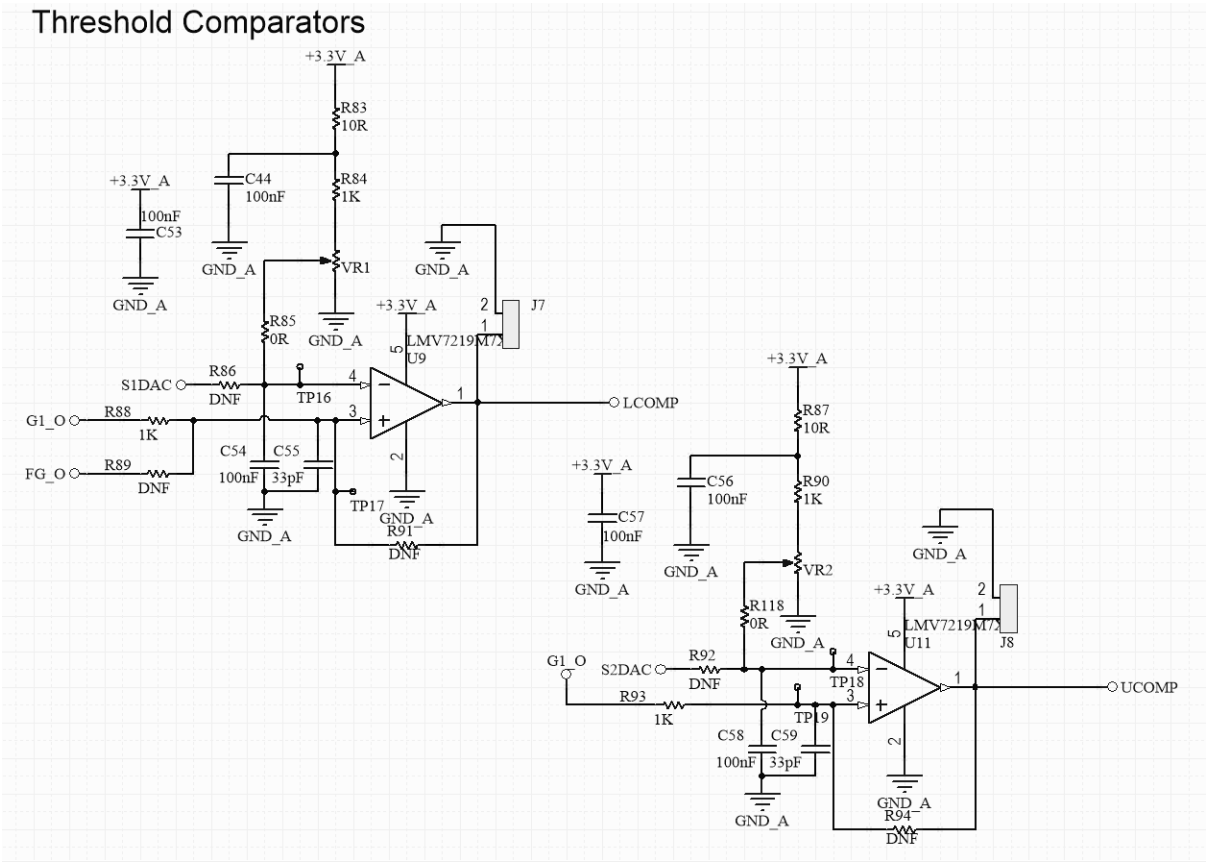


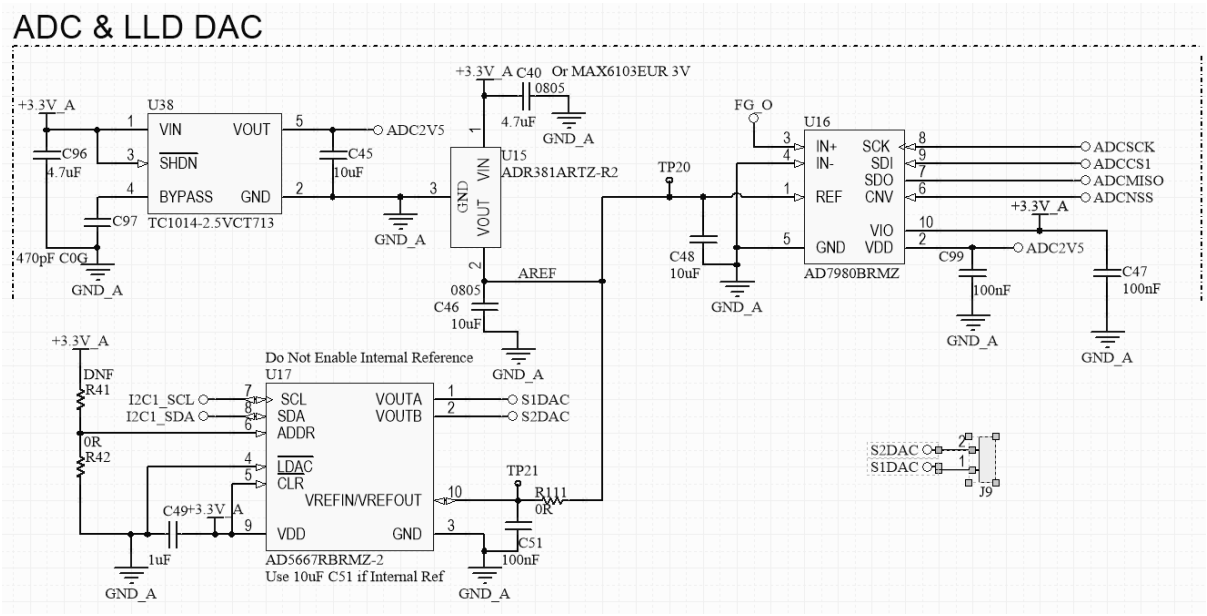


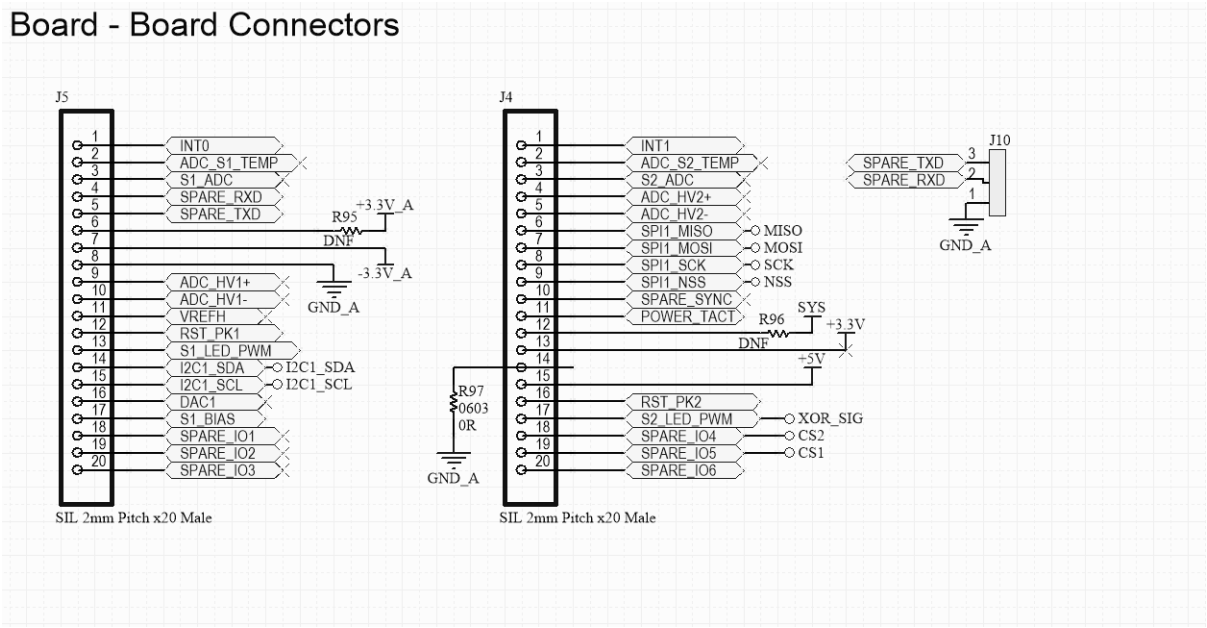


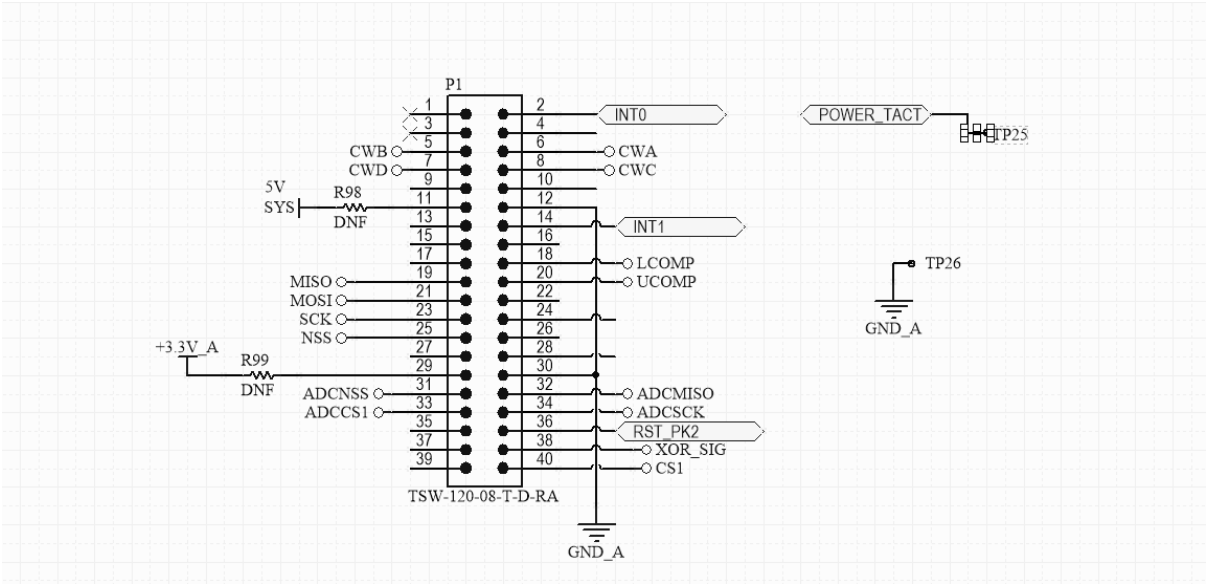

Window Generator
+3.3V_A_CW1
DG_OUT_CW1
G1_O_CW1
R47 91K
R45 DNF
R49 10R
TP6
R53 100K
C27 33pF
GND_A_CW1
C25 100nF
LMV7219M7X
U1
TP8
R57 100K
C29 33pF
R59 DNF
R48 DNF
CW1
C31 10nF
R61 DNF
R62 0R
-0.5V_A_CW1
J1 Header2.54mm 1x6
J15 Header2.54mm 1x6
R73 10R
R55 DNF
R56 DNF
R114 DNF
J3 Header2.54mm 1x6
J17 Header2.54mm 1x6
+3.3V_A_CW2
DG_OUT_CW2
G1_O_CW2
R51 300K
R46 DNF
R52 10R
TP7
R54 100K
C28 33pF
C26 100nF
U2
TP9
R58 100K
C30 33pF
R60 DNF
R50 DNF
CW2
C32 10nF
R63 DNF
R64 0R
-0.5V_A_CW2
J2 Header2.54mm 1x6
J16 Header2.54mm 1x6
R74 10R
R115 DNF
R116 DNF
R117 DNF
J6 Header2.54mm 1x6
J18 Header2.54mm 1x6
+3.3V_A_CW3
DG_OUT_CW3
G1_O_CW3
R66 300K
R65 DNF
R67 30K
TP10
R71 300K
C35 33pF
C33 100nF
U7
TP13
R75 100K
C37 33pF
R77 DNF
R110 DNF
CW3
C39 10nF
R79 DNF
R80 0R
-0.5V_A_CW3
R119 DNF
R120 10R
R121 DNF
R122 DNF
J20 Header2.54mm 1x6
J24 Header2.54mm 1x6
J21 Header2.54mm 1x6
J25 Header2.54mm 1x6
+3.3V_A_CW4
DG_OUT_CW4
G1_O_CW4
R69 62K
R68 DNF
R70 50R
TP11
R72 100K
C36 33pF
C34 100nF
U8
TP15
R76 100K
C38 33pF
R78 DNF
R113 DNF
CW4
C41 10nF
R81 DNF
R82 0R
-0.5V_A_CW4
R123 DNF
R124 DNF
R125 DNF
R126 10R
J19 Header2.54mm 1x6
J23 Header2.54mm 1x6
J22 Header2.54mm 1x6
J26 Header2.54mm 1x6

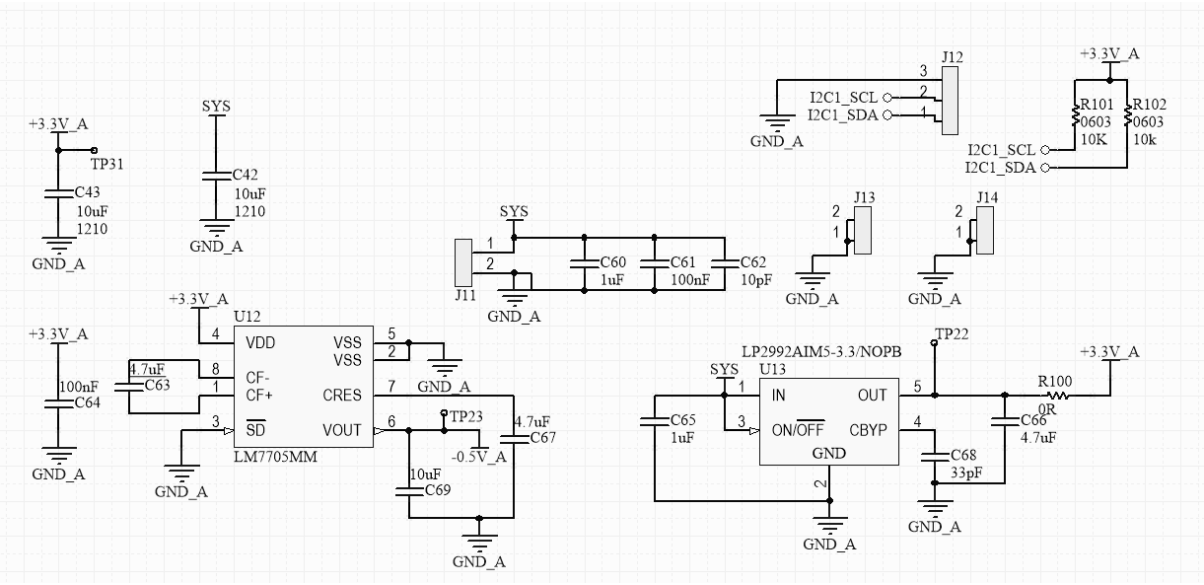

G1_O
DG_OUT
+3.3V_A
-0.5V_A
CWBCWD
CWACWC
J27
Header2.54mm 1x6
J28
Header2.54mm 1x6
GND_A


Threshold Comparators
+3.3V_A
R83
10R
C44
100nF
R84
1K
100nF
C53
VR1
R85
0R
J7
LMV7219M7
U9
S1DAC
R86
DNF
TP16
G1_O
R88
1K
FG_O
R89
DNF
C54
100nF
C55
33pF
TP17
R91
DNF
LCOMP
R87
10R
C56
100nF
R90
1K
C57
100nF
VR2
R118
0R
J8
LMV7219M7
U11
G1_O
S2DAC
R92
DNF
TP18
R93
1K
TP19
C58
100nF
C59
33pF
R94
DNF
UCOMP
GND_A

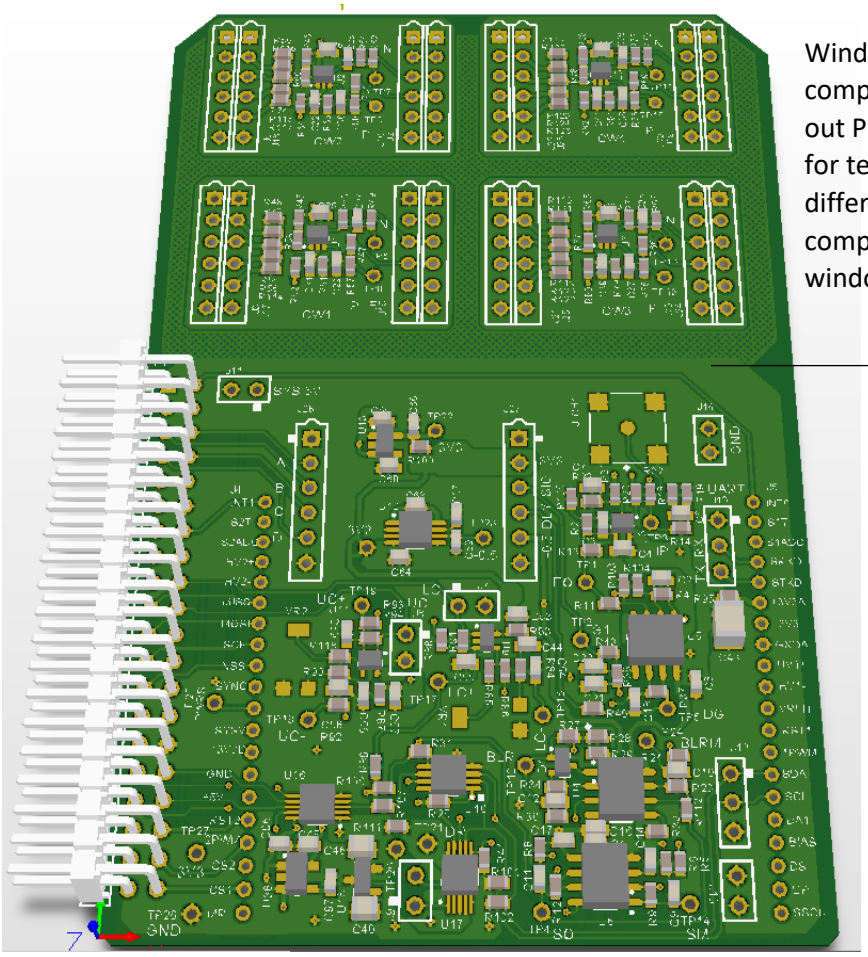

ADC & LLD DAC
+3.3V_A
U38
VIN
VOUT
SHDN
BYPASS
GND
TC1014-2.5VCT713
C96
4.7uF
C97
470pF C0G
C45
10uF
ADC2V5
C40 Or MAX6103EUR 3V
0805
4.7uF
U15
ADR381ARTZ-R2
AREF
C46
10uF
0805
TP20
FG_O
U16
IN+
IN-
REF
GND
SCK
SDI
SDO
CNV
VIO
VDD
AD7980BRMZ
ADCSCK
ADCCS1
ADCMISO
ADCNSS
C48
10uF
C99
100nF
C47
100nF
Do Not Enable Internal Reference
U17
DNF
R41
0R
R42
I2C1_SCL
I2C1_SDA
SCL
SDA
ADDR
LDAC
CLR
VREFIN/VREFOUT
VOUTA
VOUTB
S1DAC
S2DAC
TP21
R111
0R
C51
100nF
C49
1uF
AD5667RBRMZ-2
Use 10uF C51 if Internal Ref
J9
GND_A


Board - Board Connectors
J5
INT0
ADC_S1_TEMP
S1_ADC
SPARE_RXD
SPARE_TXD
R95
DNF
+3.3V_A
-3.3V_A
GND_A
ADC_HV1+
ADC_HV1-
VREFH
RST_PK1
S1_LED_PWM
I2C1_SDA
I2C1_SCL
DAC1
S1_BIAS
SPARE_IO1
SPARE_IO2
SPARE_IO3
I2C1_SDA
I2C1_SCL
SIL 2mm Pitch x20 Male
J4
INT1
ADC_S2_TEMP
S2_ADC
ADC_HV2+
ADC_HV2-
SPI1_MISO
SPI1_MOSI
SPI1_SCK
SPI1_NSS
SPARE_SYNC
POWER_TACT
MISO
MOSI
SCK
NSS
R96
DNF
SYS
+3.3V
+5V
R97
0603
0R
GND_A
RST_PK2
S2_LED_PWM
SPARE_IO4
SPARE_IO5
SPARE_IO6
XOR_SIG
CS2
CS1
SIL 2mm Pitch x20 Male
J10
SPARE_TXD
SPARE_RXD
GND_A


P1
INT0
CWB
CWD
CWA
CWC
5V
SYS
R98
DNF
INT1
LCOMP
UCOMP
MISO
MOSI
SCK
NSS
+3.3V_A
R99
DNF
ADCNSS
ADCCS1
ADCMISO
ADCSCK
RST_PK2
XOR_SIG
CS1
TSW-120-08-T-D-RA
GND_A
POWER_TACT
TP25
TP26
GND_A

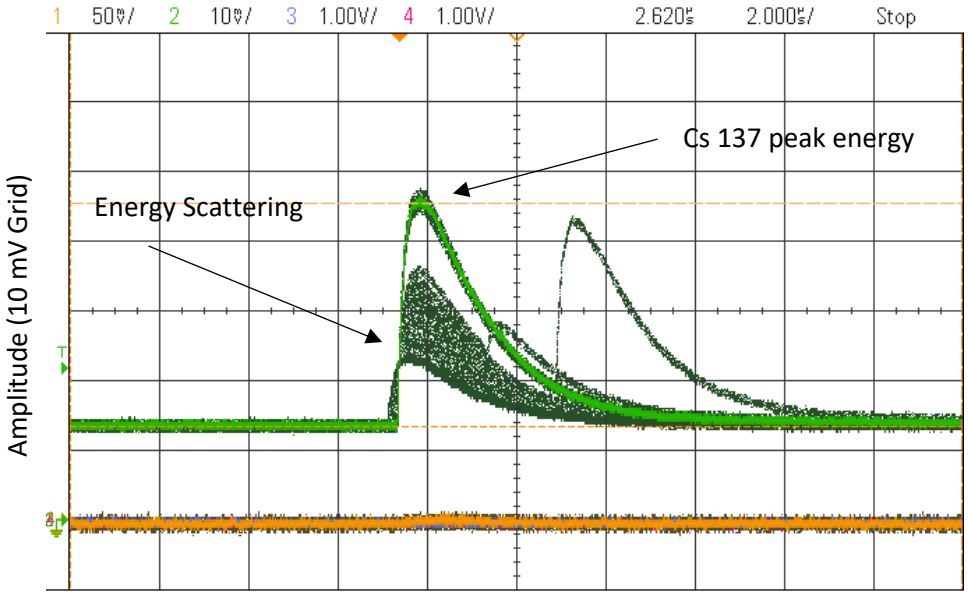


A fast turn round two-layer prototype PCB was designed and manufactured for the gamma neutron discrimination circuit.

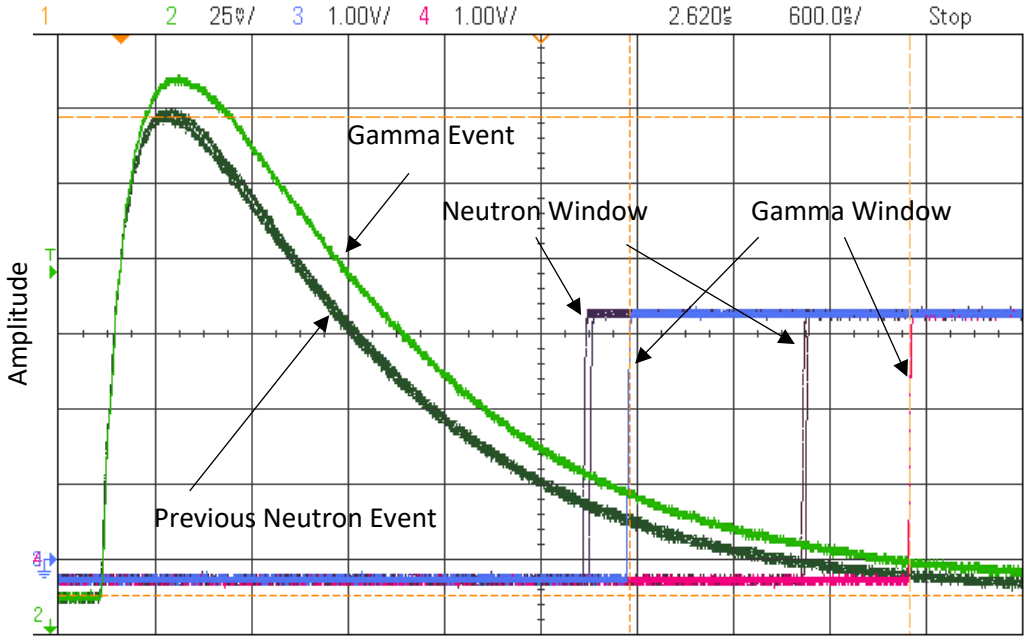


Window comparator cut out PCB modules for testing different comparators and window times.

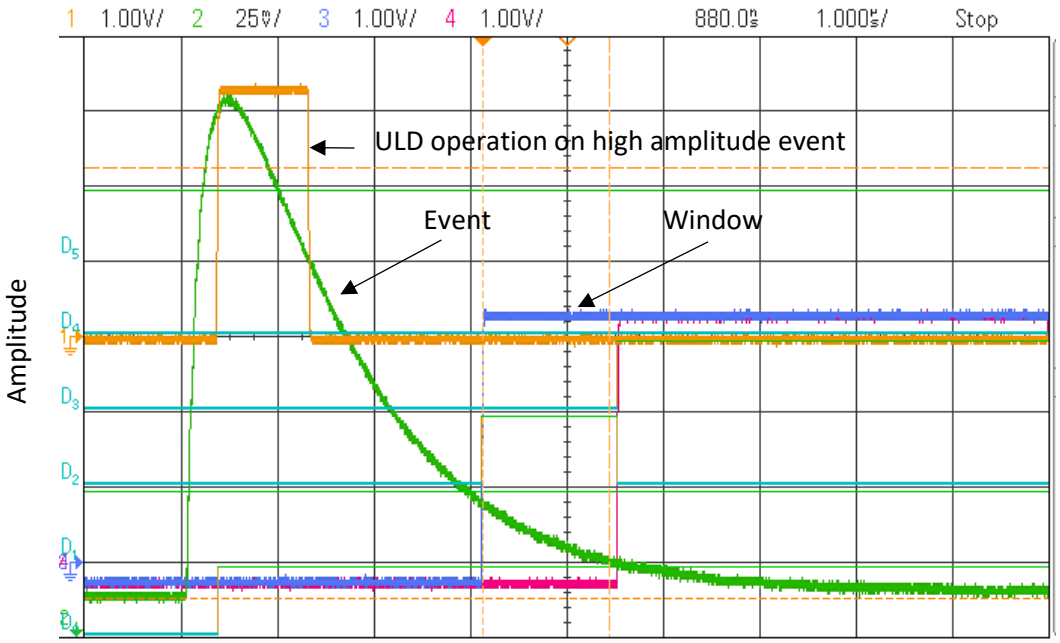
E. Discrimination Circuit Testing and Operation



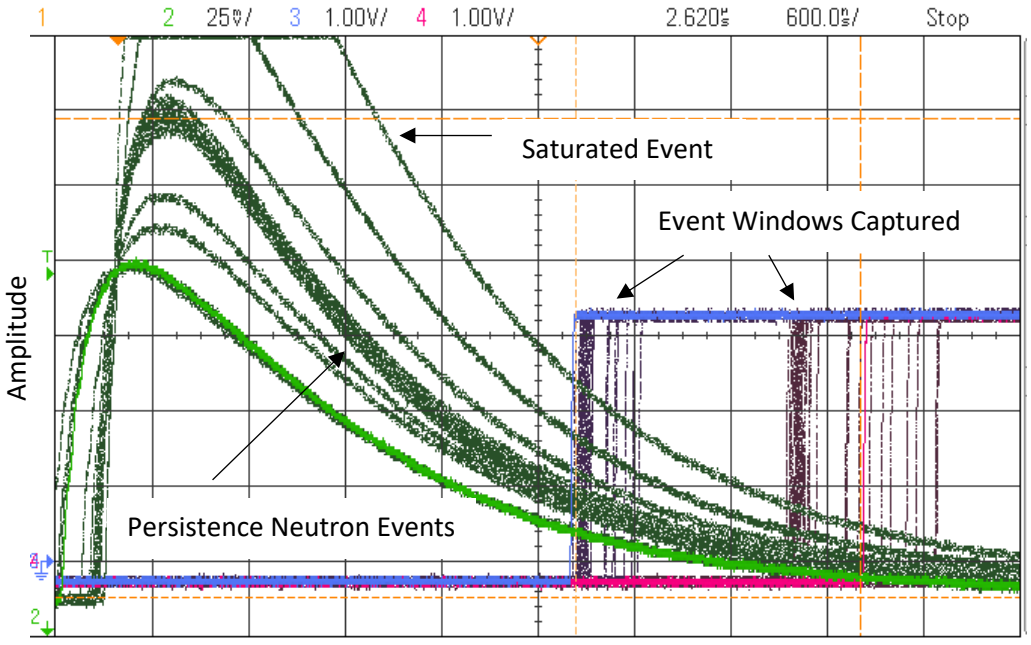
Persistence oscilloscope trace identifying the amplitude of the 662 keV peak from using a Cs137 source. This is then scaled to find the neutron amplitude given a known neutron energy.



Oscilloscope trace shows captured gamma event with cursors and neutron event persist, where the difference in window signals for the gamma and neutron radiation can be seen.

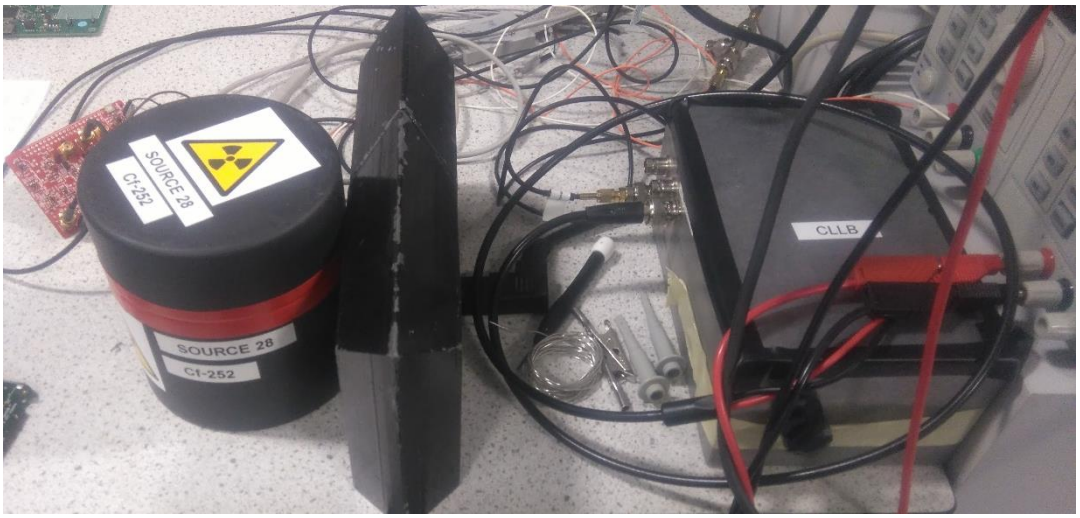


Oscilloscope trace shows the ULD operation used to perform an initial discrimination based on event amplitude.

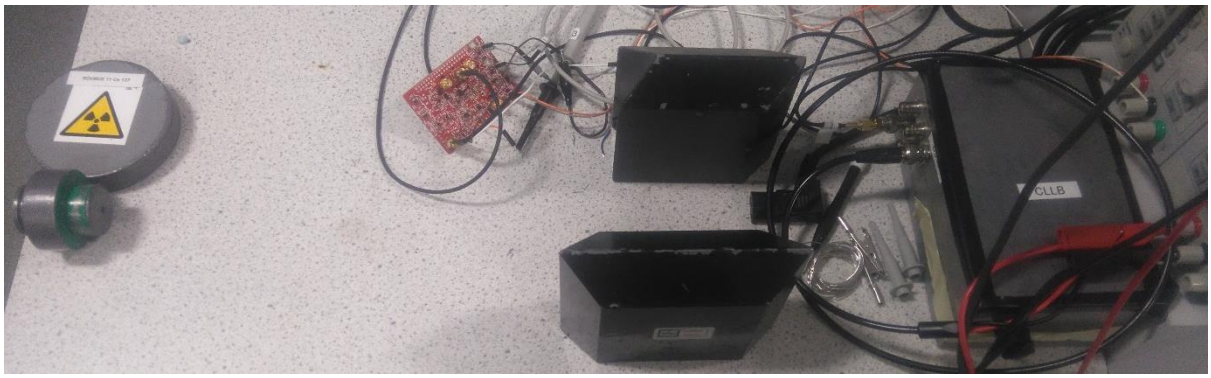


Oscilloscope trace showing the saturated pre-amplified event signal causing longer erroneous window times. The trace also shows the persistence of captured events when using the neutron source, where the main persistence is of the neutron events and associated window signals, where gamma events and windows can also be seen in less persistence depth.

Discrimination Circuit Testing and Setup Photos



The lead blocks are used to reduce the rate of the gamma events also coming from the Californium 252 source, the detection of neutron to acquire the pulse shape is required.

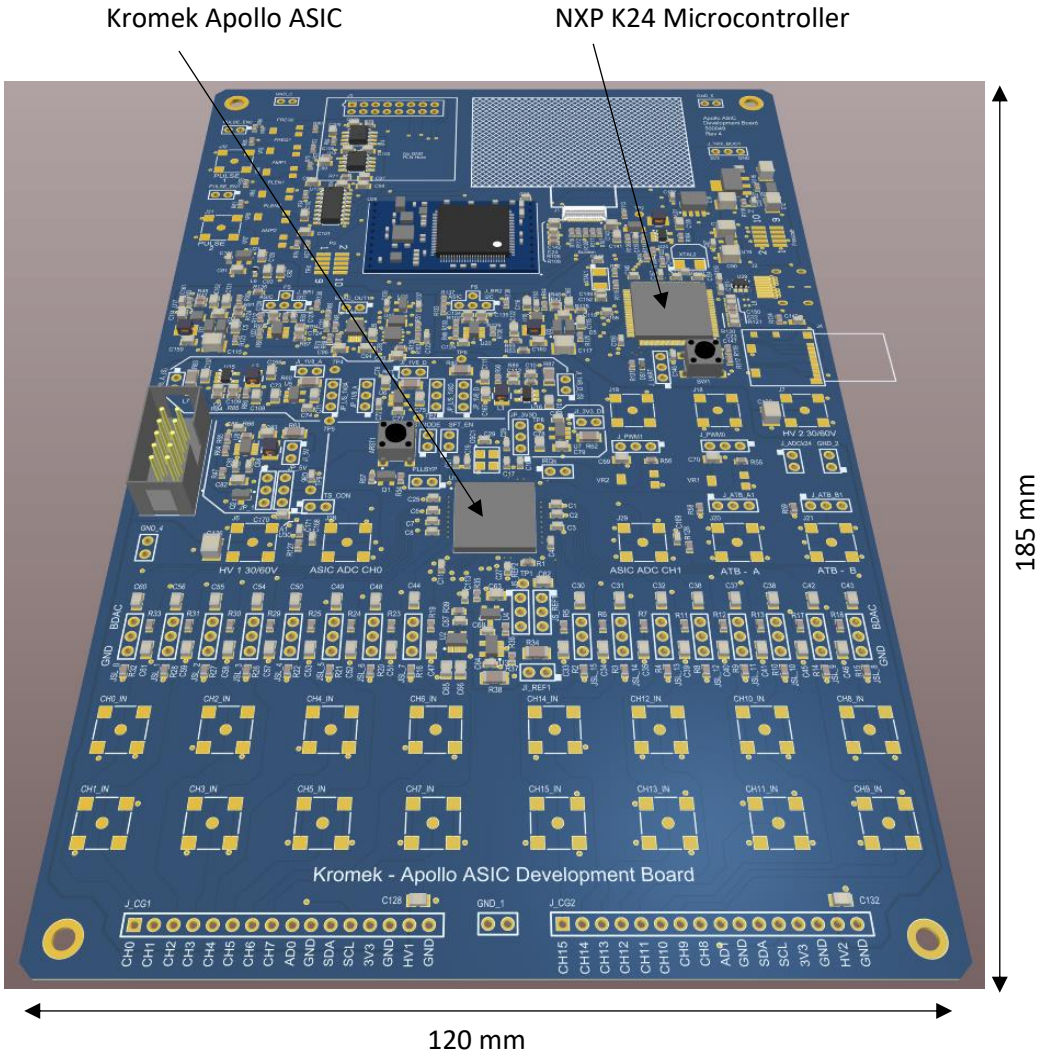


Cesium source used to identify the gamma pulse shape. The lead blocks are not used.

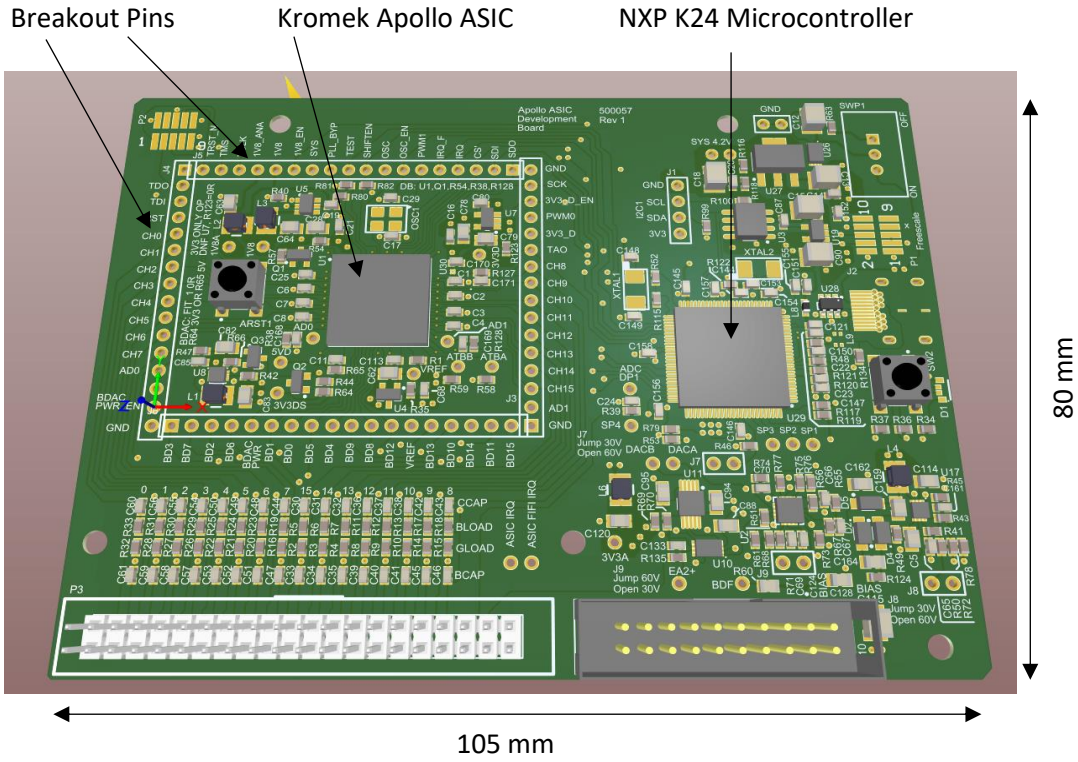
Collecting both gamma and neutron events, the lead is not used so gamma and neutron events are causing scintillation in the CLLB.

F. Kromek Apollo ASIC Development Board

Two development PCBs for the Kromek Apollo ASIC were designed and manufactured towards the end of the research project, to aid future research for radiation detection and radiation event processing. The development PCBs provide circuitry to fully exploit the 16 event processing channels available on the Kromek Apollo ASIC. 3D renderings of the development PCBs are shown below.



The development PCB breaks out the 16 available channels to SMA connectors for easy signal connections. The board is collecting and then transmitting or storing the spectroscopic data, though such methods as Bluetooth transmission and SD card writing.



Similarly, for this development board, the capabilities of the ASIC and associated processing signals are made available for in depth testing, bringing channel inputs and logic outputs to IDE connections at the bottom of the PCB. The board was designed on a 2.54 mm grid for the board test points and signal connections to match that of a standard breadboard for testing convenience.