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### Original Citation

Haigh, Richard, Upton, David, Mather, Peter and Sibley, Martin J.N. (2017) Low Power Embedded Processing of Scintillation Events with Silicon Photo Multipliers. In: URSI GASS 2017, 19-26 August 2017, Montreal, Canada.

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## Low Power Embedded Processing of Scintillation Events with Silicon Photo Multipliers

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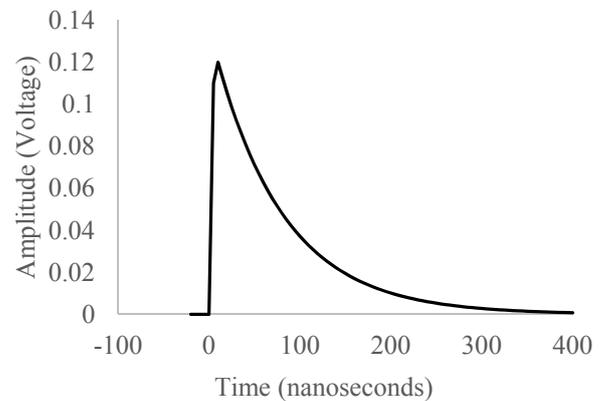
**Abstract:** The advancement and use of silicon photo multiplier (SiPM) technology has enabled portable devices for applications such as scintillation detection to be developed. The proposed analogue to digital converter (ADC) architecture and field programmable gate array (FPGA) system configuration advances on analogue signal processing methods, traditionally employed for gamma isotope identification applications. This is achieved by high speed sampling of SiPM output signals and real-time FPGA processing, whilst consuming low power, thus extending device operation times. Results demonstrate 7-bit peak capture accuracy of an 8  $\mu$ s scintillation event, using a 25 MHz ADC sample rate.

### 1. Introduction

Technological advances in Silicon Photo Multipliers (SiPMs) have allowed photon detection in compact portable products, similar in size to a modern mobile phones [1]. A portable, compact and light weight design for scintillation detection and medical imaging devices provides greater flexibility in security, medical, and industrial applications, where for example potential radioactive threat identification or dose measurement is required. A challenge for many hand held portable devices is processing ever increasing amounts of data, whilst consuming less power in order to extended operation time from the battery.

### 2. Photonics in Radiation Detection

A well-established method of gamma and neutron radiation detection is to use a scintillation detector, where ionizing radiation interacts with a scintillator, which then emits a quantity of photons proportional to the energy of the absorbed radiation. One or more SiPMs are bonded to the scintillator depending on the size, gain and efficiency required, to capture the emitted photons. SiPMs are constructed with a grid array of avalanche photo diodes (APDs) cells that are then biased in the Geiger mode range at between 25 V and 30 V, depending on the gain and noise requirements of a system. Upon photon interaction with a SiPM cell, it will breakdown causing a flow of electrical current; then with multiple photons more cells breakdown resulting in a proportional electrical pulse signal [2], as illustrated in Figure 1.



**Figure 1.** - Typical SiPM anode output of a SensL 6 mm<sup>2</sup> 60035 J series with a 16  $\Omega$  series resistor [3].

The low SiPM bias voltage requirement compared to 800 V, or more, for a Photo Multiplier Tube (PMT), as well as a small physical size ranging from 1 mm<sup>2</sup> to 6 mm<sup>2</sup> as with the SensL devices [3] enables compact battery powered devices to be developed [4].

The amplitude of the electrical pulse signal generated by a SiPM, when amplified and semi Gaussian shaped, is generally used to determine the energy of the radiation deposited in the scintillator, and hence is used in determining the radiation isotope based on the energy levels present over multiple events. The semi Gaussian shaping allows for the whole SiPM signal representation of the event to be considered when determining energy levels by capturing the shaped peak [5]. An alternative approach is to directly integrate the SiPM pulse using high speed sampling with a commercial digitiser and computer interface [6], which enables the energy and pulse shape of the radiation event to be evaluated. This however is not ideal for portable products due to the need for the external equipment and the high power requirements.

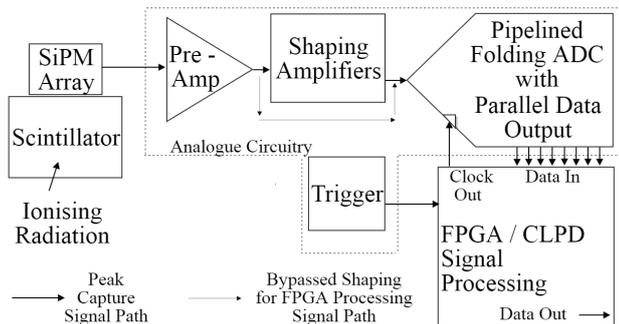
Traditional techniques of peak capture rely on analogue, op-amp based peak detection circuitry to capture and measure the maximum amplitude of the shaped signal, where longer shaping times enable more accurate peak capture due to the bandwidth limitation of the low power op-amps typically used. However, the fast count rates and high energy resolution requirements of typical radiation detection devices, demands a high speed and linearity that cannot generally be achieved employing these methods. Employing a longer shaping time increases system dead time, where given the random nature of radiation scintillation, the time delay potentially compromises the

accurate identification of multiple events [6]. Furthermore, the analogue peak hold time is dependent on the Analogue to Digital Converter (ADC) sample conversion time, adding to dead time and peak droop times. Dead time and droop issues can be significantly reduced by digitising the signal, requiring accuracy and high sample rates, where for a portable device, would have to be power efficient also.

### 3. Proposed Embedded Approach

The proposed system utilizes discrete component based, low power pipelined, folding ADC, developed with parallel Gray code data output. The ADC output data is sampled via a field programmable gate array (FPGA), which is triggered to sample event signals at high speed. The flexibility of the FPGA and data throughput of the ADC allows for both real-time and post processing of the event. Furthermore, the real-time processing enabled reduced data transmission, as only peak values or histogram data is then transmitted.

The pipelined architecture of the ADC increases available bandwidth compared to a non-pipelined architecture, for the required sample rate throughput and accuracy for peak capture. The FPGA only triggers when an event occurs, which allows for the sample clocks to be disabled when no event is present. This enables the ADC circuit power consumption to be reduced from approximately 160mW to 100 mW. Additionally, given the FPGA control over the sample rate clock, a lower ADC clock frequency can be used if a long pulse shaping time is employed for peak capture alone. The lower sample rate leads to reduced bandwidth and data processing requirements, consuming less power. The peak capture process in the FPGA uses the successive samples of the event to evaluate a current sample against previous sample in real-time, where after noise reduction, lower readings result in a confirmed peak and can be further processed.



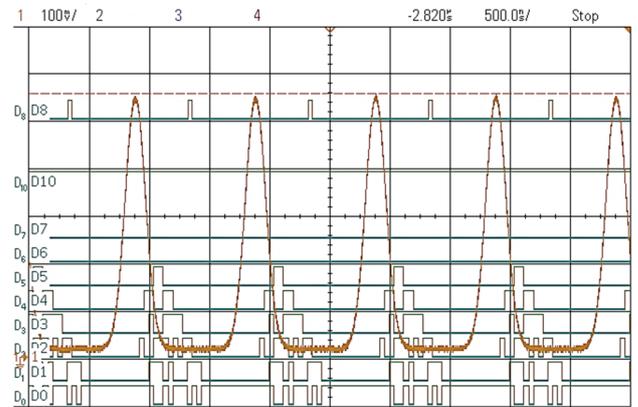
**Figure 2.** – Proposed SiPM based gamma radiation detector configuration.

When the peak of an event is evaluated by the FPGA, there is no system dead-time delay that affects the next event capture. However, the limitation in this case is the sample rate of the ADC, where sample and hold times, and internal bandwidths of the architecture limit the clock frequency that can be applied to the proposed ADC. The

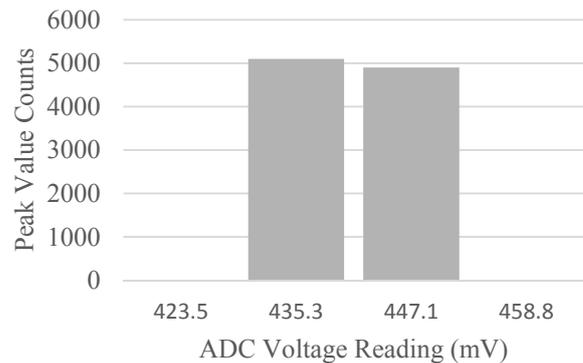
current resolution and time accuracy of the developed ADC system is 8-bit, (11.8 mV per bit) and the sample rate is 25 MSps.

### 4. Results

To evaluate the proposed system for peak capture, a semi Gaussian pulse with a 1  $\mu$ S base width, at a rate of 1 million pulses per second was used as an input signal, where the minimum voltage was 20 mV and the maximum voltage at the peak, measured using an oscilloscope was 553 mV, shown in figure 3. The FPGA was configured so that as well as peak capture storing, a parallel binary logic representation output of each sample, as well as a peak confirmed logic signal could be seen using an oscilloscope. A 10 k sample of peak capture readings was then taken and transmitted to a computer for analysis purposes.



**Figure 3.** – Oscilloscope trace of the input test signal, parallel binary and FPGA status outputs.

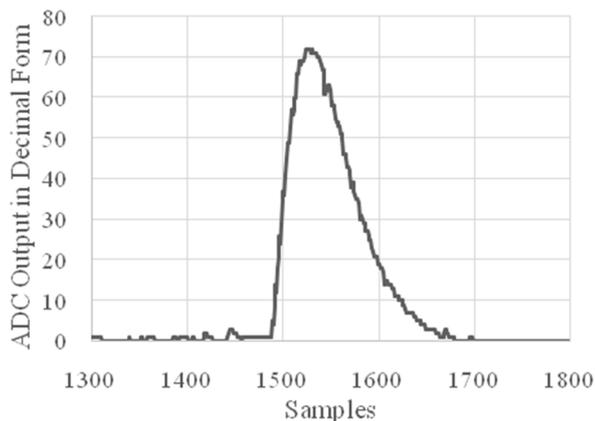


**Figure 4.** – Histogram showing peak capture accuracy.

As shown in figure 4, the peak events were captured between two histogram bins suggesting the minimum resolution of the ADC with this test was 7-bit accurate. The difference of 112 mV between input signal peak voltage and the captured peak voltage is due to gain error in the ADC architecture design and can be corrected for within the FPGA. The relative accuracy, in terms of repeatability is of higher importance than the absolute

accuracy of the analogue architecture for the given application.

To evaluate the proposed system for the use of further processing techniques such as directly integrating the SiPM pulse, or pulse shape discrimination, an amplified SiPM anode terminal was sampled directly by removing the shaping stage as shown by the dashed line signal path in figure 2, then sampled at 25 MSps. The samples were processed offline, and a peak from a random background radiation event was captured and isolated in the results, shown in figure 5.



**Figure 5.** – Sampled amplified SiPM anode output over a 50  $\Omega$  resistor

The captured event contains approximately 200 samples, equivalent to an 8 $\mu$ s pulse length given the sample rate of 25 MHz. The pulse shape is similar to that of figure 1, where enough sample points exist to show the capability for the FPGA to then integrate this pulse in real time to gain the required energy information to the 7-bit accuracy shown in figure 4. This removes the need for the shaping circuitry further lowering system power consumption. With resolution and sample rate improvements to the ADC architecture, capturing accurate samples of the sub 1  $\mu$ s event times of scintillators typically used in pulse shape discrimination applications [7], can be analysed in real-time by the FPGA, thus further enhancing system capabilities.

## 5. Conclusion

The proposed ADC architecture and FPGA control allows for enhanced operation flexibility, depending on the requirements of the system application. Where gamma isotope identification is required, both using shaping circuitry and direct high sample speed pulse integration methods can be achieved whilst employing power saving methods in the system. The flexibility of the FPGA allows for real time data analysis, compression and reduced data transmission rates to a readout system. Furthermore, to enhance portability user control and parameter readout via a screen, for example, can be driven by additional logic programmed into the FPGA.

Combining the existing benefits and improvements to resolution and sample speed, a completely embedded device can be achieved whilst meeting the low power consumption challenges for a truly portable device, with no external computer processing requirement.

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