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MICROELECTRONIC IMPLEMENTATION of ERROR CORRECTING CODES for DICODE PULSE POSITION MODULATION

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ABSTRACT

Dicode pulse position modulation (DiPPM) was proposed by Sibley as a more advantageous format than digital PPM. DiPPM can be efficiently implemented as it employs two slots to transmit one bit of pulse code modulation PCM. Thus a PCM conversion from zero to one provides a pulse in slot reset (R) and from one to zero provides a pulse in slot set (S). No signal is transmitted if the PCM data is unvarying. The line rate is two times that of the original PCM, a significant reduction in speed compared to digital PPM. As the bandwidth requirement is much smaller than digital PPM, DiPPM could be used in dense wavelength division multiplexing (DWDM) systems. DiPPM systems suffer from three types of pulse detection errors wrong-slot, false-alarm and erasure. This project will use a field programmable gate array (FPGA), to build an error correction code circuit (Reed Solomon Code) and dicode coder, decoder. This will be expected to reduce the error sources in DiPPM. According to initial results the conclusion is that the Reed Solomon error correction coded system offers improvement over uncoded DiPPM, when operating at the optimum 4/5 code rate.

Keywords pulse position modulation, dicode pulse position modulation and error correction code