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Microelectronic implementation of error correcting codes for dicode pulse position modulation

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ABSTRACT

Dicode pulse position modulation (DiPPM) was proposed by Sibley as a more advantageous form of PPM. DiPPM can be efficiently implemented as it employs only two ability to transmit one bit of pulse code modulation PCM. Thus a PCM conversion from zero to one provides a pulse in slot reset (R) and from one to zero provides a pulse in logic set (lS). No signal is transmitted when the PCM data is varying. The line rate, at which the PCM data is varying, is twice that of the clock data which is a significant reduction in speed compared to digital PPM. As the bandwidth requirement is much smaller than digital PPM, DiPPM could be used in dense wavelength division multiplexing (DWDM) systems. DWDM systems suffer from three types of pulse detection errors wrong-slot, false-alarm and erasure. This project will use a field programmable gate array (FPGA), to build an error correction code circuit (Reed Solomon Code) and dicode PPM (coder & decoder). This will be expected to reduce the error sources in DiPPM. According to initial results the conclusion is that the Reed Solomon error correction coded system offers improvement over uncoded DiPPM, when operating at the approximately 4.5 code rate.

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The main aim of this project research is to implement a DiPPM and Reed Solomon error correct & decoded using FPGA to reduce the sources of error in DiPPM.

The following main objectives will be considered:
1) simulation and modeling of the system
2) Design RS encoder and decoder circuits.
3) Implement RS and DiPPM encoder & decoder circuit by simulation and FPGA
4) Confirm theoretical predictions with measurements.
5) Compare the result with another type of coding.

Sources of Error in DiPPM

DiPPM systems suffer from three types of pulse detection errors:

- Wrong slot error
  Wrong slot errors occur when noise on the rising edge of a detected pulse causes the pulse to appear in adjacent time slots.

- Erasure errors
  Erasure errors occur when the noise is so great as to reduce the peak signal voltage to below the threshold level.

- False alarm errors
  Due to ISI, there can be a signal voltage in the slots surrounding the one containing a pulse. Noise on this voltage can lead to a threshold crossing event where the pulse is presented as a false alarm error.

AIM & OBJECTIVE

1. DICODE PULSE POSITION MODULATION SYSTEM

DiPPM signal is a transition from logic zero to a logic one coded as a V and transition from logic one to logic zero coded as a −V. As shown in figure below, a zero signal is transmitted if there is no change in the PCM signal. The positive pulse can be regarded as setting the data to logic one (pulse SET), whereas the negative pulse resets the data to logic zero (pulse RESET). In diPPM, three signals are sent in each pulse position as a data frame. Thus a PCM transition from zero to one produces a pulse in code slot and a one to zero transition generates a pulse in slot R. If this PCM data is constant, no signal is transmitted. (Although two guard slots have been used in this system, to reduce the effects of inter-symbol interference ISI, this depends on the channel characteristics. If there is minimal ISI, zero guard slots could be used.)

2. REED SOLOMON CODE

In 1960, Irving Reed and Gus Solomon published a paper in which they described a new type of error-correcting codes that are now called Reed Solomon (RS) codes. RS codes are a powerful class of non-binary forward error-correcting that can correct the maximum possible number of symbol errors with the minimum amount of redundancy. RS codes are the most commonly used error codes in practice. It is used in many applications like magnetic and optical data storage, wireline and wireless communications, and satellite communications. RS decoder has the ability to correct up to t symbols that contain errors in a codeword, where t can be defined as:

\[ t = (n-k)/2 \]

Where:
- \( n \) = Number of codeword symbols.
- \( k \) = Number of data symbols.
- \( 2t \) = Number of redundancy symbols.

BACKGROUND

1. DIODE PULSE POSITION MODULATION SYSTEM

In diode signal data transitions from logic zero to logic one are coded as a V and transitions from logic one to logic zero are coded as a −V. As shown in figure below, a zero signal is transmitted if there is no change in the PCM signal. The positive pulse can be regarded as setting the data to logic one (pulse SET), whereas the negative pulse resets the data to logic zero (pulse RESET). In diode PPM, these SET and RESET signals are converted into two pulse positions in a data frame. Thus a PCM transition from zero to one produces a pulse in slot S and a one to zero transition generates a pulse in slot R. If the PCM data is constant, no signal is transmitted. (Although two guard slots have been used in this system, to reduce the effects of inter-symbol interference ISI, this depends on the channel characteristics. If there is minimal ISI, zero guard slots could be used.)

FUTURE WORK

- Determine a suitable algorithm for Reed Solomon Code.
- Design RS encoder and decoder circuits by choosing the proper parameters.
- Implement RS, DiPPM encoder and decoder circuit by programming the FPGA using very high speed integrated circuit Hardware Description Language (VHDL).
- Verify theoretical predictions with measurements.

A system model tries to simulate some characteristics of a system. The model corresponds to the forward error correction (FEC) communication scheme, which is dependent on a RS error-control code. The behaviour of each block of the model is described in Mathcad software.