ABSTRACT

The main aim of this project research is to implement a DiPPM and Reed Solomon Code encoder & decoder using FPGA to reduce the sources of error in DiPPM.

The following main objectives will be considered:
1. Determine the relevant DiPPM parameters.
2. Design RS encoder and decoder circuits.
3. Implement RS and DiPPM encoder & decoder circuit by using MATLAB and FPGA.
4. Confirm theoretical predictions with measurements.
5. Compare the results with another type of coding.

Sources of Error in DiPPM

DiPPM systems suffer from three types of pulse detection errors:

1. Wrong slot error.
   Wrong slot errors occur when noise on the rising edge of a detected pulse causes the pulse to appear in adjacent time slots.

2. Erasure errors.
   Erasure errors occur when the noise is so great as to reduce the peak signal voltage to below the threshold level.

3. False alarm errors.
   Due to ISI, there can be a signal voltage in the slots surrounding the one containing a pulse. Noise on this voltage can lead to a threshold crossing event wherein pulse is presented; so called false alarm errors.

AIM & OBJECTIVE

1. DICE PULSE POSITION MODULATION SYSTEM

In digital signaling data transitions from logic zero to logic one are coded as +V transitions and transitions from logic one to logic zero are coded as -V. As shown in figure below, a zero signal is transmitted if there is no change in the PCM signal. The positive pulse can be regarded as setting the data to logic one (pulse SET), whereas the negative pulse resets the data to logic zero (pulse RESET). In digital PPM, these SET and RESET signals are converted into two pulse positions in a data frame. Thus a PCM transition from zero to one produces a pulse in slot S and a one to zero transition generates a pulse in slot R. If the PCM data is constant, no signal is transmitted. (Although two guard slots have been used in this system, to reduce the effects of inter-symbol interference (ISI), this depends on the channel characteristics. If there is minimal ISI, zero guard slots could be used.)

2. REED SOLOMON CODE

In 1960, Irving Reed and Gus Solomon published a paper in which they described a new type of error-correcting codes that are now called Reed Solomon (RS) codes. RS codes are a powerful class of non-binary forward error-correcting that can correct the maximum possible number of errors with the minimum data overhead. RS codes are the most commonly used error codes in practice. It is used in many applications like magnetic and optical data storage, wireless and wired communications, and satellite communications. RS decoder has the ability to correct up to t symbols that contain errors in a codeword, where t can be defined as:

\[ t = \frac{n-k}{2} \]

Where:
- \( n \) = Number of codeword symbols.
- \( k \) = Number of data symbols.
- \( 2t \) = Number of redundancy symbols.

SYSTEM MODEL

This research will concentrate on employing Reed Solomon (RS) codes to code the Digital Pulse Position Modulation System (DiPPM). RS is expected to reduce the source of errors, which a DiPPM system suffers from. In this report a literature review has been written to explain the problems of DiPPM system and going to find a solution. The general block diagram of the system has been given. According to initial results the conclusion is that the Reed Solomon error correction coded system offers improvement over uncoded DiPPM, which operates at approximately 1/8 of the code rate, and this will lead to a gain in the RS system (coder & decoder). Finally, the overall system will be implemented using FPGA and the results will be compared with maximum likelihood sequence detection (MLSD).

CONCLUSIONS

- Determine a suitable algorithm for Reed Solomon Code.
- Design RS encoder and decoder circuits by choosing the parameters.
- Implement RS, DiPPM encoder and decoder circuit by programming the FPGA using Very high speed integrated circuit Hardware Description Language (VHDL).
- Verify theoretical predictions with measurements.

FUTURE WORK

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