University of Huddersfield Repository

Al-Nedawe, Basman, Sibley, Martin J.N. and Mather, Peter

Microelectronic implementation of error correcting codes for dicode pulse position modulation

Original Citation


This version is available at http://eprints.hud.ac.uk/9335/

The University Repository is a digital collection of the research output of the University, available on Open Access. Copyright and Moral Rights for the items on this site are retained by the individual author and/or other copyright owners. Users may access full items free of charge; copies of full text items generally can be reproduced, displayed or performed and given to third parties in any format or medium for personal research or study, educational or not-for-profit purposes without prior permission or charge, provided:

- The authors, title and full bibliographic details is credited in any copy;
- A hyperlink and/or URL is included for the original metadata page; and
- The content is not changed in any way.

For more information, including our policy and submission procedure, please contact the Repository Team at: E.mailbox@hud.ac.uk.

http://eprints.hud.ac.uk/
ABSTRACT

DiPPM systems suffer from three types of pulse detection errors: wrong-slot, false-alarm and erasure. This project will use a field programmable gate array (FPGA), to build an error correction code circuit (Reed Solomon Code) and decode PPM (coder & decoder). This will be expected to reduce the error sources in DiPPM. According to initial results the conclusion is that the Reed Solomon error correction coded system offers improvement over uncoded DiPPM, when operating at the approximately 4/5 code rate.

AIM & OBJECTIVE

1. Finding the Reed Solomon (RS) optimum parameters.
2. Design RS encoder and decoder circuits.
3. Implement RS and DiPPM (encoder & decoder) circuit by programming the FPGA.
4. Confirm theoretical predictions with measurements.
5. Compare the result with another type of coding.

SYSTEM MODEL

A system model tries to simulate some characteristics of a system. The model corresponds to the forward error correction (FEC) communication scheme, which is dependent on a RS error-control code. The behaviour of each block of the model is described in Matlab software.

CONCLUSIONS

This research will concentrate on employing Reed Solomon (RS) codes to code the Diode Pulse Position Modulation System (DiPPM). RS is expected to reduce the source of errors, which a DiPPM system suffers from. In this report a literature review has been written to explain the problems of DiPPM system and trying to find a solution, the general block diagram of the system has been given. According to initial results the conclusion is that the Reed Solomon error correction coded system offers improvement over uncoded DiPPM, when operating at approximately (4/5) code rate, and this will lead to a practical RS system (coder & decoder). Finally, the overall system will be implemented using FPGA and the results will be compared with maximum likelihood sequence detection (MLSD).

FUTURE WORK

- Determine a suitable algorithm for Reed Solomon Code.
- Design RS encoder and decoder circuits by choosing the proper parameters.
- Implement RS, DiPPM encoder and decoder circuit by programming the FPGA using Very high speed integrated circuit Hardware Description Language (VHDL).
- Verify theoretical predictions with measurements.