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Al-Nedawe, Basman, Sibley, Martin J.N. and Mather, Peter

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ABSTRACT

Microelectronic Implementation of Error Correcting Codes for DiPulse Position Modulation

B. Al-Nedawe, Dr. M. Sibley, Dr. P. Mather

DiPulse position modulation (DiPPM) was proposed by Sibley as a more advantageous form of PPM. DiPPM can be efficiently implemented in hardware using FPGA to reduce the sources of error in DiPPM. The following main objectives will be considered: 1) Determine an appropriate encoder and decoder for DiPPM. 2) Design RS encoder and decoder circuits. 3) Implement RS and DiPPM encoder and decoder circuits by programming an FPGA. 4) Conform theoretical predictions with measurements. 5) Compare the result with another type of coding. Sources of Error in DiPPM

DIPPM systems suffer from three types of pulse detection errors:

- Wrong slot error
- Erasure errors
- False alarm errors

The main aim of this project research is to implement a DiPPM and Reed Solomon (RS) encoder & decoder using FPGA to reduce the sources of error in DiPPM.

AIM & OBJECTIVE

System Model

CONCLUSIONS

FUTURE WORK

This research will concentrate on employing Reed Solomon (RS) codes to code the DiPulse Pulse Position Modulation System (DiPPM). RS is expected to reduce the source of error, which a DiPPM system suffers from. If this research is successful, it will provide a solution to the problem of DiPPM. Finally, the overall system will be implemented using FPGA and the results will be compared with maximum likelihood sequence detection (MLSD).

Microelectronic Implementation of Error Correcting Codes for DiPulse Position Modulation System

The main aim of this project research is to implement a DiPPM and Reed Solomon (RS) encoder & decoder using FPGA to reduce the sources of error in DiPPM. The following main objectives will be considered:

1. Determine an appropriate encoder and decoder for DiPPM.
2. Design RS encoder and decoder circuits.
3. Implement RS and DiPPM encoder and decoder circuits by programming an FPGA.
4. Conform theoretical predictions with measurements.
5. Compare the result with another type of coding.

A system model tries to simulate some characteristics of a system. The model corresponds to the forward error correction (FEC) communication scheme, which is dependent on a RS error-control code. The behaviour of each block of the model is described in Matlab software.

1. DIPOLE PULSE POSITION MODULATION SYSTEM

In diode signalling data transitions from logic zero to logic one are coded as +V and transitions from logic one to logic zero are coded as -V. As shown in figure below, a zero signal is transmitted if there is no change in the PCM signal. The positive pulse can be regarded as setting the data to logic one (pulse SET), whereas the negative pulse resets the data to logic zero (pulse RESET). In diode PPM these SET and RESET signals are converted into two pulse positions in a data frame. Thus a PCM transition from zero to one produces a pulse in slot S and a one to zero transition generates a pulse in slot R. If the PCM data is constant, no signal is transmitted. (Although two guard slots have been used in this system, to reduce the effects of inter-symbol interference (ISI), this depends on the channel characteristics. If there is minimal ISI, zero guard slots could be used.)

2. REED SOLOMON CODE

In 1960, Irving Reed and Gus Solomon published a paper in which they described a new type of error-correcting codes that are now called Reed Solomon (RS) codes. RS codes are a powerful class of non-binary forward error-correcting that can correct the maximum possible number of errors with the minimum data overhead. RS codes are the most commonly used error codes in practice. It is used in many applications like magnetic and optical data storage, wireline and wireless communications, and satellite communications. RS decoder has the ability to correct up to t symbols that contain errors in a codeword, where t can be defined as:

\[ t = \frac{n-k}{2} \]

Where:
- \( n \) = Number of codeword symbols.
- \( k \) = Number of data symbols.
- \( 2t \) = Number of redundancy symbols.

\[ i_j = i_{j-1} + T_\text{p} \]

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