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Microelectronic implementation of error correcting codes for dicode pulse position modulation

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Dicode pulse position modulation (DiPPM) was proposed by Sibley as a more advantageous format than digital PPM. DiPPM can be efficiently implemented as it employs two slots to transmit one bit of pulse code modulation PCM. Thus, a PCM conversion from zero to one provides a pulse in slot reset (R) and from one to zero provides a pulse in slot set (S). No signal is transmitted if the PCM data is unvarying. The line rate is two times that of the original PCM, a significant reduction in speed compared to digital PPM. As the bandwidth requirement is much smaller than digital PPM, DiPPM could be used in dense wavelength division multiplexing (DWDM) systems. DiPPM systems suffer from three types of pulse detection errors: wrong-slot, false-alarm and erasure. This project will use a field programmable gate array (FPGA) to build an error correction code circuit (Reed Solomon Code) and dicode PPM (coder & decoder). This will be expected to reduce the error sources in DiPPM. According to initial results the conclusion is that the Reed Solomon error correction coded system offers improvement over uncoded DiPPM, when operating at the approximately 4/5 code rate.

**AIM & OBJECTIVE**

The main aim of this project research is to implement a DiPPM and Reed Solomon ( coder & decoder) using FPGA to reduce the sources of error in DiPPM.

The following main objectives will be considered: 1) Design Reed Solomon (RS) encoder & decoder parameters. 2) Design RS encoder and decoder circuits. 3) Implement RS and DiPPM encoder & decoder circuit by programming the FPGA. 4) Confirm theoretical predictions with measurements. 5) Compare the result with another type of coding.

**Sources of Error in DiPPM**

DiPPM systems suffer from three types of pulse detection errors:

- **Wrong slot error.** Wrong slot errors occur when noise on the rising edge of a detected pulse causes the pulse to appear in adjacent time slots.

- **Erasure errors.** Erasure errors occur when the noise is so great as to reduce the peak signal voltage to below the threshold level.

- **False alarm errors.** Due to ISI, there can be a signal voltage in the slots surrounding the one containing a pulse. Noise on this voltage can lead to a threshold crossing event when no pulse is present; so called false alarm errors.

**SYSTEM MODEL**

A system model tries to simulate some characteristics of a system. The model corresponds to the forward error correction (FEC) communication scheme, which is dependent on an RS error-control code. The behaviour of each block of the model is described in Mathcad software.

This research will concentrate on employing Reed Solomon (RS) codes to code the Dicode Pulse Position Modulation System (DiPPM). RS is expected to reduce the source of errors, which a DiPPM system suffers from. In this report a literature review has been written to explain the problems of DiPPM system and trying to find a solution, the general block diagram of the system has been given. According to initial results the conclusion is that the Reed Solomon error correction coded system offers improvement over uncoded DiPPM, when operating at approximately 4/5 code rate, and this will lead to a practical RS system (coder & decoder). Finally, the overall system will be implemented using FPGA and the results will be compared with maximum likelihood sequence detection (MLSD).

**FUTURE WORK**

- Determine a suitable algorithm for Reed Solomon Code.
- Design RS encoder and decoder circuits by choosing the proper parameters.
- Implement RS, DiPPM encoder and decoder circuit by programming the FPGA using Very high speed integrated circuit Hardware Description Language (VHDL).
- Verify theoretical predictions with measurements.