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# Practical implementation of duobinary pulse position modulation using FPGA and visible light communication

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**Abstract**—Low bandwidth expansion modulation schemes are preferred for free space and optical fibre data transmission, where limited bandwidth is available. One such scheme is duobinary pulse position modulation (DuoPPM), which is the subject of this paper. DuoPPM scheme is not as sensitive to bandwidth expansion issues as digital PPM, with a line rate of twice the data rate. This paper discusses first time practical implementation of DuoPPM coding scheme and its application in free space using visible light LED (30 W) for transmission purposes. Experimental results achieved at the data rate of 14 Mbit/s indicate an error rate that is better than 1 error in  $10^9$ . The main aim is to analyse the practicality, robustness and limitations of DuoPPM.

**Keywords**—DPPM; duobinary; LED; PPM; visible light communication

## I. INTRODUCTION

In recent years, many pulse position modulation (PPM) techniques have been proposed and investigated for both free space and optical fiber. One of the earliest PPM techniques purposed was digital PPM (DPPM), and it has been shown that it is an effective method of data transmission offering high sensitivity, low average power with low mark : space ratio [1-7]. In DPPM, one pulse per frame is required to transmit one codeword. Thus, to transfer M bits of data, one pulse must be placed in  $2^M$  slots and line rate becomes  $2^M/M$  times the original data rate [3]. The high sensitivity of DPPM comes at the price of large bandwidth expansion which has motivated researchers to many alternate reduced bandwidth PPM schemes, for example offset PPM, DuoPPM, dicode PPM, multipulse PPM and Differential PPM [3-8]. DuoPPM is a reduced bandwidth modulation scheme considered for first time practical implementation in this paper.

In DuoPPM [5], a pulse is generated when the data is constant at high or low, with no pulse being generated when there is a change in data from high to low or vice versa. It was demonstrated by Sibley [5], that DuoPPM has twice the line rate of the original non-return to zero (NRZ) on-off keying (OOK) data. Table I shows the DuoPPM signal representation. A continuous stream of 0's produces a pulse in slot 0 of DuoPPM frame and continuous stream of 1's produces a pulse in slot 1 of DuoPPM frame. No extra bits are appended in a

DuoPPM frame. DPPM has higher sensitivity and low average power than DuoPPM, since there is only one pulse per frame. However, in DPPM the practical implementation becomes impossible or very expensive due to very large bandwidth expansion. In order to reduce errors Maximum likelihood sequence detection (MLSD) technique has been suggested by Sibley [5] for DuoPPM coding scheme. Fig. 1 represents the conversion of pulse code modulation (PCM) into DuoPPM.

TABLE I. DUOBINARY PPM SIGNAL REPRESENTATION

Data	Probability	DuoPPM	Symbol
00	1/4	Pulse in slot 0	0
01	1/4	No pulse	C – change
10	1/4	No pulse	C – change
11	1/4	Pulse in slot 1	1

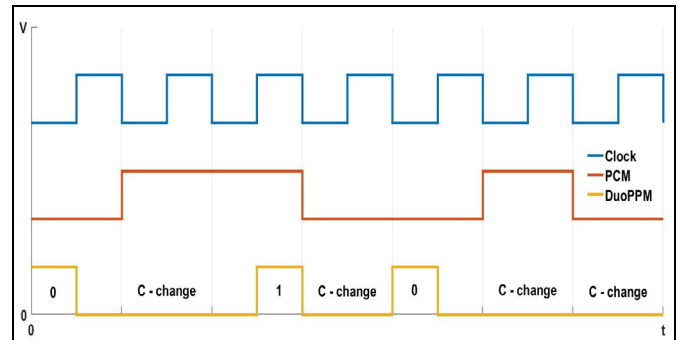


Fig. 1. PCM to DuoPPM conversion.

## II. VISIBLE LIGHT COMMUNICATIONS

In future, LED lighting will probably replace fluorescent and other lighting sources, since it offers many advantages over fluorescent lightening, such as: long life, fast switching and low power consumption. Along with illumination, LEDs hold the potential to transmit data. The optical wireless communication (OWC) and visible light communication (VLC) have become promising techniques where LEDs are used for high data transmission, which are potentially faster than other systems such as radio frequency (RF) or infrared

(IR) [9-11]. VLC equipment is typically light weight, low cost and occupies less space than RF, where frequency bands are becoming congested and more expensive [12, 13].

A VLC based experimental setup has been used in this work to test DuoPPM coding scheme, using a LED (30 W) and FPGA. The experimental setup is described in Fig. 2.

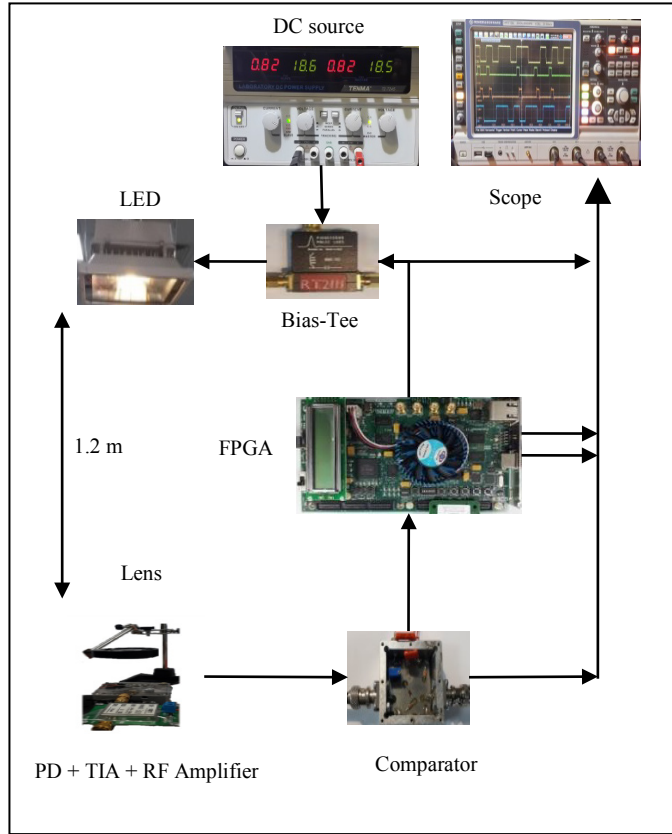


Fig. 2. VLC based experimental setup.

The coding scheme was programmed, for this purpose into the FPGA (Cyclone IV GX-EP4CGX150DF31C7) through the Quartus Prime 16.1 software using Very High Speed Integrated Circuits (VHSIC) Hardware Description Language (VHDL). In the first place, a modulated signal to be transmitted was generated by the FPGA, and delivered directly to the high-power LED (30 W LED floodlight, waterproof IP65) via Bias-Tee (Picosecond Pulse Labs 5575A). A free space distance of 1.2 m was taken between the PIN photodiode (PD) (type BPW34) and the LED. An optical convex lens (60 mm focal length) was placed in front of the PD, to converge the light at the PD, built into the trans-impedance preamplifier (TIA) board to convert the output of the PD to a voltage, as shown in Fig. 3a. The RF amplifier (0.01- 1000 MHz bandwidth, gain 32 dB) was used to amplify the output voltage of the TIA. Lastly, a low power, high-speed comparator (MAX942) was used to output a digital voltage as shown in Fig. 3b. The comparator output was returned to the FPGA to be demodulated and compared with the transmitted signal and then presented the results on the PC through the USB cable via the Signal Tap II Logic Analyzer in Quartus Prime 16.1 software. Furthermore, the signals have been observed by using a four-channel digital oscilloscope (Rohde & Schwarz RTO1044; 4 GHz).

### III. PRACTICAL IMPLEMENTATION OF DUOPPM

The block diagram in Fig. 4 describes the complete design of the DuoPPM coding scheme, developed through VHDL and the communication link. The system specifications are listed in Table II. The Phase-Locked Loop (PLL) was used to generate the desired frequency, 14 MHz, which was applied to a pseudo random binary sequence (PRBS) source block, DuoPPM (encoder/decoder) blocks and ‘synchronize + bit error rate (BER)’ block.

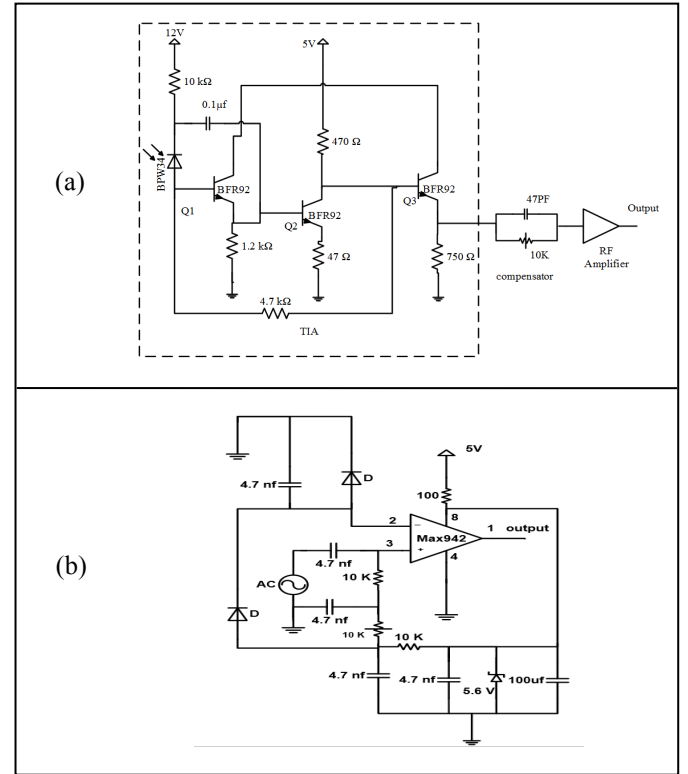


Fig. 3. a) PD + TIA., b) Comparator design.

The 15-bit serial output PRBS was used to produce a data signal, which was delivered to the DuoPPM encoder block to generate the encoded signal. The encoded signal was applied to the LED through the Bias-Tee for transmission to the PD at a free space distance of 1.2 m. The received signal from the comparator was sent into FPGA to DuoPPM decoder block. The decoded output from DuoPPM decoder block was transferred to ‘synchronize + BER’ block.

TABLE II. SYSTEM SPECIFICATION

Parameter	Value
Data rate	14 Mbit/s
Modulation scheme	Duobinary pulse position modulation (DuoPPM)
BER	$<10^{-9}$ upto 14 Mbit/s
Communication link	Visible light communication (white light LED 30 W)
FPGA board	Cyclone IV GX: EP4CGX150DF31C7

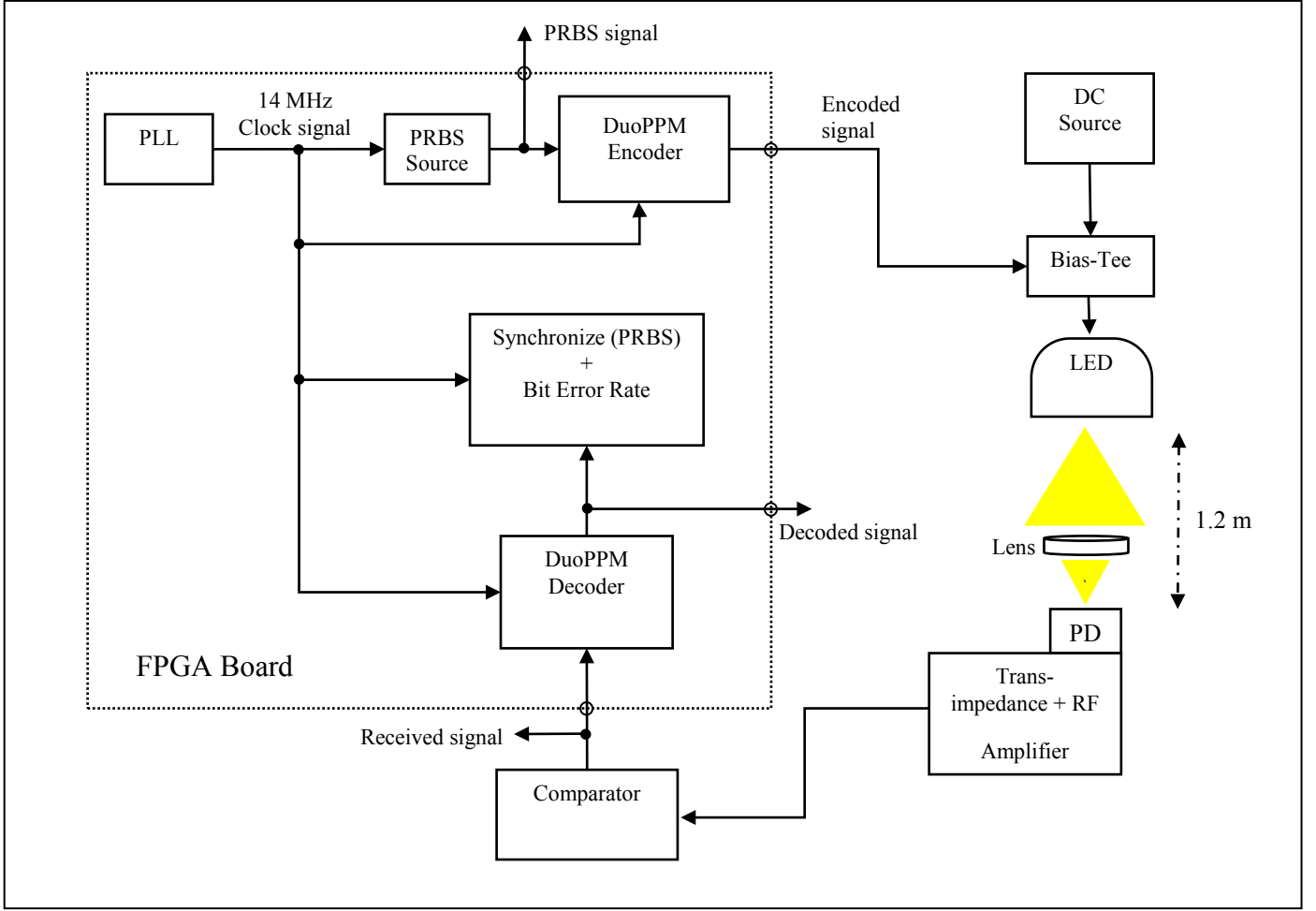


Fig. 4. Block diagram of DuoPPM system using VLC.

Within the ‘synchronize + BER’ block, the decoded signal is compared with a 15-bit PRBS signal having structure identical to source PRBS, to synchronize the data and check for errors. Error checking is performed by XORing the synchronized PRBS signal with the decoded received data. The BER was calculated by counting errors between the synchronized PRBS signal and the received signal against the clock pulses. The output simulations and BER was analyzed using Signal Tap II Analyzer.

#### IV. RESULTS AND DISCUSSIONS

DuoPPM coding system was successfully implemented for the first time to prove practical performance within a VLC based system. This experiment has been a success having  $<10^{-9}$  BER up to 14 MHz at free space distance of 1.2 m. The measured signals and BER are shown in Fig. 5 and 6, respectively. Commercially available white light LED (30 W), was used for transmission purposes, which can also be used for illumination.

Intersymbol interference (ISI) starts to occur above 14 MHz. As the frequency increases, the pulse width decreases and the distance between two consecutive pulses reduces

resulting in ISI. Above 14 MHz the received signal shows noticeable difference due to ISI as shown in Fig. 7. Once an error has occurred the decoded data will be corrupted until the correct pulse is received to re-synchronize the signal.

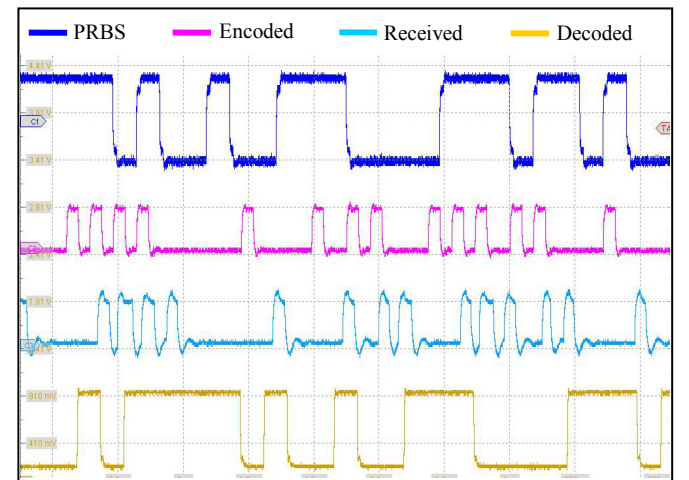


Fig. 5. Measured signals using oscilloscope.

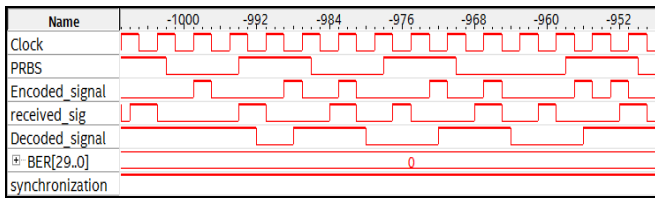


Fig. 6. Signal Tap II Logic Analyzer.

The ISI effect occurs due to the comparator circuitry, when the pulse width reduces the output of comparator falls short of the threshold voltage of the FPGA and the pulse goes undetected. The ISI can be reduced by either adding coding blocks implementing MLSD or by improving analogue hardware circuitry.

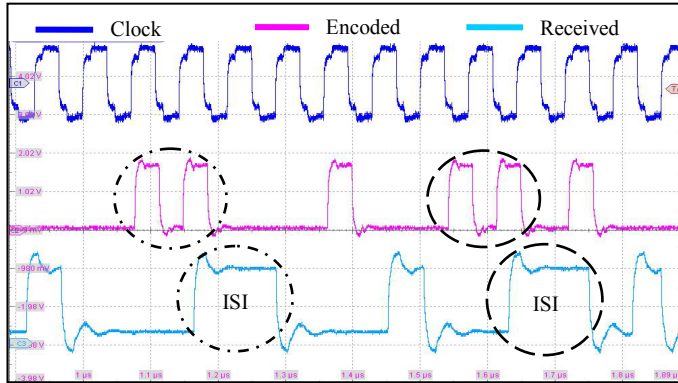


Fig. 7. Typical effect of ISI.

## V. CONCLUSION

This paper has outlined the successful implementation of DuoPPM coding system using VLC, and proves that the application of DuoPPM is possible for free space links. At a maximum working frequency of 14 MHz, the BER was recorded as less than  $10^{-9}$  at a free space distance of 1.2 m between transmitter and receiver. DuoPPM can be considered as an improved bandwidth utilization technique and alternate to conventional PPM techniques.

In future, MLSD can be used with this coding scheme for error correction. High speed and improved circuitry is required to test the coding scheme at higher line rates and greater distance for further performance analysis.

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